DRA72x EVM CPU Board User's Guide

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1 Introduction

The DRA72x evaluation module (EVM) is an evaluation platform designed to speed up development efforts and reduce time to market for applications such as infotainment, reconfigurable digital cluster or integrated digital cockpit. To allow scalability and re-use across DRA72x Jacinto Infotainment SoCs, the EVM is based on the Jacinto 6 Eco DRA718 SoC that incorporates a heterogeneous, scalable architecture that includes a mix of an ARM® Cortex®-A15 core, two ARM Cortex-M4 processing subsystems, one C66x Digital Signal Processors (DSPs), 2D- and 3D-graphics processing units including Imagination Technologies POWERVR™ SGX544 and a high-definition image and video accelerator. It also integrates a host of peripherals including multi-camera interfaces (both parallel and serial) for LVDS-based surround view systems, displays, CAN and Gigabit Ethernet AVB.

The main CPU board integrates these key peripherals such as Ethernet or HDMI, while the infotainment application daughter board (JAMR3) and LCD/TS daughter board will complement the CPU board to deliver complete system to jump start your evaluation and application development.

2 Overview

An EVM system is comprised of a CPU board with one or more application boards. The CPU board (shown in Figure 1) can be used standalone for software debug and development. Each EVM system is designed to enable customers to evaluate the processor performance and flexibility in the following targeted markets:

- Automotive and infotainment applications
- Automotive and ADAS applications

The CPU board contains the DRA72x (Superset part) applications processor, a companion power solution (TPS65917), DDR3 DRAM, several types of flash memories (QSPI, eMMC, NAND, and NOR), and a multitude of interface ports and expansion connectors. The board provides additional support components that provide software debugging, signal routing, and configuration controls that are not needed in a final product. Different versions of the CPU boards will be built to support the development process that include:

- Socketed processor for wakeup, early SW development, and quick and easy chip revision evaluation
- Soldered-down processor for high-performance use cases and evaluations

All other components on-board are soldered-down.

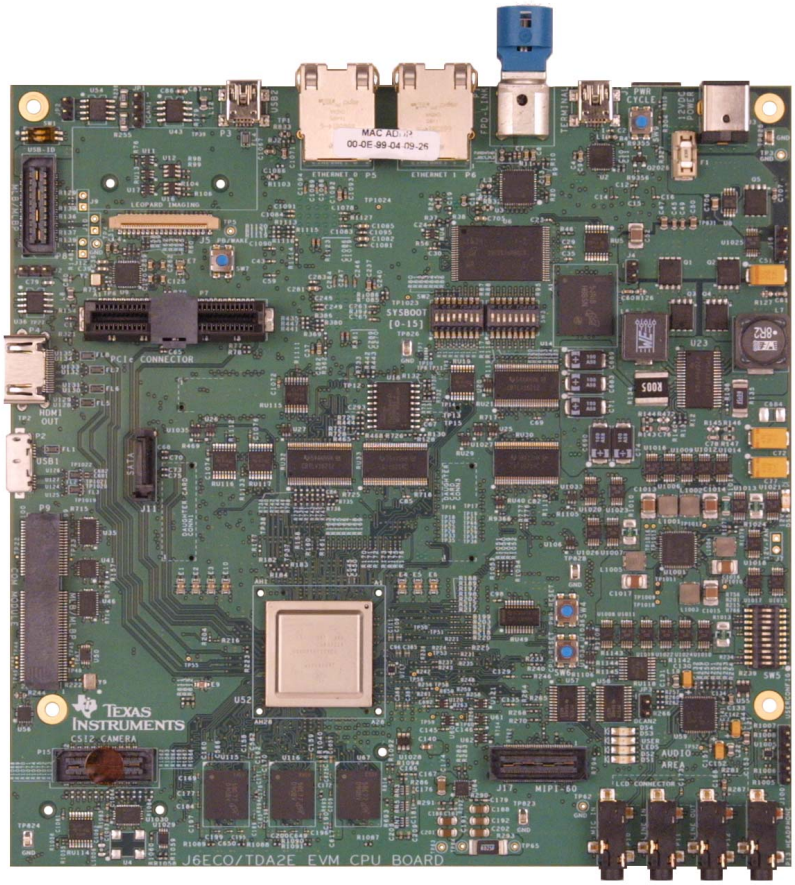


Figure 1. CPU Board

2.1 EVM System Configurations

2.1.1 Revisions

- ES1.0 is on CPU board through Rev B
- ES2.0 is on CPU boards Rev C on
- Table 1 through Table 3 indicates the obsolete versions
- Table 4 through Table 6 indicates valid production versions

Table 1. EVM Wake-Up Board and Kits (Obsolete)

Wake-Up Platforms	Description	Model Number
J6Eco ES1.0 CPU Board	Socketed CPU Board, Power Supply, Limited Accessory Cables.	EVMDR72BG-01-00-S0
J6Eco ES1.0 EVM Kit	Socketed CPU Board, LCD/TS Daughter Bd, Power Supply, Limited Accessory Cables.	EVMDR72G-01-00-S0
J6Eco ES1.0 EVM Infotainment Kit	Socketed CPU Board, JAMR3 Apps Bd, LCD/TS Daughter Bd, Power Supply, Limited Accessory Cables.	EVMDR72G-01-20-S0

Table 2. Production Boards (Obsolete)

Production Boards	Description	Model Number
J6Eco CPU Bd ES1.0 GP	CPU Board, Power Supply, Limited Accessory Cables.	EVMDR72BG-01-00-00
J6Eco CPU Bd ES1.0 HS	CPU Board, Power Supply, Limited Accessory Cables.	EVMDR72BH-01-00-00

Table 3. Production Kits (Obsolete)

Production Kits	Description	Model Number
J6Eco ES1.0 GP EVM Kit	CPU Board, 10.1” LCD/TS Daughter Bd, Power Supply, Limited Accessory Cables.	EVMDR72G-01-01-00
J6Eco ES1.0 GP EVM Infotainment Kit	CPU Board, JAMR3 Apps Bd, 10.1” LCD/TS Daughter Bd, Power Supply, Limited Accessory Cables.	EVMDR72G-01-21-00

Table 4. EVM Wake-Up Board and Kits (Production)

Wake-Up Platforms	Description	Model Number
DRA72x/TDA2Ex ES2.0 CPU Bd	Socketed CPU Board, and Limited Accessory Cables.	EVMDR72BG-02-00-S0

Table 5. Production Boards (Production)

Production Boards	Description	Model Number
DRA72x/TDA2Ex CPU Bd ES2.0 GP	CPU Board, Power Supply, Limited Accessory Cables.	EVMDR72BG-02-00-00
DRA72x/TDA2Ex CPU Bd ES2.0 HS	CPU Board, Power Supply, Limited Accessory Cables.	EVMDR72BH-02-00-00
10.1” LCD/TS Daughter Board	10.1-inch 1920X1200 LCD (24-bit color) with projective and capacitive touch-screen	EVM5777LCDTS-V3-0
JAMR3 Application Board	Head-unit DIN form-factor Application Board with radio tuners, multiple audio I/Os, and video input extendibility	EVM5777JAMR3-V1-0
Vision Application Board	Support for multiple camera inputs for surround view, stereo vision, and proprietary camera board interfaces, AD7611 HDMI receiver	EVM5777VISION-V2-0

Table 6. Production Kits (Production)

Production Kits	Description	Model Number
DRA72x/TDA2Ex ES2.0 GP EVM Kit	CPU Board, 10.1” LCD/TS Daughter Bd, and Limited Accessory Cables.	EVMDR72G-02-00-00
DRA72x ES2.0 GP EVM Infotainment Kit	CPU Board, JAMR3 Apps Bd, 10.1” LCD/TS Daughter Bd, and Limited Accessory Cables.	EVMDR72G-02-20-00
TDA2Ex ES2.0 GP EVM Vision Kit	CPU Board, Vision Apps Bd, and Limited Accessory Cables.	EVMTDA2EG-02-40-00

Table 7. EVM Kit Truth Table

Kit Name	CPU Bd	JAMR3 App Bd	LCD/TS Daughter Bd	Vision App Bd	2.1-mm to 2.5-mm Power Supply Adapter
GP EVM	X		X		X
GP EVM Infotainment	X	X	X		X
GP EVM Vision	X			X	X

2.2 CPU Board Feature List

- Processor:
  - Superset SOC (23-mm × 23-mm package, 0.8-mm pitch with 28 × 28 via-channel array)
  - Support for corresponding socket

- Memory:
  - EMIF1 - DDR3L-1333 (with ECC): 2-Gbyte (four 4-Gbit × 8 + one 4-Gbit × 8 ECC)
  - Quad SPI flash: 256 Mbit
  - eMMC flash: 8 Gbit (v.4.51 compliant)
  - NAND flash: 2 Gbit
  - NOR flash: 512 Mbit
  - I2C EEPROM, 256 Kbit
  - MicroSD card cage
- Boot mode selection DIP switch
- Onboard temperature sensor
  - TMP102
- JTAG/Emulator:
  - 60-pin MIPI-60 JTAG/Trace connector
  - 20-pin CTI adapter: 10 × 2, 1.27-mm pitch
  - 14-pin adapter: 7 × 2, 2.54-mm pitch
- Audio input and output:
  - AIC3106 codec: Headphone OUT, Line OUT, Line IN, Microphone IN
- Supported interfaces and peripherals:
  - CAN interface – 2-wire PHY on DCAN1
  - Two USB host receptacles:
    - USB3.0 (micro-USB)
    - USB2.0 (mini-USB)
  - PCIe ×1 (×2 support with component change)
  - Video – one HDMI Out, one FPD-Link III, one LCD
  - Camera sensors support through Leopard Imaging Module interface, parallel and CSI2
  - CSI2 generic connector interface
  - MLB and MLBP on Mictor connector
  - RS232 through USB FTDI converter (mini-A/B USB)
  - COM8 module connector interface for *Bluetooth*® and WLAN support
  - Gigabit Ethernet PHY (RJ45) x 2 (DP83867)
  - SATA interface
  - I2C GPIO expander
  - LCD daughter board connector
- Expansion connectors to support specific applications
- Power supply:
  - 12-V DC input
  - Optimized power management IC (TPS65917)
  - Compliant with power-sequencing requirements
  - Integrated power measurement

- PCB:
  - Dimension (W × D) 170 mm × 170 mm
  - 100% PTH technology

2.2.1 CPU Board Component Identification

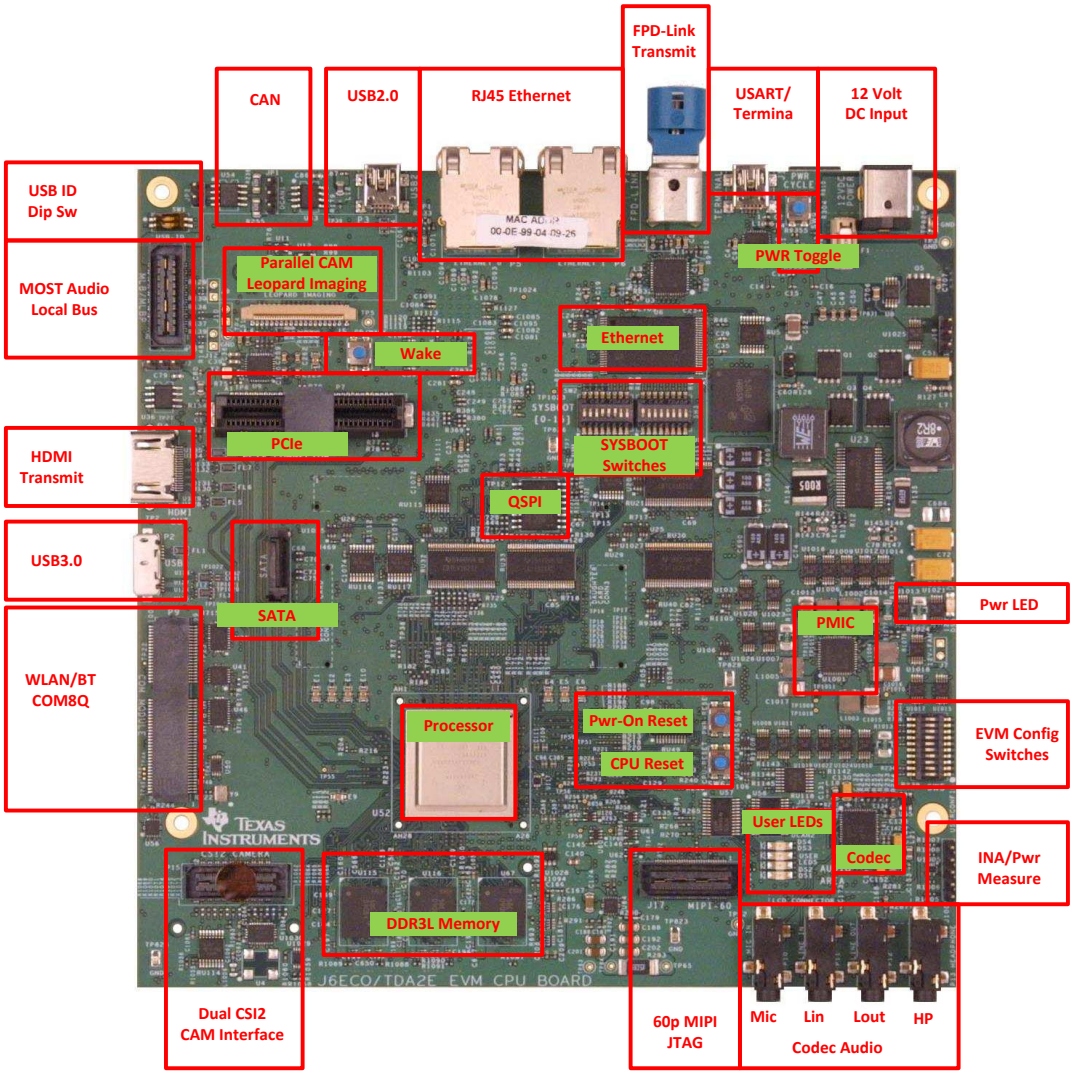


Figure 2. CPU Board – Front

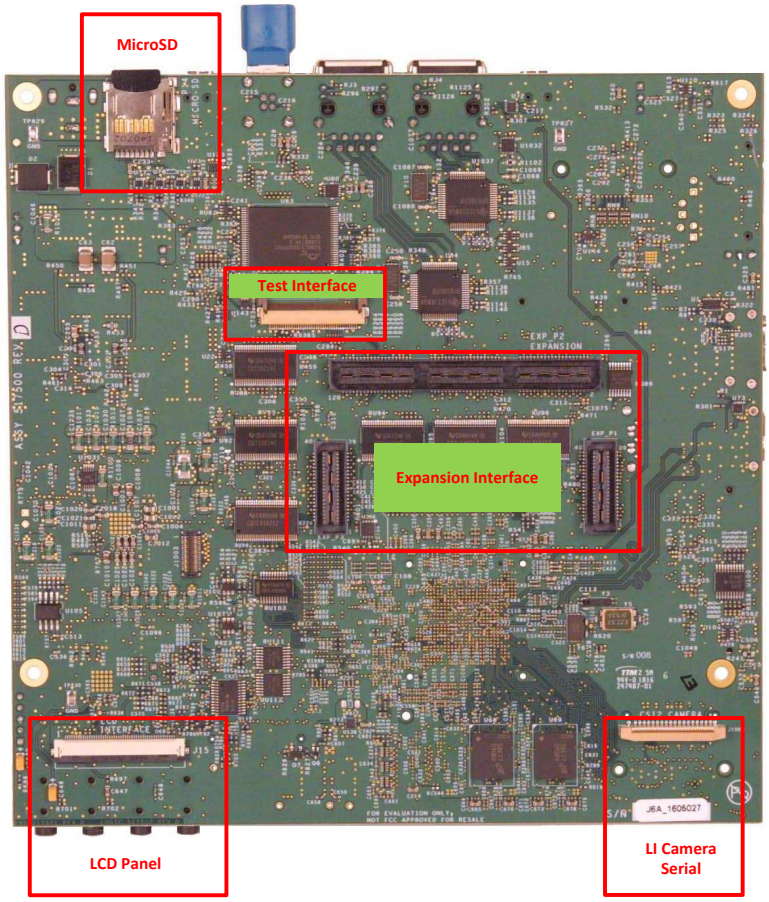


Figure 3. CPU Board – Back

3 Hardware

3.1 Hardware Architecture

Figure 4 shows the functional block diagram.

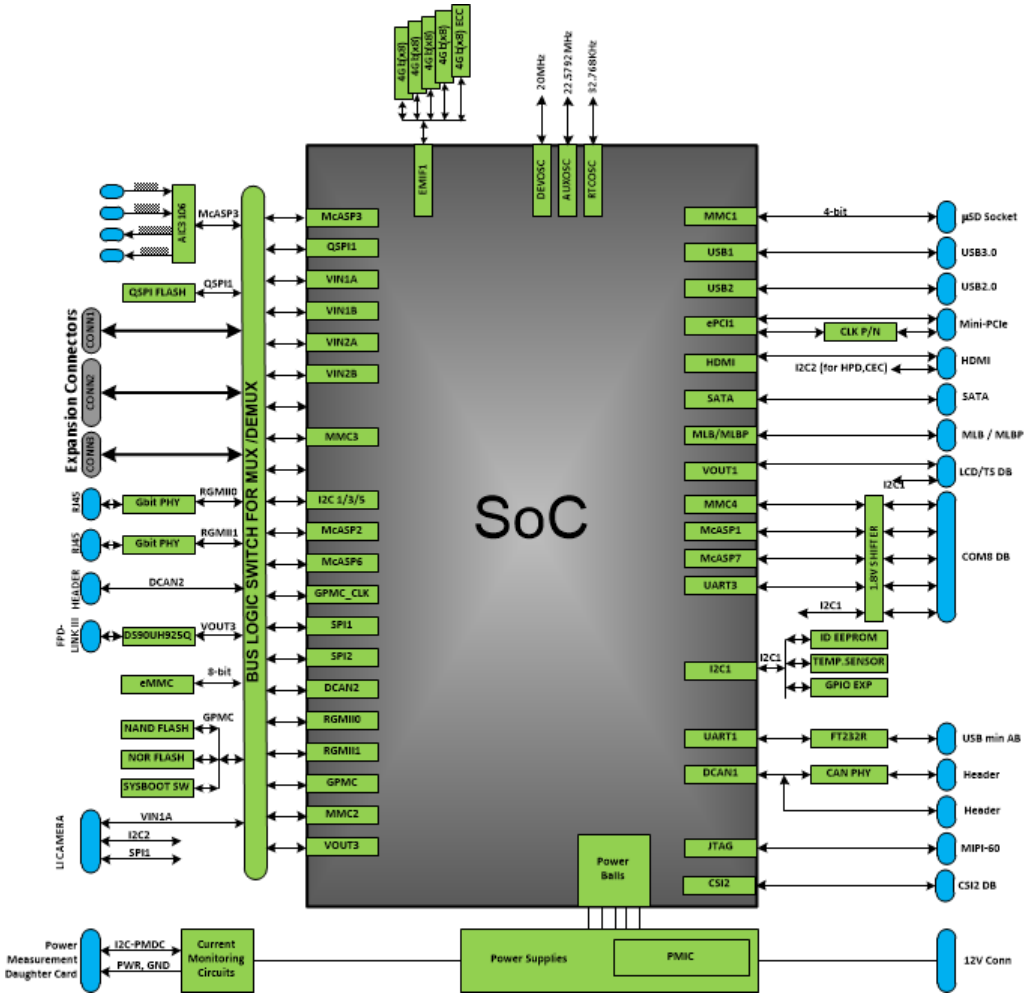


Figure 4. CPU Board Block Diagram

3.2 Power Architecture

Figure 5 shows the complete power distribution system of the EVM. The companion power management IC (PMIC) for SoC is the TPS65917-Q1. A step-down 12-V to 3.3-V and 5-V converter is available to provide a 3.3-V and 5-V DC input to the PMIC, as well as 3.3-V and 5-V power rails at the board level.

Refer to the PMIC data sheet for the power on/off sequence.

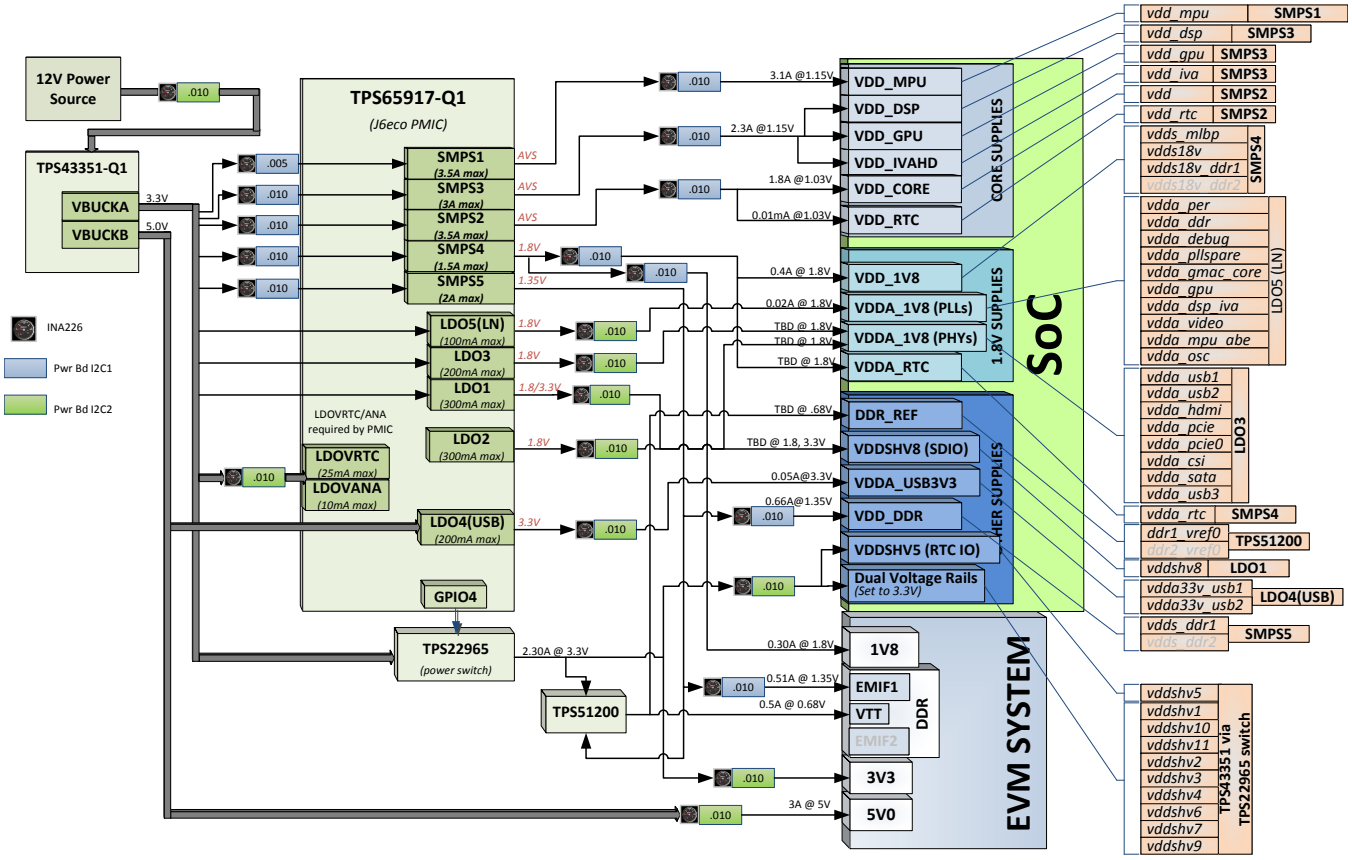


Figure 5. Power Distribution Block Diagram

An external power is required to power the EVM, but is not included as part of the EVM kit. The external power supply requirements are:

- Power Jack: 2.5-mm ID, 5.5-mm OD
- Nom voltage: 12 VDC
- Max Current: 5000 mA
- Efficiency Level V

Table 8 includes recommended and tested supplies for use with the EVM.

Table 8. EVM Supplies

Digi-Key Part Number	Manufacturer Part Number	Manufacturer	Output Connector	Notes
102-3417-ND	SDI65-12-U-P5	CUI Inc	Barrel Plug, 2.1-mm I.D. × 5.5-mm O.D. × 9.5 mm	Required adapter, provided in EVM kit
62-1221-ND	KTPS65-1250DT-3P-VI-C-P1	Volgen America/Kaga Electronics USA	Barrel Plug, 2.1-mm I.D. × 5.5-mm O.D. × 9.5 mm	Required adapter, provided in EVM kit
102-3419-ND	SDI65-12-UD-P5	CUI Inc	Barrel Plug, 2.1-mm I.D. × 5.5-mm O.D. × 9.5 mm	Required adapter, provided in EVM kit
SDI65-12-U-P6-ND	SDI65-12-U-P6	CUI Inc	Barrel Plug, 2.1-mm I.D. × 5.5-mm O.D. × 9.5 mm	
SDI65-12-UD-P6-ND	SDI65-12-UD-P6	CUI Inc	Barrel Plug, 2.1-mm I.D. × 5.5-mm O.D. × 9.5 mm	

External Power Supply Regulatory Compliance Certifications: Recommended selection and use of an external power supply which meets TI's required minimum electrical ratings, in addition to complying with applicable regional product regulatory and safety certification requirements, such as UL, CSA, VDE, CCC, PSE, and so forth.

3.3 Reset Structure

The reset structure is shown in Figure 6. The power-on reset timing is controlled primarily from the system PMIC (TPS65917-Q1). There are two push buttons for user-controlled resets. One is the power-on reset (SW4) for a complete SoC reset. The other is for warm reset (SW5). The warm reset can also be sourced from the MIPI-60 JTAG/Trace connector.

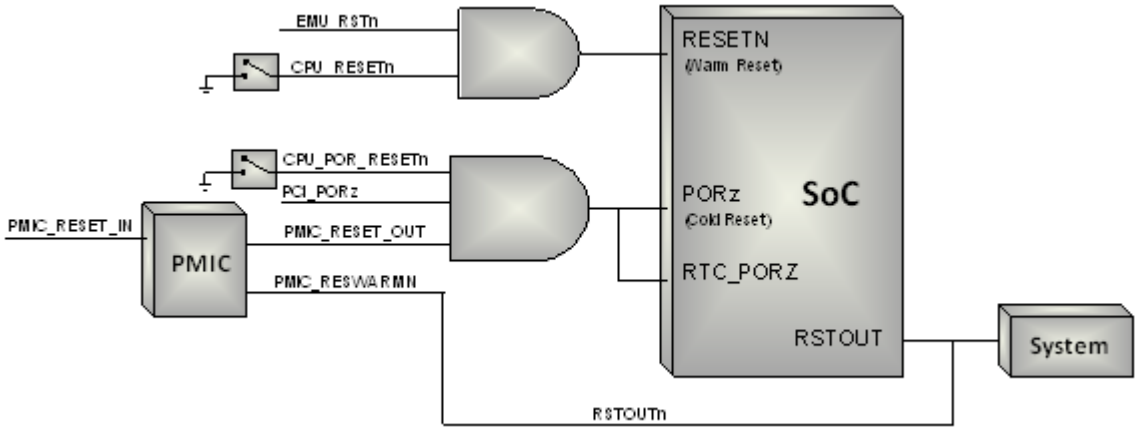


Figure 6. Reset Structure

Table 9 summarizes the reset signals.

Table 9. Reset Signals Structure

Reset Type	Reset Signal Sources	Comments
Power-on reset (as whole system reset)	CPU_POR_RESETn	PORn push button reset
	PCI_PORz	PCIe inbound reset
	PMIC_RESET_OUT	Power on reset from PMIC
Warm reset	CPU_RESETn	Warm push button reset
	EMU_RSTn	Reset from emulator
PMIC power-on reset	PMIC_RESET_IN	PMIC reset input
Processor reset out	RSTOUTn	Reset output from processor to system, PMIC (warm reset input)

3.4 Clocks

The SoC supports three primary clock inputs. The device clock (OSC0) is provided by a 20-MHz crystal, and the auxiliary clock (OSC1) is provided by a 22.5792-MHz crystal. The RTC clock input is provided by a 32.768-KHz crystal.

In addition to the SoC clock inputs, the EVM includes other clock sources. A 25-MHz oscillator is provided to a CDCM9102 clock driver for sourcing the PCI 100-MHz reference clock. Each Ethernet PHY also includes a local 25-Mhz crystal to provide its network reference clock.

3.5 Memory

3.5.1 SDRAM Memory

The EVM includes 2 GBytes of DDR3L memory, and can operate at clock speeds up to 667 MHz (DDR3-1333). The memory is configured with four devices of 4 Gbit each (x8b devices). ECC is also supported.

DDR3L device used: Micron MT41K512M8RH-125-AA:E (4 × 8bit at 4 Gbit/ea) (or equivalent).

EEC device used: Micron MT41K512M8RH-125-AA:E (1 × 8bit at 4 Gbit) (or equivalent).

The DDR3L power is generated from the PMIC (TPS65917-Q1) and set to 1.35 V. It uses fly-by topology with VTT termination. VTT supply is generated using a sink and source termination regulator (TPS51200).

3.5.2 QSPI Flash Memory

As a primary non-volatile boot device, the EVM includes 256 Mbit of Quad-SPI flash memory. The device is supported on chip select zero of the QSPI interface. The interface can be configured to support either serial mode (1x) or quad mode (4x).

QSPI device used: Spansion S25FL256S

Booting from the QSPI flash memory is supported on the EVM. No EVM configuration is required, as the QSPI flash is connected by default. Ensure the correct SoC boot mode using the SYS_BOOT switches (SW2, SW3).

3.5.3 EMMC Flash Memory

As a primary non-volatile storage device, the EVM includes 8 GBytes of eMMC flash memory. The memory device is EMMC v4.51-compliant, and connects to MMC2 port of the SoC. The design can supports rates up to HS-200.

EMMC device used: Micron MTFC8GLWDM-3M AIT Z

Booting from the EMMC flash memory is supported on the EVM. The on-board mux must be set to enable EMMC by setting the SW5.p3 to ON. Ensure the correct SoC boot mode is set using the SYS_BOOT switches (SW2, SW3).

3.5.4 MicroSD Card Cage

For non-volatile storage expansion, the EVM includes a microSD card cage. The cage is connected to the MMC1 port of the SoC. To support higher-speed cards that operate at lower voltages, the IO supply is changed from 3v3 to 1v8 through the PMIC LDO configuration (see the PMIC data manual for instructions on how to change the voltage level). The SD card power can be cycled using the IO expander (EXP2, PP5). For specific information regarding supported card types, densities, and speeds, see the device-specific data manual for SoC.

Booting from the microSD card cage is supported on the EVM. No configuration is required, as the SD card is selected by default. Ensure the correct SoC boot mode is set using the SYS_BOOT switches (SW2, SW3).

3.5.5 GPMC NOR Flash Memory

A 512-Mbit NOR flash memory (x16) is supported as a non-volatile memory option on the EVM. It is supported on chip select CS0, and thus can also be used as a boot device. To access, the onboard mux must be enabled by setting SW5.p2 to ON. For booting, ensure the correct SoC boot mode is selected using the SYS_BOOT switches (SW2, SW3).

NOR device used: Spansion S29GL512S10TFI010

3.5.6 GPMC NAND Flash Memory

A 2-Gbit NAND flash memory (x16) is supported as a non-volatile memory option on the EVM. It is supported on chip select CS0, and thus can also be used as a boot device. To access, the onboard mux must be enabled by setting SW5.p1 to ON. For booting, ensure the correct SoC boot mode is selected using the SYS_BOOT switches (SW2, SW3).

NAND device used: Micron MT29F2G16AADWP:D

3.6 Boot Modes

The SoC supports a variety of different boot modes, determined by the 16-bit system boot setting present on the shared specific I/O balls during the power-on sequence (see the TRM for details). Boot mode selection is accomplished by setting the DIP switches SW2 and SW3 as shown in Table 10, prior to cycling of power.

These SoC resources can be redeployed to support alternate interfaces after boot-up, by way of both SoC and EVM mux settings.

An ON setting selects a logic 1 for the signals, and an OFF setting selects a logic 0.

Table 10. SoC Boot Mode Switch Settings

SoC Interface (Internal System Boot Input)	CPU Bd Net	DIP Switch Ref Des. Position # Connections	Factory Settings
GPMC_AD0 (sysboot0)	GPMC_D00	SW2.P1	ON
GPMC_AD1 (sysboot1)	GPMC_D01	SW2.P2	OFF
GPMC_AD2 (sysboot2)	GPMC_D02	SW2.P3	ON
GPMC_AD3 (sysboot3)	GPMC_D03	SW2.P4	OFF
GPMC_AD4 (sysboot4)	GPMC_D04	SW2.P5	ON
GPMC_AD5 (sysboot5)	GPMC_D05	SW2.P6	OFF
GPMC_AD6 (sysboot6)	GPMC_D06	SW2.P7	OFF
GPMC_AD7 (sysboot7)	GPMC_D07	SW2.P8	OFF
GPMC_AD8 (sysboot8)	GPMC_D08	SW3.P1	ON
GPMC_AD9 (sysboot9)	GPMC_D09	SW3.P2	OFF
GPMC_AD10 (sysboot10)	GPMC_D10	SW3.P3	OFF
GPMC_AD11 (sysboot11)	GPMC_D11	SW3.P4	OFF
GPMC_AD12 (sysboot12)	GPMC_D12	SW3.P5	OFF
GPMC_AD13 (sysboot13)	GPMC_D13	SW3.P6	OFF

Table 10. SoC Boot Mode Switch Settings (continued)

SoC Interface (Internal System Boot Input)	CPU Bd Net	DIP Switch Ref Des. Position # Connections	Factory Settings
GPMC_AD14 (sysboot14)	GPMC_D14	SW3.P7	OFF
GPMC_AD15 (sysboot15)	GPMC_D15	SW3.P8	ON

In addition to the SoC boot settings, the EVM resources must also be set for the desired interface, as shown in Table 11. DIP switch SW5 is used to configure the various EVM memories for boot.

An ON setting selects a logic 0 for the signals, and an OFF setting selects a logic 1. This polarity is OPPOSITE the SYS_BOOT settings.

Table 11. Board Controls for Memory Booting Options

Signals	Description	DIP Switch	Factory Settings	I2C1 GPIO Expander
NAND_BOOTn(1)	Low = Enable GPMC_nCS0 for NAND flash boot	SW5.1	OFF	U57.P10
NOR_BOOTn(1)	Low = Enable GPMC_nCS0 for NOR flash boot	SW5.2	OFF	U57.P11
MMC2_BOOT	Low = Enable MMC2 Interface for eMMC flash boot	SW5.3	OFF	U57.P12
UART_SEL1_3	High = UART3 Interface for UART boot is enabled. Low = UART1 interface for terminal	SW5.5	ON	U57.P14

(1) Routing control for GPMC_nCS0 is shared between NOR and NAND flash memories. Ensure that only one DIP switch, SW5.P1 or SW5.P2, is ever set to the ON state at any one time, so that GMPC_nCS0 is only connected to one memory. Failure to adhere to this requirement will cause NOR and NAND memory data bus contention.

Table 12. Board Controls for Signaling and Operational Modes

Signals	Description	DIP Switch	Factory Settings	I2C1 GPIO Expander
MCASP1_ENn	Low = Enable COMx signal paths	SW5.6	OFF	U57.P15
NOR_ALT_ADDRn	High = Selects default pin location for GPMC ADDR Low – Selects alternate/new pin locations for GPMC	SW5.7	OFF	U57.P6
PCI_RESET_SEL	High = PCIe device may reset SoC Low = SoC may reset the PCIe device	SW5.8	OFF	NA
GPMC_WPN	Low = Enable write protection of NAND Flash	SW5.9	OFF	NA
I2C_EEPROM_WP	High = Enable write protection of Board identification EEPROM	SW5.10	OFF	NA

3.7 JTAG and Emulator

The JTAG emulation interface is supported through the MIPI 60-pin interfaces. The EVM kit includes an adapter for supporting other JTAG interfaces, including TI's 20-pin cJTAG interface. Reset (warm reset) through the emulator is supported.

The EVM supports up to 20 trace bits. At the SoC and EVM level, the trace pins are muxed with VOUT1 (LCD panel) pins. Thus, these interfaces cannot be used simultaneously. TI recommends any LCD panel be removed from the system using debug or trace features.

3.8 UART Terminal

The EVM supports a single UART connection for a user terminal. A FT232 device is used to transport the UART information over USB to a host PC. The EVM is designed to use UART1 as the primary terminal connection, but can also support an alternate configuration to use UART3 (required to support peripheral and UART booting). The USB-side of the FT232 device is powered from the USB port, and the connection stays active regardless of the power state of the EVM.

USART device to be used: FTD Chip FT232RQ

A USB mini-AB receptacle is used to support USB connection, and is included as part of the EVM kit.

3.9 DCAN and CAN Interfaces

The EVM supports access to two DCAN interfaces though pin headers. It supports a single 3-pin CAN interface, connecting DCAN1 through a CAN transceiver.

CAN device used: Texas Instruments SN65HVDA541

3.10 Universal Serial Bus (USB)

Two independent USB ports are supported on the EVM. USB3.0 Super-Speed bus (USB1) is supported using port USB1 to a mini-AB type connector. This interface supports rates up to 5 Gbps. USB2.0 interface is supported using port USB2 to a micro-AB type connector. It can support rates up to 480 Mbps. Both ports can operate either as host or device mode. VBUS can be supplied to a peripheral when in host mode by enabling the VBUS switch (controlled through the SoC). However, the EVM cannot be powered from VBUS when operating in device mode.

The EVM includes capabilities to set and read each connector ID pin. This is supported using the IO expander (EXP2 P1 for USB1, P2 for USB2). In addition, DIP switch SW1 provides the ability to manual set the individual ID value either high (OFF) or low (ON).

3.11 Wired Ethernet

Dual Gigabit Ethernet ports are supported on the EVM. RGMII ports 0 and 1 drive the Texas Instruments DP83867 Gigabit PHYs. The PHYs are configured through the Management Data Input/Output bus (MDIO), with address set to 0x2 (port 0) and 0x3 (port 1). PHYs are reset at power-on, but can also be independently reset using the IO expander. Both ports share a common interrupt signal (GPIO6_16).

IO Expander Control: EXP1, P10 (PHY 0 Reset), P11 (PHY 1 Reset)

NOTE: For PHY configuration, the user must configure the DP83867 RGMII Control register (RGMIICTL) for RGMII mode, and the RGMII Delay Control register (RGMIIDCTL) for 0-ns TX delay, and 2.25-ns RX delay. Set the IO Drive Strength register (IO_IMPEDANCE_CTRL) to maximum drive.

3.12 Video Output

The EVM supports three different options for supporting video output: HDMI, Display Panel, and FPD Link. Each can be supported independently, or all used simultaneously.

3.12.1 HDMI Display

The SoC includes a dedicated HDMI display interface, which is supported on to a type A HDMI connector. The interface will support 1080p with 24b color. A communication channel (DDC/CEC) is supported to the HDMI connector for communication with the HDMI panel. A monitor detect indication is also provided. The DDC/CED interface and monitor detect signals (HPD) are translated through the transceiver, and can be controlled using IO from the expander.

DDC Transceiver used: Texas Instruments TPD12S016

IO Expander Control: EXP3, P4 (Lvl Shift Reg Enable, HPD), P5 (DDC/CEC Enable)

3.12.2 LCD Touch Panel

The EVM supports a LCD panel interface for supporting video output to a LCD panel. The SoC VOUT1 resource is used drive up to 24b RGB data to interface. The interface supports resource connections for interfacing with a touch panel for advanced user interfaces. These include a control bus (I2C1) and interrupt for touch indications (GPIO)

An LCD panel is not included with the CPU EVM, but can be ordered and included as part of an assembly kit.

Connector used: Molex

3.12.3 FPD-Link III Output and Panel

The EVM includes a FPD-Link III parallel-to-serial interface on VOUT3. It supports up to 24bits of data and can operate at pixel rates up to 85 MHz. The interrupt is supported to enable back-channel communication, typically needed if supporting touch screen. The transceiver is configured using I2C (port 5, 0x1B).

Serializer device used: Texas Instruments DS90UH925Q

Connector used: Automotive HSD Connector, right-angle plug for PCB, Rosenberger D4S20D-40ML5-Z.

3.13 Video Input

3.13.1 Parallel Imaging

Parallel video input is supported through connections from external sensors and transceivers. The SoC port VIN2A is routed to a connector interface designed to mate with camera sensors from Leopard Imaging. This approach provides flexibility for customers to select from a variety of available modules, while also supporting connections of custom solutions. The attached module can be configured using either I2C (port 5) or SPI (port 1).

Connector used: FPC 36 position, 0.5 mm, Molex 052559-3679.

3.13.2 Serial Imaging

Serial video input is supported through connections from external sensors and transceivers. The SoC port CSI2-0 is routed to connector interfaced designed to mate with camera sensors from Leopard Imaging. This approach provides flexibility for customers to select from a variety of available modules. Both serial ports (CSI2-0 and CSI2-1) are routed to an expansion connector for supporting a variety of custom solutions. Both interfaces support additional signals for the control and configuration of the attached modules. These interfaces (I2C port 5, SPI port 1) are translated to 1.8-V IO (with resistor option to leave at 3.3-V IO).

LI Connector used: FPC 36 position, 0.5 mm, Molex 052559-3679

Connector used: Samtec QSH-020-01-L-D-DP-A

3.14 PCIe

The EVM supports a PCIe (single-lane) interface for connecting with a variety of external modules. A second lane is available with a component modification (FL2, FL3). An on-board clock generator CDCM9102 provides the 100-MHz reference clock to both the SoC and attached modules. The EVM support two different PCIe reset configurations, select using DIP switch SW5 position 8. The default setting of ON lets SoC reset the PCIe peripheral. The switch setting of OFFlets the PCIe peripheral reset the SoC.

3.15 Media Local Bus (MLB)

The EVM supports a Media Local Bus interface for connecting to external hardware (such as SMSC OS81110/2+0 Physical Interface Board). The interface supports both 3-pin MediaLB and 6-pin MediaLB+ configurations.

Connector used: Samtec QSH-020-01-L-D-DP-A

3.16 Audio

The EVM supports onboard AIC3106 audio codec for analog audio conversions. Analog inputs are supported on two 3.5-mm audio jacks, including stereo line inputs (P12) and mono microphone (P11). Analog outputs are supported on two 3.5-mm audio jacks, providing stereo line outputs (P13) and stereo headset (P14). The digital audio is connected to the SoC using multi-channel serial port (McASP3). The codec requires a master clock (AHCLKX). The audio codec is configured using I2C1, and is accessed at address 0x19.

3.17 COM8 Module Interface

A connector is provided to facilitate the plugging in of TI COM8Q modules, which provide features such as Bluetooth and Wi-Fi™. The COM8Q interface requires a 3.6-V power supply; thus, a dedicated regulator is provided. All signals on the COM8Q interface are required to 1.8 volts, thus voltage translators are placed to convert from the standard IO levels of 3.3 V. UART interface (UART3) is used for BT-HCI port, I2S port (McASP7) is used for BT-audio, and MMC4 port is use for WiFi communication.

Connector used: Samtec MEC6-150-02-S-D-RA1

3.18 User Interface LEDs

The CPU board has four user interface LEDs for debug, status indication, and so forth. Table 13 details the user interface LED and its control.

Table 13. User LEDs

LED	Controlled By
DS4	IO Expander EXP1, position P7
DS3	IO Expander EXP1, position P6
DS2	IO Expander EXP1, position P5
DS1	IO Expander EXP1, position P4

3.19 Power Monitoring

The CPU board has provisions to monitor power for many of the systems core power rails. The measurement system is implemented using the TI INA226 I2C current shunt and power monitors. The INA226 device monitors both the power supply voltage and shunt current measurements. Information is connected from the INA226 devices using dedicated I2C buses. The INA226s can be controlled through an off-board module (FTDI USART, MSP430, or a similar device).

Table 14 shows a mapping of the current monitoring system. INA226 are located at each shunt location.

Table 14. Power Monitor Mapping

I2C BUS A			
I2C Addr	**Power Net**	**Shunt / Resistor**	**Description**
0x40	SMPS1_IN	5m-Ω	TPS65917 SMPS1 power input (MPU)
0x41	SMPS2_IN	10m-Ω	TPS65917 SMPS1 power input (GPU/DSP)
0x42	SMPS3_IN	10m-Ω	TPS65917 SMPS1 power input (CORE)
0x43	SMPS4_IN	10m-Ω	TPS65917 SMPS1 power input (1V8)
0x44	SMPS5_IN	10m-Ω	TPS65917 SMPS1 power input (DDR)
0x45	J6_VDD_MPU	10m-Ω	CPU MPU power rail (TPS65917 SMPS1)
0x46	J6_VDD_GPU	10m-Ω	CPU GPU/DSP/IVA (TPS65917 SMPS2)
0x47	J6_VDD_CORE	10m-Ω	CPU CORE power rail (TPS65917 SMPS3)
0x48	J6_VDD_1V8	10m-Ω	CPU 1v8 power rail(s)
0x49	EVM_VDD_1V8	10m-Ω	EVM 1v8 Peripheral Rail
0x4A	J6_VDD_DDR	10m-Ω	CPU DDR Power Rail
0x4B	EVM_VDD_DDR	10m-Ω	DDR Power Rail
I2C BUS B			
I2C Addr	**Power Net**	**Shunt / Resistor**	**Description**
0x40	VDDSHV8	10m-Ω	CPU IO Rail for SD/MMC
0x41	VDDSHV5	10m-Ω	CPU IO Rail for RTC
0x42	VDDA_PHY	10m-Ω	CPU PHY LDO Rail
0x43	VDDA_USB3v3	10m-Ω	CPU USB PHY LDO Rail
0x44	VDDA_PLL	10m-Ω	CPU PLL LDO Rail
0x45	EVM_5v0	10m-Ω	EVM 5v0 Peripheral Rail
0x46	EVM_3v3	10m-Ω	EVM 3v3 Peripheral Rail
0x47	VCCA_IN	10m-Ω	Total System power rail
0x48	EVM_12V	10m-Ω	Total System 12v power rail
0x49	1v8_PHY2	10m-Ω	CPU PHY LDO Rail

3.20 I2C Peripheral Map

Table 15 shows the list of I2C interfaces available on the EVM, with a list of device connected to each I2C interface and its corresponding device address.

Table 15. I2C Device Address Chart

CPU Board	Part No	I2C1	I2C3	I2C4	I2C5	Device Addr (7b)
EEPROM	24WC256	X				0x50
Digital Temperature Sensor	TMP102AIDRLT	X				0x48
GPIO Expander #1	PCF8575	X				0x20
GPIO Expander #2	PCF8575	X				0x21
GPIO Expander #3	PCF8575				X	0x26
MLB Connector	Connector	X				NA
LCD Interface	Connector	X				NA
COM8 Connector	Connector	X				NA
Audio Codec	TLV320AIC3106	X				0X19
Expansion Connector	Connector	X	X	X		NA
PMIC	LP8733	X				0x60
	LP8732	X				0x61
FPD Link	DS90UH925Q				X	0x1B
LI Camera	Connector				X	NA
CSI2 Camera	Connector				X	NA

3.21 GPIO List

Table 16 shows the list of SoC GPIOs. Signals used for GPIO on expansion boards are not included in this list, as they are dependent upon the application board used.

Table 16. SoC GPIO Map

Feature	Peripheral Device	EVM Bd Net	Function	SoC GPIO
Connectivity on Module	COM8 Connector	GP5[4]	BT_EN	GPIO5_4
Connectivity on Module	COM8 Connector	GP5[5]	GPS_PPS_OUT	GPIO5_5
Connectivity on Module	COM8 Connector	GP5[6]	GPS_TIME_STAMP	GPIO5_6
Connectivity on Module	COM8 Connector	GP5[7]	WLAN_IRQ	GPIO5_7
Connectivity on Module	COM8 Connector	GP5[8]	WL_EN	GPIO5_8
Media Local Bus(MLB)	MLB Connector	GP5[9]	NA	GPIO5_9
Media Local Bus(MLB)	MLB Connector	GP6_[28]	NA	GPIO6_28
IO Expander	PCF8575	PCF8575_INT	IOEXP_IRQ	GPIO3_30
Gig Ethernet	Ethernet PHY	ENET_INTSn	ENET_IRQ	GPIO6_16
LCD Touch Panel	Display Connector	GP1[15]	TS_LCD_IRQ	GPIO1_15
FPD-Link Panel	FPD-Link Txmt	VOUT2_INTB	FPDTX_IRQ	GPIO3_38
Power Mgmt	PMIC	WAKEUP3	PMIC_IRQ	GPIO1_3
SD Card	Micro-SD	MMC1_SDCD	CARD_DETECT	GPIO6_27
Test	Automated Test	GP5[0]	USER_DEFINED	GPIO5_0

NOTE: Functional signals of pinmux are not consider for this table. For more details, see the *DRA72x_TDA2Ex CPU EVM Schematic Rev D* (http://www.ti.com/lit/zip/sprr236).

3.22 IO Expander List

Table 17. I/O Expander Map

Device	Slave Address	I2C I/F	Expander IO	Netname	Description
EXP1	0b0010 000 (0x20)	I2C1	INT#	PCF8575_INT	Interrupt output to SoC
			P0	TS_LCD_GPIO1	Press Button Switch 1
			P1	TS_LCD_GPIO2	Press Button Switch 2
			P2	TS_LCD_GPIO3	Press Button Switch 3
			P3	TS_LCD_GPIO4	Press Button Switch 4
			P4	USER_LED1	User LED 1
			P5	USER_LED2	User LED 2
			P6	USER_LED3	User LED 3
			P7	USER_LED4	User LED 4
			P10	EXP_ETH0_RSTn	RGMII0 Reset
			P11	EXP_ETH1_RSTn	RGMII1 Reset
			P12	USB1-VBUS_OCN	USB1 Over Current Indication
			P13	USB2-VBUS_OCN	USB2 Over Current Indication
			P14	PCI_SW_RESETn	PCI Interface SW Reset
			P15	CON_LCD_PWR_DN	LCD Board Master power enable
			P16		Open
			P17	TMP102_ALERT	Temperature Sensor Alarm
EXP2	0b0010 001 (0x21)	I2C1	INT#	PCF8575_INT	Interrupt output to SoC
			P0	SEL_GPMC_AD_VID_S0	MUX out control signal for GPMC Vs VOUT3B vs VIN1A
			P1	USB1_ID	USB1 ID PIN
			P2	USB2_ID	USB2 ID PIN
			P3	SEL_I2C3_CAN2	MUX out control signal for I2C3 Vs DCAN2
			P4	SEL_ENET_MUX_S0	MUX out control signal for RGMII0 Vs VIN
			P5	MMC_PWR_ON	Power on regulator to MMC card
			P6	NOR_ALT_ADDRn	MUX out control signals for alternate location of GPMC control signals
			P7	SEL_GPMC_AD_VID_S2	MUX out control signal for GPMC vs VOUT3B vs VIN1A
			P10	NAND_BOOTn	NAND boot Chip select enable signal
			P11	NOR_BOOTn	NOR boot Chip select enable signal
			P12	MMC2_BOOT	MUX out control signal for GPMC Vs MMC2
			P13	QSPI_SELn	Not used, as QSPI is enabled with resistor mux
			P14	UART_SEL1_3	MUX out control signal for UART1 vs UART for terminal access
			P15	MCASP1_ENn	COM8 interface level shifter enable signal
			P16	SEL_UART3_SPI2	MUX out control signal for UART3 Vs SPI2
			P17		Open

Table 17. I/O Expander Map (continued)

Device	Slave Address	I2C I/F	Expander IO	Netname	Description
EXP3	0b0010 010 (0x26)	I2C5	P0	PM_OEn	Enable to connect PM Bus with I2C3
			P1	VIN6_SEL_S0	MUX out control signal for VIN6A and McASPx
			P2	VIN2_S0	MUX out control signal for EMAC1 & VIN2A Signals
			P3	PM_SEL	Selection to connect I2C3 to either PM bus 1 or 2
			P4	HDMI_CT_HPD	HDMI Hot Plug Detect
			P5	HDMI_LS_OE	HDMI Level Shifter Enable
			P6	VIN2_S2	MUX out control signal for VIN2A vs expansion signals
			P7		Open
			P10	SEL_CSI2n	MUX out control signal for CSI2 configuration
			P11	EXVIN2_S0	MUX out control signal for EMAC1 vs VIN2A vs expansion signals
			P12	EXVIN2_S2	MUX out control signal for EMAC1 vs VIN2A vs expansion signals
			P13	MMC3_SEL	MUX out control signal for MMC3 vs VIN2B
			P14	MMC2_BOOT_OVR_OEN	MMC2 DIP Switch Override Enable
			P15	MMC2_BOOT_OVR	MMC2 DIP Switch Override
			P16	NOR_BOOT_OVR_OEN	NOR BOOT DIP Switch Override Enable
			P17	NOR_BOOT_OVR	NOR BOOT DIP Switch Override

3.23 Configuration EEPROM

The CPU board contains a EEPROM memory device for storing and retrieving configuration information. The EEPROM provides 256Kb (or 32KBytes) of storage space, and is accessible through I2C. Device location information is located in the Table 15. The configuration ID information is programmed by the factory at the time of manufacturing, and should not be altered. Below is the configuration data format within the EEPROM.

EEPROM device used: Catalyst Semiconductor CAT24C256WI-G

I2C Bus/Addr: I2C1,0x50

Data format of the EEPROM is provided in Table 18.

Table 18. EEPROM Data Format

EEPROM Field	Byte Location	Value	Description
ID.HEADER	[3:0]	0xAA5533EE	Fixed value at start of header ID.
ID.BOARD_NAME	[19:4]	'DRA72x-TDA2Ex' (ascii)	Fixed value of 'J6ECOCPU' or 'DRA72x-TDA2Ex'
ID.VERSION_MAJOR	[21:20]	0x3	A = 0x1 B = 0x2 C = 0x3
ID.VERSION_MINOR	[23:22]	0x0	0x0 for major revision 0x1-0x15 for others
ID.CONFIG_OPTION	[27:24]	0x1E	Bit 6: 1 – EMIF2 ECC Supported, 0 – No Bit 5: 1 – EMIF2 Supported, 0 – No Bit 4: 1 – EMIF1 ECC Supported, 0 – No Bit 3: 1 – EMIF1 Supported, 0 – No Bit 2: 1 – Extended Memory EEPROM Cfg Support, 0 – No(1) Bit 1: 1 – MAC addr in EEPROM (default) Bit 0: 0 - QSPI (default), 1 - NOR
EMIF1_SIZE_BYTES	[31:28]	0x8000 0000	Memory size for EMIF1 in bytes (unsigned long)(2)
EMIF2_SIZE_BYTES	[35:32]	0x0000 0000	Memory size for EMIF2 in bytes (unsigned long)(2)
RESERVED	[55:36]	0x0	Reserved(2)
MAC_ADDR	0x7F00	00.0E.99.zz.yy.xx	Optional MAC address

(1) If Bit 2 set to 0, all EEPROM data beyond is set to 0 (not defined or used). If set to 1, the mapping is per the table.
(2) Prior to Rev C, Bytes [55:28] were reserved and set to 0x0.

For reference, a C-style coded structure is provided:

```
Struct EEPROM_ID_T
{
    Unsigned long header;        4
    Char board_name[16];        16
    Unsigned short version_major;    2
    Unsigned short version_minor;    2
    Unsigned long config_option;        4
    Unsigned long emif1_size_bytes;     4
    Unsigned long emif2_size_bytes;    4
    Char reserved[28];            20
} eeprom_id;
```

4 Signal Multiplex Logic

Due to the high level of multiplexing on the SoC (16+ levels), multiplex control logic is required to use different signals on the same SoC pins with their various functionality. The information below provides description of the logic.

An I2C-based IO expander is used to control the onboard muxes. Table 19 shows the specific bits assigned to each mux, as well as the specific settings for the various selections.

Table 19. Onboard Mux Settings and Control

MUX	Control Bits	Value	Mux Setting
A	n/a	n/a	QSPI Memory (default)
		n/a	NOR Memory (Requires resistor change)
C (RU21)	SW5.3	OFF	NOR Memory
		ON	EMMC Memory
	EXP3.P[12:11]	00	Reserved
		01	NOR Memory selected (by SW5.2)
		10	EMMC Memory selected (by SW5.3)
		11	NOR Memory selected (default)
B (RU88, RU94, RU33)	EXP2.P[7,0]	00	Reserved
		01	VIN1A to Expansion
		10	VOUT3 to LCD Panel
		11	GPMC NOR/NAND (default)
E (RU30)	EXP3.P[6,2]	00	Reserved
		01	VIN2A to LI Camera
		10	VIN2A to Expansion
		11	Reserved (default)
F (RU93)	EXP3.P[12,11]	00	Reserved
		01	VIN2A to LI Camera
		10	VIN2A to Expansion
		11	RGMII1 to Ethernet Port 1 (default)
K (RU111)	EXP2.P16	0	UART3 to COM8Q
		1	Route to Expansion (SPI2) (default)
L (RU113)	EXP2.P3	0	Route to Expansion (I2C3)
		1	Route to DCAN2 Connector (default)
J (RU95)	EXP2.P4	0	Route to Expansion (VIN1B)
		1	RGMII0 to Ethernet Port 0 (default)
M (RU117)	EXP3.P13	0	Route to Expansion (VIN2B)
		1	Route to Expansion (MMC3/legacy)(default)
G (RU96)	SW5.7	OFF	Use Default NOR Address (default)
		ON	Use Alternate NOR Address (w/ EMMC)
H (RU99)	EXP3.P1	0	Route to COM8Q (MASP3/7)
		1	Route to Expansion (McASP3/7)(default)

4.1 GPMC and QSPI Selection (Mux A)

Figure 7 is part of the SoC pinmux table for GPMC. The SoC device supports additional functions not shown in the table. The functions shown are intended to reflect those supported on the EVM. These include:

- Memory Bus (GPMC): A[18:13]
- Quad Serial Bus (QSPI): SCLK, D[3:0], CS[0], RTCLK

Pad Name	Function 1		Function 2	
gpmc_a[13]	GPMC	gpmc_a[13]	QSPI1	qspi1_rtclk
gpmc_a[14]	GPMC	gpmc_a[14]	QSPI1	qspi1_d[3]
gpmc_a[15]	GPMC	gpmc_a[15]	QSPI1	qspi1_d[2]
gpmc_a[16]	GPMC	gpmc_a[16]	QSPI1	qspi1_d[0]
gpmc_a[17]	GPMC	gpmc_a[17]	QSPI1	qspi1_d[1]
gpmc_a[18]	GPMC	gpmc_a[18]	QSPI1	qspi1_sclk
gpmc_cs[2]	GPMC	gpmc_cs[2]	QSPI1	qspi1_cs[0]

Figure 7. SoC Pinmux for GPMC and QSPI

Mux A: Selects between NOR and QSPI memory support.

NOTE: The mux is implemented using resistors. This was due to the signal rate and routing restrictions of the QSPI device. To enable the GPMC signals to NOR (shown in RED in Figure 8), the board must be modified to move resistors.

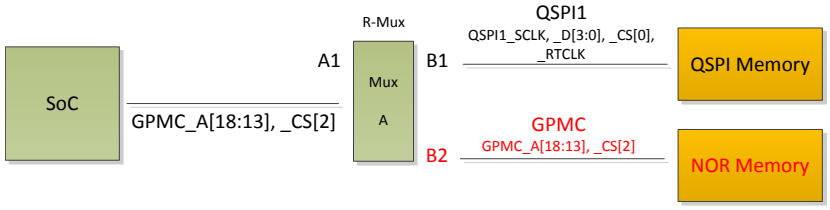


Figure 8. Mux Diagram for GPMC and QSPI

4.2 GPMC/VIN1/VOUT3 Selection (Mux B)

Figure 9 is part of the SoC pinmux table for GPMC. The SoC device supports additional functions not shown in the table. The functions shown are intended to reflect those supported on the EVM. These include:

- Memory Bus (GPMC): AD[15:0], A[12:0]
- Video Input Port (VIN1A): CLK, HSYNC, VSYNC, DE, D[23:0]
- Video Output Port (VOUT3): CLK, HSYNC, VSYNC, DE, D[23:0]
- Boot Mode Selection (SYSBOOT): SYSBOOT[15:0]

Pad Name	Function 1		Function 3		Function 4		Function 16	
gpmc_ad[0]	GPMC	gpmc_ad[0]	VIP1	vin1a_d[0]	DSS	vout3_d[0]	CHIPGLUE	sysboot0
gpmc_ad[1]	GPMC	gpmc_ad[1]	VIP1	vin1a_d[1]	DSS	vout3_d[1]	CHIPGLUE	sysboot1
gpmc_ad[2]	GPMC	gpmc_ad[2]	VIP1	vin1a_d[2]	DSS	vout3_d[2]	CHIPGLUE	sysboot2
gpmc_ad[3]	GPMC	gpmc_ad[3]	VIP1	vin1a_d[3]	DSS	vout3_d[3]	CHIPGLUE	sysboot3
gpmc_ad[4]	GPMC	gpmc_ad[4]	VIP1	vin1a_d[4]	DSS	vout3_d[4]	CHIPGLUE	sysboot4
gpmc_ad[5]	GPMC	gpmc_ad[5]	VIP1	vin1a_d[5]	DSS	vout3_d[5]	CHIPGLUE	sysboot5
gpmc_ad[6]	GPMC	gpmc_ad[6]	VIP1	vin1a_d[6]	DSS	vout3_d[6]	CHIPGLUE	sysboot6
gpmc_ad[7]	GPMC	gpmc_ad[7]	VIP1	vin1a_d[7]	DSS	vout3_d[7]	CHIPGLUE	sysboot7
gpmc_ad[8]	GPMC	gpmc_ad[8]	VIP1	vin1a_d[8]	DSS	vout3_d[8]	CHIPGLUE	sysboot8
gpmc_ad[9]	GPMC	gpmc_ad[9]	VIP1	vin1a_d[9]	DSS	vout3_d[9]	CHIPGLUE	sysboot9
gpmc_ad[10]	GPMC	gpmc_ad[10]	VIP1	vin1a_d[10	DSS	vout3_d[10]	CHIPGLUE	sysboot10
gpmc_ad[11]	GPMC	gpmc_ad[11]	VIP1	vin1a_d[11	DSS	vout3_d[11]	CHIPGLUE	sysboot11
gpmc_ad[12]	GPMC	gpmc_ad[12]	VIP1	vin1a_d[12	DSS	vout3_d[12]	CHIPGLUE	sysboot12
gpmc_ad[13]	GPMC	gpmc_ad[13]	VIP1	vin1a_d[13	DSS	vout3_d[13]	CHIPGLUE	sysboot13
gpmc_ad[14]	GPMC	gpmc_ad[14]	VIP1	vin1a_d[14	DSS	vout3_d[14]	CHIPGLUE	sysboot14
gpmc_ad[15]	GPMC	gpmc_ad[15]	VIP1	vin1a_d[15	DSS	vout3_d[15]	CHIPGLUE	sysboot15
gpmc_a[0]	GPMC	gpmc_a[0]	VIP1	vin1a_d[16	DSS	vout3_d[16]		
gpmc_a[1]	GPMC	gpmc_a[1]	VIP1	vin1a_d[17	DSS	vout3_d[17]		
gpmc_a[2]	GPMC	gpmc_a[2]	VIP1	vin1a_d[18	DSS	vout3_d[18]		
gpmc_a[3]	GPMC	gpmc_a[3]	VIP1	vin1a_d[19	DSS	vout3_d[19]		
gpmc_a[4]	GPMC	gpmc_a[4]	VIP1	vin1a_d[20	DSS	vout3_d[20]		
gpmc_a[5]	GPMC	gpmc_a[5]	VIP1	vin1a_d[21	DSS	vout3_d[21]		
gpmc_a[6]	GPMC	gpmc_a[6]	VIP1	vin1a_d[22	DSS	vout3_d[22]		
gpmc_a[7]	GPMC	gpmc_a[7]	VIP1	vin1a_d[23	DSS	vout3_d[23]		
gpmc_a[8]	GPMC	gpmc_a[8]	VIP1	vin1a_hsyr	DSS	vout3_hsync		
gpmc_a[9]	GPMC	gpmc_a[9]	VIP1	vin1a_vsyn	DSS	vout3_vsync		
gpmc_a[10]	GPMC	gpmc_a[10]	VIP1	vin1a_de0	DSS	vout3_de		
gpmc_a[11]	GPMC	gpmc_a[11]	VIP1	vin1a_fld0	DSS	vout3_fld		
gpmc_a[12]	GPMC	gpmc_a[12]						
gpmc_cs[3]	GPMC	gpmc_cs[3]	VIP1	vin1a_clk0	DSS	vout3_clk		

Figure 9. SoC Pinmux for GPMC/VIN1/VOUT3

Mux B: Selects between NOR/NAND memories, FPD Linkl for video, and expansion, as shown in Figure 10. The selection is made using the IO expander #2, and bits P7 and P0. The defaults are set to enable GPMC to NOR/NAND memories, required for SYSBOOT mode latching.

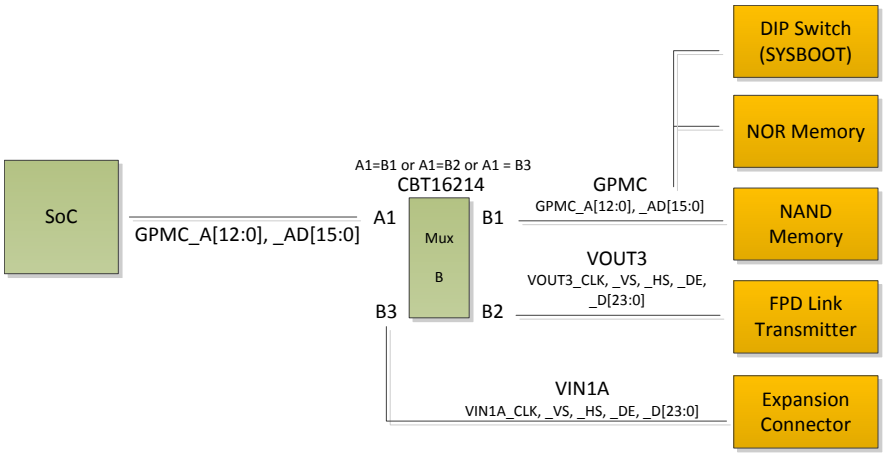


Figure 10. Mux Diagram for GPMC/VIN1/VOUT3

4.3 GPMC and EMMC Selection (Mux C)

Figure 11 is part of the SoC pinmux table for GPMC. The SoC device supports additional functions not shown in the table. The functions shown are intended to reflect those supported on the EVM. These include:

- Memory Bus (GPMC): A[27:19], CS1
- EMMC Memory (MMC2): CLK, CMD, D[7:0]

Pad Name	Function 1		Function 2	
gpmc_a[19]	GPMC	gpmc_a[19]	MMC2	mmc2_dat[4]
gpmc_a[20]	GPMC	gpmc_a[20]	MMC2	mmc2_dat[5]
gpmc_a[21]	GPMC	gpmc_a[21]	MMC2	mmc2_dat[6]
gpmc_a[22]	GPMC	gpmc_a[22]	MMC2	mmc2_dat[7]
gpmc_a[23]	GPMC	*gpmc_a[23]*	MMC2	mmc2_clk
gpmc_a[24]	GPMC	*gpmc_a[24]*	MMC2	mmc2_dat[0]
gpmc_a[25]	GPMC	*gpmc_a[25]*	MMC2	mmc2_dat[1]
gpmc_a[26]	GPMC	*gpmc_a[26]*	MMC2	mmc2_dat[2]
gpmc_a[27]	GPMC	*gpmc_a[27]*	MMC2	mmc2_dat[3]
gpmc_cs[1]	GPMC	gpmc_cs[1]	MMC2	mmc2_cmd

Figure 11. SoC Pinmux for GPMC/EMMC

Mux C: Selects between NOR memory and EMMC memory, as shown in Figure 12. The selection is made using the IO expander #3, and bits P15 and P14. If booting from EMMC, the DIP Switch SW5 position 3 is used to select interface (by default).

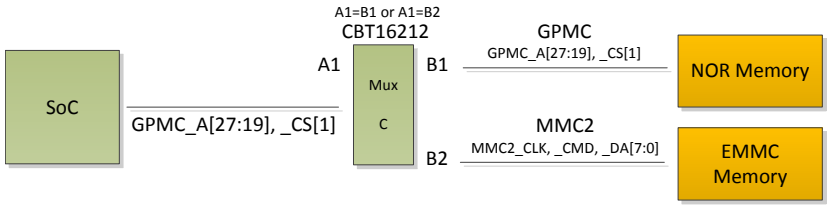


Figure 12. Mux Diagram for GPMC and EMMC

4.4 VIN2A Selection (Mux E)

Figure 13 is part of the SoC pinmux table for VIN2A. The SoC device supports additional functions not shown in the table. The functions shown are intended to reflect those supported on the EVM. These include:

- Video Input Port (VIN2A): CLK, HSYNC, VSYNC, DE, D[9:0]

Pad Name	Function 1		Function 4		Function 5		Function 6	
vin2a_clk0	VIP1	vin2a_clk0			DSS	vout2_fld	DEBUGSS	emu5
vin2a_de0	VIP1	vin2a_de0	VIP1	vin2b_de1	DSS	vout2_de	DEBUGSS	emu6
vin2a_fld0	VIP1	vin2a_fld0			DSS	vout2_clk	DEBUGSS	emu7
vin2a_hsync0	VIP1	vin2a_hsync0	VIP1	vin2b_hsync1	DSS	vout2_hsync	DEBUGSS	emu8
vin2a_vsync0	VIP1	vin2a_vsync0	VIP1	vin2b_vsync1	DSS	vout2_vsync	DEBUGSS	emu9
vin2a_d[0]	VIP1	vin2a_d[0]			DSS	vout2_d[23]	DEBUGSS	emu10
vin2a_d[1]	VIP1	vin2a_d[1]			DSS	vout2_d[22]	DEBUGSS	emu11
vin2a_d[2]	VIP1	vin2a_d[2]			DSS	vout2_d[21]	DEBUGSS	emu12
vin2a_d[3]	VIP1	vin2a_d[3]			DSS	vout2_d[20]	DEBUGSS	emu13
vin2a_d[4]	VIP1	vin2a_d[4]			DSS	vout2_d[19]	DEBUGSS	emu14
vin2a_d[5]	VIP1	vin2a_d[5]			DSS	vout2_d[18]	DEBUGSS	emu15
vin2a_d[6]	VIP1	vin2a_d[6]			DSS	vout2_d[17]	DEBUGSS	emu16
vin2a_d[7]	VIP1	vin2a_d[7]			DSS	vout2_d[16]	DEBUGSS	emu17
vin2a_d[8]	VIP1	vin2a_d[8]			DSS	vout2_d[15]	DEBUGSS	emu18
vin2a_d[9]	VIP1	vin2a_d[9]			DSS	vout2_d[14]	DEBUGSS	emu19

Figure 13. SoC Pinmux for VIN2A and EMU

Mux E: Selects between LI camera and expansion, as shown in Figure 14. The selection is made using the IO expander #3, and bits P6 and P2. The default mode is set to expansion.

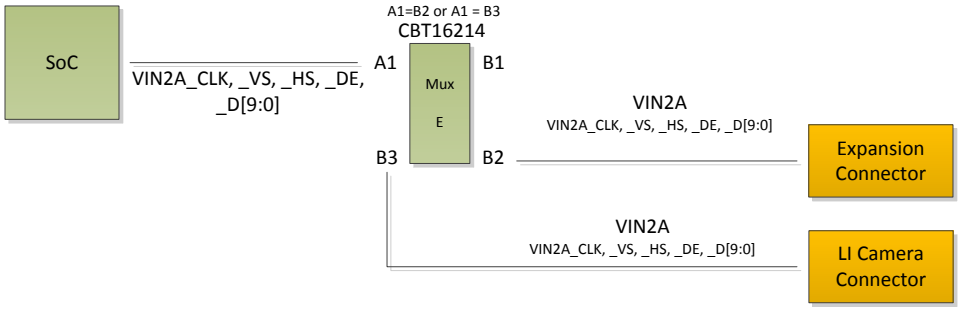


Figure 14. Mux Diagram for VIN2A and EMU

4.5 VIN2A and RGMII1 Selection (Mux F)

Figure 15 is part of the SoC pinmux table for VIN2A. The SoC device supports additional functions not shown in the table. The functions shown are intended to reflect those supported on the EVM. These include:

- Video Input Port (VIN2A): D[23:10]
- Gig Ethernet (RGMII1): TXC, TXCTL, TXD[3:0], RXC, RXCTL, RXD[3:0]
- Management Data I/O (MDIO): MCLK, D

Pad Name	Function 1		Function 4		Function 5	
vin2a_d[10]	VIP1	vin2a_d[10]	EMAC	*mdio_mclk*	DSS	vout2_d[13]
vin2a_d[11]	VIP1	vin2a_d[11]	EMAC	*mdio_d*	DSS	vout2_d[12]
vin2a_d[12]	VIP1	vin2a_d[12]	EMAC	rgmii1_txc	DSS	vout2_d[11]
vin2a_d[13]	VIP1	vin2a_d[13]	EMAC	rgmii1_txctl	DSS	vout2_d[10]
vin2a_d[14]	VIP1	vin2a_d[14]	EMAC	rgmii1_txd[3]	DSS	vout2_d[9]
vin2a_d[15]	VIP1	vin2a_d[15]	EMAC	rgmii1_txd[2]	DSS	vout2_d[8]
vin2a_d[16]	VIP1	vin2a_d[16]	EMAC	rgmii1_txd[1]	DSS	vout2_d[7]
vin2a_d[17]	VIP1	vin2a_d[17]	EMAC	rgmii1_txd[0]	DSS	vout2_d[6]
vin2a_d[18]	VIP1	vin2a_d[18]	EMAC	rgmii1_rxc	DSS	vout2_d[5]
vin2a_d[19]	VIP1	vin2a_d[19]	EMAC	rgmii1_rxctl	DSS	vout2_d[4]
vin2a_d[20]	VIP1	vin2a_d[20]	EMAC	rgmii1_rxd[3]	DSS	vout2_d[3]
vin2a_d[21]	VIP1	vin2a_d[21]	EMAC	rgmii1_rxd[2]	DSS	vout2_d[2]
vin2a_d[22]	VIP1	vin2a_d[22]	EMAC	rgmii1_rxd[1]	DSS	vout2_d[1]
vin2a_d[23]	VIP1	vin2a_d[23]	EMAC	rgmii1_rxd[0]	DSS	vout2_d[0]

Figure 15. SoC Pinmux for VIN2A and RGMII1

Mux F: Selects between Gig Ethernet, expansion, and combines with Mux E to support LI camera. The selection is made using the IO expander #3, and bits P12 and P11, with the default set to Gig Ethernet.

The MDIO mux setting (shown in RED in Figure 16) is only used if RGMII0 port is not selected. Otherwise, the MDIO function is provided by other pins. The mux selection for MDIO is automatic, based on the RGMII0 mux setting.

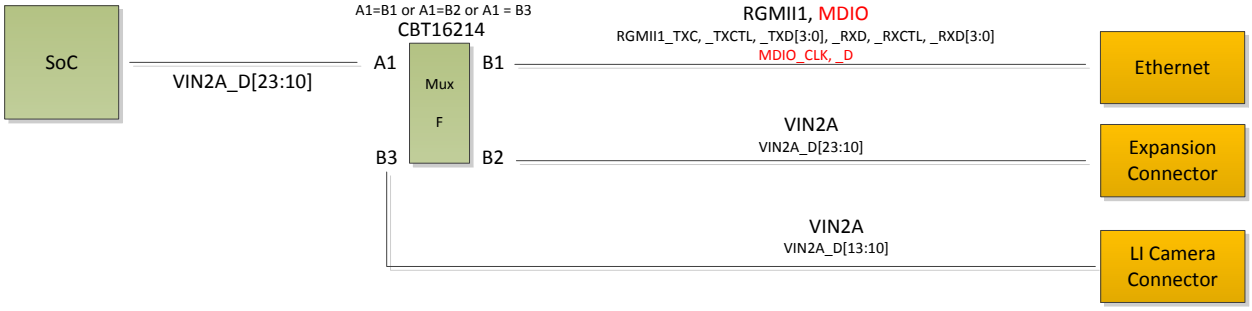


Figure 16. Mux Diagram for VIN2A and RGMII1

4.6 RGMII0 and VIN1B Selection (Mux J)

Figure 17 is part of the SoC pinmux table for RGMII0. The SoC device supports additional functions not shown in the table. The functions shown are intended to reflect those supported on the EVM. These include:

- Gig Ethernet (RGMII0): TXC, TXCTL, TXD[3:0], RXC, RXCTL, RXD[3:0]
- Management Data I/O (MDIO): MCLK, D
- Video Input Port (VIN1B): CLK, HSYNC, VSYNC, DE, [7:0]

Pad Name	Function 1		Function 6	
mdio_mclk	EMAC	mdio_mclk	VIP1	vin1b_clk1
mdio_d	EMAC	mdio_d	VIP1	vin1b_d[0]
uart3_rxd	UART3	uart3_rxd	VIP1	vin1b_d[1]
uart3_txd	UART3	uart3_txd	VIP1	vin1b_d[2]
rgmii0_txc	EMAC	rgmii0_txc	VIP1	vin1b_d[3]
rgmii0_txctl	EMAC	rgmii0_txctl	VIP1	vin1b_d[4]
rgmii0_txd[3]	EMAC	rgmii0_txd[3]	VIP1	vin1b_de1
rgmii0_txd[2]	EMAC	rgmii0_txd[2]	VIP1	vin1b_hsync1
rgmii0_txd[1]	EMAC	rgmii0_txd[1]	VIP1	vin1b_vsync1
rgmii0_txd[0]	EMAC	rgmii0_txd[0]		
rgmii0_rxc	EMAC	rgmii0_rxc	VIP1	vin1b_d[5]
rgmii0_rxctl	EMAC	rgmii0_rxctl	VIP1	vin1b_d[6]
rgmii0_rxd[3]	EMAC	rgmii0_rxd[3]	VIP1	vin1b_d[7]
rgmii0_rxd[2]	EMAC	rgmii0_rxd[2]		
rgmii0_rxd[1]	EMAC	rgmii0_rxd[1]		
rgmii0_rxd[0]	EMAC	rgmii0_rxd[0]	VIP1	vin1b_fld1

Figure 17. SoC Pinmux for RGMII0 and VIN1B

Mux J: Selects between Gig Ethernet and expansion, as shown in Figure 18. The selection is made using the IO expander #2 and bit P4, defaulting to Gig Ethernet.

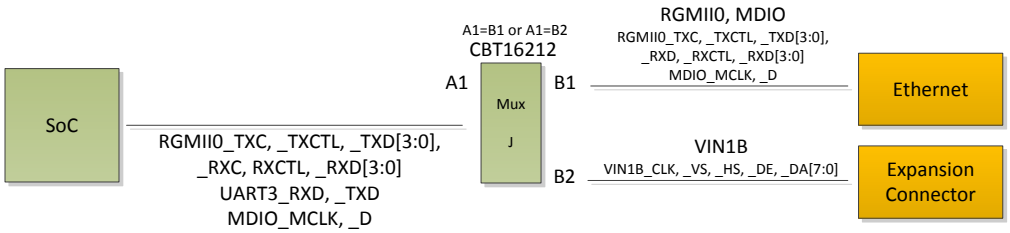


Figure 18. Mux Diagram for RGMII0 and VIN1B

4.7 SPI2 and UART3 Selection (Mux K)

Figure 19 is part of the SoC pinmux table for SPI2. The SoC device supports additional functions not shown in the table. The functions shown are intended to reflect those supported on the EVM. These include:

- SPI Serial Bus (SPI2): SCLK, D[1:0], CS[0]
- UART Serial Bus (UART3): TXD, RXD, CTSN, RTSN

Pad Name	Function 1		Function 2	
spi2_sclk	SPI2	spi2_sclk	UART3	uart3_rxd
spi2_d[1]	SPI2	spi2_d[1]	UART3	uart3_txd
spi2_d[0]	SPI2	spi2_d[0]	UART3	uart3_ctsn
spi2_cs[0]	SPI2	spi2_cs[0]	UART3	uart3_rtsn

Figure 19. SoC Pinmux for SPI2 and UART3

Mux K: Selects between Bluetooth (COM8Q module) and expansion interface, as shown in Figure 20. The selection is made using the IO expander #2 and bits P16, defaulting to expansion.

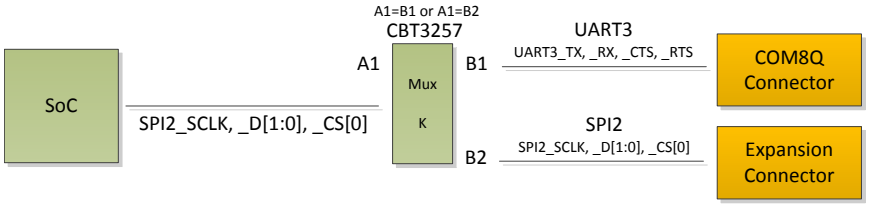


Figure 20. Mux Diagram for SPI2 and UART3

4.8 DCAN2 and I2C3 Selection (Mux L)

Figure 21 is part of the SoC pinmux table for DCAN2. The SoC device supports additional functions not shown in the table. The functions shown are intended to reflect those supported on the EVM. These include:

- Digital CAN Bus (DCAN2): TX, RX
- I2C Serial Bus (I2C3): SCL, SDA

Pad Name	Function 3		Function 10	
gpio6_14	DCAN2	dcan2_tx	I2C3	i2c3_sda
gpio6_15	DCAN2	dcan2_rx	I2C3	i2c3_scl

Figure 21. SoC Pinmux for DCAN2

Mux L: Selects between the DCAN2 header and expansion interface, as shown in Figure 22. The selection is made using the IO expander #2 and bits P3, defaulting to on-board DCAN header.

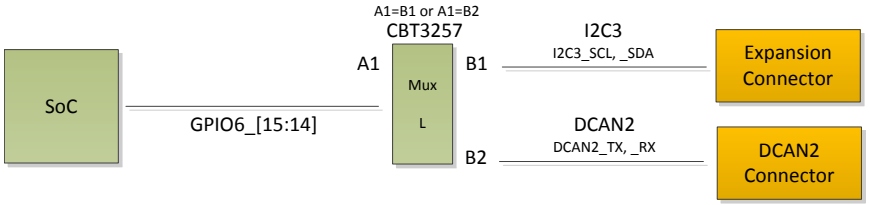


Figure 22. Mux Diagram for DCAN2 and I2C

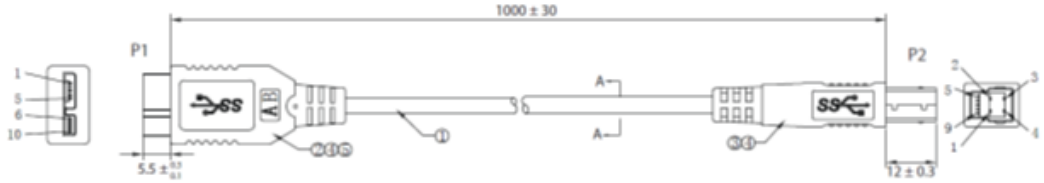
5 USB3-Supported Configurations

The following USB3.x combinations are supportable:

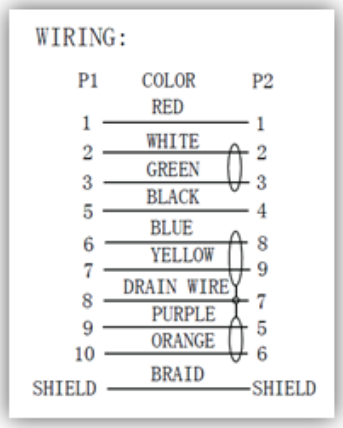
- Micro-A plug to standard-b plug
  - Connect to hub or external drive or device that has a standard-B receptacle
- Micro-A plug to micro-B plug
  - EVM connects to hub or external drive or device that has a micro-B receptacle
  - Host connects to the EVM acting as a device
- Standard-A plug to Micro-B plug
  - Host connects to the EVM acting as a device

5.1 Option 1: Micro-A Plug to Standard-B Plug

Use a USB3.0 micro-A to standard-B and USB3.0 hub, as the SIIG one shown in Figure 23.



uEVM5432 side HUB side



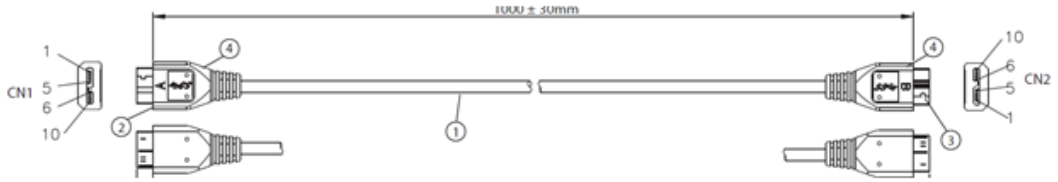
3023009-01M USB 3.0 Micro-AB TO Standard-B 1m (3.28')

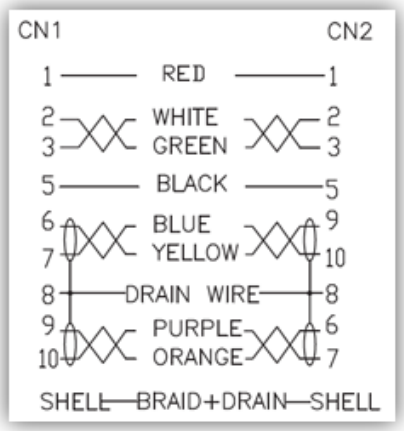
Qualtek SIIG **JU-H40312-S1**4-port USB3.0 Super Speed USB Hub

Figure 23. Option 1

5.2 Option 2: Micro-A Plug to Micro-B Plug

Use a USB3.0 micro-A to micro-B and USB3.0 hub, as the IOGEAR one shown in Figure 24.





Qualtek **3023007-01M** USB3.0 Micro-AB to Micro-B 1m (3.28')

IOGEAR **GUH374** 4-port USB3.0 HUB

Figure 24. Option 2

5.3 Option 3: Standard-A Plug to Micro-B Plug

Use a USB3.0 micro-B to standard-A. Host PC connects to the EVM acting as a device, as shown in Figure 25.

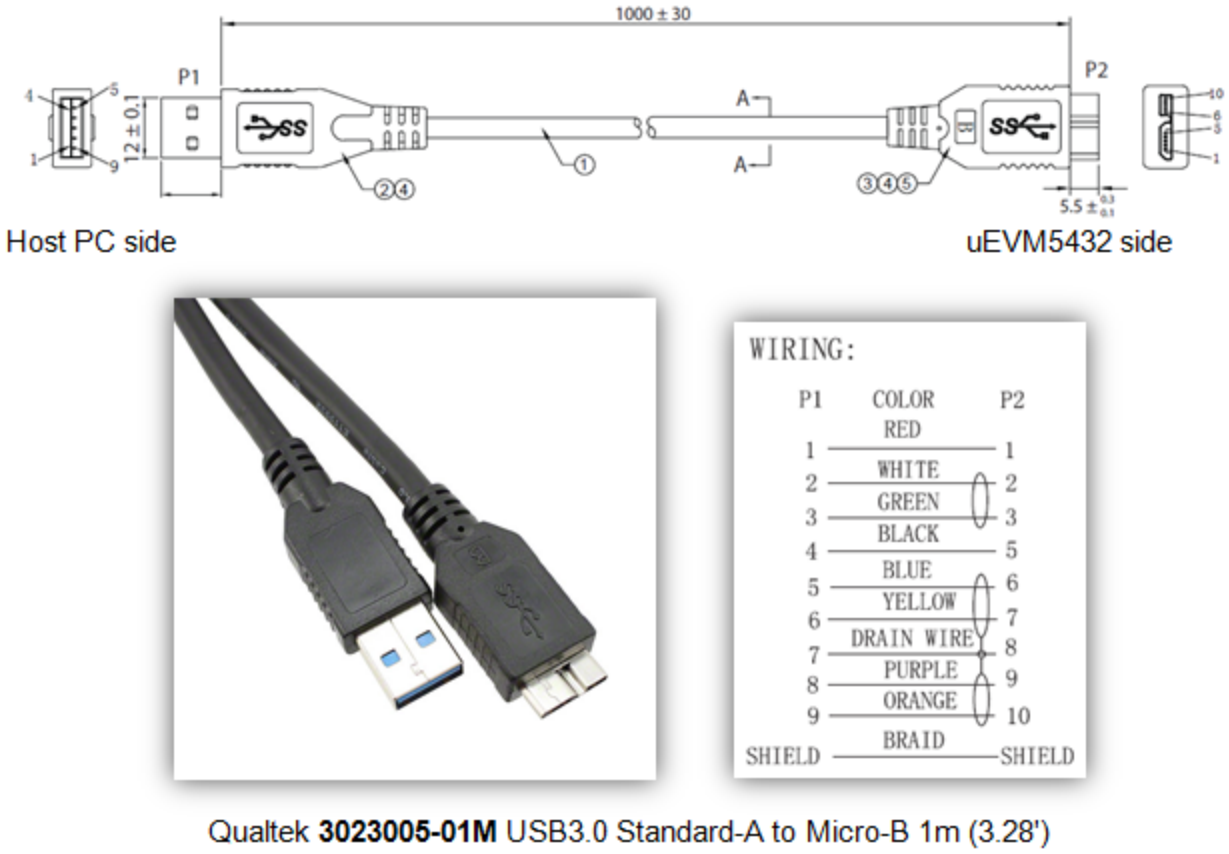


Figure 25. Option 3

6 References

- *DRA72x_TDA2Ex CPU EVM PCB Rev D*
- *DRA72x_TDA2Ex CPU EVM Schematic Rev D*
- *DRA72x_TDA2Ex CPU EVM BOM Rev D*
- *DRA72x_TDA2Ex CPU EVM CPU Assembly Drawing Rev D*
- *DRA72x_TDA2Ex CPU EVM CPU PCB Drawing Rev D*

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      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

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If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

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