WHITE PAPER

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TEXAS INSTRUMENTS

Efficient fixed- and floating-point code execution on the TMS320C674x core delivers faster code development and reduces system cost with improved performance

Executive summary

DSP chip design has followed two distinct paths – utilizing either fixed-point or floating-point instruction sets to create processors targeted at different applications and performance goals. Floating-point DSPs deliver high dynamic range, high precision and a simplified programming environment. Additionally, since a majority of PC-based development tools generate floating-point code, developers can easily migrate from PC-based development environments to DSP. Fixed-point devices, on the other hand, traditionally dominate markets and applications in which low power, low cost and a high degree of connectivity with peripherals are paramount. With the new TMS320C674x core from Texas Instruments (TI), that handles both fixed- and floating-point operations, designers now have access to a new breed of signal-processing platforms that reduce bill of materials (BOM) cost, facilitate faster time-to-market and deliver a unified software development environment.

The TMS320C674x core is not a dual-core implementation. It is a single core that combines the capabilities of the floating-point TMS320C67x+ core and fixed-point TMS3320C64x+™ core. This means the C674x instruction set is a superset of the C64x+™ instruction set and C67x+ instruction set. On every instruction cycle, the C674x can either execute the advanced fixed-point instructions supported by the C64x+ core, the floating-point instructions supported by the C67x+ core, or both.

The first TI chips based on the C674x core (TMS320C6742, TMS320C6743, TMS320C6745, TMS320C6746, TMS320C6747 and TMS320C6748 DSPs, OMAP-L137 and OMAP-L138 processors) add a set of carefully selected peripherals to complement varying end applications. For example, the C6748 DSP has an integrated universal parallel port (uPP), Serial ATA (SATA), video interface, 10/100 Ethernet MAC (EMAC), USB 2.0/1.1 and UART for connectivity as well as a memory card (MMC/SD), NAND and USB for data storage. This results in a unique, highly-integrated platform that speeds software development by eliminating the need for additional external peripherals.

Figure 1 shows the C674x core and the peripherals integrated into the C6748 DSP.

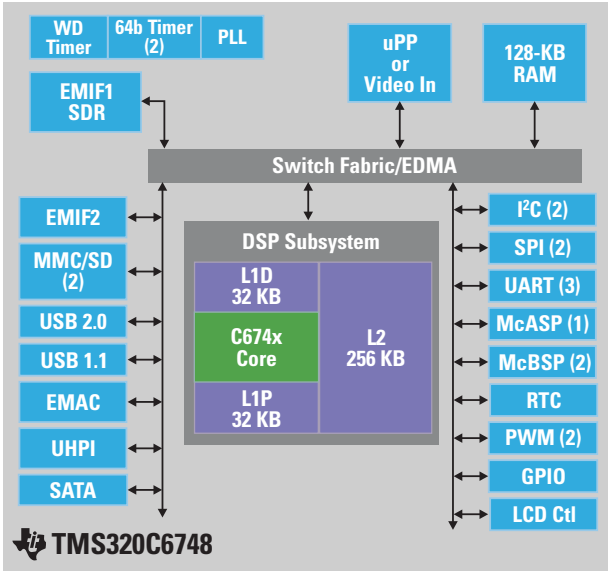

Figure 1. TMS320C6748 DSP block diagram

Processors based on the C674x core are upward code compatible with all TMS320C6000™ fixed- and floating-point devices. The C674x core provides several cost- and time-saving features. It also provides features that boost performance. Key features are listed below:

- Native support for IEEE 754 single- and double-precision floating-point formats
- An advanced software pipeline loop (SPLOOP) buffer
- Enhanced system events handling including support of exceptions
- Improved cache coherence mechanism
- A two-level system of privileged program execution with supervisor and user mode
- An internal DMA controller

Performance enhancements

The C674x generation's ability to execute both fixed-point and floating-point math adds a new dimension to the capabilities available to the algorithm developer. By selectively using the advanced fixed-point instruction set and the floating-point instruction set, the developer can achieve significantly higher performance for their algorithm.

Availability of advanced fixed-point instruction set in combination with floating-point support enhances the quality and performance of key audio codecs. For example, there is a 20 to 30 percent improvement with the C674x core over C674x+ core for the Digital Theatre System-HD (DTS-HD) audio codec. These improvements free up processing bandwidth that can be used for innovation and differentiation for applications like set-top boxes, portable medical diagnostics, public safety radios, power protection systems and many more.

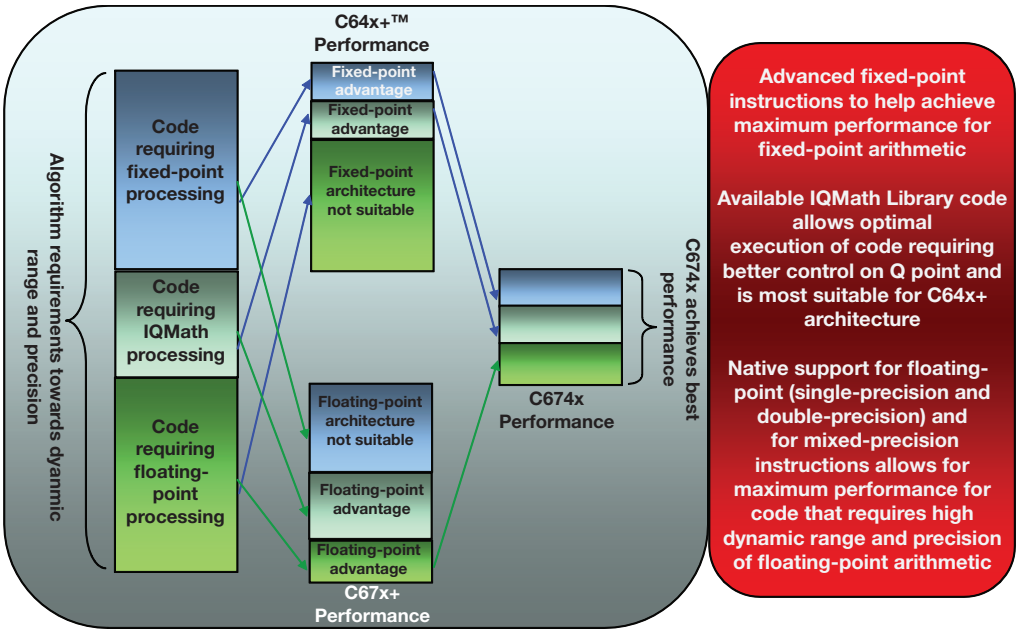

Figure 2.

To optimize floating-point performance, the C674x core implements native support for IEEE 754 single-precision and double-precision instructions. In addition to conforming to the IEEE standard, mixed-precision instructions result in highest-performance audio algorithms, which in turn deliver the highest-quality sound.

Fixed-point performance is significantly enhanced through the C674x instruction set, which includes support for the following operations per clock cycle: two 32 × 32-bit multiplies; four 16 × 16-bit multiplies or eight 8 × 8-bit multiplies. Additional instructions are included to support complex multiplies allowing up to eight 16-bit multiply/add/subtracts per clock cycle.

Memory utilization always plays a major role in achieving top performance metrics and architectural flexibility is a key feature for optimizing memory utilization. The C674x core implements a memory architecture in which the L1 or L2 memories can be configured as cache for flexibility and ease of development but can also be configured as RAM for more control and improved performance. The configuration can be changed dynamically thus providing additional flexibility.

Core enhancements result in performance improvements for core signal-processing kernels that are key to various applications, such as power-protection systems, software-defined radios and home theatre systems. For instance, with a single-precision floating-point complex-FFT kernel, there is a 20 percent performance improvement with the C674x core when compared to the C67x+ core.

Code size

Software pipelining is a technique that takes advantage of the eight execution units of the C674x CPU to schedule instructions from a loop so that multiple iterations of the loop execute in parallel. The C674x core includes a software pipeline buffer that implements the software pipelining in hardware.

The software pipeline loop (SPLOOP) feature offers several advantages. For example, employing software pipelining requires a prolog (the number of cycles “getting ready” for the loop) and epilog (the number of cycles spent “cleaning up” after the loop is completed). Previously, the prolog and epilog required additional code to be inserted. With hardware support, offered by SPLOOP, there is no need to explicitly code the prolog and epilog. As a result, code size is significantly reduced.

Two additional SPLOOP benefits are: (1) memory bandwidth and power requirements are reduced because instructions in the loop do not need to be fetched on each cycle and (2) the C674x core’s SPLOOP implementation allows the kernel to be interrupted, which results in lower interrupt latency (non-SPLOOP kernels in most cases cannot be interrupted).

Code size is further reduced by adding support that replaces 32-bit instructions with 16-bit compact equivalents. This feature has been added without having a negative impact on either functionality or speed. Additionally, the code-generation tools automatically leverage the instruction packing feature of the C674x core to provide code size equivalence for eight instructions executed serially or in parallel. In addition to reducing code size, this feature speeds program fetches and reduces power consumption.

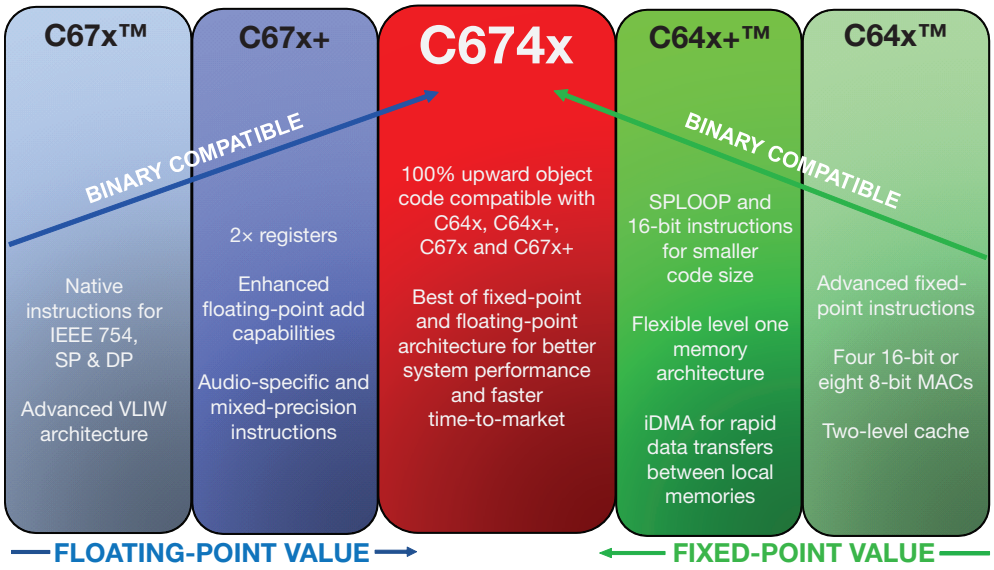

Figure 3.

Simplified code development

Typically, signal-processing algorithms are developed on host development platforms because they commonly support visual-programming interfaces. The generated code from these development platforms is typically using floating-point arithmetic but for cost and performance reasons, system developers are usually constrained to choose fixed-point DSPs when migrating to an embedded platform.

The downside of this practice is the significant effort required to modify floating-point code to fixed-point. The continuing cost of code maintenance for two platforms afterwards is also something designers would prefer to avoid. The C674x DSP's native support for industry standard floating-point formats – it supports IEEE 754 single-precision and double-precision floating-point instructions – makes the migration to an embedded platform virtually transparent to the algorithm designer.

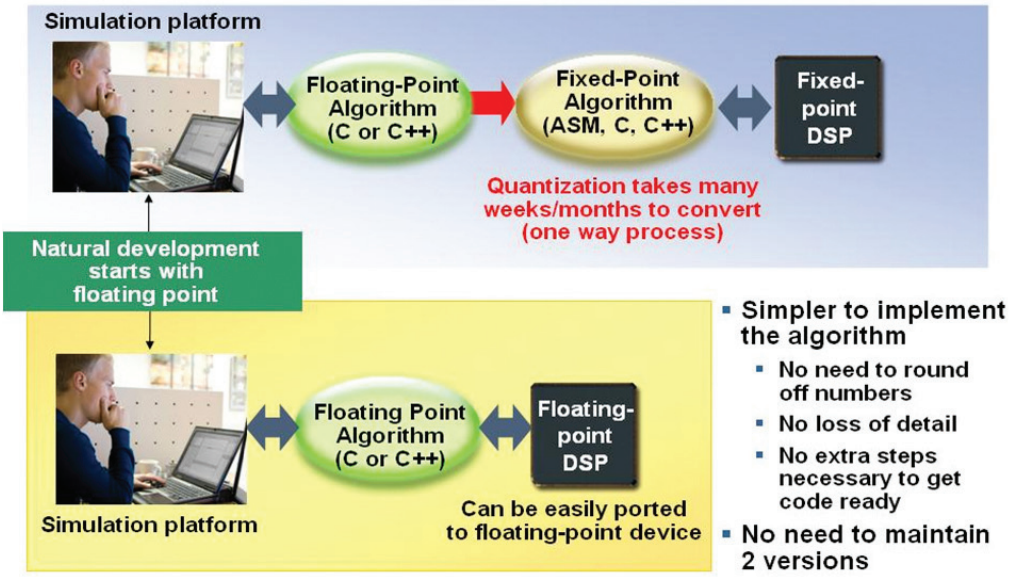

Figure 4.

Faster time-to-market

Cache coherence, privileged program execution, an internal DMA (iDMA) controller and support for non-aligned memory access all contribute to making it easier for designers to develop code for the C674x platform.

- The C674x core supports two-level cache memory architecture. Cache coherence feature increases system performance by automatically synchronizing the C674x core's internal cache and level two memory.
- Privileged program execution allows the ability to design more robust and safe end equipments, particularly in conjunction with exceptions support. Also, it allows the system to implement features such as memory protection. These features not only help make the system robust, they also reduce the development time by aiding in the debug of complex system issues during development phase.
- When something unexpected happens, the last thing a designer wants the chip to do is to end up in a state from which it can't recover. By implementing exceptions handling in its CPU, the C674x DSP provides recovery mechanisms. Support consists of error detection and subsequent redirection to error-handling routines, thus saving the designer time and resources to debug the issue. Support includes exceptions generated inside or outside the CPU.
- The internal DMA (iDMA) controller is a dedicated DMA engine for the CPU. The primary advantage of iDMA is that it handles data transfers between the L2 RAM and the faster L1D data memory without requiring CPU intervention. Since it operates in the background of CPU processing, latency is reduced and stalls due to slow cache response are minimized. The iDMA controller also provides a fast means of paging data sections to any memory-mapped RAM local to the CPU.
- Efficient access of data is an important factor in optimizing processor performance. Access of aligned 32-bit (word) and 64-bit (double word) data in most processors is efficient. However, performance is degraded for non-aligned data array accesses because unaligned accesses require multiple load and store operations. The C674x core has added support for these non-aligned data accesses. In addition to restoring performance, this feature also reduces code size because multiple load/store instructions are no longer required.

Conclusion

Until now, system designers have had to choose between the benefits of floating-point and fixed-point architectures. Fixed-point devices were typically less expensive and consumed less power but did not offer the mathematical precision and dynamic range of floating-point devices.

The increased usage of PC-based algorithm development tools complicated the choice. Since these tools develop floating-point algorithms, system developers had to convert them to fixed point to run on fixed-point DSPs and maintain two versions of the code through product generations and updates.

The C674x core resolves these long-standing design issues by supporting both fixed- and floating-point operations. It ushers in a new breed of DSPs that combine high precision, dynamic range and ease-of-use with low-power, cost-efficient connectivity.

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