Technical Article

A Survival Guide to Scaling Your PLL Loop Filter Design

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Let's say that you have already spent some time optimizing your phase-locked loop (PLL) by iteratively massaging the phase margin and loop bandwidth. Unfortunately, you may still be unable to get a good compromise between phase noise, spurs and lock time. Frustrated? Ready to give up? Wait! Have you ever played around with the gamma optimization parameter?

Gamma Optimization Parameter

Gamma is a variable with a value greater than zero. When gamma equals 1, phase margin will be maximized at the loop bandwidth (Figure 1). Many loop-filter design techniques assume a gamma value of 1, which is a good starting point, but there is further room for optimization.

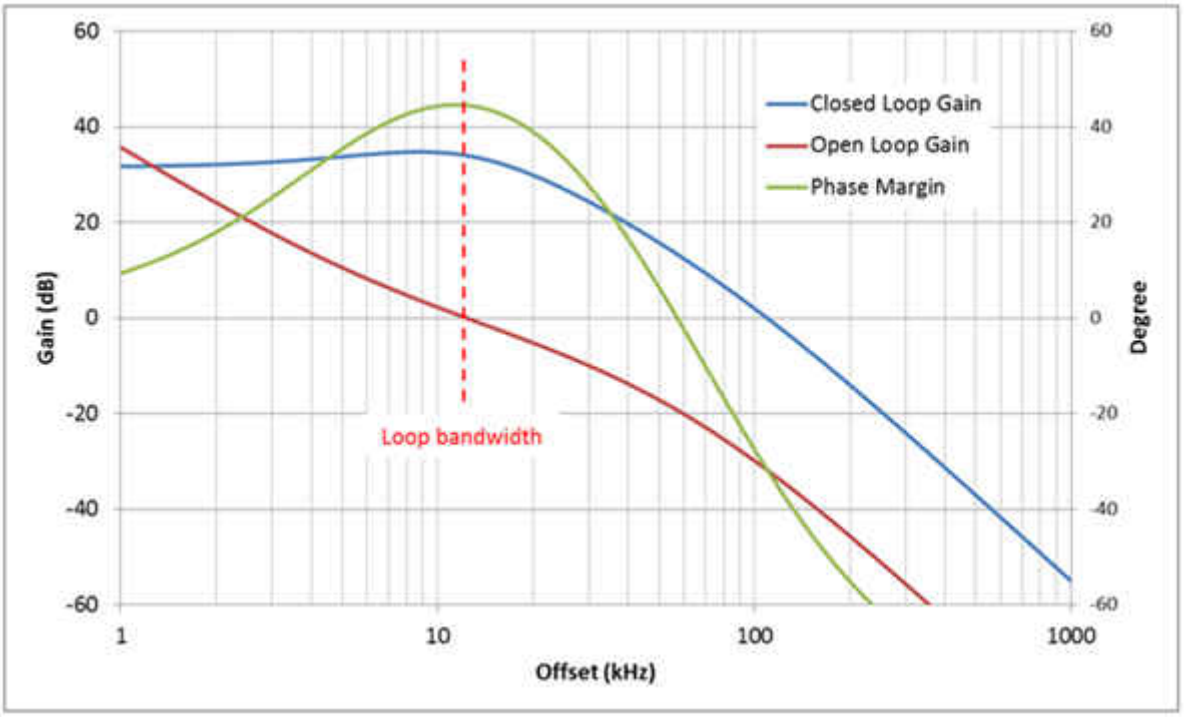

Figure 1. Bode Plot with Gamma Equal to 1

Gamma is useful in optimizing in-band phase noise, especially peaking due to the voltage-controlled oscillator (VCO). Furthermore, if you are not able to get a higher loop bandwidth due to phase-detector frequency constraints and charge-pump current, gamma will help you unlock the maximum achievable loop bandwidth. Unfortunately, if you make gamma large, it degrades lock time severely.

Figure 2 shows the effect of gamma on phase noise. Loop bandwidth and phase margin are the same, while gamma is different. With a higher gamma, the peaking of the VCO will be smaller because the flatness of the noise-shaping loop filter increases.

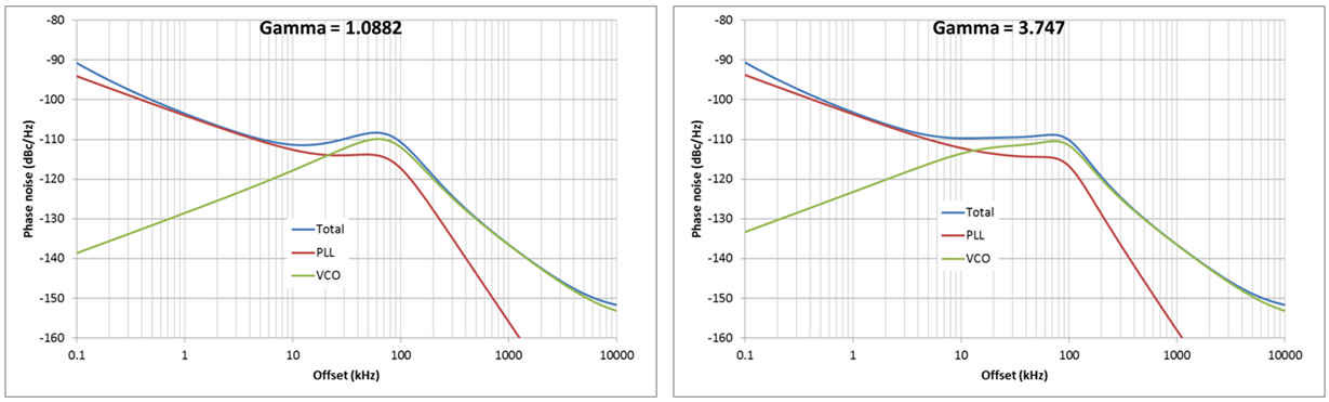

Figure 2. Phase Noise vs. Gamma at 1.0882 (a); Phase Noise vs. Gamma at 3.747 (b)

Figure 3 shows the maximum achievable loop bandwidth vs. different gamma values with a second-order loop filter. The phase-detector frequency as well as the charge-pump current remain unchanged.

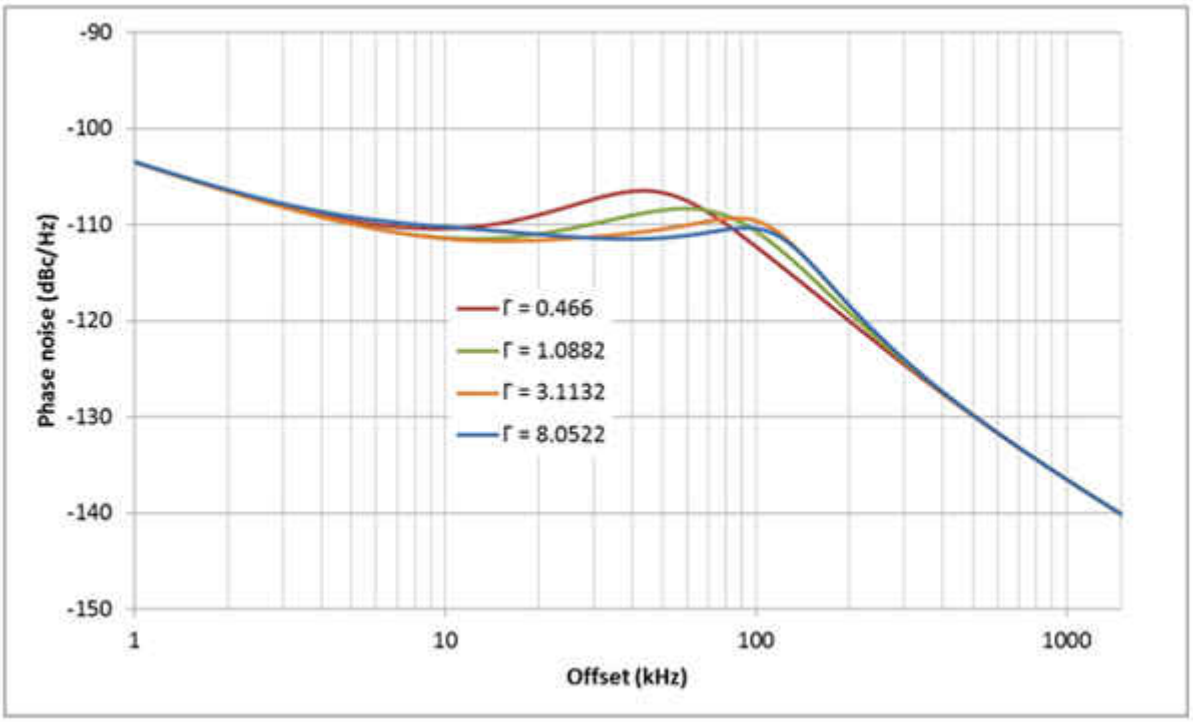

Figure 3. Loop Bandwidth vs. Gamma

If the design target is a 100kHz loop bandwidth with a 45-degree phase margin, when gamma is restricted to 1, you can only get a maximum loop bandwidth of 79kHz. However, if you can accept a higher gamma – for example, gamma equals 8 – you will be able to meet the design target. Now the loop bandwidth becomes 96.6kHz with a 43.4-degree phase margin.

There is a penalty for a higher gamma: a longer required lock time. Figure 4 shows the lock time of a 200MHz frequency jump with different gamma values; loop bandwidth and phase margin are unchanged. When the gamma and loop bandwidth equal 1 and 3.7 and the settle tolerance is within ±100Hz, the simulated lock time values equal 46.5µs and 118µs, respectively.

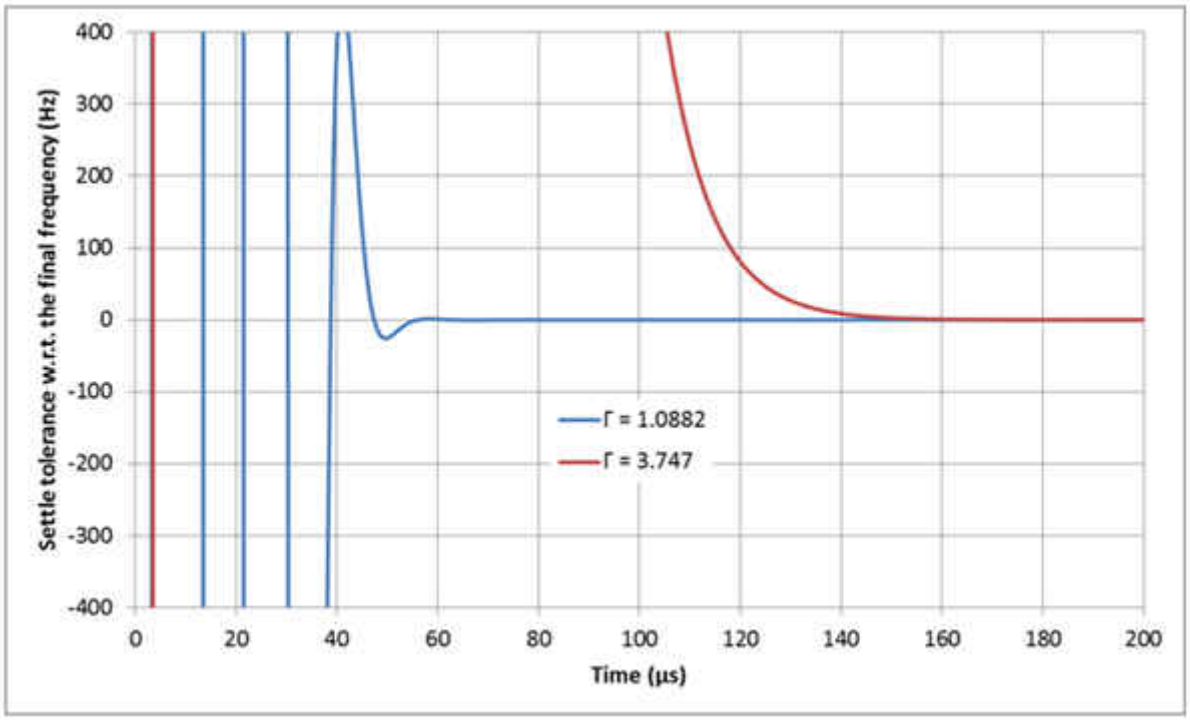

Figure 4. Lock Time vs. Gamma

Use Case Example

As long as the gamma optimization parameter is not restricted to 1, you have more freedom to get the best out of your PLL loop. For example, if minimum jitter is the goal, usually you will make the loop bandwidth and phase margin higher. If gamma equals 1, you may not be able to get desirably high loop bandwidth because the peak of the phase margin response is coincident with the loop bandwidth. In that situation, you can sacrifice lock time by designing for a gamma greater than 1. As such, you will be able to get a higher loop bandwidth.

Learn how to calculate your gamma and PLL values quickly with the PLLatinum™ simulator tool. Select Advanced in the Feature Level check box to unlock the gamma optimization parameter option.

Additional Resources

- Download the LMX2592 data sheet.
- Check out these design tools:
  - Clocks and synthesizers (TICS) programming software.
  - CodeLoader software for design register programming.

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