Technical Article
Decrease Power Consumption with an LDO

Texas Instruments

Chonghyuk Kwon

A low-dropout regulator (LDO) can function as a DC linear voltage regulator at an output voltage very close to the supply voltage, which is an important factor in decreasing power dissipation across the LDO. This capability is the primary difference between a linear voltage regulator and a LDO. "Low-dropout" is self-explanatory; however, there are other characteristics where implementing LDOs can benefit design size and performance.

A significant advantage that a LDO has over a DC/DC regulator is the nonexistence of switching noise. This benefit proves critical for applications involving ripples in the output voltage that may affect the accuracy of devices such as sensors, timers, and controllers. Another key feature of a LDO is the quiescent current, I_Q. Applications that do not require constant operation should have low I_Q to minimize power dissipation during idle periods. Figure 1 is a block diagram of a related TI Designs reference design, LDO Regulator Post AC/DC Rectifier Ripple Cleaner Reference Design for Industrial Applications (TID-00896).

Many industrial applications require the microcontroller unit (MCU) be in sleep mode when the operation is not running to reduce battery consumption. Figure 1 is a conceptual block diagram of an isolated AC to DC rectification signal being filtered by an LDO. The blue blocks indicate the variability of applications that require this low I_Q power management design in order to reduce power dissipation when the MCU is in sleep mode.
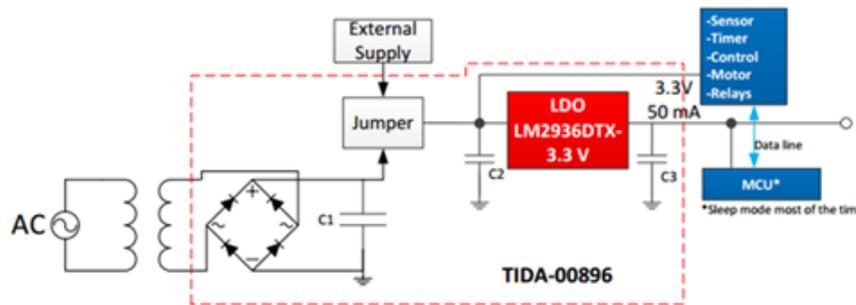

Figure 1. TIDA-00896 High-level Block Diagram

Figure 2 shows the TI LM2936 with a 15-µA ultra-low I_Q at a 100-µA load. Notice the linearity of the low I_Q supported by the LM2936 as the input voltage rises. This feature distinguishes the LM2936 to be an optimal choice in battery operated systems due to the consistency of low I_Q in the standby mode.
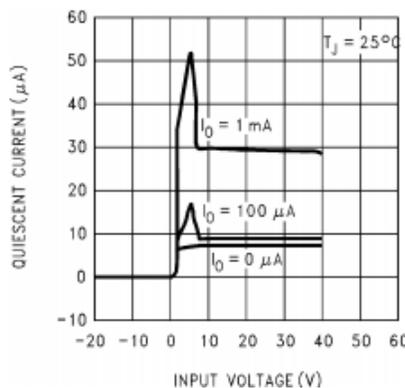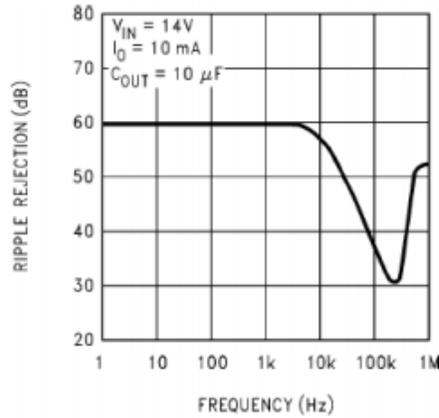

Figure 2. I_Q For LM2936

Another significant characteristic for LDOs in industrial applications is the wide input-voltage (V_{IN}) range. The LM2936 has a wide-V_{IN} range and 40-V maximum operating voltage limit that make it crucial for applications with acute transients at the input.

The power-supply rejection ratio (PSRR) blocks unwanted noise generated by the power supply. Figure 3 illustrates that the PSRR for the LM2936 is at a steady 60-dB from low frequencies all the way up to 10-kHz. This feature is important for noise-sensitive applications such as motion detectors, smart meters, and smoke detectors.

Figure 3. PSRR for LM2936

Noise can be a defining factor for selecting an LDO over other devices used in applications such as medical and test and measurement devices. The two key components that drive noise-sensitive end equipment are PSRR and output-voltage noise; the LP38798 offers high PSRR and ultra-low output-voltage noise. Table 1 highlights the PSRR and output-voltage noise values for the LP38798.

Table 1. PSRR and Output-voltage Noise for the LP38798

PARAMETER		TEST CONDITIONS	MIN[1]	TYP[2]	MAX[1]	UNIT
e_N	Output noise voltage (RMS)	V_{IN} = 3 V, V_{OUT} = 1.2 V C_{OUT} = 1 µF X7R BW = 10 Hz to 100 kHz		4.96		$µV_{(RMS)}$
		V_{IN} = 3 V, V_{OUT} = 1.2 V BW = 10 Hz to 100 kHz		5.21		
		V_{IN} = 3 V, V_{OUT} = 1.2 V BW = 10 Hz to 10 MHz		11.53		
		V_{IN} = 6 V, V_{OUT} = 5 V C_{OUT} = 1 µF X7R BW = 10 Hz to 100 kHz		5.38		
		V_{IN} = 6 V, V_{OUT} = 5 V BW = 10 Hz to 100 kHz		5.43		
		V_{IN} = 6 V, V_{OUT} = 5 V BW = 10 Hz to 10 MHz		11.58		
PSRR	Power Supply Rejection Ratio	V_{OUT} = 1.2 V, f = 10 kHz		110		dB
		V_{OUT} = 5 V, f = 10 kHz		90		
		V_{OUT} = 1.2 V, f = 100 kHz		90		
		V_{OUT} = 5 V, f = 100 kHz		60		
		V_{OUT} = 1.2 V, f = 1 MHz		70		
		V_{OUT} = 5 V, f = 1 MHz		60		

There are many applications, especially industrial, that require standby time to minimize power consumption, using less power during times that aren't necessary for the entire system to be in the on-state. Often, these applications can be battery powered, thus, conserving power will increase efficiency and ultimately save battery life. Therefore, when designing a system that requires optimal performance at a low power rating, implementing an LDO to power the devices that require frequent standby times can preserve power usage. For more information on this topic, read the blog post, "How LDOs contribute to power efficiency."

Check out TI's complete LDO portfolio.

Additional Resources:

- Download the TI Designs:
  - LDO Regulator Post AC/DC Rectifier Ripple Cleaner Reference Design for Industrial Applications (TIDA-00896).
  - Rail Cleaner with Adjustable Output Voltage Drop and Soft-start Capabilities Reference Design (TIDA-00533).

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