Errata

IWR2944 Device Errata Silicon Revisions 1.0, 2.0

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1 Introduction

This document describes the known exceptions to the functional and performance specifications to TI CMOS Radar Devices (IWR2944).

2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of Radar / millimeter Wave sensor devices. Each of the Radar devices has one of the two prefixes: XIx or IWR2x (for example: **IWR2944ABSALT**). These prefixes represent evolutionary stages of product development from engineering prototypes (XIx) through fully qualified production devices (IWR2x).

Device development evolutionary flow:

XIx — Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

IWR2x — Production version of the silicon die that is fully qualified.

XIx devices are shipped with the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Texas Instruments recommends that these devices not to be used in any production system as their expected end –use failure rate is still undefined.

3 Device Markings

Figure 3-1 shows an example of the IWR2944 Radar Device's package symbolization.

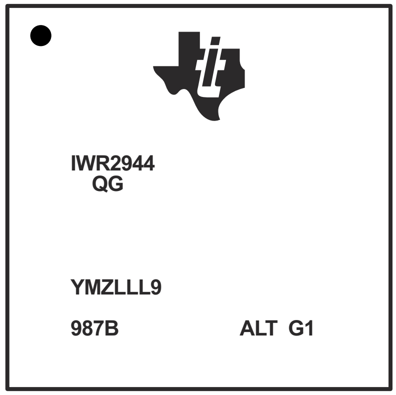

Figure 3-1. Example of Device Part Markings

This identifying number contains the following information:

- **Line 1:** Device Number
- **Line 2:** Safety Level and Security Grade
  - Q = Non-Functional Safety
  - B = SIL-2 capable
  - G = General
  - A = Authenticated boot
- **Line 3:** Lot Trace Code
  - YM = Year/Month Date Code
  - Z = Secondary Site Code
  - LLL = Assembly Lot Code
  - 9 = Primary Site Code
- **Line 4:**
  - 987B = Device Identifier
  - ALL = Package Identifier
  - G1 = "Green" Package Build (must be underlined)

4 Advisory to Silicon Variant / Revision Map

Table 4-1. Advisory to Silicon Variant / Revision Map

ADVISORY NUMBER	ADVISORY TITLE	IWR2944	
		ES1.0	ES2.0
	MAIN SUBSYSTEM		
MSS#25	Debugger May Display Unpredictable Data in the Memory Browser Window if a System Reset Occurs	X	X
MSS#27	MibSPI in Peripheral Mode in 3- or 4-Pin Communication Transmits Data Incorrectly for Slow SPICLK Frequencies and for Clock Phase = 1	X	X
MSS#28	A Data Length Error is Generated Repeatedly in Peripheral Mode When IO Loopback is Enabled	X	X
MSS#29	Spurious RX DMA REQ From a Peripheral Mode MibSPI	X	X
MSS#30	MibSPI RX RAM RXEMPTY Bit Does Not Get Cleared After Reading	X	X
MSS#33	MibSPI RAM ECC is Not Read Correctly in DIAG Mode	X	X
MSS#40	Any EDMA Transfer That Spans ACCEL_MEM1 +ACCEL_MEM2 Memories of Hardware Accelerator May Result In Data Corruption Without Any Notification Of Error From The SoC	X	X
MSS#46	Hardware Accelerator (HWA) Sniffers as a part of the Measurement Data output (MDO) interface are not operational.	X	
MSS#48	Measurement Data Output (MDO) software marker inserted at FIFO threshold location other than for *Sniffer 0* is not sent out and is bound to get missed	X	
MSS#49	Issues seen in potential interoperability with receiver supporting only Strict Alignment User Flow Control Stripping during Overflow message transmission in Aurora 64B/66B Protocol	X	X
MSS#52	DSS L2 Parity Issue: When DSP sends out an access beyond configured memory size	X	X
MSS#53	Incorrect behavior seen when context switch happens in the last parameter-set in HWA 2.0		X
MSS#54	Aurora TX UDP size<=4 is invalid	X	X
MSS#55	PMIC CLKOUT dithering in chirp-to-chirp staircase mode not supported	X	X
MSS#56	CR4 STC Boot Monitor Failure		X
MSS#57	Loss of data observed on Flush/Marker or completion of packet over MDO interface.	X	X
MSS#58	ePWM: Glitch during Chopper mode of operation	X	X
MSS#59	CRC: CRC 8-bit data width and CRC8-SAE-J1850 and CRC8-H2F possible use in CAN module is not supported	X	X
MSS#60	Mismatch in Read and Write address for 6-internal registers of PCR	X	X
MSS#61	Data aborts seen while access made to last 24 bytes of the configured MPU region and cache is enabled	X	X
MSS#62	HWA hangs when using back to back FFT3X paramsets	X	X
	ANALOG / MILLIMETER WAVE		
ANA#12A	Second Harmonic (HD2) Present in the Receiver	X	X
ANA#32A	High inter-TX gain and phase mismatch drift over temperature	X	
ANA#33A	High inter-RX gain and phase mismatch drift over temperature	X	
ANA#34A	Low inter-TX isolation between adjacent channels (TX1/TX2 or TX3/TX4)	X	
ANA#35A	Low inter-RX isolation between adjacent channels (RX1/RX2 or RX3/RX4)	X	X
ANA#36	TX4 phase shifter DAC monitor and fault injection not functional	X	
ANA#37A	High RX gain droop across LO frequency	X	X
ANA#38	Return loss on RX pins not meeting the -10dB S11 target	X	
ANA#39	HPF cutoff frequency 2800kHz configuration can result in incorrect RX IFA gains and filter corner frequencies	X	X
ANA#43	Errors seen in Synthesizer Frequency Live monitor	X	X
ANA#44	In 3.3V IO mode, back power is observed on the 1.8V rail from 3.3V rail	X	X
ANA#45	Spurs Caused due to Digital Activity	X	X
ANA#46	Spurs caused due to data transfer activity	X	X

Table 4-1. Advisory to Silicon Variant / Revision Map (continued)

ADVISORY NUMBER	ADVISORY TITLE	IWR2944	
		ES1.0	ES2.0
ANA#47	RX Spurs observed across RXs in Idle Channel Scenario	X	X

5 Known Design Exceptions to Functional Specifications

MSS#25 ***Debugger May Display Unpredictable Data in the Memory Browser Window if a System Reset Occurs***

Revision(s) Affected: IWR2944 ES1.0, ES2.0

Description:

If a system reset (nRST goes low) occurs while the debugger is performing an access on the system resource using system view, a peripheral error should be replied to the debugger. If the access was a read, instead the response might indicate that the access completed successfully and return unpredictable data.

This issue occurs under this condition: when a system reset is asserted (nRST low) on a specific cycle, while the debugger is completing an access on the system, using the system view. An example would be, when a debugger, like the CCS-IDE memory browser window, is refreshing content using the system view. This is not an issue for a CPU only reset and, this is not an issue during a power-on-reset (nPORRST) either.

Workaround(s):

Avoid performing debug reads and writes while the device might be in reset.

MSS#27 — *MibSPI in Peripheral Mode in 3- or 4-Pin Communication Transmits Data Incorrectly for Slow SPICLK Frequencies and for Clock Phase = 1*

Revision(s) Affected: IWR2944 ES1.0, ES2.0

Description:

The MibSPI module, when configured in multibuffered peripheral mode with 3-functional pins (CLK, SIMO, SOMI) or 4-functional pins (CLK, SIMO, SOMI, nENA), could transmit incorrect data when all the following conditions are met:

- MibSPI module is configured in multibuffered mode,
- Module is configured to be a peripheral in the SPI communication,
- SPI communication is configured to be in 3-pin mode or 4-pin mode with nENA,
- Clock phase for SPICLK is 1, and
- SPICLK frequency is MSS_VCLK frequency / 12 or slower

Workaround(s):

The issue can be avoided by setting the CSHOLD bit in the control field of the TX RAM (Multi-Buffer RAM Transmit Data Register). The nCS is not used as a functional signal in this communication; hence, setting the CSHOLD bit does not cause any other effect on the SPI communication.

MSS#28 *A Data Length Error is Generated Repeatedly in Peripheral Mode When IO Loopback is Enabled*

Revision(s) Affected: IWR2944 ES1.0, ES2.0

Description:

When a DLEN error is created in Peripheral mode of the SPI using nSCS pins in IO Loopback Test mode, the SPI module re-transmits the data with the DLEN error instead of aborting the ongoing transfer and stopping. This is only an issue for an IOLPBK mode peripheral in Analog Loopback configuration, when the intentional error generation feature is triggered using CTRLDLENERR (IOLPBKTSTCR.16).

Workaround(s):

After the DLEN_ERR interrupt is detected in IOLPBK mode, disable the transfers by clearing the SPIEN (bit 24) in the SPIGCR1 register and then, re-enable the transfers by resetting the SPIEN bit.

MSS#29 ***Spurious RX DMA REQ From a Peripheral Mode MibSPI***

Revision(s) Affected: IWR2944 ES1.0, ES2.0

Description:

A spurious DMA request could be generated even when the SPI Peripheral is not transferring data in the following condition sequence:

- The MIBSPI is configured in standard (non-multibuffered) SPI mode, as a Peripheral
- The DMAREQEN bit (SPIINT0.16) is set to enable DMA requests
- The Chip Select (nSCS) pin is in an active state, but no transfers are active
- The SPI is disabled by clearing the SPIEN (SPIGCR1.24) bit from '1' to '0'

The above sequence triggers a false request pulse on the Receive DMA Request as soon as the SPIEN bit is cleared from '1' to '0'.

Workaround(s):

Whenever disabling the SPI, by clearing the SPIEN bit (SPIGCR1.24), first clear the DMAREQEN bit (SPIINT0.16) to '0', and then, clear the SPIEN bit.

MSS#30 *MibSPI RX RAM RXEMPTY bit Does Not Get Cleared After Reading*

Revision(s) Affected: IWR2944 ES1.0, ES2.0

Description:

The RXEMPTY flag may not be auto-cleared after a CPU or DMA read when the following conditions are met:

- The TXFULL flag of the latest buffer that the sequencer read out of transmit RAM for the currently active transfer group is 0,
- A higher-priority transfer group interrupts the current transfer group and the sequencer starts to read the first buffer of the new transfer group from the transmit RAM, and
- Simultaneously, the Host (CPU/DMA) is reading out a receive RAM location that contains valid received data from the previous transfers.

Workaround(s):

Avoid transfer groups interrupting one another.

If dummy buffers are used in lower-priority transfer groups, select the appropriate "BUFMODE" for them (like, SKIP/DISABLED) unless, there is a specific need to use the "SUSPEND" mode.

MSS#33 — *MibSPI RAM ECC is Not Read Correctly in DIAG Mode*

Revision(s) Affected: IWR2944 ES1.0, ES2.0

Description:

A Read operation to the ECC address space of the MibSPI RAM in DIAG mode does not return the correct ECC value for the first 128 buffers, if the Extended Buffer support is implemented, but the Extended Mode is disabled for the particular MibSPI instance.

Workaround(s):

None

MSS#40 *Any EDMA Transfer That Spans ACCEL_MEM1 +ACCEL_MEM2 Memories of Hardware Accelerator May Result In Data Corruption Without Any Notification Of Error From The SoC*

Revision(s) Affected: IWR2944 ES1.0, ES2.0

Description:

As per TPTC IP Spec, a Transfer request (TR) is supposed to access a single peripheral end point. ACCEL_MEM0/ACCEL_MEM1 memory banks of HWA are available via single peripheral point and ACCEL_MEM2/ ACCEL_MEM3 memory banks of HWA are available as another peripheral point (different from that of ACCEL_MEM0/ ACCEL_MEM1). Hence if a single TR is used to access a buffer spanning ACCEL_MEM1 and ACCEL_MEM2 memories of the HWA (i.e. a single buffer spanning 2 different peripheral points), the spec is not being adhered to. This errata is explicitly highlighting this spec requirement.

Note

The ACCEL_MEM1 and ACCEL_MEM2 memories are referred to as DSS_HWA_DMA0 and DSS_HWA_DMA1 at the SoC level.

Workaround(s):

Split the access into 2 TRs so that a single TR does not span ACCEL_MEM1 +ACCEL_MEM2. The 2 TRs can be chained.

MSS#46 ***Hardware Accelerator (HWA) Sniffers as a part of the Measurement Data output (MDO) interface are not operational.***

Revisions Affected

IWR2944 ES1.0 ONLY

Details

Measurement Data Output (MDO) is used to capture the transactions on the bus connected from different interfaces of the IWR2944 device and transmit outside over LVDS (4-data lanes). MDO is comprised of a sniffer, FIFO, and an aggregator. The MDO sniffer module is responsible for monitoring the hardware interfaces in the chip and capturing the transactions on the bus which are within the configured addressing region of interest.

Hence, the sniffer module, as the name suggests, can sniff a bus interface and transfer contents to the MDO FIFO and aggregator. It can access the data from Radar Sub-System EDMA, L3 memory, DMA, local RAM, hardware accelerator etc.

Currently, Hardware accelerator (HWA) sniffers for MDO interface are not operational.

Workaround

The required data to be sent out over the Aurora interface can be transferred out using the Generic DSS MDO FIFO (F2) using an EDMA to sequence the transfers.

MSS#48 *Measurement Data Output (MDO) software marker inserted at FIFO threshold location other than for Sniffer 0 is not sent out and is bound to get missed.*

Revisions Affected

IWR2944ES1.0 Only

Details

Measurement Data Output (MDO) is used to capture the transactions on the bus connected from different interfaces of the IWR2944 device and transmit outside over LVDS (4-data lanes). MDO is comprised of a sniffer, FIFO, and an aggregator. The corresponding sniffer module sniffs a bus interface and accumulates data in the FIFO. When a FIFO threshold is reached, the data is sent out to the aggregator as a burst transfer.

An MDO source can also inject a marker indicator along with its data for tracking or other related purpose. Now, if a marker is inserted such that it is a part of the last element of the FIFO threshold location, it is bound to get missed.

This happens only when a sniffer other than *Sniffer 0* is used for transfer.

Workaround

The following two workarounds can be used to ensure the inserted maker is registered without fail :

1. Multiple back to back markers (>1) can be sent out by the user to ensure at least one of them is registered by the receiver.
2. The same sniffer configurations should be programmed to *Sniffer 0* registers. This way the markers would be sent out and registered by the receiver.
   This workaround is only beneficial where *Sniffer 0* is not in use and is idle for replicating other sniffer configurations.

Note

The above workarounds are only required when using markers in operation. There are no restrictions on the sniffers when markers are not in use.

MSS#49 *Issues seen in potential interoperability with receiver supporting only Strict Alignment User Flow Control Stripping during Overflow message transmission in Aurora 64B/66B Protocol.*

Revisions Affected

IWR2944 ES1.0, ES2.0

Details

Measurement Data Output (MDO) is used to capture the transactions on the bus connected from different interfaces of the IWR2944 device and transmit outside over Aurora LVDS Interface (4-data lanes). MDO is comprised of a sniffer, FIFO, and an aggregator. The MDO sniffer module is responsible for monitoring the hardware interfaces in the chip and capturing the transactions on the bus which are within the configured addressing region of interest.

Data loss due to overflow can occur at the sniffer. This overflow information is sent as an interrupt to the CPU and the Aurora Tx IP. A User-Flow-Control (UFC) packet is generated by the Aurora TX IP in case of a data overflow condition in order to notify the user of this error condition. This is an error scenario and is not expected to occur in normal transfer functionality. At this stage, the data integrity is already compromised.

Aurora IP only supports UFC packet generation as per Section 6.6 of Aurora 64B/66B Protocol Specification, i.e. the UFC header block precedes the UFC data blocks. *Strict Alignment User Flow Control Stripping* (refer to Section 6.7 of Aurora 64B/66B Protocol Specification) is currently not supported.

Workaround

For MDO, the input data rate should be less than the output data rate so as to keep the effective data rate well within reasonable limits to avoid any overflow condition altogether.

Note

It is inadvisable for Aurora 64B/66B protocol to use *TOP_AURORA_TX:AURORA_TX_UFC_MSG_REQ* register to send UFC packets without overflow.

MSS#52 — *DSS L2 Parity Issue: When DSP sends out an access beyond configured memory size*

Revision(s) Affected: IWR2944 ES1.0, ES2.0

Description:

The DSP IP is sending out an access to the L2 memory for access beyond the configured DSP L2 memory size of 384 KB (reserved space access) i.e. beyond 0x8085 FFFC.

If parity is enabled, an L2 Parity error is observed for reads to the reserved locations beyond 0x80860000 - 0x8087FFFC

> **Note**
> Reserved Memory locations from 0x80860000 to 0x8087FFFC is accessible to read and write. Memory Locations from 0x80860000 to 0x8087FFFC are aliased at 0x80840000 to 0x8085FFFC and 0x80850000 to 0x8085FFFC is replicated at 0x80870000 to 0x8087FFFC, hence the actual L2RAM is of 384KB only.

Workaround(s):

Configuring the MPU : (L2MPPA24- L2MPPA31) to 0.

Write access to reserved space is blocked. No Aliasing & No L2 Parity Error. This ensures the data integrity of valid L2 Region is maintained.

Read access to reserved space still leads to L2 Parity Error (If Parity is enabled).

Debug access(Read & Write) are not blocked: Still leads to Aliasing + L2 Parity Error : Its not feasible to block the debug access despite configuring the MPPA registers for Protection enabled

Memory Protection Fault Address Register(0184 A000h:: L2MPFAR/0184 AC00h:: L1DMPFAR) are populated with the address which are blocked(beyond 384KB boundary in this case) & still accessed

Address(L2MPFAR/L1DMPFAR) & Status(L2MPFSR/L1DMPFSR) Registers are required to be cleared for the next read using Clear registers(L2MPFCR/L1DMPFCR) with values 1

Observations(Both when L1D Cache Enabled/Disabled)

For Read : MPU Protection Errors are observed on L1D with L1MPFAR registers populated with the blocked address access

For Write : MPU Protection Errors are observed on L2 with L2MPFAR registers populated with the blocked address access

MSS#53 ***Incorrect behavior seen when context switch happens in the last parameter-set in the Hardware Accelerator (HWA 2.1)***

Revision(s) Affected: IWR2944 ES2.0 Only

Description:

At the end of the last parameter-set of the last loop in low-priority context, if a context-switch happens to high priority, then an incorrect behavior is observed when returning back to low-priority. This incorrect behavior can manifest itself as a fresh (unintended) re-start of the low-priority loop once completed. Following are the erroneous conditions:

- CONTEXT_SW_EN or FORCED_CONTEXT_SW_EN set in the last paramset of the low priority thread.

Similarly, forced context switch (FORCED_CONTEXT_SW_EN) shouldn't be enabled in last paramset of high priority thread .

Workaround(s):

It is recommended to not enable context switch in the last parameter-set of the above mentioned conditions. In case, the last parameter-set has to have context switch enabled, user could add a dummy parameter-set with context switch disabled as the last parameter-set.

MSS#54 *Aurora TX UDP size<=4 is invalid*

Revisions Affected: IWR2944 ES1.0, ES2.0

Description:

Aurora TX UDP size<=4 is invalid during transfer.

Valid UDP sizes for Aurora 8b/10b and Aurora 64b/66b are :

1. AURORA_TX_UDP_CONFIG_PACK_MODE_SEL = 0 (Bytes) : Valid Udp sizes - AURORA_TX_UDP_SIZE = 8, 12, 16, 20.....so on
2. AURORA_TX_UDP_CONFIG_PACK_MODE_SEL = 1 (TWP) : Valid Udp sizes - AURORA_TX_UDP_SIZE = 5, 6, 7, 8.....so on

Workaround:

It is recommended to use only the valid UDP sizes as described above.

MSS#55 ***PMIC CLKOUT dithering in chirp-to-chirp staircase mode not supported***

Revision(s) Affected: IWR2944 ES1.0, ES2.0

Description:

The PMIC CLKOUT has an option to add dithering to the clk frequency to reduce the impact of the clk spurs. The continuous mode of dithering is supported, while the chirp-to-chirp staircase mode of dithering is unsupported. This is because of the DFE reset not reaching the PMIC CLKOUT block.

Workaround(s):

It is recommended to use continuous dithering mode in PMIC CLKOUT.

MSS#56	***CR4 STC Boot Monitor Failure***
Revision(s) Affected:	IWR2944 ES2.0 ONLY
Description:	Cortex CR4 STC Boot Monitor Failure is observed in the device.
Workaround(s):	It is recommended to execute a sequence (MSS_CTRL:MSS_PBIST_KEY_RST[3:0] = 0) to clear the PBIST registers before starting CR4 (BSS) execution in the Secondary boot loader (SBL). Refer to the SBL example code provided by TI.

MSS#57 *Loss of data observed on Flush/Marker or completion of packet over MDO interface.*

Revision(s) Affected: IWR2944 ES1.0, ES2.0

Description:

421-24008 IWR2944: Data frames sent over MDO discards the last 6 bytes at the end of the frame

It is observed that data transfer over the MDO having data_size = 6 get dropped. To ensure complete data gets transferred, the data size needs to adhere to 4byte and 8byte aligned data. If not done, a loss of the last 6 bytes of data on Flush/Marker trigger or completion of packet could be observed.

Data Flow: EDMA -> SNIFFER -> FIFO --> AGGREGATOR -> STM -> TPIU -> AURORA TX.

With Data transfer using MSS_TPCC to MDO_DSS_FIFO having data size of 6 bytes results in the 6 bytes getting dropped. STM module has cxstm500_axislvif_write block which samples data based on WSTRB. There is no case inside the STM which can handle 6 bytes of incoming data.

Design Limitation in STM module to handle 6 bytes of data.

1, 2, 4, 8 bytes of data get handled. But 6 bytes results in data getting dropped.

Workaround(s):

It is recommended to include 2 dummy bytes during transfer to make the WSTRB handle 8 bytes.

MSS#58 — *ePWM: Glitch during Chopper mode of operation*

Revision(s) Affected

IWR2944 ES1.0, ES2.0

Details

During chopper mode operation, a glitch may be observed on the ePWMA and ePWMB output signals from the ePWM module.

Workaround

If the use case is impacted by a glitch, it is recommended to disable the PWM chopper control function by setting the LPRADAR:APP_PWM:PCCTL:CHPEN register bit to 0.

The below table shows the Register Address for above workaround.

Bits	Name	Address
0	IWR2944:MSS_ETPWM:PCCTL:CHPEN	0x03F7 8**n**3C, where 'n' = C, D or E for PWMA, PWMB, PWMC respectively

MSS#59 *CRC: CRC 8-bit data width and CRC8-SAE-J1850 and CRC8-H2F possible use in CAN module is not supported*

Revision(s) Affected IWR2944 ES1.0, ES2.0

Details

1. 8-bit data width is not suppported. Minimum data width supported is 16-bit.
2. CRC types CRC8-SAE-J1850 and CRC8-H2F are not supported.

Workaround

1. 16/32/64-bit data widths are supported.
2. It is recommended to not use the above mentioned unsupported polynomials.

MSS#60 *Mismatch in Read and Write address for 6-internal registers of PCR*

Revision(s) Affected

IWR2944 ES1.0, ES2.0

Details

Below is the set of common registers and their corresponding read-address offset and write-address offset for all PCRs in the Device

Register	Write Address offset	Read Address offset
PPROTSET_2	0x0000 0028	0x0000 002C
PPROTSET_3	0x0000 002C	0x0000 0040
PPROTCLR0	0x0000 0040	0x0000 0044
PPROTCLR1	0x0000 0044	0x0000 0048
PPROTCLR2	0x0000 0048	0x0000 004C
PPROTCLR3	0x0000 004C	0x0000 00260

Workaround

The above mentioned mapping to be used while performing any read-modify-writes or Read-back checks to these specific set of registers.

MSS#61 *Data aborts seen while access made to last 24 bytes of the configured MPU region and cache is enabled.*

Revision(s) Affected

IWR2944 ES1.0, ES2.0

Details

When R5F performs access to a byte or word in the cacheable region, the access from cache is 32bytes long (One cache line size) with the starting address being the critical word being fetched.

The MPU assumes (Incorrectly) that the end address of the ongoing transaction to be Critical word + 32Bytes and compares this with the end address programmed in the MPU. MPU treats this as access violation and faults the transaction (Ex : 0x701FFFF8 + 32 byte = 0x7020 0018 > 0x70FF FFFF).

This issue is not applicable if MPU regions are marked as non-cacheable.

Workaround

If Cache is enabled, do not have any data in the last 32Bytes of the MPU region.

MSS#62 *HWA hangs when using back to back FFT3X paramsets*

Revision(s) Affected

IWR2944 ES1.0, ES2.0

Details

If FFT3X is enabled in back to back paramsets or as first and last paramsets of a loop, the HWA state machine hangs after the 1st FFT3X paramset is executed without raising any param done interrupt.

Workaround

Use any paramset with FFT3X disabled before using a paramset with FFT3X enabled (users may also go for a No Operation paramset with ACCEL_MODE = 0b111)

ANA#12A — *Second Harmonic (HD2) Present in the Receiver*

Revision(s) Affected: IWR2944 ES1.0, ES2.0

Description:

There is a finite isolation between the RF pins/package and the FMCW synthesizer. This can create spurious tones at the synthesizer output and lead to appearance of 2nd order harmonics and inter-modulations of expected IF frequencies at RX ADC output. The amplitude of the 2nd harmonic could be as high as -55 dBc, referenced to the power level of the intended tone at the LNA input.

Workaround(s):

No workaround available at this time. However, in many typical radar use cases the HD2 does not affect the system performance due to two reasons:

1. Since the HD2 comes from a coupling to the LO signal, there is an inherent suppression of the HD2 level due to the self-mixing effect (that is, phase noise and phase spur suppression effect at the mixer).
2. In real-life scenarios there is often a double-bounce effect of the radar signal reflected from the target, which leads to a ghost object at twice the distance of the actual object. This effect is often indistinguishable from the effect of HD2 itself.

ANA#32A — *High inter-TX gain and phase mismatch drift over temperature*

Revisions Affected

IWR2944 ES1.0 ONLY

Details

TX4/TX1 or TX4/TX2 combination exhibits up to +/-9 degree variation in phase mismatch over the full allowed temperature range in IWR2944

Workaround

In applications where high gain/phase accuracy is desired between TX channels, a background calibration can be used to correct for mismatch variation over temperature.

TX phase mismatch variation has improved to +/-6 degree in IWR2944 ES2.0 silicon across the full temperature range.

ANA#33A — *High inter-RX gain and phase mismatch drift over temperature*

Revisions Affected

IWR2944 ES1.0 ONLY

Details

RX4 and RX3 exhibit +/-6 degree phase mismatch variation over the full allowed temperature range with respect to RX1 in IWR2944 in ES1.0 silicon.

Workaround

In applications where high gain/phase accuracy is desired between RX channels, a background calibration can be used to correct for mismatch variation over temperature.

RX phase mismatch variation has improved to +/-4 degree in IWR2944 ES2.0 silicon across the full temperature range with respect to RX1.

ANA#34A — *Low inter-TX isolation between adjacent channels (TX1/TX2 or TX3/TX4)*

Revisions Affected

IWR2944 ES1.0 ONLY

Details

TX1/TX2 and TX3/TX4 pairs exhibit low inter-channel isolation (22dB) in IWR2944 ES1.0 device.

This number has improved to >30dB in IWR2944 ES2.0 device.

Workaround

If the isolation is still limiting the angular accuracy, zero angle calibration can be extended to multiple angles to calibrate the antenna gain & phase mismatch to improve the angular accuracy.

Silicon Fix is provided in IWR2944 ES2.0.

ANA#35A — *Low inter-RX isolation between adjacent channels (RX1/RX2 or RX3/RX4)*

Revisions Affected

IWR2944 ES1.0, ES2.0

Details

RX1/RX2 and RX3/RX4 pairs exhibit low interchannel isolation of 25dB.

Workaround

No workaround is available.

If the isolation is limiting the angular accuracy, zero angle calibration can be extended to multiple angles to calibrate the antenna gain & phase mismatch in order to improve the angular accuracy.

ANA#36 *TX4 phase shifter DAC monitor and fault injection are not functional*

Revisions Affected

IWR2944 ES1.0 ONLY

Details

TX4 phase shifter DAC (Digital to Analog Conversion) monitor is not functional due to a design bug in the Silicon. Similarly, the associated fault injection mechanism is also not functional on Silicon.

Workaround

No Workaround is available in ES 1.0.

Silicon Fix is provided in ES 2.0.

TX gain/phase mismatch monitor and phase shifter monitor are available as additional diagnostics that can cover the TX-DAC from a safety perspective.

ANA#37A — *High RX gain droop across LO frequency*

Revisions Affected

IWR2944ES1.0, ES2.0

Details

RX gain droop is ~4.5dB across the full operating frequency range of the device.

Workaround

Negligible impact on system performance since there is an insignificant impact on noise figure due to the gain droop.

ANA#38A — *Return loss on RX pins not meeting the -10dB S11 target*

Revisions Affected

IWR2944 ES1.0 ONLY

Details

Measured input match (S11) at RX input pins on the PCB is ~-4dB at 81GHz for IWR2944 ES1.0 silicon.

Workaround

The noise figure number measured includes the degraded S11 on the Rx ports.

Silicon Fix is provided in IWR2944 ES2.0.

ANA#39 *HPF cutoff frequency 2800kHz configuration can result in incorrect RX IFA gains and filter corner frequencies.*

Revisions Affected

IWR2944 ES1.0, ES2.0

Details

The analog IF stages include a second order high pass filter that can be configured to the following -6dB corner frequencies :

300, 350, 700, 1400, 2800 KHz.

Out of these, HPF cutoff frequency 2800kHz configuration can result in incorrect RX IFA gains and filter corner frequencies.

Workaround

Use of 2800kHz cutoff configuration is not recommended.

ANA#43 *Errors seen in Synthesizer Frequency Live monitor*

Revision(s) Affected: IWR2944 ES1.0, ES2.0

Description: Large errors are seen in excess of 20 MHz in the Synthesizer Frequency Live monitor after 100C for ramp configurations between 80.5GHz to 81GHz with a slope > 50MHz/us.

Workaround(s): For slopes >50MHz/us, it is recommended to utilize chirps under 80.5GHz.

ANA#44 ***In 3.3V IO mode, back power is observed on the 1.8V rail from 3.3V rail***

Revision(s) Affected: IWR2944 ES1.0, ES2.0

Description: When the 3.3V power rail comes up and 1.8V has not been supplied yet, there is a voltage rise seen on the 1.8V VIOIN rail due to the leakage path within the IO cell.

Workaround(s): It is recommended to use the following workarounds:

1. Use appropriate Supply Sequencing: Supply 1.8V first and then 3.3V.
2. In case the PMIC fails to powerup due to sensing an existing voltage at its output, this voltage detection scheme in the PMIC should be disabled.

ANA#45 — *Spurs Caused due to Digital Activity*

Revision(s) Affected: IWR2944 ES1.0, ES2.0

Description:

Digital filtering activity can potentially couple to analog circuits leading to spurs in the LO, which may also be seen in the Rx data. Such a spur in the Rx data would be seen at the spur frequency offset around a strong object.

Following are the different spurs that can potentially be observed:

1. Spurs at (2Fs-40) MHz IF frequency for sampling rate +/-0.5Msps around 20 Msps.
2. Spurs at (2Fs-60) MHz IF frequency for sampling rate +/-0.5Msps around 30 Msps.
3. Spurs at (4Fs-140) MHz IF frequency for sampling rate +/-0.3Msps around 35 Msps.
4. Spurs at (4Fs-100) MHz IF frequency for sampling rates in the range 22 to 23.5 Msps and 26.5 to 28 Msps

[Fs=Profile Sampling Rate]

Workaround(s):

The user should avoid sampling rates in the range mentioned above or use exactly the center of the sampling rate range (so that spur is at 0 Hz).

ANA#46	*Spurs caused due to data transfer activity*
Revision(s) Affected:	IWR2944 ES1.0, ES2.0
Description:	Digital activity related to ADC data transfer between subsystems inside the chip can potentially create spurious tones in the signal due to undesired intra-chip parasitic coupling to RF. This coupling has been observed to cause weak spurs at 5.17MHz, 8.82 MHz and 10.71MHz offsets. The spur in the Rx data would be seen at the spur frequency offset around a strong object.
Workaround(s):	The start time of data transfer from ADCBUF can be configured to have a random value across chirps. This helps to spread the spur across doppler bins and reduce spur level by ~15dB.

ANA#47 — *RX Spurs observed across RXs in Idle Channel Scenario*

Revision(s) Affected: IWR2944 ES1.0, ES2.0

Description:

In scenarios of no object being present, or a very weak object being present in the vicinity, the sigma delta ADC output could have spurs in the RX spectrum. This is observed only for low RX gain settings. The spur frequency could vary across RX channels. In presence of a real object, this would not be observed.

Workaround(s):

- *Workaround#1* : Use higher rx gain (>40dB) in these situations.
- *Workaround#2* : Idle channel spur is spread across all doppler bins in 2DFFT at the spur range bin. While detecting peaks in 2D-FFT, users can apply 2D neighborhood peak search (e.g. 2D CFAR-CA), which compares the level with all surrounding bins. This can help avoid detection of idle channel spur as ghost object.

Trademarks

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6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2024	*	Initial Release

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