

1 2 3 4 5 6

A

B

C

D

A

B

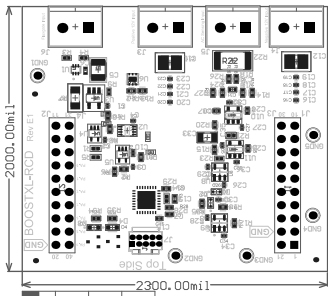
C

Design

D

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer		1.40mil		
	Dielectric 1	FR-4	8.00mil	4.2	
2	GND		1.40mil		
	Dielectric 2	FR-4	40.00mil	4.2	
3	Power		1.40mil		
	Dielectric 3	FR-4	8.00mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
 Z22 ■ This Assembly Note will show in the PcbDoc and associated outputs
 Z23 ■ This Assembly Note will show in the PcbDoc and associated outputs
 Z24 ■ This Assembly Note will show in the PcbDoc and associated outputs



COMPONENTS MARKED 'DNP' SHOULD NOT BE ORDERED. TO ORDER, MARK COMPONENTS WITH 'DNP' IN THE BOARD ASSEMBLY VARIANT: 001

DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNUAL RING 0.05mm (2MIL) EXTERNAL PER PC-D-275 CLASS 2 LEVEL C REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL	
MATERIAL:	
<input type="checkbox"/> FR-408	<input checked="" type="checkbox"/> FR-4 High Tg <input type="checkbox"/> OTHER
THICKNESS:	<input checked="" type="checkbox"/> 62 MIL (1.6mm) +/-10% <input type="checkbox"/> OTHER
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/-
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/-
DRILLING:	
REFERENCE:	<input checked="" type="checkbox"/> AS SHOWN <input checked="" type="checkbox"/> NC_DRILL FILES
PTH COPPER THICKNESS:	<input checked="" type="checkbox"/> 20-30 um <input type="checkbox"/> OTHER
BOARD FINISH:	
SILKSCREEN:	<input checked="" type="checkbox"/> TOP <input checked="" type="checkbox"/> BOTTOM
SILKSCREEN COLOR:	<input checked="" type="checkbox"/> WHITE <input type="checkbox"/> OTHER
SOLDER RESIST COLOR:	<input type="checkbox"/> GREEN <input checked="" type="checkbox"/> OTHER_RED <input checked="" type="checkbox"/> MATTE <input type="checkbox"/> SEMI-GLOSS
SURFACE FINISH:	
<input checked="" type="checkbox"/> IMMERSION GOLD (ENIG)	<input type="checkbox"/> ENEPIG
<input type="checkbox"/> IMM. TIN/SILVER OR EQUIV	<input type="checkbox"/> OTHER
ARRAY/PANEL:	
<input type="checkbox"/> CUT AND TRM PER M1 BOARD OUTLINE	<input type="checkbox"/> N.C. ROUTE <input checked="" type="checkbox"/> V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS ->	<input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3
<input checked="" type="checkbox"/> RoHS	<input type="checkbox"/> OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION:	<input type="checkbox"/> YES
BARE BOARD ELEC. TEST:	<input type="checkbox"/> NONE <input checked="" type="checkbox"/> REQUIRED <input type="checkbox"/> PER ORDER



PROJECT TITLE:
AC and DC Current Fault Detection Reference Design

DESIGNED FOR:
Public Release

FILE NAME:
TIDA-010237.PcbDoc

REV: 001	DATE: 12/23/2023	BY: [Signature]	DESCRIPTION: [Signature]
LAYER NAME: TOP	TID #: TIDA010237	DATE: 12/23/2023	BY: [Signature]
PLATE NUMBER: [Signature]			

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ENGINEER:
Nic Gough

LAYOUT BY:
Who did the Layout?

SCALE: 0.69

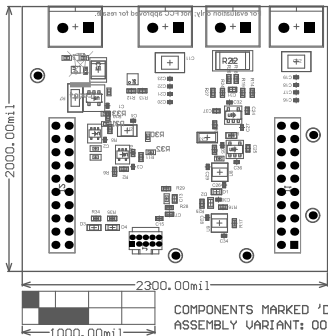
ALTIM DESIGNER VERSION:
23.0.1.38

1 2 3 4 5 6

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer		1.40mil		
	Dielectric 1	FR-4	8.00mil	4.2	
2	GND		1.40mil		
	Dielectric 2	FR-4	40.00mil	4.2	
3	Power		1.40mil		
	Dielectric 3	FR-4	8.00mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				

DESIGN INFORMATION	
MIN. TRACK WIDTH:	8_MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24_MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER PC-D-275 CLASS 2 LEVEL C REGISTRATION TOLERANCES: METAL +/- 5_MIL HOLES +/- 3_MIL HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3_MIL	
MATERIAL:	
<input type="checkbox"/> FR-408	<input checked="" type="checkbox"/> FR-4 High Tg <input type="checkbox"/> OTHER
THICKNESS:	<input checked="" type="checkbox"/> 62 MIL (1.6mm) +/-10% <input type="checkbox"/> OTHER
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/-
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/-
DRILLING:	
REFERENCE:	<input checked="" type="checkbox"/> AS SHOWN <input checked="" type="checkbox"/> NC_DRILL FILES
PTH COPPER THICKNESS:	<input checked="" type="checkbox"/> 20-30 um <input type="checkbox"/> OTHER
BOARD FINISH:	
SILKSCREEN:	<input checked="" type="checkbox"/> TOP <input checked="" type="checkbox"/> BOTTOM
SILKSCREEN COLOR:	<input checked="" type="checkbox"/> WHITE <input type="checkbox"/> OTHER
SOLDER RESIST COLOR:	<input type="checkbox"/> GREEN <input checked="" type="checkbox"/> OTHER_RED <input checked="" type="checkbox"/> MATTE <input type="checkbox"/> SEMI-GLOSS
SURFACE FINISH:	
<input checked="" type="checkbox"/> IMMERSION GOLD (ENIG)	<input type="checkbox"/> ENEPIG
<input type="checkbox"/> IMM. TIN/SILVER OR EQUIV	<input type="checkbox"/> OTHER
ARRAY/PANEL:	
<input type="checkbox"/> CUT AND TRIM PER M1 BOARD OUTLINE	<input type="checkbox"/> N.C. ROUTE <input checked="" type="checkbox"/> V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS ->	<input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3
<input checked="" type="checkbox"/> RoHS	<input type="checkbox"/> OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION:	<input type="checkbox"/> YES
BARE BOARD ELEC. TEST:	<input type="checkbox"/> NONE <input checked="" type="checkbox"/> REQUIRED <input type="checkbox"/> PER ORDER

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
 Z22 ■ This Assembly Note will show in the PcbDoc and associated outputs
 Z23 ■ This Assembly Note will show in the PcbDoc and associated outputs
 Z24 ■ This Assembly Note will show in the PcbDoc and associated outputs



COMPONENTS MARKED 'DNP' SHOULD NOT BE ORDERED. TO ORDER 'DNP' COMPONENTS, MARK ASSEMBLY VARIANT: 001
 ASSEMBLY VARIANT: 001

REV: 001	DATE: 12/23/2023	BY: [Signature]	DESCRIPTION: BOARD
LAYER NAME = Bottom		TID #: 01010237	# DIT
PROJECT NAME: TIDA-010237		DATE: 12/23/2023	TIME: 10:32 AM

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ENGINEER:	LAYOUT BY:
Nic Gough	Who did the Layout?
SCALE: 0.69	ALTUM DESIGNER VERSION:
	23.0.1.38

Design

D

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer		1.40mil		
	Dielectric 1	FR-4	8.00mil	4.2	
2	GND		1.40mil		
	Dielectric 2	FR-4	40.00mil	4.2	
3	Power		1.40mil		
	Dielectric 3	FR-4	8.00mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER PC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____

THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER_RED
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

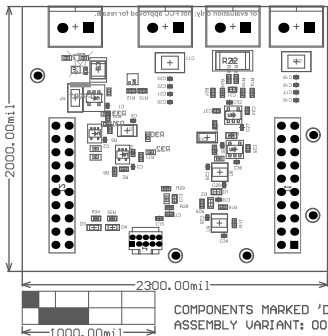
ARRAY/PANEL: CUT AND TRIM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94-V0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
 Z22 ■ This Assembly Note will show in the PcbDoc and associated outputs
 Z23 ■ This Assembly Note will show in the PcbDoc and associated outputs
 Z24 ■ This Assembly Note will show in the PcbDoc and associated outputs



COMPONENTS MARKED 'DNP' SHOULD NOT BE ORDERED. TO ORDER 'DNP' COMPONENTS, ASSEMBLY VARIANT: 001

REV: 001	DATE: 12/23/2023	BY: [Signature]	DESCRIPTION: BOARD	PROJECT: TIDA-010237	DESCRIPTION: AC and DC Current Fault Detection Reference
LAYER NAME = Bottom		TID #: TIDA-010237		DATE: 12/23/2023	
PROJECT: TIDA-010237		ASSEMBLY VARIANT: 001		DATE: 12/23/2023	

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TEXAS INSTRUMENTS

PROJECT TITLE:
AC and DC Current Fault Detection Reference

DESIGNED FOR:
Public Release

FILE NAME:
TIDA-010237.PcbDoc

ENGINEER:
Nic Gough

LAYOUT BY:
Who did the Layout?

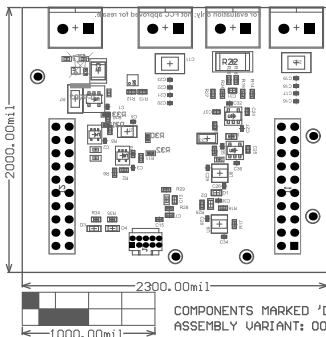
SCALE: 0.69

ALTIM DESIGNER VERSION:
23.0.1.38

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer		1.40mil		
	Dielectric 1	FR-4	8.00mil	4.2	
2	GND		1.40mil		
	Dielectric 2	FR-4	40.00mil	4.2	
3	Power		1.40mil		
	Dielectric 3	FR-4	8.00mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				

DESIGN INFORMATION	
MIN. TRACK WIDTH:	8_MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24_MIL
MINIMUM ANNUAL RING 0.05mm (2MIL) EXTERNAL PER PC-D-275 CLASS 2 LEVEL C REGISTRATION TOLERANCES: METAL +/- 5_MIL HOLES +/- 3_MIL HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3_MIL	
MATERIAL:	
<input type="checkbox"/> FR-408	<input checked="" type="checkbox"/> FR-4 High Tg <input type="checkbox"/> OTHER
THICKNESS:	<input checked="" type="checkbox"/> 62 MIL (1.6mm) +/-10% <input type="checkbox"/> OTHER
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/-
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/-
DRILLING:	
REFERENCE:	<input checked="" type="checkbox"/> AS SHOWN <input checked="" type="checkbox"/> NC_DRILL FILES
PTH COPPER THICKNESS:	<input checked="" type="checkbox"/> 20-30 um <input type="checkbox"/> OTHER
BOARD FINISH:	
SILKSCREEN:	<input checked="" type="checkbox"/> TOP <input checked="" type="checkbox"/> BOTTOM
SILKSCREEN COLOR:	<input checked="" type="checkbox"/> WHITE <input type="checkbox"/> OTHER
SOLDER RESIST COLOR:	<input type="checkbox"/> GREEN <input checked="" type="checkbox"/> OTHER_RED <input checked="" type="checkbox"/> MATTE <input type="checkbox"/> SEMI-GLOSS
SURFACE FINISH:	
<input checked="" type="checkbox"/> IMMERSION GOLD (ENIG)	<input type="checkbox"/> ENEPIG
<input type="checkbox"/> IMM. TIN/SILVER OR EQUIV	<input type="checkbox"/> OTHER
ARRAY/PANEL:	
<input type="checkbox"/> CUT AND TRM PER M1 BOARD OUTLINE	<input type="checkbox"/> N.C. ROUTE <input checked="" type="checkbox"/> V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS ->	<input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3
<input checked="" type="checkbox"/> RoHS	<input type="checkbox"/> OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94-V0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION:	<input type="checkbox"/> YES
BARE BOARD ELEC. TEST:	<input type="checkbox"/> NONE <input checked="" type="checkbox"/> REQUIRED <input type="checkbox"/> PER ORDER

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
 Z22 ■ This Assembly Note will show in the PcbDoc and associated outputs
 Z23 ■ This Assembly Note will show in the PcbDoc and associated outputs
 Z24 ■ This Assembly Note will show in the PcbDoc and associated outputs



COMPONENTS MARKED 'DNP' SHOULD NOT BE ORDERED. DNP COMPONENTS SHOULD NOT BE ORDERED.
 ASSEMBLY VARIANT: 001
 ASSEMBLY VARIANT: 001

REV: 1	DATE: 12/23/2023	BY: [Signature]	DESCRIPTION: [Signature]	DESIGNER: [Signature]	DATE: 12/23/2023	BY: [Signature]	DESCRIPTION: [Signature]	DESIGNER: [Signature]	DATE: 12/23/2023	BY: [Signature]	DESCRIPTION: [Signature]	DESIGNER: [Signature]	DATE: 12/23/2023	BY: [Signature]	DESCRIPTION: [Signature]	DESIGNER: [Signature]	DATE: 12/23/2023	BY: [Signature]	DESCRIPTION: [Signature]	DESIGNER: [Signature]	DATE: 12/23/2023	BY: [Signature]	DESCRIPTION: [Signature]		
LAYER NAME = Main Board Top		TID #: 01010237		DATE: 12/23/2023		BY: [Signature]		DESCRIPTION: [Signature]		DESIGNER: [Signature]		DATE: 12/23/2023		BY: [Signature]		DESCRIPTION: [Signature]		DESIGNER: [Signature]		DATE: 12/23/2023		BY: [Signature]		DESCRIPTION: [Signature]	
PROJECT NAME: [Signature]		LAYER ASSEMBLY: [Signature]		DATE: 12/23/2023		BY: [Signature]		DESCRIPTION: [Signature]		DESIGNER: [Signature]		DATE: 12/23/2023		BY: [Signature]		DESCRIPTION: [Signature]		DESIGNER: [Signature]		DATE: 12/23/2023		BY: [Signature]		DESCRIPTION: [Signature]	

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PROJECT TITLE: AC and DC Current Fault Detection Reference Design	
DESIGNED FOR: Public Release	
FILE NAME: TIDA-010237.PcbDoc	
ENGINEER: Nic Gough	LAYOUT BY: Who did the Layout?
SCALE: 0.69	ALTIM DESIGNER VERSION: 23.0.1.38

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