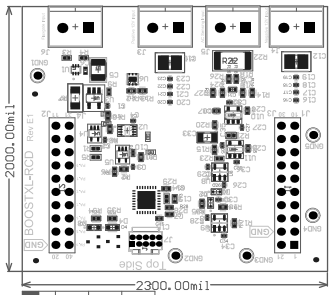
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer		1.40mil		
	Dielectric1	FR-4	8.00mil	4.2	
2	GND		1.40mil		
	Dielectric 2	FR-4	40.00mil	4.2	
3	Power		1.40mil		
	Dielectric 3	FR-4	8.00mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				

Z21 ■Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■This Assembly Note will show in the PcbDoc and associated outputs
Z23 ■This Assembly Note will show in the PcbDoc and associated outputs
Z24 ■This Assembly Note will show in the PcbDoc and associated outputs



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: 001

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [ ] GREEN [X] OTHER RED
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

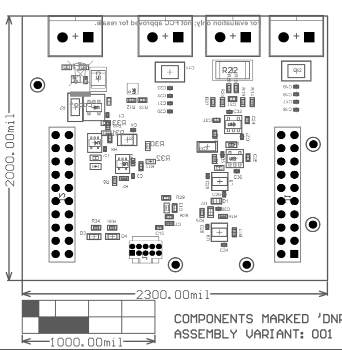
TEXAS INSTRUMENTS

PROJECT TITLE: AC and DC Current Fault Detection Reference Design
DESIGNED FOR: Public Release
FILE NAME: TIDA-010237.PcbDoc

ENGINEER: Nic Gough	LAYOUT BY: Who did the Layout?
SCALE: 0.69	ALTIUM DESIGNER VERSION: 23.0.1.38

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer		1.40mil		
	Dielectric1	FR-4	8.00mil	4.2	
2	GND		1.40mil		
	Dielectric 2	FR-4	40.00mil	4.2	
3	Power		1.40mil		
	Dielectric 3	FR-4	8.00mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
ZZ2 ■ This Assembly Note will show in the PcbDoc and associated outputs
ZZ3 ■ This Assembly Note will show in the PcbDoc and associated outputs
ZZ4 ■ This Assembly Note will show in the PcbDoc and associated outputs



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: 001

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [ ] GREEN [X] OTHER RED
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

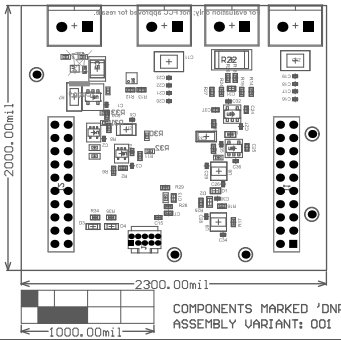
TEXAS INSTRUMENTS

PROJECT TITLE: AC and DC Current Fault Detection Reference Design
DESIGNED FOR: Public Release
FILE NAME: TIDA-010237.PcbDoc
ENGINEER: Nic Gough
LAYOUT BY: Who did the Layout?
SCALE: 0.69
ALTIUM DESIGNER VERSION: 23.0.1.38

	BOARD #: TIDA-010237	REV: E1	
LAYER NAME =	TID #: TIDA-010237		
PLOT NAME = Assembly Drawing	GENERATED : 12/23/2022 9:10:32 AM		TEXAS INSTRUMENTS

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer		1.40mil		
	Dielectric1	FR-4	8.00mil	4.2	
2	GND		1.40mil		
	Dielectric 2	FR-4	40.00mil	4.2	
3	Power		1.40mil		
	Dielectric 3	FR-4	8.00mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				

Z21 ■Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■This Assembly Note will show in the PcbDoc and associated outputs
Z23 ■This Assembly Note will show in the PcbDoc and associated outputs
Z24 ■This Assembly Note will show in the PcbDoc and associated outputs



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: 001

DESIGN INFORMATION	
MIN. TRACK WIDTH: 8 MIL	
MIN. CLEARANCE: 0.2 mm	
MIN. VIA PAD SIZE: 24 MIL	
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL	
MATERIAL:	
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER	
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER	
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2	
[ ] OTHER +/-	
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2	
[ ] OTHER +/-	
DRILLING:	
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES	
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER	
BOARD FINISH:	
SILKSCREEN: [X] TOP [X] BOTTOM	
SILKSCREEN COLOR: [X] WHITE [ ] OTHER	
SOLDER RESIST COLOR: [ ] GREEN [X] OTHER RED	
[X] MATTE [ ] SEMI-GLOSS	
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG	
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER	
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE	
[ ] N.C. ROUTE [X] V. SCORE	
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:	
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3	
[X] RoHS [ ] OTHER PER ORDER	
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.	
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION: [ ] YES	
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER	

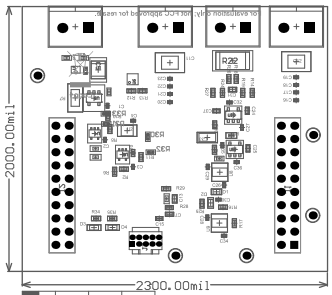
TEXAS INSTRUMENTS

PROJECT TITLE: AC and DC Current Fault Detection Reference Design	
DESIGNED FOR: Public Release	
FILE NAME: TIDA-010237.PcbDoc	
ENGINEER: Nic Gough	LAYOUT BY: Who did the Layout?
SCALE: 0.69	ALTIUM DESIGNER VERSION: 23.0.1.38

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer		1.40mil		
	Dielectric1	FR-4	8.00mil	4.2	
2	GND		1.40mil		
	Dielectric 2	FR-4	40.00mil	4.2	
3	Power		1.40mil		
	Dielectric 3	FR-4	8.00mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				

DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL
MATERIAL:	[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS:	[X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE:	[X] ANSI IPC-6012 TYPE 3 CLASS 2
	[ ] OTHER +/-
BOW & TWIST:	[X] ANSI IPC-6012 TYPE 3 CLASS 2
	[ ] OTHER +/-
DRILLING:	
REFERENCE:	[X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS:	[X] 20-30 um [ ] OTHER
BOARD FINISH:	
SILKSCREEN:	[X] TOP [X] BOTTOM
SILKSCREEN COLOR:	[X] WHITE [ ] OTHER
SOLDER RESIST COLOR:	[ ] GREEN [X] OTHER RED
	[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH:	[X] IMMERSION GOLD (ENIG) [ ] ENEPIG
	[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL:	[ ] CUT AND TRIM PER M1 BOARD OUTLINE
	[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION:	MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
	[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
	[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-VO REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION:	[ ] YES
BARE BOARD ELEC. TEST:	[ ] NONE [X] REQUIRED [ ] PER ORDER

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ This Assembly Note will show in the PcbDoc and associated outputs
Z23 ■ This Assembly Note will show in the PcbDoc and associated outputs
Z24 ■ This Assembly Note will show in the PcbDoc and associated outputs



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: 001

TEXAS INSTRUMENTS

PROJECT TITLE: AC and DC Current Fault Detection Reference Design
DESIGNED FOR: Public Release
FILE NAME: TIDA-010237.PcbDoc

ENGINEER: Nic Gough	LAYOUT BY: Who did the Layout?
SCALE: 0.69	ALTIUM DESIGNER VERSION: 23.0.1.38

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265