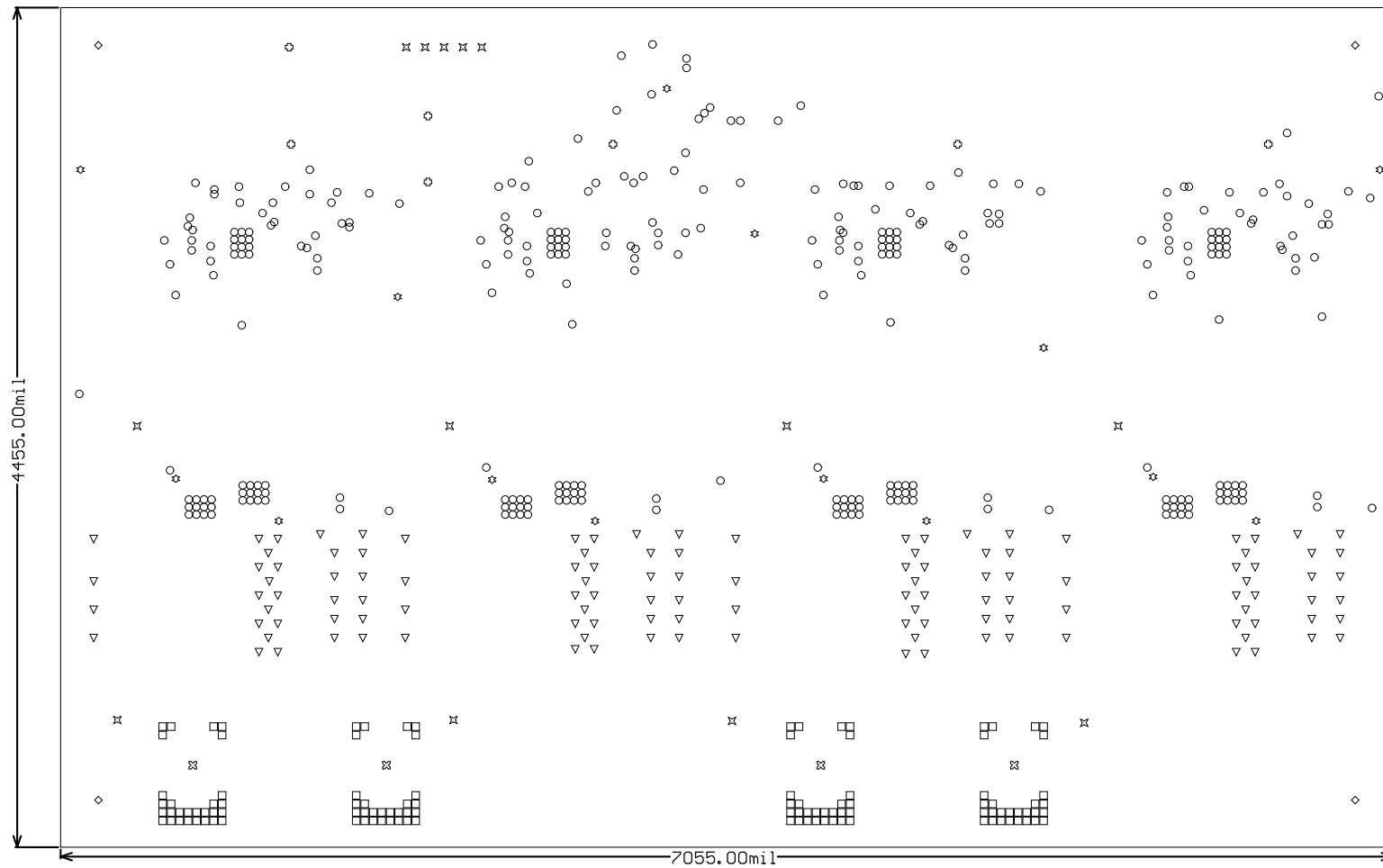


**Layer Stack Up Detail for: SAT0085E1-1.PcbDoc**

Layer Name	Order Document	Copper Thickness	Dielectric Material
Top Solder Mask	<.GTS>		Solder Resist
Top Layer	<.G1>	1.4mil	FR-4 High TG
MidLayer1	<.G1>	0.7mil	FR-4 High TG
MidLayer2	<.G2>	0.7mil	FR-4 High TG
Bottom Layer	<.GBL>	1.4mil	FR-4 High TG
Bottom Solder Mask	<.GBS>		Solder Resist

Symbol	Hit Count	Tool Size	Plated	Hole Type
○	322	10mil (0.254mm)	PTH	Round
☆	14	15mil (0.381mm)	PTH	Round
□	112	16mil (0.406mm)	PTH	Round
▽	120	28mil (0.711mm)	PTH	Round
⊠	13	40mil (1.016mm)	PTH	Round
◇	7	63mil (1.6mm)	PTH	Round
⊞	4	125.984mil (3.2mm)	PTH	Round
⊞	4	188mil (4.775mm)	PTH	Round
<b>596 Total</b>				

Drill Table



**DESIGN INFORMATION**

BOARD SIZE (REFER ALSO ARRAY/PANEL PROFILING INFORMATION)  
7055MIL X 4455MIL

Number of Layers : 4  
 MIN. TRACK WIDTH: 8 MIL  
 MIN. CLEARANCE: 10 MIL  
 MIN. VIA PAD SIZE: 20 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL  
 PER IPC-D-275 CLASS 2 LEVEL C  
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

**MATERIAL:**  
 FR-4  FR-4 High Tg  OTHER \_\_\_\_\_  
 THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER \_\_\_\_\_  
 TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_  
 BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

**COPPER THICKNESS (FINISHED):**  
 OUTER:  1.4MIL (1oz)  2MIL (1.4oz)  2.8MIL (2oz)  
 INNER SIGNAL:  0.7MIL (0.5oz)  2.8MIL (2oz)

**DRILLING:**  
 REFERENCE:  AS SHOWN  NC\_DRILL FILES  
 PTH MIN COPPER THICKNESS:  1MIL  OTHER \_\_\_\_\_

**BOARD FINISH:**  
 SILKSCREEN:  TOP  BOTTOM  
 SILKSCREEN COLOR:  WHITE  OTHER \_\_\_\_\_  
 SOLDER RESIST COLOR:  GREEN  BLUE  OTHER \_\_\_\_\_

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  Pb-FREE HASL  
 OTHER \_\_\_\_\_

**ARRAY/PANEL:**  CUT AND TRIM PER MECH LAYER 1  
 N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:  
 ANSI IPC-A-600F CLASS ->  1  2  3  
 UL 94V-0  RoHS  OTHER PER ORDER

**ADDITIONAL REQUIREMENTS:**  
 MICROSECTION:  YES  
 BARE BOARD ELEC. TEST:  NONE  REQUIRED  PER ORDER  
 MANUFACTURER'S ID/LOGO:  RAIL  METAL  SILK



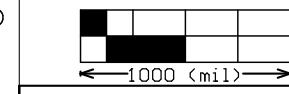
PROJECT TITLE:  
LM5122 4 phase boost

DESIGNED FOR:  
Public Release

FILE NAME:  
SAT0085E1-1.PcbDoc

ENGINEER: Viktor Schneigelberger      LAYOUT BY: Krypton Solutions/RS

SCALE: 1.09      ALTIUM DESIGNER VERSION: 10.0.0.27009



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: SAT0085	REV: E1.1	SUN REV: Not In VersionControl	Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME = 02085E1-1.PcbDoc				
PLOT NAME = Fabrication Drawing	GENERATED : 7/10/2014 2:48:48 PM	TEXAS INSTRUMENTS		

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