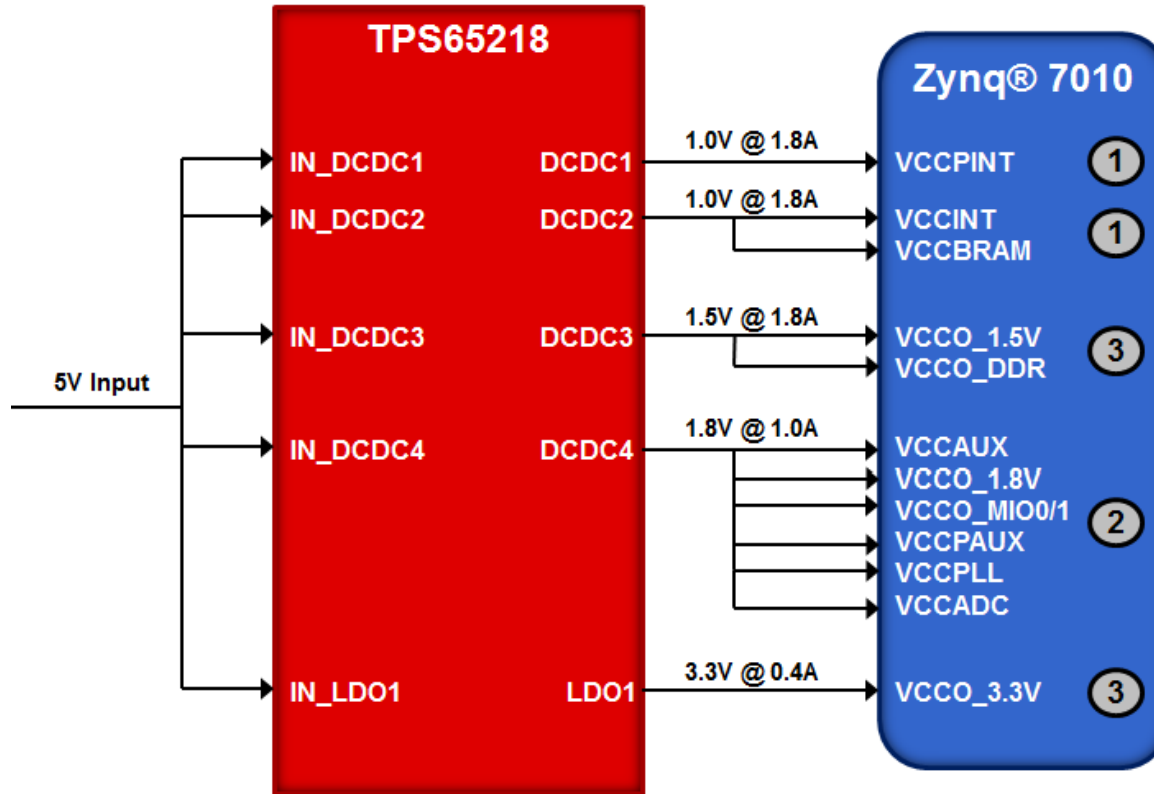


## Xilinx® Zynq® 7010 TPS65218 Block Diagram

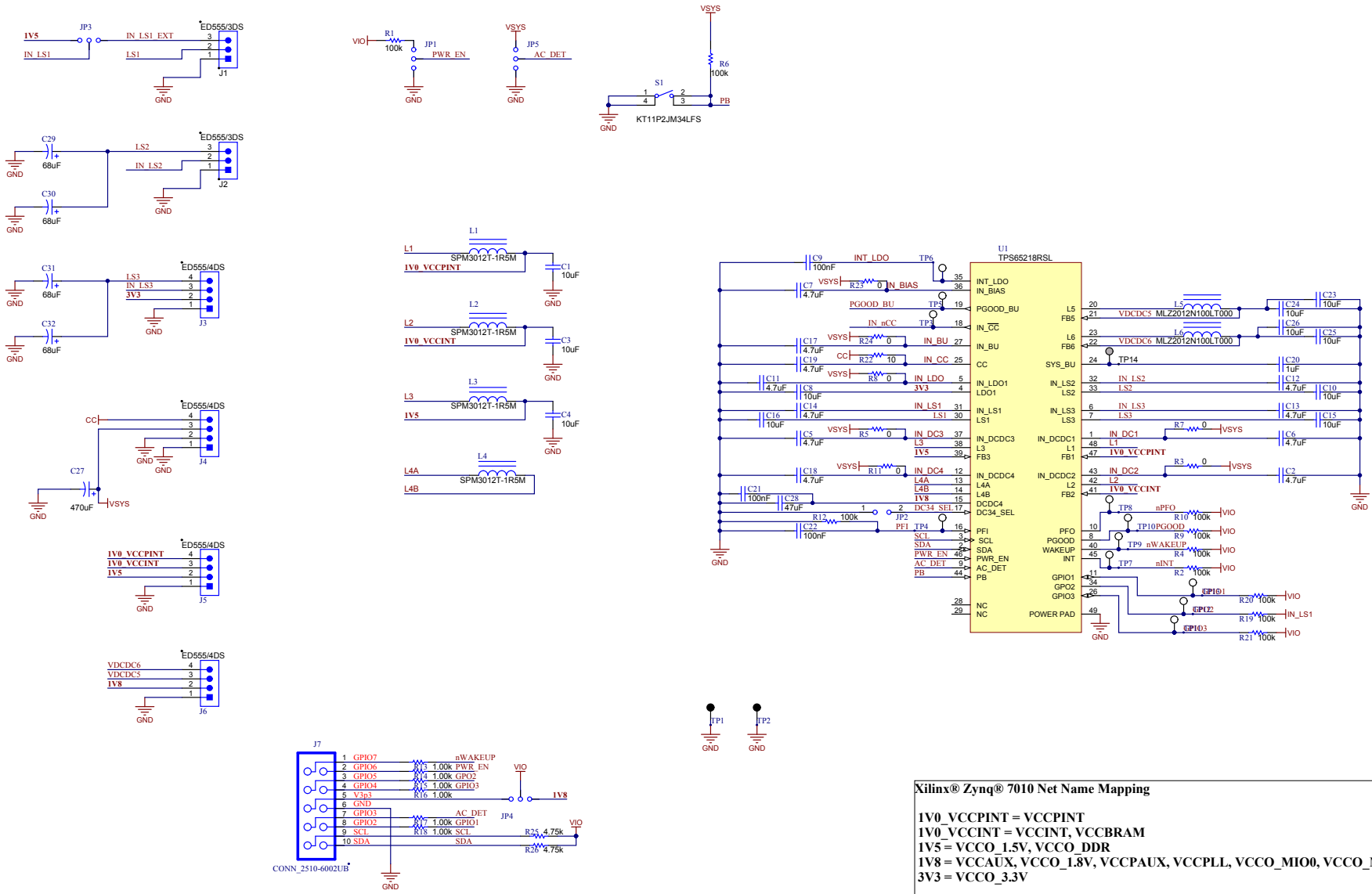


**Note:**

**(X) = Power Sequence Order**

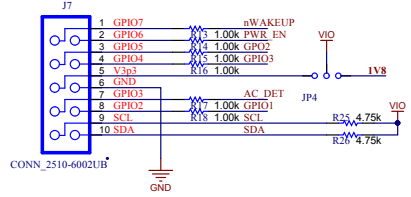
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Project Title: TIDA-00478			
Number: HVL100	Rev: A	Sheet Title: TIDA-00478	
SVN Rev: Not in version control		Assembly Variant: (No Variations)	Sheet 1 of 1
Drawn By: Paul Kundmueller		File: TPS65218_Zynq_7010_Block_Diagram_SchDoc Size: B	
Engineer:		Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	<a href="http://www.ti.com">http://www.ti.com</a>



**Xilinx® Zynq® 7010 Net Name Mapping**

**IV0\_VCCPINT = VCCPINT**  
**IV0\_VCCINT = VCCINT, VCCBRAM**  
**IV5 = VCCO\_1.5V, VCCO\_DDR**  
**IV8 = VCCAUX, VCCO\_1.8V, VCCPAUX, VCCPLL, VCCO\_MIO0, VCCO\_MIO1, VCCADC**  
**3V3 = VCCO\_3.3V**



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Designed for: Public Release		Mod. Date: 2/17/2015	
Project Title: TIDA-00478		Sheet Title:	
Number: HVL100	Rev: A	Assembly Variant: [No Variations]	Sheet: 1 of 1
Drawn By: Paul Kundmueller		File: TIDA00478_SchDoc	Size: B
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