

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Layer 1 - Top Layer	Copper	1.40mil		
4	Dielectric1	370HR	90.20mil	4.8	
5	Layer 2 - Bottom Layer	Copper	1.40mil		
6	Bottom Solder	Solder Resist	0.40mil	3.5	
7	Bottom Overlay				

**DESIGN INFORMATION**

MIN. TRACK WIDTH: 12 MIL  
 MIN. CLEARANCE: 0.2 mm  
 MIN. VIA PAD SIZE: 28 MIL  
 MINIMUM ANNULAR RING 0.05mm (2ML) EXTERNAL  
 PER IPC-D-275 CLASS 2 LEVEL C  
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

**MATERIAL:**  
 FR-408  FR-4 High Tg  OTHER \_\_\_\_\_  
 THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER 93 MIL +/-10%  
 TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_  
 BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

**DRILLING:**  
 REFERENCE:  AS SHOWN  NC\_DRILL FILES  
 PTH MIN COPPER THICKNESS:  1MIL  OTHER \_\_\_\_\_

**BOARD FINISH:**  
 SILKSCREEN:  TOP  BOTTOM  
 SILKSCREEN COLOR:  WHITE  OTHER \_\_\_\_\_  
 SOLDER RESIST COLOR:  GREEN  BLUE  OTHER BLACK

**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENEPIG  
 IMM. TIN/SILVER OR EQUIV  OTHER \_\_\_\_\_

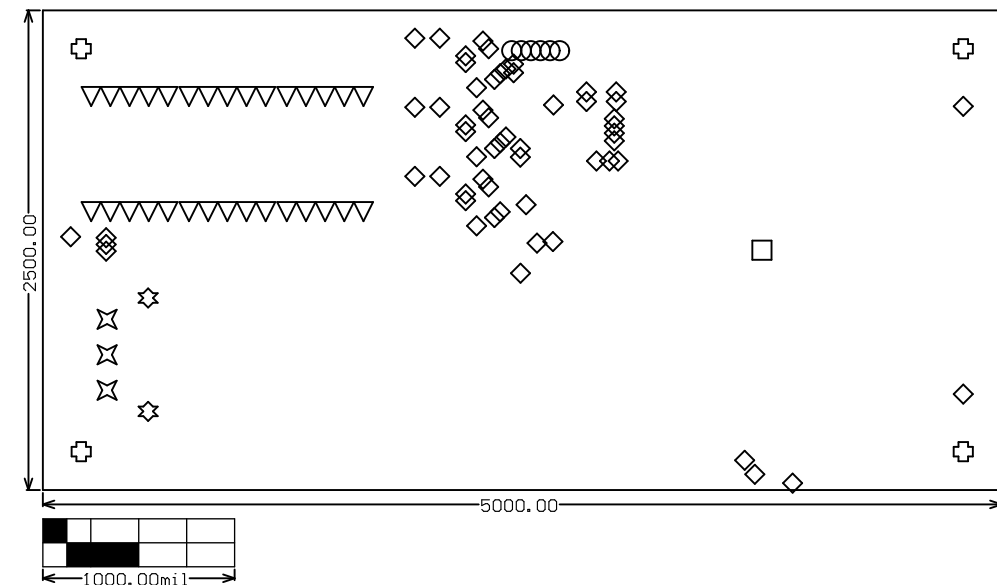
**ARRAY/PANEL:**  CUT AND TRIM PER MECH LAYER 1  
 N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:  
 ANSI IPC-A-600F CLASS ->  1  2  3  
 UL 94V-0  RoHS  OTHER PER ORDER

**ADDITIONAL REQUIREMENTS:**  
 MICROSECTION:  YES  
 BARE BOARD ELEC. TEST:  NONE  REQUIRED  PER ORDER  
 MANUFACTURER'S UL:  RAIL  METAL  SILK

**Fab. shop may not add any markings to the top of the board. U/L and RoHS may be added to the bottom. All vias must be tented on top and bottom. Soldermask must have glossy finish.**

Symbol	Quantity	Finished Hole Size	Plated	Hole Type
□	1	185.00mil (4.699mm)	NPTH	Round
◇	58	12.00mil (0.305mm)	PTH	Round
○	6	26.00mil (0.660mm)	PTH	Round
▽	30	33.46mil (0.850mm)	PTH	Round
☆	2	50.00mil (1.270mm)	PTH	Round
✱	3	72.83mil (1.850mm)	PTH	Round
⊕	4	125.98mil (3.200mm)	PTH	Round
	104 Total			



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00480	REV: E1	SUN REV: Not In VersionControl	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME = <b>0005-00480</b>				
PLOT NAME = Fabrication Drawing	GENERATED : 2/18/2015 2:26:32 PM	TEXAS INSTRUMENTS		
ENGINEER: Nikkan Yadegary		LAYOUT BY: <b>krypton</b> solutions		
SCALE: 1.00		ALTIM DESIGNER VERSION: 14.3.14.34663		

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