REVISION RECORD				
WHO:	SCH REV:	PCB REV:	NOTES:	DATE:
TI-BL	R1.0	R1.0	Draft	05-Jun-2013
TI-BL	R1.1	R1.1	Edited SVS circuitry (U3,U4); Changed power supply (U14) resistors Changed F28377D (U1) pinout and connector pinout (J1) Changed ADC VREFHI circuitry (U17,U13) and switches (SW3, SW4)	24-Oct-2013
TI-BL	R1.1 ASSY A	R1.1	R16: 2K2 to 0R, R72: 0R0 to 100K, R74: 0R0 to 10K X1: Move to crystal with lower ESR U1: Swap VREFLOB and VREFLOD to match datasheet U1: Rename ADCINCAL0 & CAL1 to ADCIN14 & 15 Net Rename: HSEC_ADC-CAL0 & CAL1 to HSEC_ADCIN14 & 15 Net Rename: MCU_ADC-CAL0 & CAL1 to MCU_ADCIN14 & 15	09-May-2014

NOTES:

1) USB Differential Pairs - 90 Ohm

(A) USB-DM & USB-DP

(B) USB0_GPIO-42 & USB0_GPIO-43

(C) MCU_GPIO-42 & MCU_GPIO-43

2) EMIF - External Memory Interface Impedance Matching from J1 to U1

(A) MCU_GPIO-39:41, MCU_GPIO-44:52, MCU_GPIO-86:94 - Address [0:21]

(B) MCU_GPIO-85, MCU_GPIO-83:53 - Data [0:31]

(C) MCU_GPIO-30 - Clock

(D) MCU_GPIO-37, 31, 29 - Read/Write/ClkEn Pins

(E) MCU_GPIO-32, 34, 35, 28 - Chip Select Pins

3) ADC Differential Pair Impedance Matching

(A) HSEC_ADC even pins should match with HSEC_ADC + 1 pin (ie HSEC_ADC-C2 should match with HSEC_ADC-C3)

(B) MCU_ADC even pins should match with MCU_ADC + 1 pin (ie MCU_ADC-A0 should match with MCU_ADC-A1)

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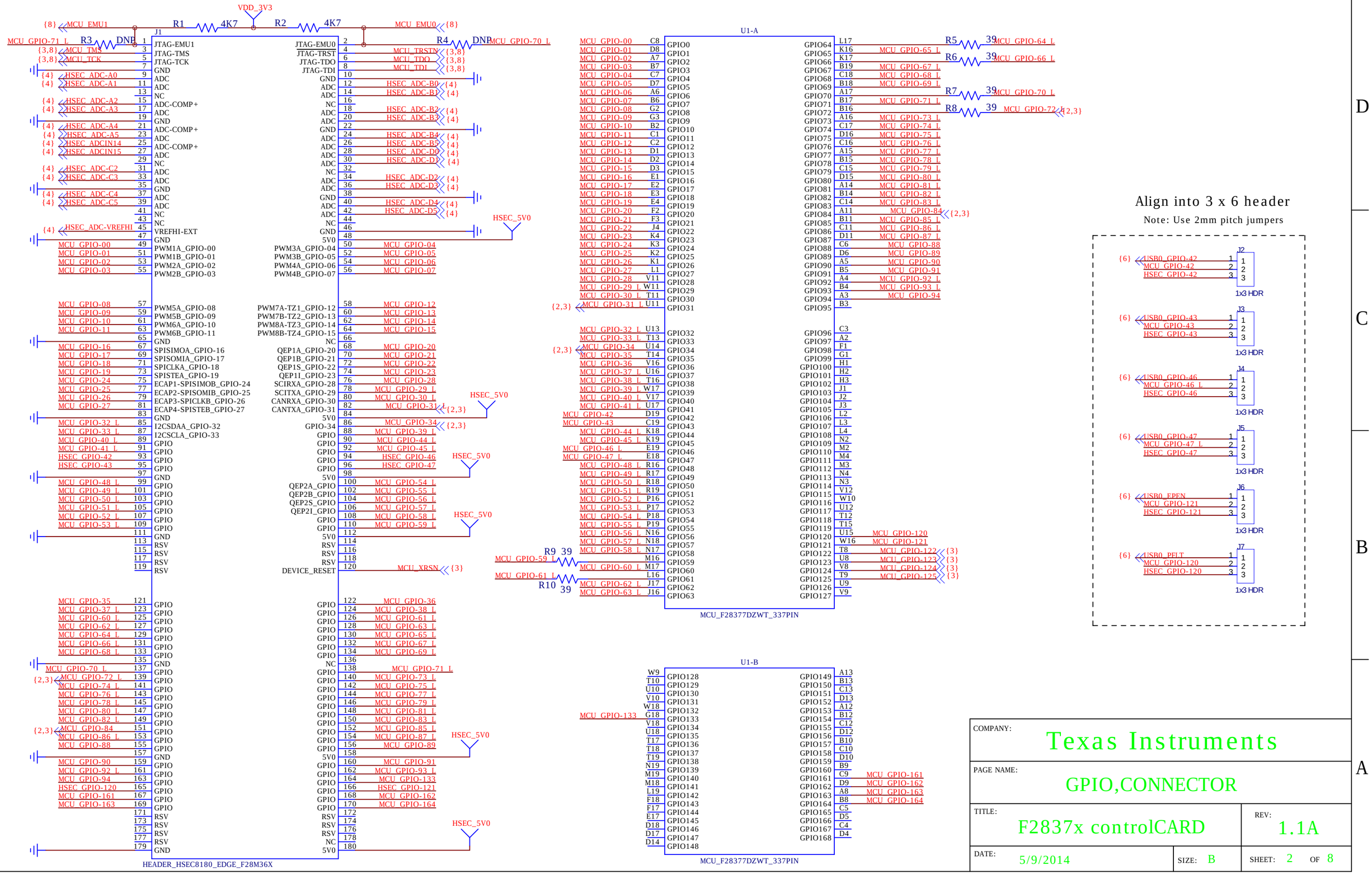
6
5
4
3
2
1
D
C
B
A
VDD_3V3
R1 4K7
R2 4K7
R3 DNP
R4 DNP
J1
JTAG-EMU1
JTAG-TMS
JTAG-TCK
JTAG-EMU0
JTAG-TRST
JTAG-TDO
JTAG-TDI
HEADER_HSEC8180_EDGE_F28M36X
U1-A
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
GPIO18
GPIO19
GPIO20
GPIO21
GPIO22
GPIO23
GPIO24
GPIO25
GPIO26
GPIO27
GPIO28
GPIO29
GPIO30
GPIO31
GPIO32
GPIO33
GPIO34
GPIO35
GPIO36
GPIO37
GPIO38
GPIO39
GPIO40
GPIO41
GPIO42
GPIO43
GPIO44
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GPIO46
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GPIO99
GPIO100
GPIO101
GPIO102
GPIO103
GPIO104
GPIO105
GPIO106
GPIO107
GPIO108
GPIO109
GPIO110
GPIO111
GPIO112
GPIO113
GPIO114
GPIO115
GPIO116
GPIO117
GPIO118
GPIO119
GPIO120
GPIO121
GPIO122
GPIO123
GPIO124
GPIO125
GPIO126
GPIO127
MCU_F28377DZWT_337PIN
U1-B
GPIO128
GPIO129
GPIO130
GPIO131
GPIO132
GPIO133
GPIO134
GPIO135
GPIO136
GPIO137
GPIO138
GPIO139
GPIO140
GPIO141
GPIO142
GPIO143
GPIO144
GPIO145
GPIO146
GPIO147
GPIO148
GPIO149
GPIO150
GPIO151
GPIO152
GPIO153
GPIO154
GPIO155
GPIO156
GPIO157
GPIO158
GPIO159
GPIO160
GPIO161
GPIO162
GPIO163
GPIO164
GPIO165
GPIO166
GPIO167
GPIO168
MCU_F28377DZWT_337PIN
R5 39
R6 39
R7 39
R8 39
R9 39
R10 39
Align into 3 x 6 header
Note: Use 2mm pitch jumpers
J2
J3
J4
J5
J6
J7
1x3 HDR
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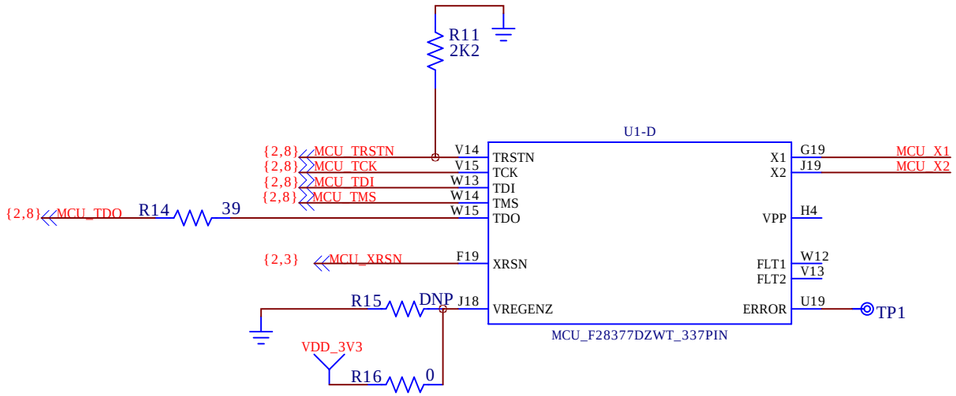
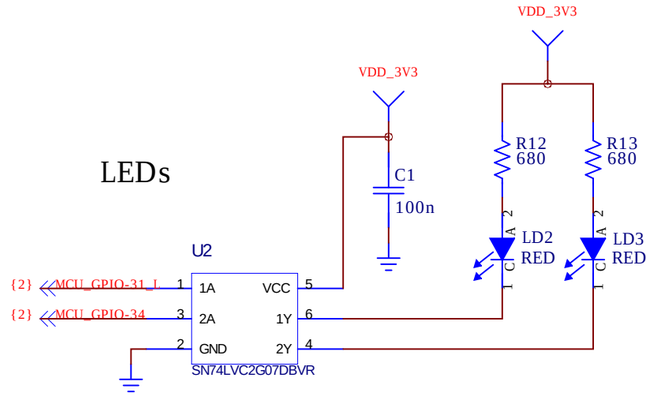
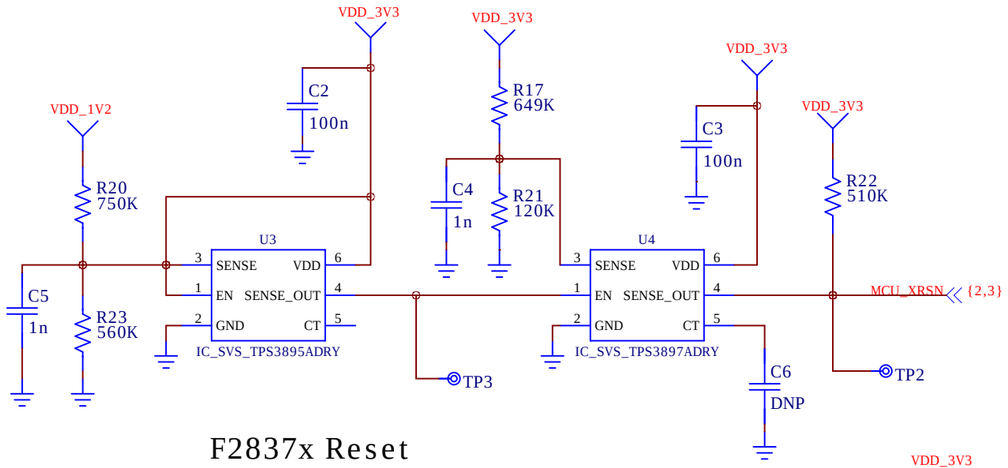
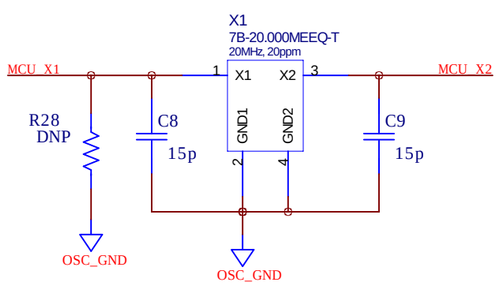


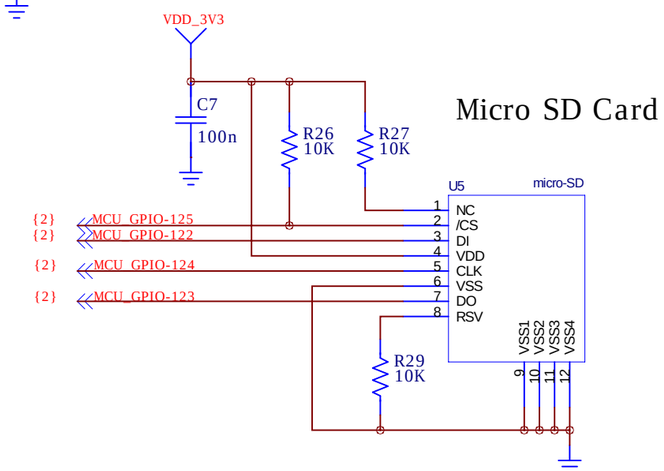




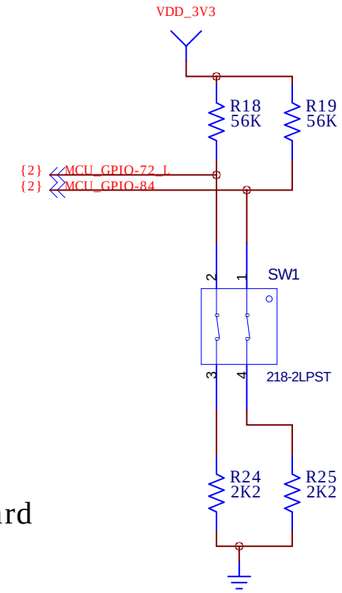
F2837x Reset



F2837x Clock



Micro SD Card



Boot Mode Selection Switch

*SW1 placed upside-down (so UP is open (1), DOWN is closed (0))

Selected Boot Mode Chart

(see datasheet for other boot modes and more information)

Mode #	GPIO72	GPIO84	Boot Mode
00	0	0	Boot from Parallel GPIO
01	0	1	Boot from SCI
02	1	0	Wait Boot Mode
03	1	1	Get Mode (Flash by default)

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If desired, isolate (or semi-isolate) all GND nets on this page (GNDA) from the main GND. If done, the GND terminal of C82 should also go to GNDA.

All positions of SW2 should be in the ON/up state.

VDDA_MCU_3V3

C10 100n C11 100n C12 100n

U6 U7 U8 U9 U10 U11 NUP4201MR6T1G (VP, VN, I/O_6, I/O_4, I/O_3, I/O_1)

HSEC_ADC-A0 R30 0
HSEC_ADC-A1 R31 0
HSEC_ADC-A2 R32 0
HSEC_ADC-A3 R33 0
HSEC_ADC-A4 R34 0
HSEC_ADC-A5 R35 0

HSEC_ADC-B0 R36 0
HSEC_ADC-B1 R37 0
HSEC_ADC-B2 R38 0
HSEC_ADC-B3 R39 0
HSEC_ADC-B4 R40 0
HSEC_ADC-B5 R41 0

HSEC_ADCIN14 R44 0
HSEC_ADCIN15 R45 0

HSEC_ADC-C2 R46 0
HSEC_ADC-C3 R47 0
HSEC_ADC-C4 R48 0
HSEC_ADC-C5 R49 0

HSEC_ADC-D0 R50 0
HSEC_ADC-D1 R51 0
HSEC_ADC-D2 R52 0
HSEC_ADC-D3 R53 0
HSEC_ADC-D4 R54 0
HSEC_ADC-D5 R55 0

U1-C

U1	ADCINA0
T1	ADCINA1
U2	ADCINA2
T2	ADCINA3
U3	ADCINA4
T3	ADCINA5
V2	ADCINB0
W2	ADCINB1
V3	ADCINB2
W3	ADCINB3
V4	ADCINB4
W4	ADCINB5
T4	ADCIN14
U4	ADCIN15
R3	ADCINC2
P3	ADCINC3
R4	ADCINC4
P4	ADCINC5
T5	ADCIND0
U5	ADCIND1
T6	ADCIND2
U6	ADCIND3
T7	ADCIND4
U7	ADCIND5

MCU_F28377DZWT_337PIN

C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 DNP

Place near U1

VDDA_MCU_3V3

VDDA	P6
VDDA	R6
VSSA	P1
VSSA	P5
VSSA	R5
VSSA	V7
VSSA	W1

C13 100n C14 100n

VREFHIA	V1
VREFHIB	W5
VREFHIC	R1
VREFHID	V5
VREFLOA	R2
VREFLOB	V6
VREFLOC	P2
VREFLOD	W6

C15 2u2 C16 2u2 C17 2u2 C18 2u2

SW2 4xSPST

Place near U1

IN_5V0

C95 100n
C96 2u2

VDDA_MCU_3V3

C43 100n
C44 2u2

U17 REF3033AIDBZR (IN, GND, OUT) 3.3V vref

U13 REF3030AIDBZR (IN, GND, OUT) 3.0V vref

R42 0
R43 DNP

HSEC_ADC-VREFHI {2}

C46 470n

SW3 CAS-D20TA

SW4 CAS-D20TA

VDDA_MCU_3V3

C45 100n

U12-A IC_OPA_LMP7709MT

U12-B IC_OPA_LMP7709MT

U12-C IC_OPA_LMP7709MT

U12-D IC_OPA_LMP7709MT

C97 100n C98 100n C99 100n C100 100n

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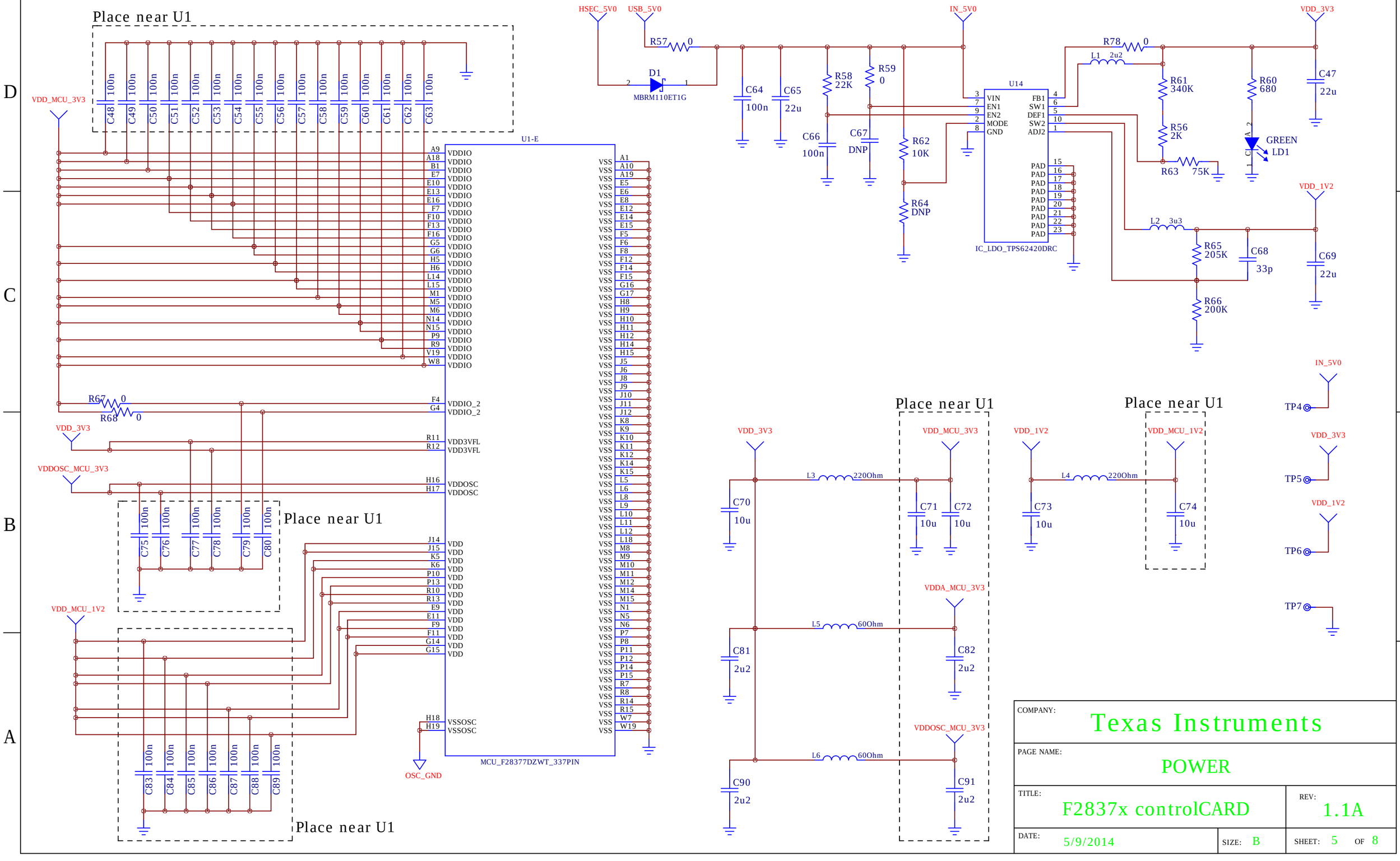
Place near U1
VDD_MCU_3V3
C48 100n
C49 100n
C50 100n
C51 100n
C52 100n
C53 100n
C54 100n
C55 100n
C56 100n
C57 100n
C58 100n
C59 100n
C60 100n
C61 100n
C62 100n
C63 100n
U1-E
A9 VDDIO
A18 VDDIO
B1 VDDIO
E7 VDDIO
E10 VDDIO
E13 VDDIO
E16 VDDIO
F7 VDDIO
F10 VDDIO
F13 VDDIO
F16 VDDIO
G5 VDDIO
G6 VDDIO
H5 VDDIO
H6 VDDIO
L14 VDDIO
L15 VDDIO
M1 VDDIO
M5 VDDIO
M6 VDDIO
N14 VDDIO
N15 VDDIO
P9 VDDIO
R9 VDDIO
V19 VDDIO
W8 VDDIO
R67 0
R68 0
F4 VDDIO_2
G4 VDDIO_2
VDD_3V3
R11 VDD3VFL
R12 VDD3VFL
VDDOSC_MCU_3V3
H16 VDDOSC
H17 VDDOSC
C75 100n
C76 100n
C77 100n
C78 100n
C79 100n
C80 100n
Place near U1
J14 VDD
J15 VDD
K5 VDD
K6 VDD
P10 VDD
P13 VDD
R10 VDD
R13 VDD
E9 VDD
E11 VDD
F9 VDD
F11 VDD
G14 VDD
G15 VDD
VDD_MCU_1V2
C83 100n
C84 100n
C85 100n
C86 100n
C87 100n
C88 100n
C89 100n
Place near U1
H18 VSSOSC
H19 VSSOSC
OSC_GND
VSS A1
VSS A10
VSS A19
VSS E5
VSS E6
VSS E8
VSS E12
VSS E14
VSS E15
VSS F5
VSS F6
VSS F8
VSS F12
VSS F14
VSS F15
VSS G16
VSS G17
VSS H8
VSS H9
VSS H10
VSS H11
VSS H12
VSS H14
VSS H15
VSS J5
VSS J6
VSS J8
VSS J9
VSS J10
VSS J11
VSS J12
VSS K8
VSS K9
VSS K10
VSS K11
VSS K12
VSS K14
VSS K15
VSS L5
VSS L6
VSS L8
VSS L9
VSS L10
VSS L11
VSS L12
VSS L18
VSS M8
VSS M9
VSS M10
VSS M11
VSS M12
VSS M14
VSS M15
VSS N1
VSS N5
VSS N6
VSS P7
VSS P8
VSS P11
VSS P12
VSS P14
VSS P15
VSS R7
VSS R8
VSS R14
VSS R15
VSS W7
VSS W19
MCU_F28377DZWT_337PIN
HSEC_5V0
USB_5V0
R57 0
D1
MBRM110ET1G
C64 100n
C65 22u
R58 22K
R59 0
C66 100n
C67 DNP
R62 10K
R64 DNP
IN_5V0
U14
VIN
EN1
EN2
MODE
GND
FB1
SW1
DEF1
SW2
ADJ2
PAD
IC_LDO_TPS62420DRC
R78 0
L1 2u2
R61 340K
R56 2K
R63 75K
R60 680
GREEN
LD1
VDD_3V3
C47 22u
VDD_1V2
L2 3u3
R65 205K
C68 33p
R66 200K
C69 22u
Place near U1
VDD_3V3
L3 220Ohm
C70 10u
VDD_MCU_3V3
C71 10u
C72 10u
VDDA_MCU_3V3
L5 60Ohm
C81 2u2
C82 2u2
VDDOSC_MCU_3V3
L6 60Ohm
C90 2u2
C91 2u2
Place near U1
VDD_1V2
L4 220Ohm
C73 10u
VDD_MCU_1V2
C74 10u
IN_5V0
TP4
VDD_3V3
TP5
VDD_1V2
TP6
TP7
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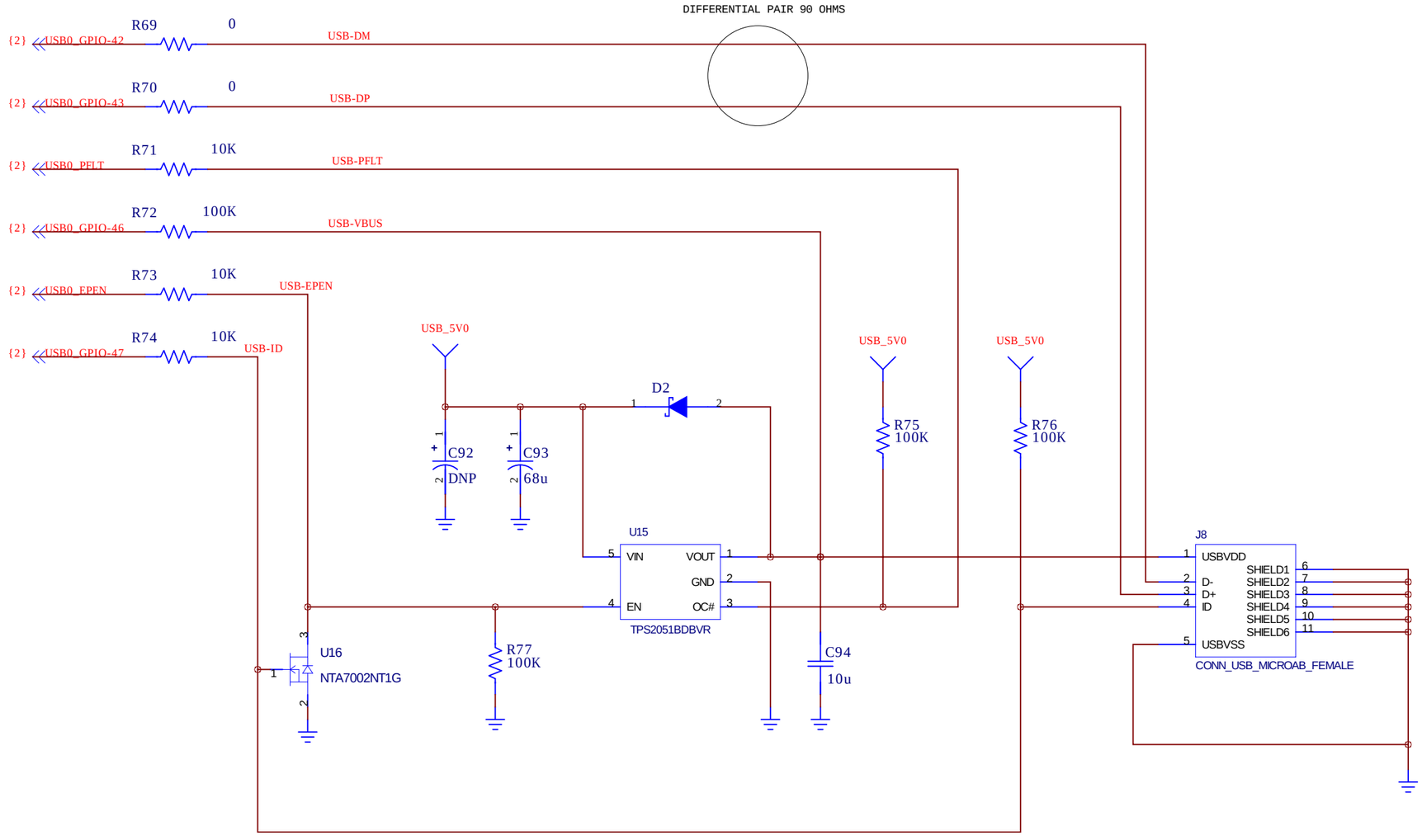

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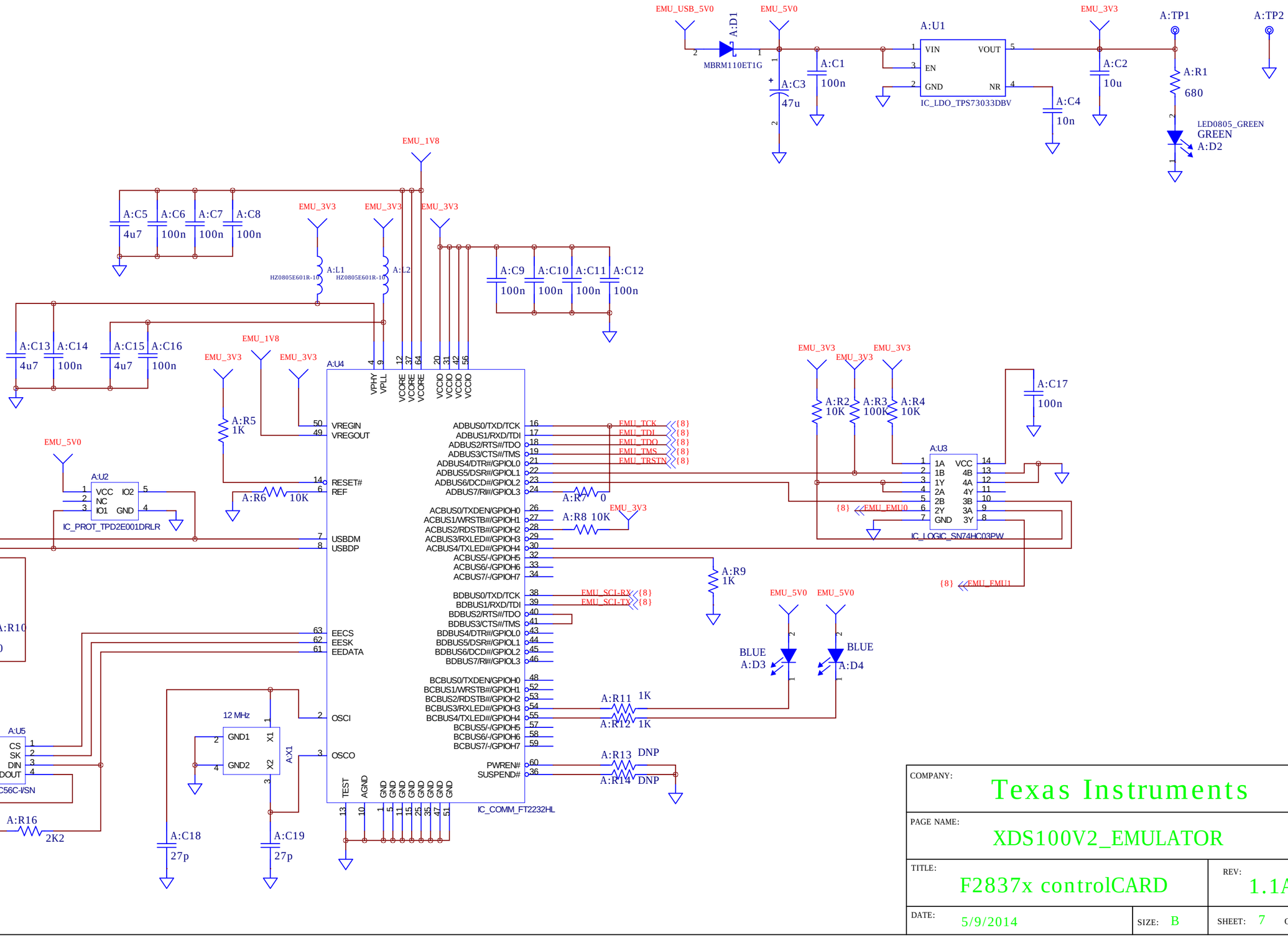

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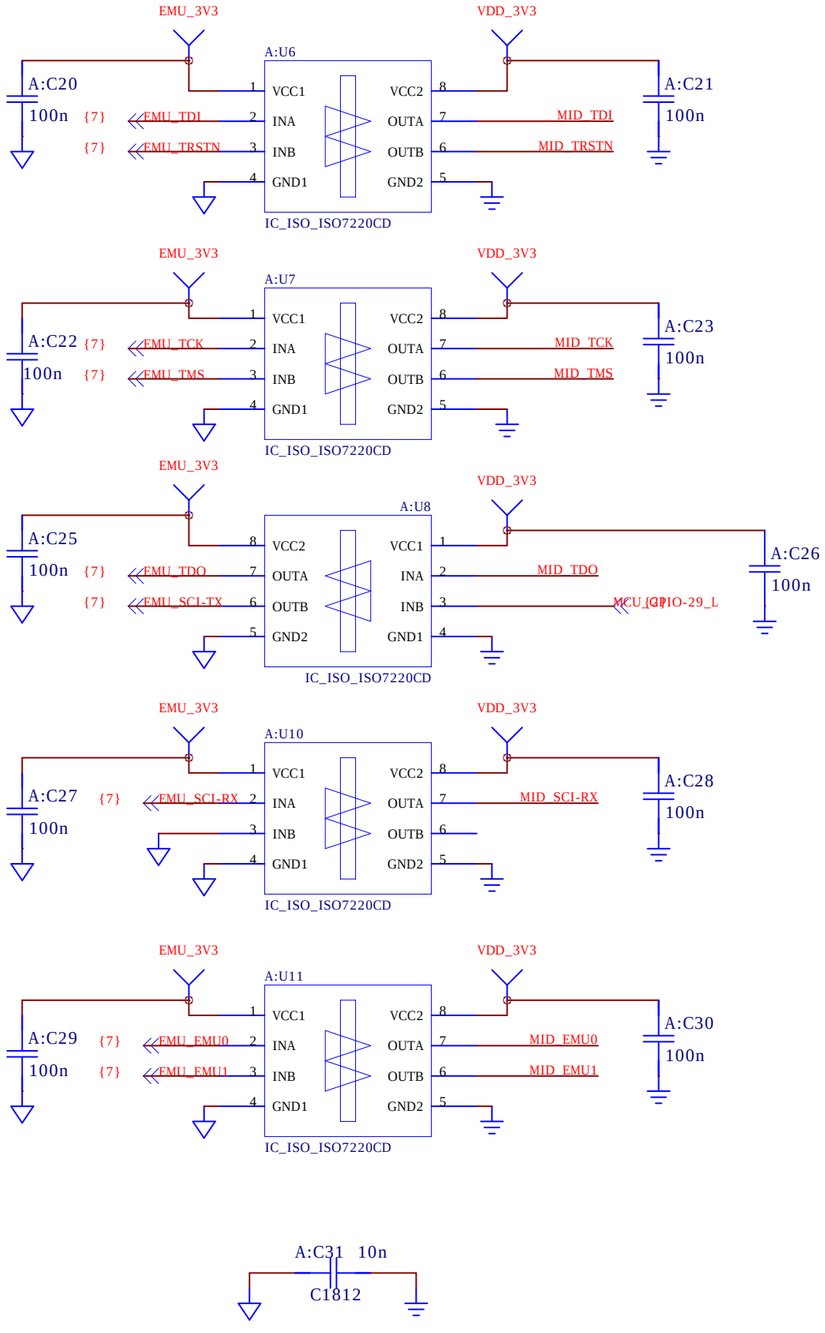
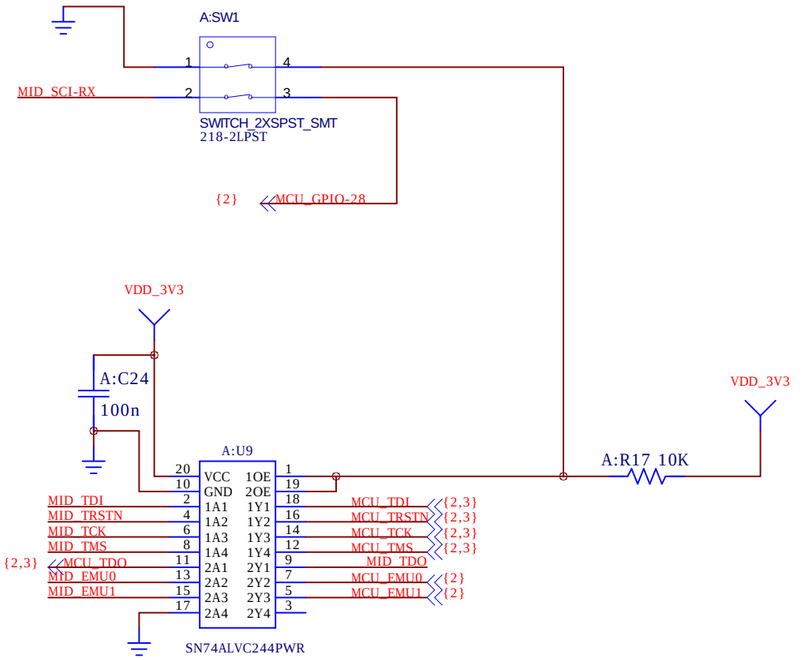


A:SW1 - Emulation & GPIO28 Switch

Pos 1 ON: Use xds100v2 emulator that is on the cCARD
Pos 1 OFF: Boot from FLASH/peripheral (see boot mode switch) OR use emulator on baseboard
Pos 2 ON: GPIO28 will be controlled by the USB-to-UART adapter on the FTDI chip
Pos 2 OFF: GPIO-28 can be controlled by a pin in HSEC connector



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