Optimized Radar System Design Using 66AK2L06 DSP+ARM® SoC and ADC14X250

Major Component Product Pages

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TI LMK04828 Product Page

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Revision History

Revision	Notes
Rev 1.0	Initial revision release

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Number: | Rev: E1 | Sheet Title:
SVN Rev: Version control disabled | Assembly Variant: 001 | Sheet: 1 of 35
Drawn By: | File: CoverSheet_01.SchDoc | Size: B
Engineer: a0271760 | Contact: http://www.ti.com/support

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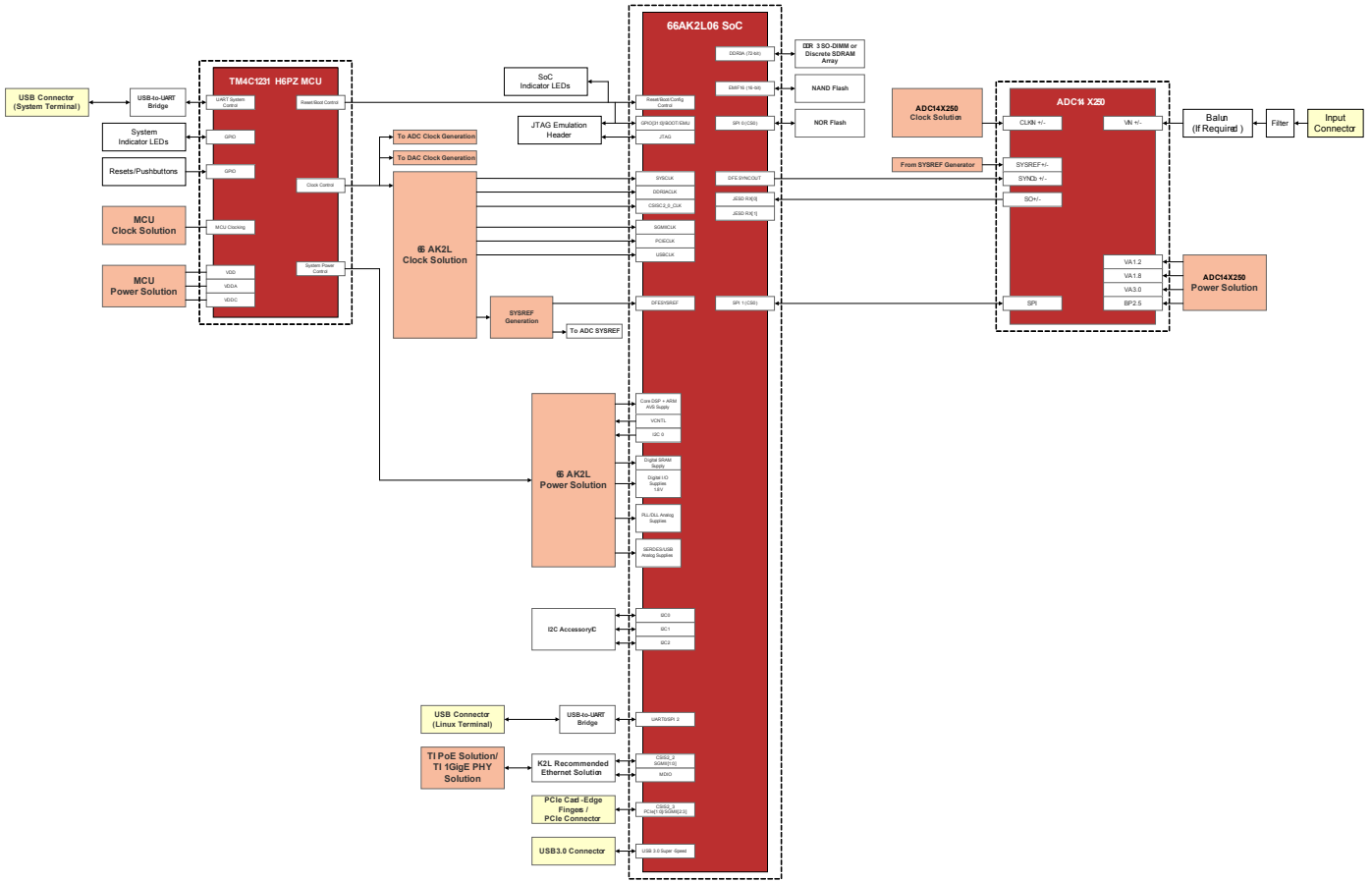
TI66AK2L06 and ADC14X250 Example System Diagram



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Drawn By: a0271760		File: system_diagram.SchDoc	Size: B
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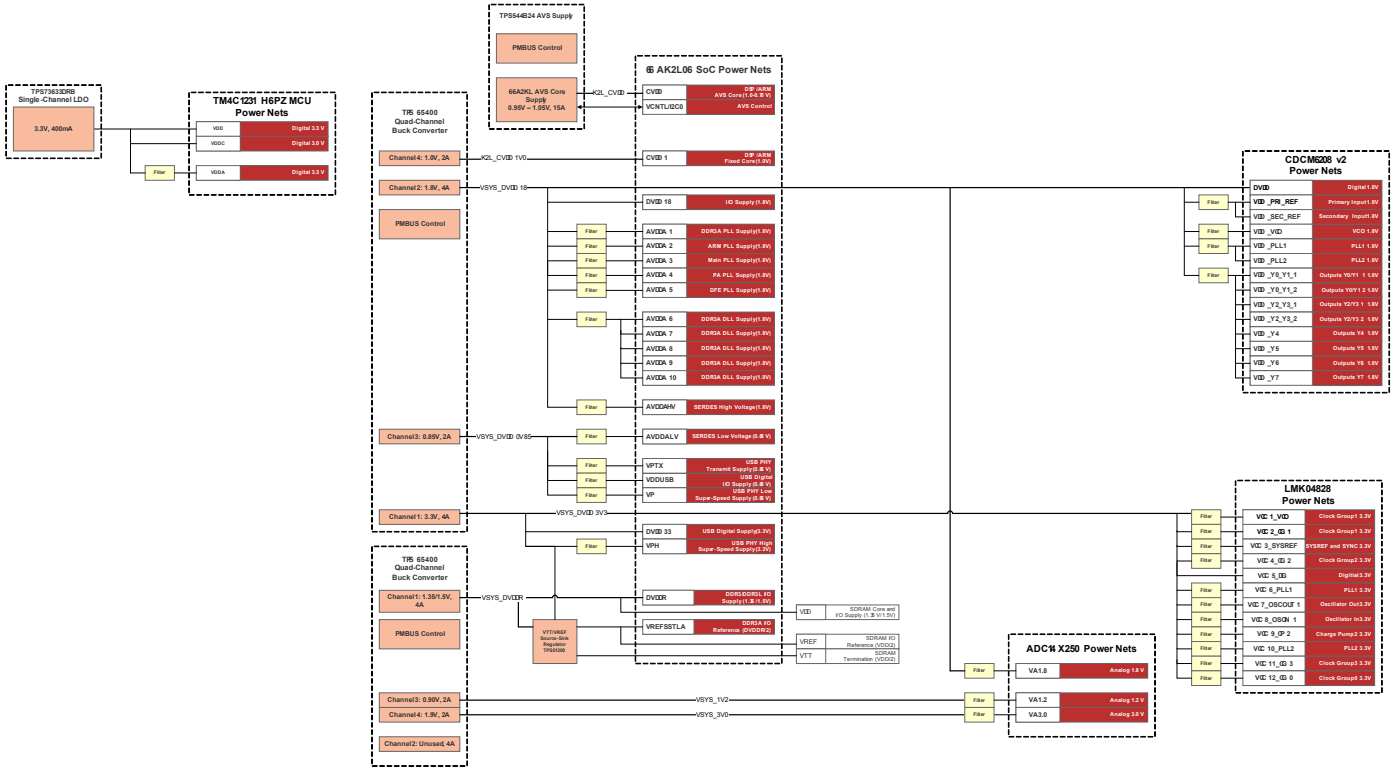
TI66AK2L06 and ADC14X250 Example System Power Supply Diagram



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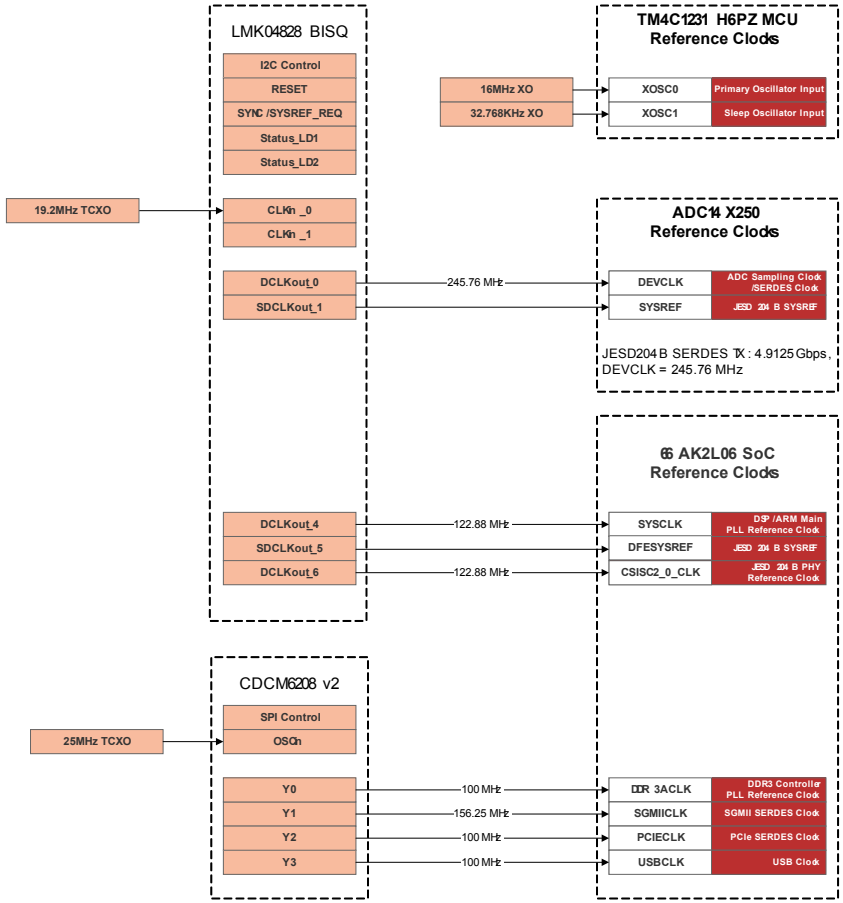
TI66AK2L06 and ADC14X250 Example System Clocking Diagram



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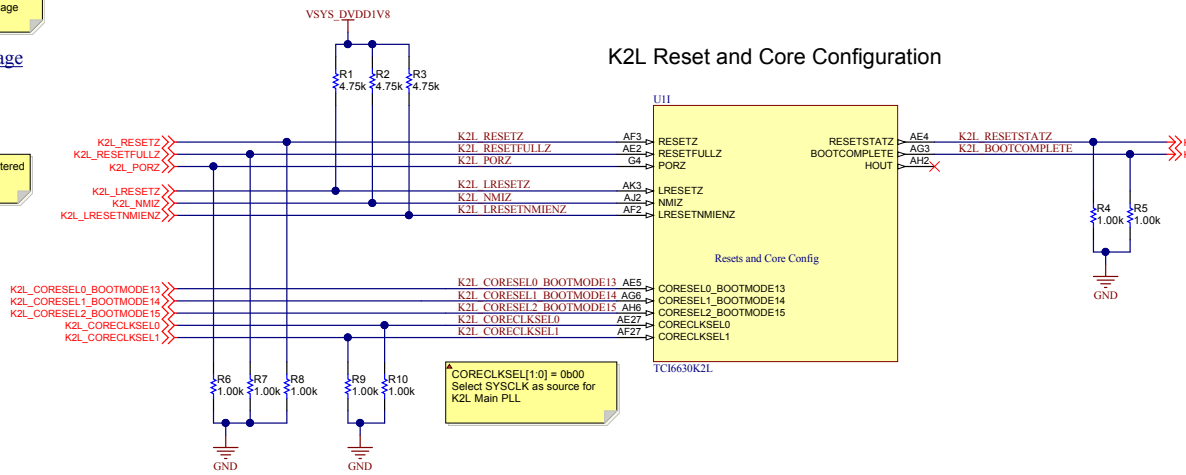
For schematic and layout recommendations and requirements see the K2L product page linked below.

TI 66AK2L06 Product Page

K2L Reset and Core Configuration

K2L BOOTMODE and RESET pins mastered by Board Mangement Controller (microcontroller) not shown here.



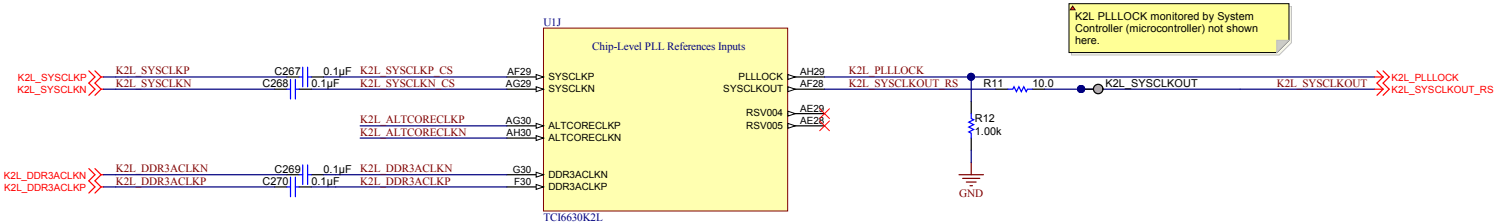
K2L RESETSTAT and BOOTCOMPLETE monitored by System Controller (microcontroller) not shown here.

CORECLKSEL[1:0] = 0b00
Select SYSCLK as source for K2L Main PLL

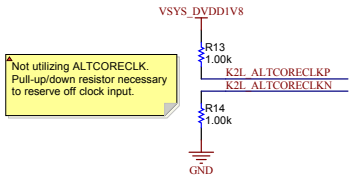
K2L Core Reference Clock Inputs

K2L SYSCLK sourced my LMK04828. When utilizing LVDS outputs of LMK04828 only AC-coupling is necessary.

K2L PLLLOCK monitored by System Controller (microcontroller) not shown here.



DDR3 controller reference clock solution not shown. Please see K2L EVM schematics.



Not utilizing ALTCORECLK. Pull-up/down resistor necessary to reserve off clock input.

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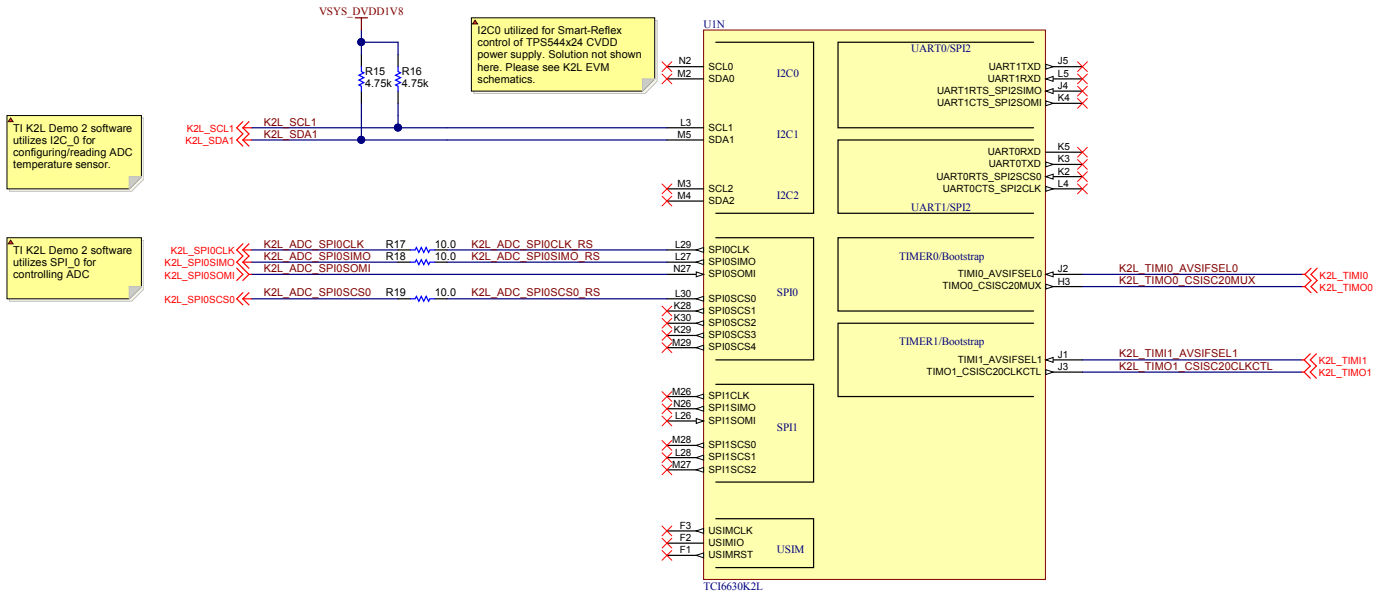
K2L Boot-Config, I2C, SPI, UART, Timer, and USIM



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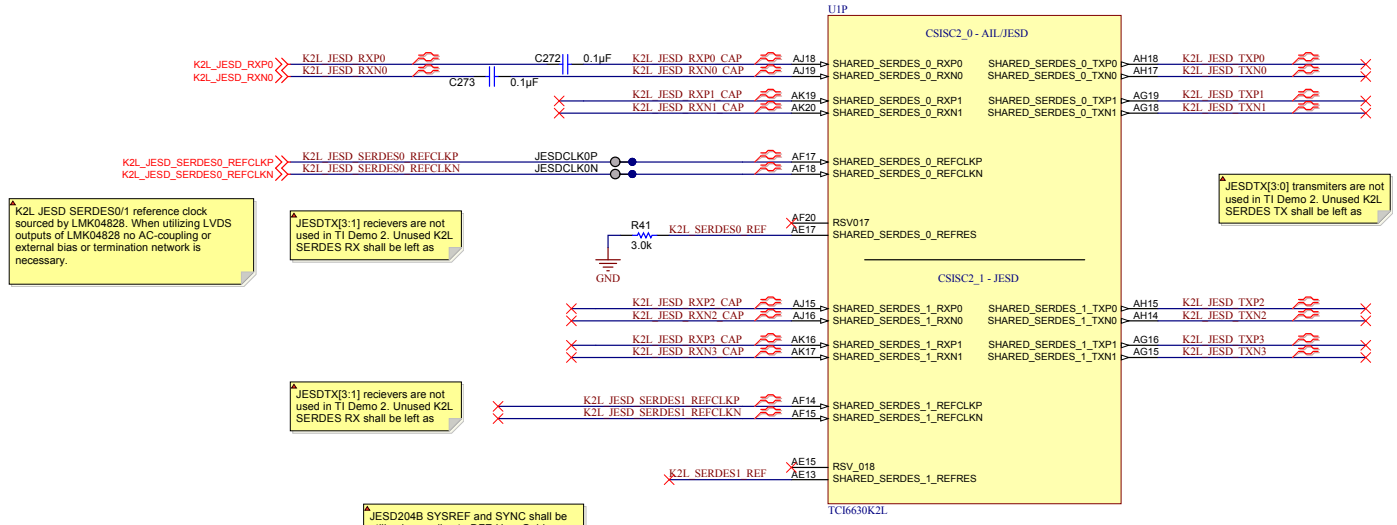
For schematic and layout recommendations and requirements see the K2L product page linked below.

TI 66AK2L06 Product Page

JESD204B SERDES shall be routed according to routing rules specified in the Keystone 2 SERDES User Guide (SPRUH03)

Keystone2 SERDES User Guide (SPRUHO3)

DFE JESD204B SERDES



K2L JESD SERDES0/1 reference clock sourced by LMK04828. When utilizing LVDS outputs of LMK04828 no AC-coupling or external bias or termination network is necessary.

JESDTX[3:1] recievers are not used in TI Demo 2. Unused K2L SERDES RX shall be left as

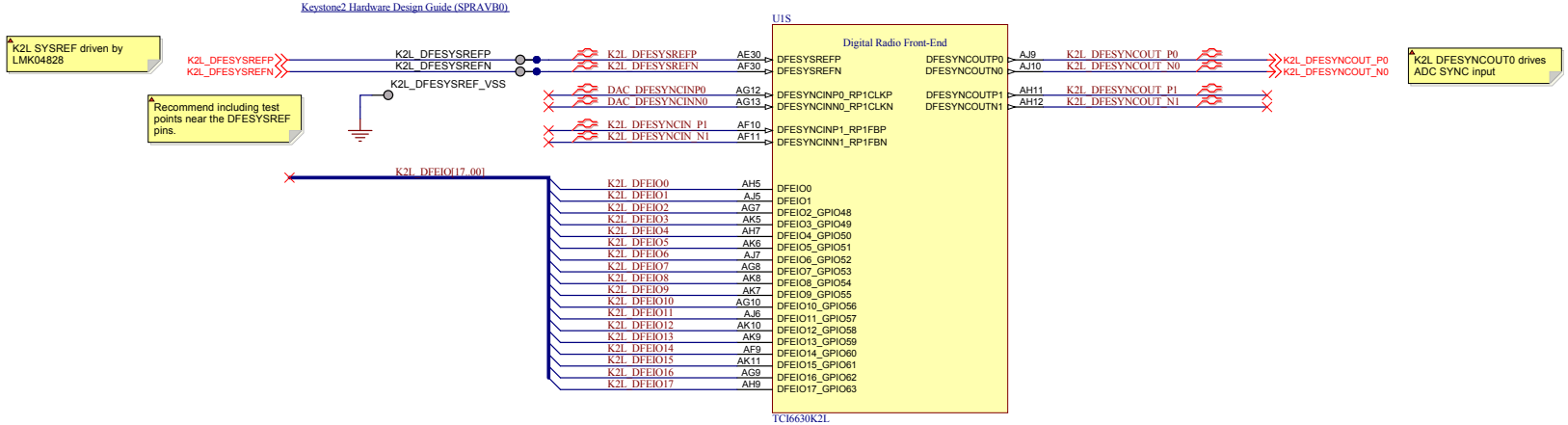
JESDTX[3:0] transmiters are not used in TI Demo 2. Unused K2L SERDES TX shall be left as

JESDTX[3:1] recievers are not used in TI Demo 2. Unused K2L SERDES RX shall be left as

JESD204B SYSREF and SYNC shall be utilized according to DFE User Guide (SPRUHX8) and routed according to Keystone 2 Hardware Design Guide (SPRAVB0) DFE peripheral section.

Keystone2 Hardware Design Guide (SPRAVB0)

DFE JESD204B SYSREF, SYNCIN/OUT and DFE I/O



K2L SYSREF driven by LMK04828

Recommend including test points near the DFESYSREF pins.

K2L DFESYNCOUT0 drives ADC SYNC input

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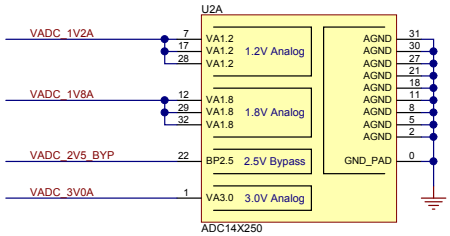
For schematic and layout recommendations and requirements see the ADC14X250 product page linked below.

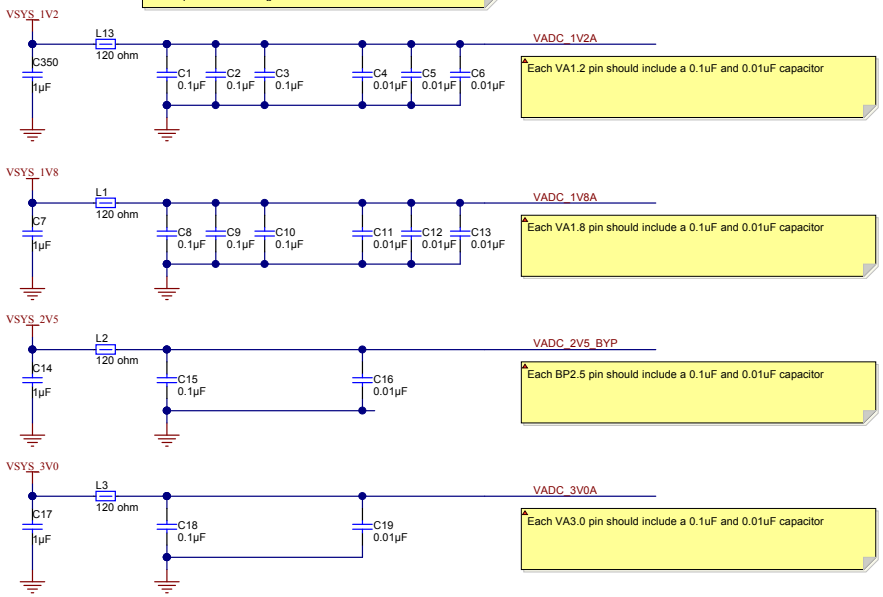
TI ADC14X250 Product Page

ADC Power Pins and Decoupling Capacitors



The ADC14X250 thermal pad (Pin 0) provides thermal dissipation for the ADC. Please ensure layout includes ground stitching vias to create a good thermal coupling between the ADC GND pad and the PCB GND layers

Decoupling caps shall be placed as close to ADC power pins as possible. Utilize minimal via dog-bones (via-in pad ideally) to ensure lowest possible mounting inductance.



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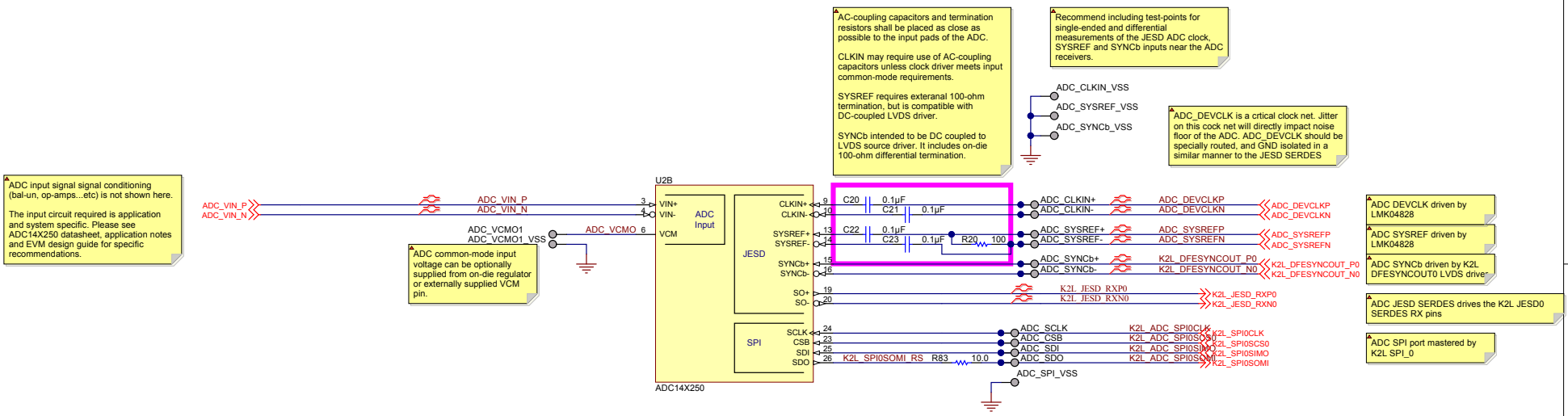
TI ADC14X250 Product Page

ADC Input, JESD204B Interface, SPI and Discrete I/O Control



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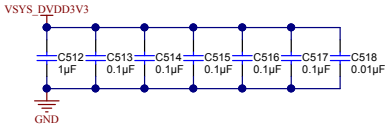
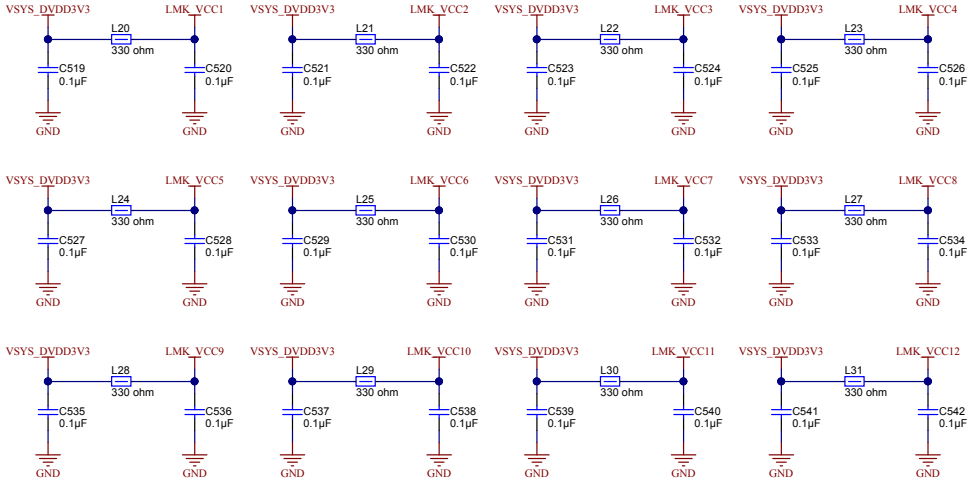
LMK04828 Decoupling Capacitors

LMK04828 decoupling shall be placed as close to the IC package as possible. See LMK04828 datasheet and EVM for example decoupling layout.





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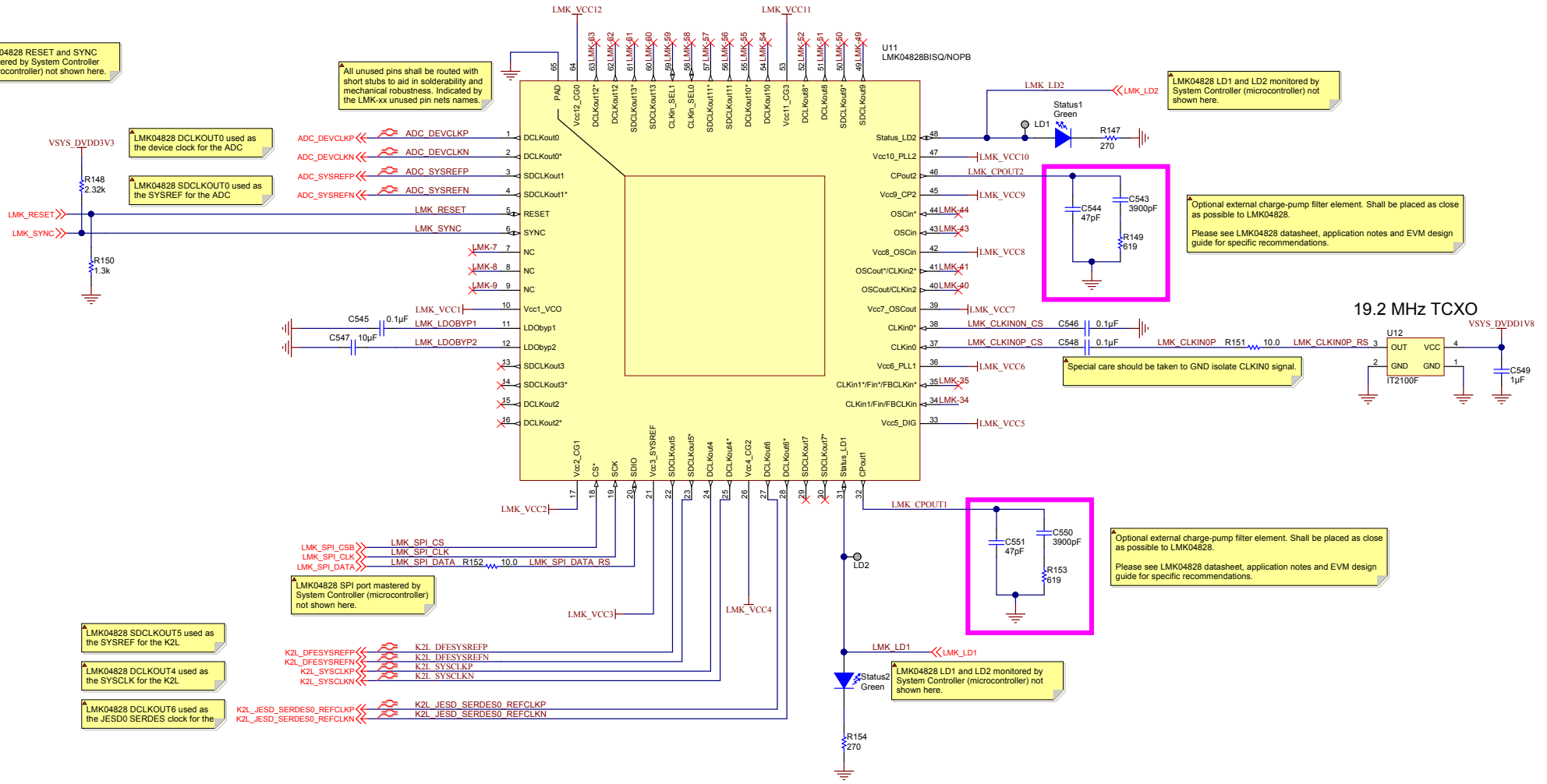

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