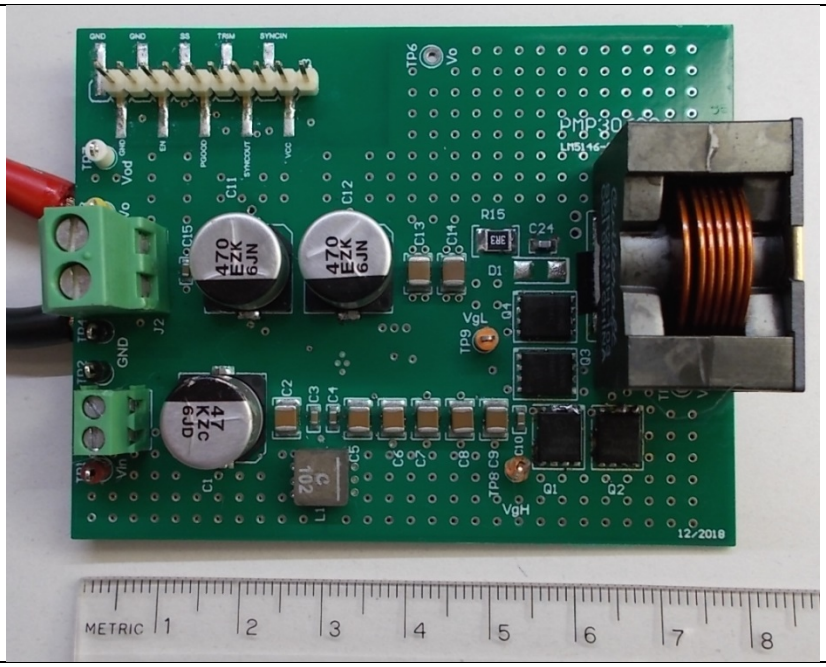
Test Report: PMP30600-TH

20-A Automotive Pre-Regulator Reference Design With Extended Input Voltage Range for Trucks

Description

This reference design is a 100 W synchronous buck converter primarily to supply automotive loads. The IC is LM5146-Q1 in fixed frequency operation at 100 kHz to ensure low noise operation. To minimize conducted emissions an input filter prevents from reflected ripple. Furthermore a RC snubber attenuates noise in the RF band to reduce radiated emissions. To reduce system EMI the design is prepared either to synchronize other converters (output) or just to be externally synchronized (input). The power stage itself withstands surge voltages up to 75Vpk.



1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Input Voltage Range	10 V to 36 V (75 V surge)
Output Voltage	5 V
Maximum Output Current	20 A
Calculated Switching Frequency	100 kHz

*1.2 Considerations**

The circuit is built on PCB PMP30600RevA.

2 Testing and Results

2.1 Efficiency Graphs

The efficiency is shown in the Figure 1 below. The input voltage was set to 28V

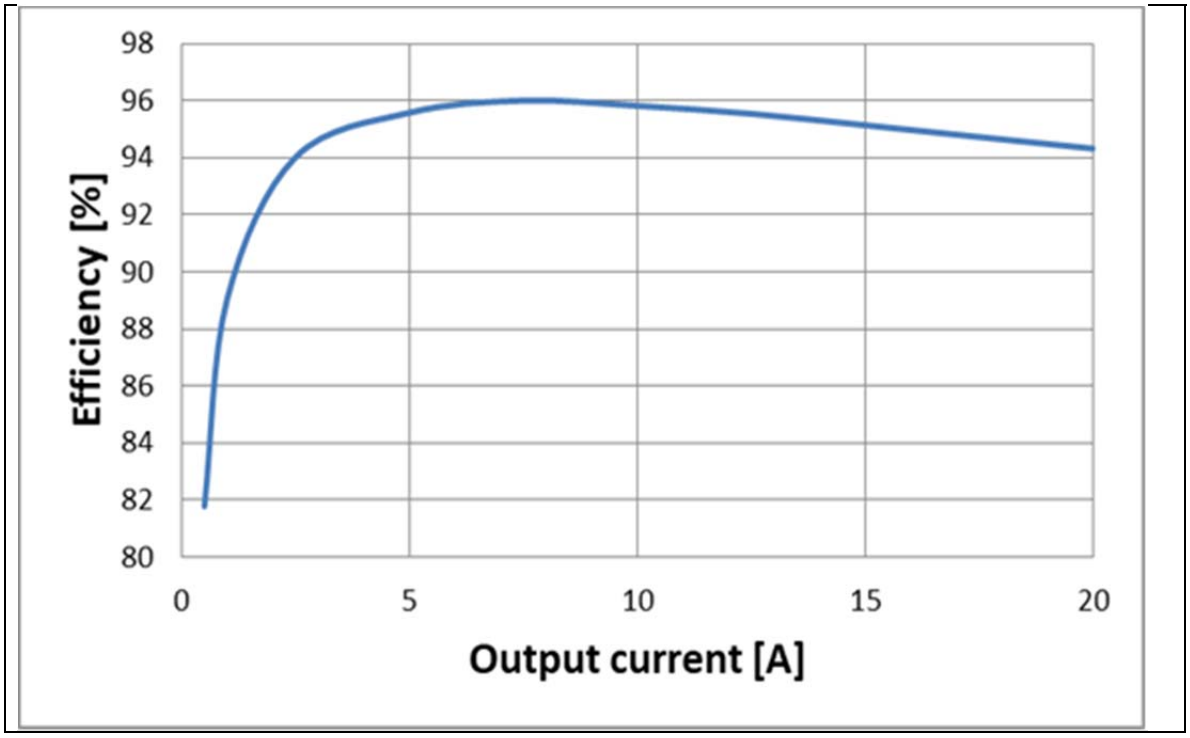
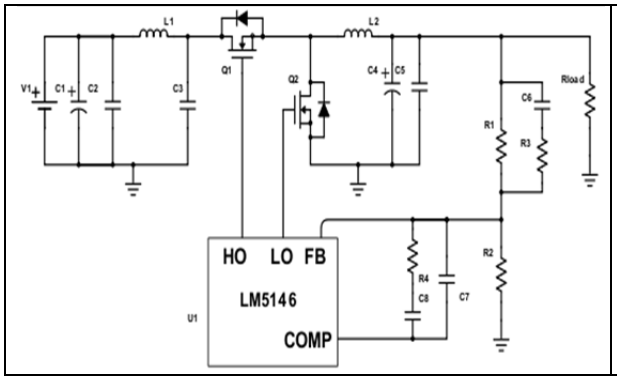


Figure 1

Full load efficiency 94.32%, calculated 94.8%;
Deviation by self heating of inductor and switching losses

Maximum efficiency 96.01% at 7.5A.

Efficiency ≥94% in a range 2.5A to 20A, so 12.5% load to 100% load



Power stage as calculated before:

Cin 5x 4.7uF/80V/X7R/1210

NFET Infineon BSC117N08NS5 (high side)
Infineon BSC061N08NS5 (low side)

Inductor 10uF/2.6mOhm/28Asat

Cout 2x 470uF/25V

2.2 Load Regulation

The load regulation of the output is shown in the Figure 2 below. The input voltage was set to 28V.

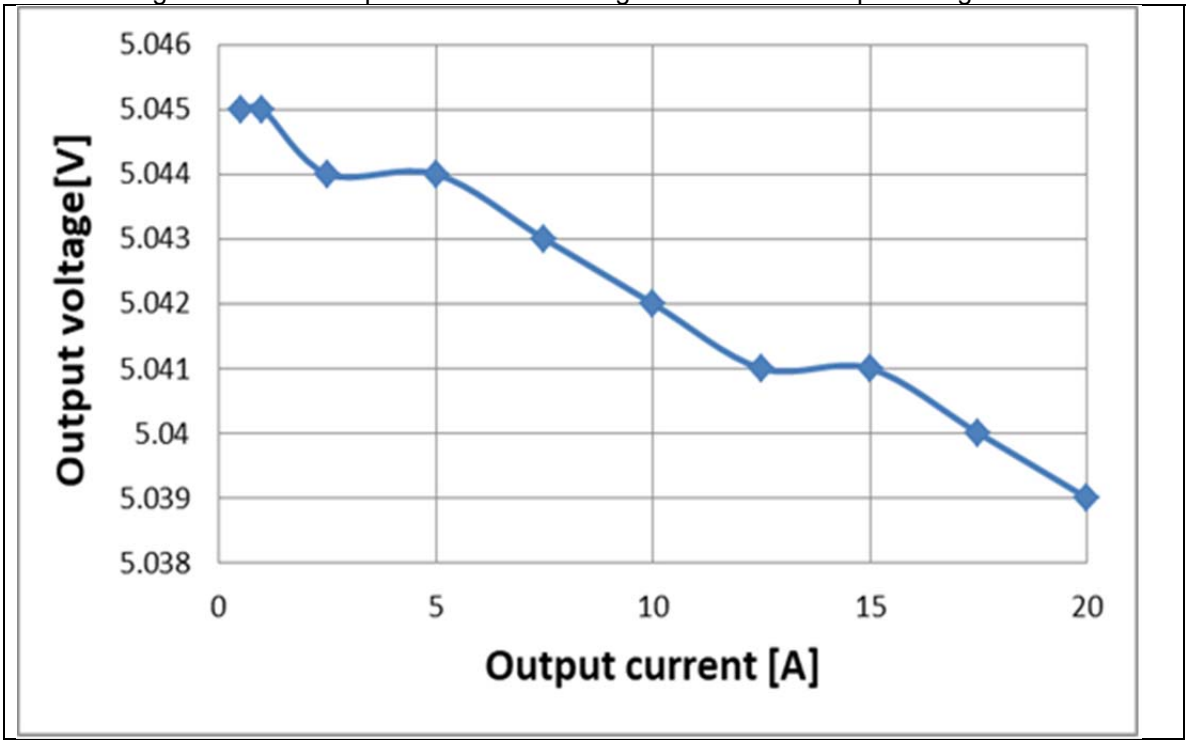


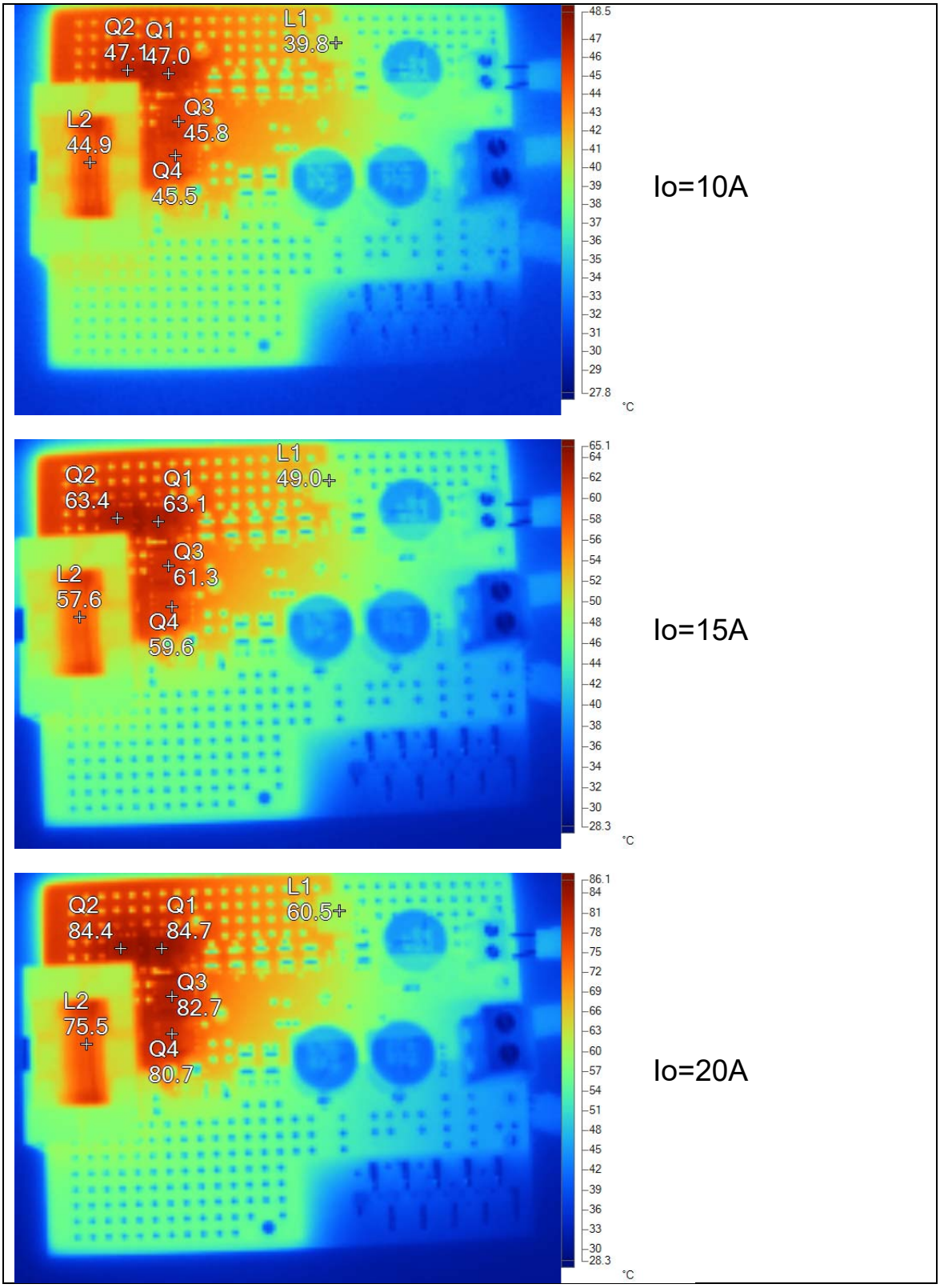
Figure 2

Min. Vout 5.039V, max Vout 5.045V,

Output voltage variation 6.0mV, so 0.12%, negligible.

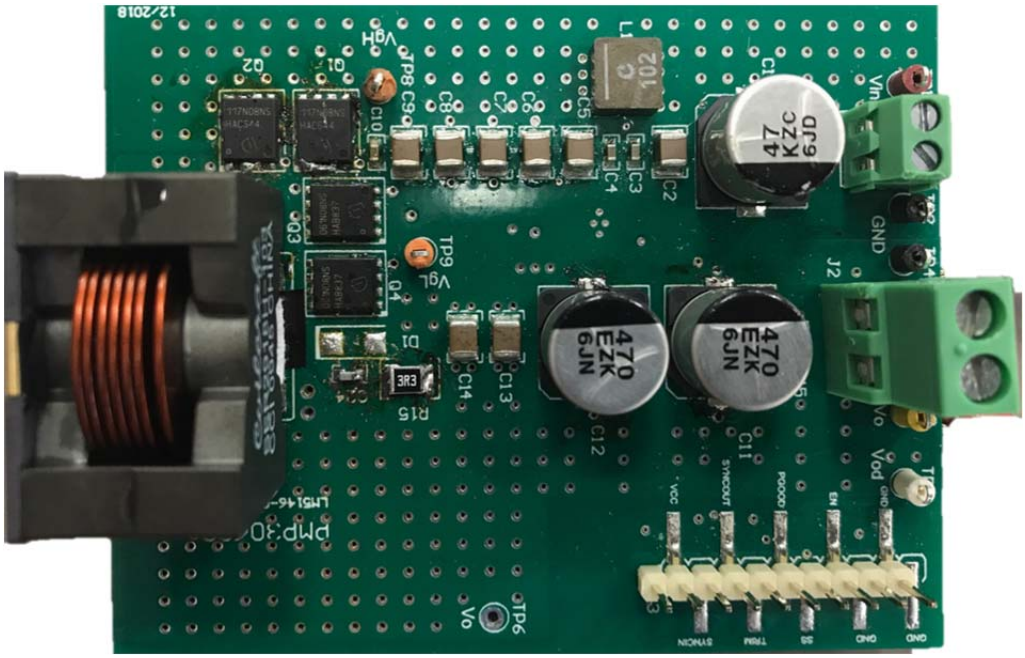
2.3 Thermal Images

Thermal image at 28V input and full load 20Amp after 30 minutes continuous operation [Rt = 25c]:



Name	Temperature		
	10A	15A	20A
Q1	47.0°C	63.1°C	84.7°C
Q2	47.1°C	63.4°C	84.4°C
Q3	45.8°C	61.3°C	82.7°C
Q4	45.5°C	59.6°C	80.7°C
L1	39.8°C	49.0°C	60.5°C
L2	44.9°C	57.6°C	75.5°C

Temperature rise is below 50K, a proper design of the power stage with maximum efficiency results in relaxed thermal stress because inductor and MOSFETs are almost same temperature; good balance.



Filter inductor and RC snubber have been placed externally

2.4 Dimensions

The extensions of the board are 79 mm x 62 mm.

3 Waveforms

3.1 Switching

3.1.1 Low Side FET

With input voltage set to 28V and 20A Iout results in the waveform shown in Figure 3

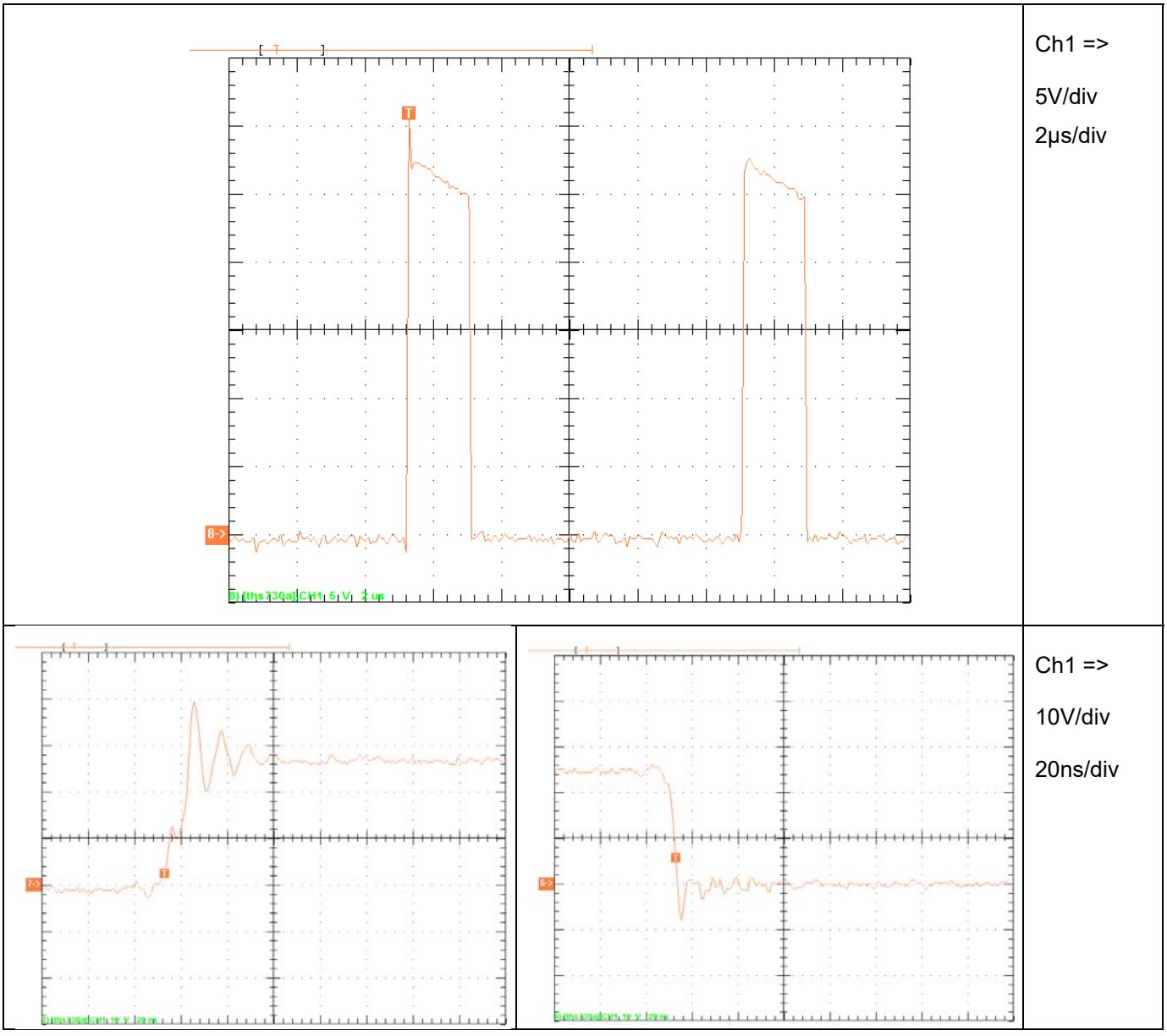
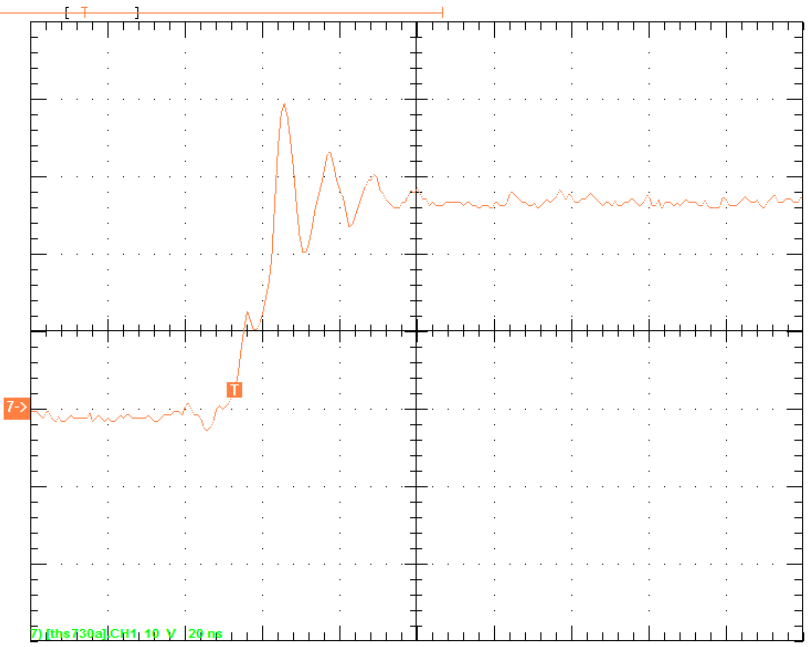


Figure 3

Maximum input voltage is 39V and the overshoot is around 11V.
Vds rating of BSC117N08NS5 and BSC061N08NS5 are 80V – enough margins.
RC snubber circuit was implemented to demonstrate RF suppression:

Measure ringing frequency at switch node w/ RF probe (no GND leads, use GND clip), here 80MHz – could cause trouble , radiated emissions:



Ch1=>

switch node

no snubber

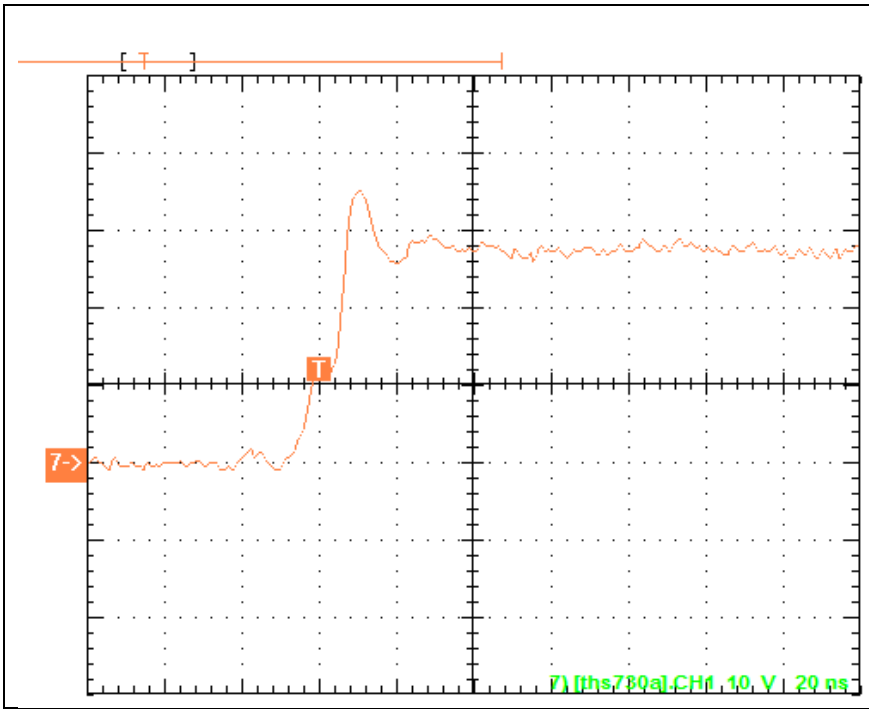
10V/div

full BW

20ns/div

1) **add capacitor from switch node to GND to achieve half of the prior frequency**, here 0.68nF

2) **add resistor in series to achieve half of the prior overshoot**, here 3.3Ω reduced overshoot from 11V to 7V:



Ch1=>

switch node

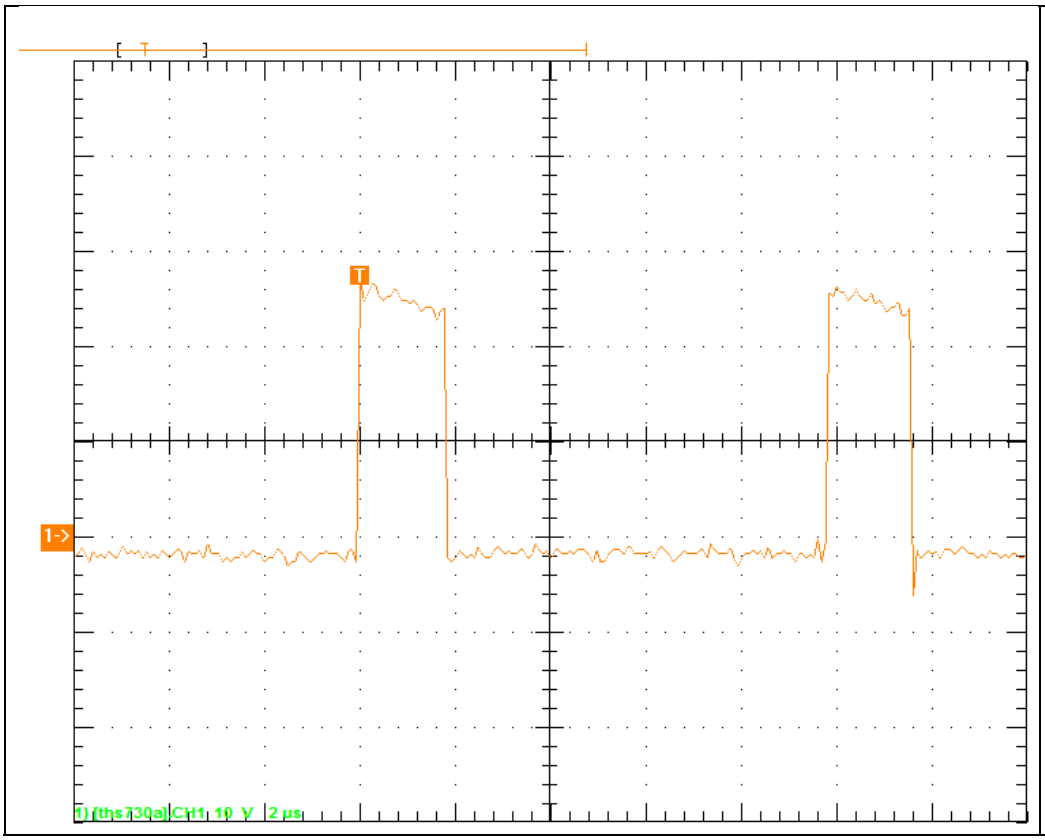
0.68nF+3.3Ω RC snubber

10V/div

full BW

20ns/div

Clamping network 0.68nF / 3.3 Ohm reduces RF content at the switch node, less EMI !



By experience could be said that a drop in efficiency from 0.2% to 0.5% is typically caused by adding the RC snubber circuit. For a middle power design like PMP30600 geometry 1206 or 1210 might fit, but for high power designs be aware of losses up to 500mW:

- 0603 <100mW
- 0805 <150mW
- 1206 <200mW
- 1210 <250mW
- 1812 <500mW
- 2010 <750mW
- 2512 <1W

3.1.2 High Side FET Source - Drain (referenced to VIN)

With input voltage set to 24V and 20A Iout results in the waveform shown in Figure 1

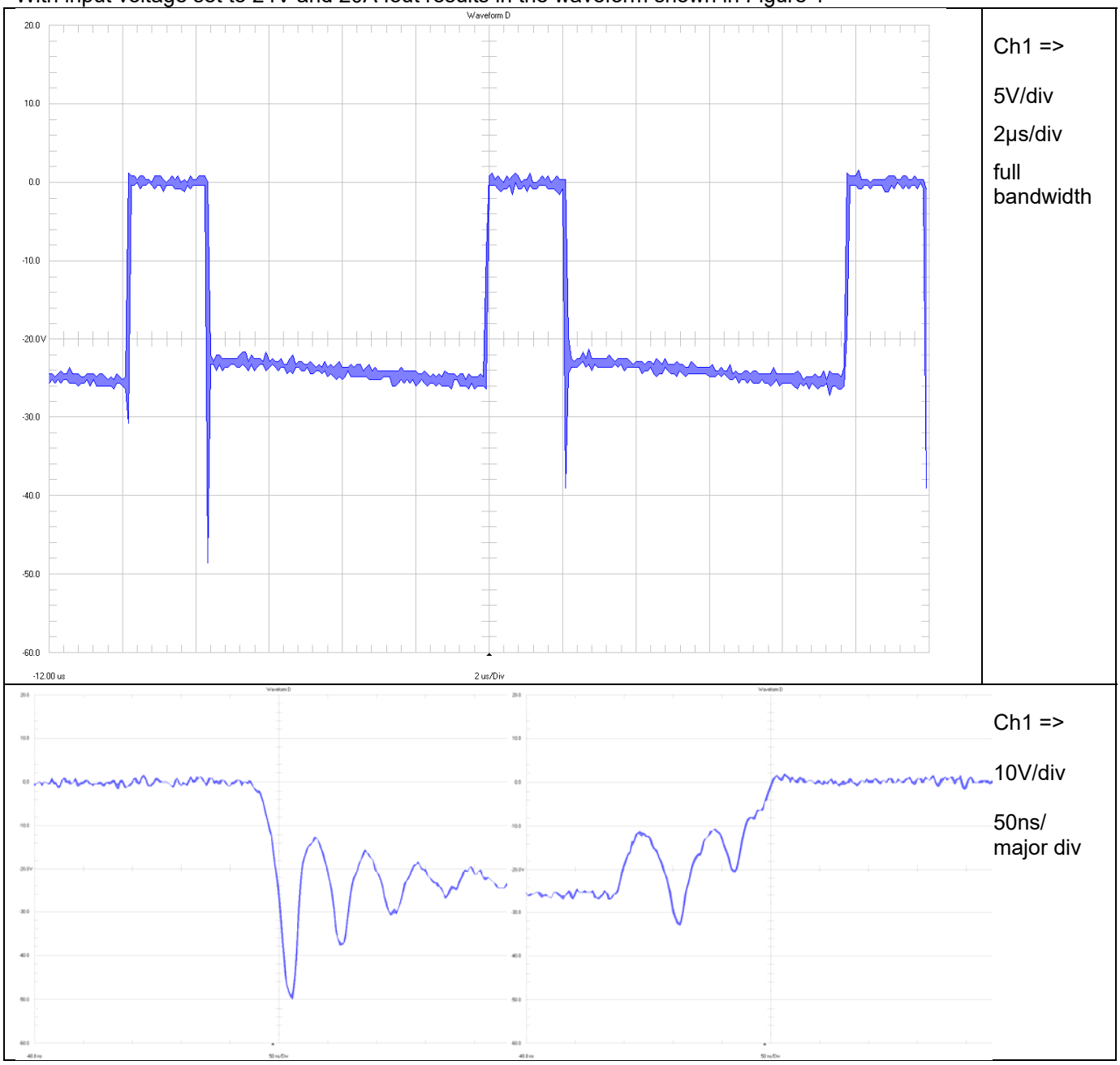


Figure 4

3.1.3 Gate to Source of MOS-FET (High-Side)

With input voltage set to 28V and 20A Iout results in the waveform shown in Figure 3.

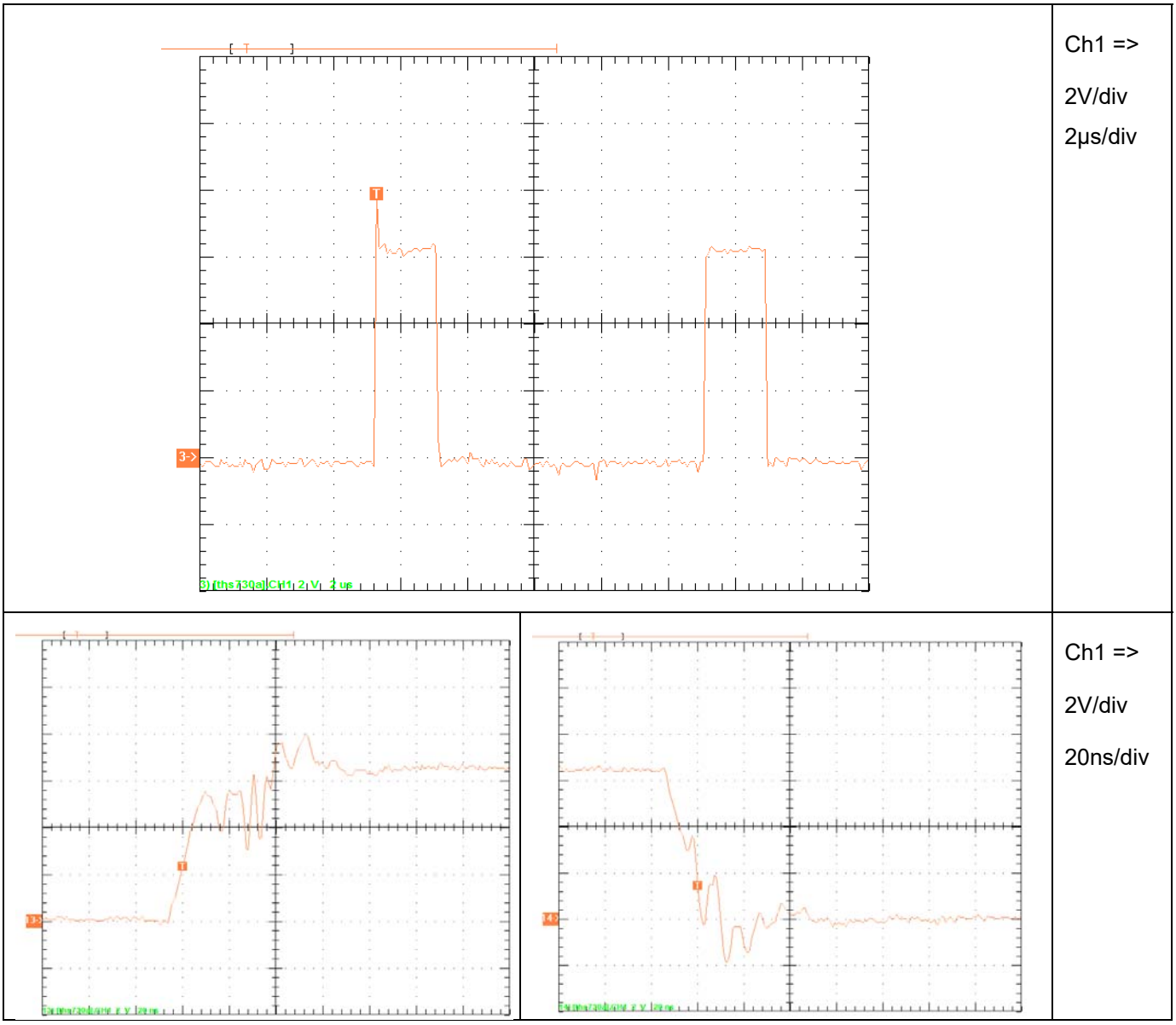


Figure 5 High side

3.1.4 Gate to Source of MOS-FET (Low-Side)

With input voltage set to 28V and 20A Iout results in the waveform shown in Figure 6.

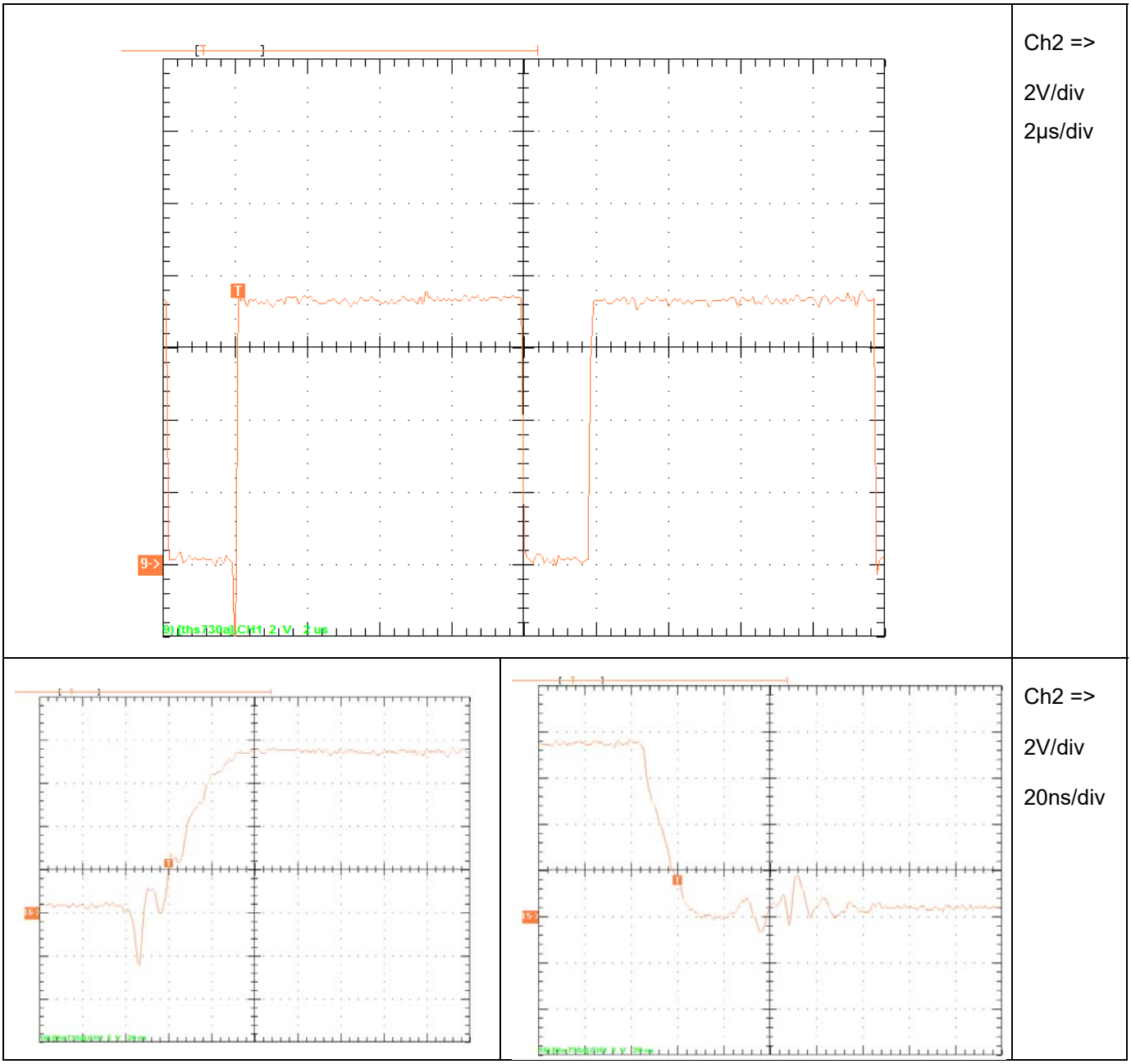
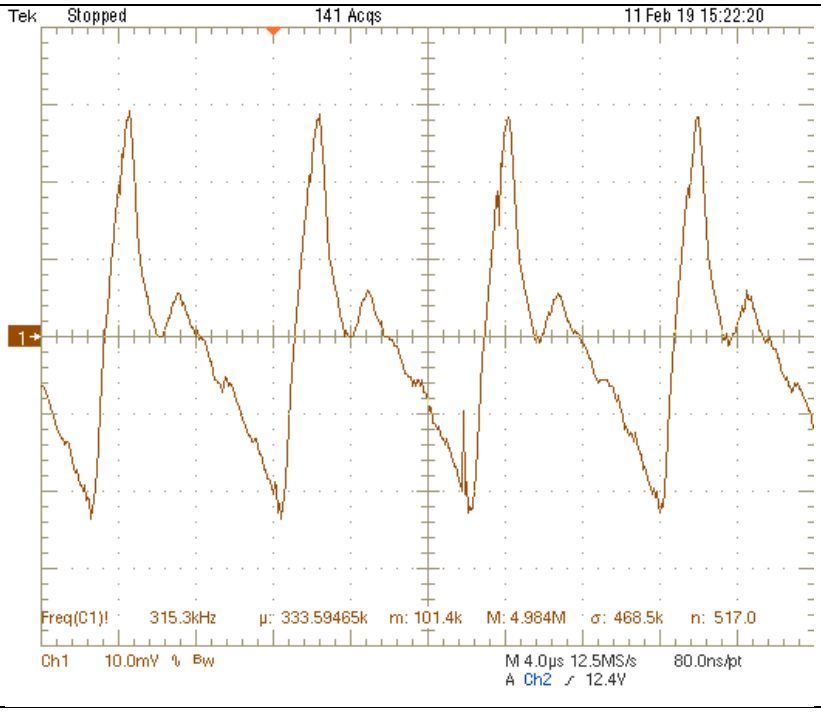


Figure 6 Low side

3.2 Output Voltage Ripple

The output ripple voltage is shown in Figure 7. The image was taken with 20A load 28V at the input. The output ripple voltage is roughly 50mV.



Ch1=> output voltage 10mV/div

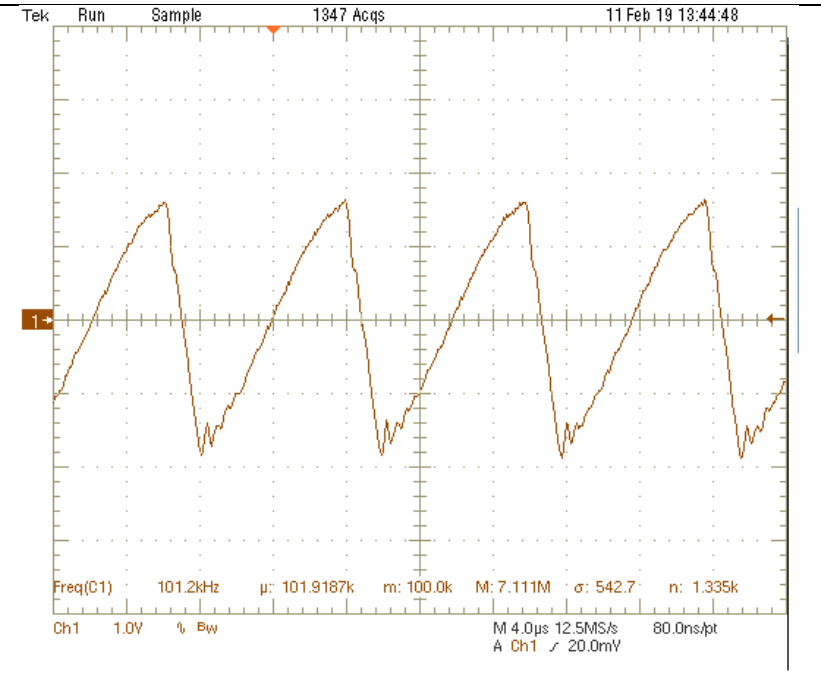
AC coupled

4μs/div

Figure 7

3.3 Input Ripple Voltage

The input ripple voltage is shown in Figure 8. This was taken with 20A full load 28V at the input.



Ch1 => Vin 1V/div

AC coupled

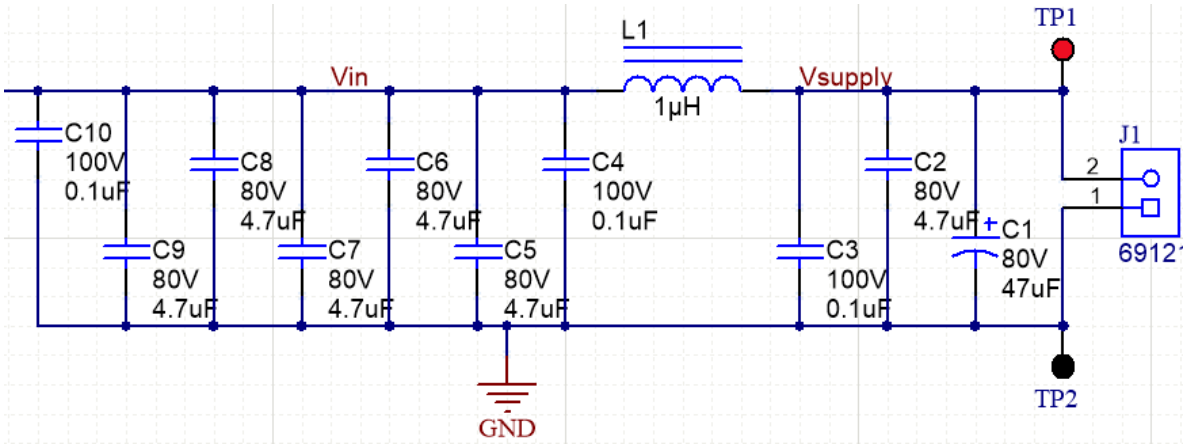
4μs/div

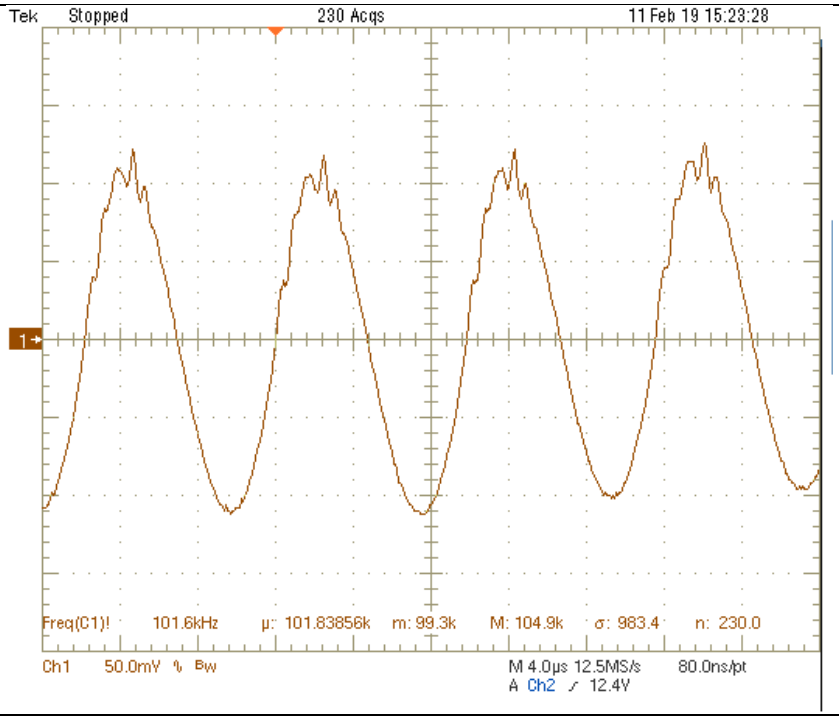
Figure 8

Input voltage ripple is around 3.5V.

Reflected ripple = conducted emissions, EMI

Finally the input voltage by using PI filter 47uF – 1uH – 5x 4.7uF;
A small ceramic capacitor 100nF was added to the electrolytic to suppress glitches:





Ch1=> Vsupply
50mV/div

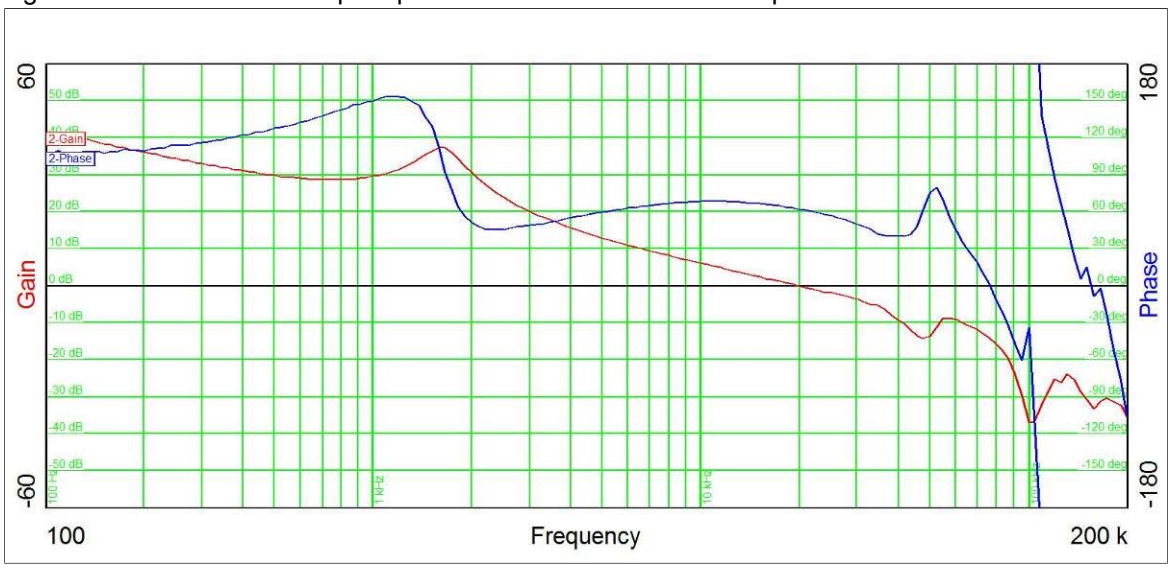
AC coupled

4µs/div

Input voltage is reduced to 200mV; reduction rate is 1/17.
A tremendous reduction of reflected ripple resulted in better EMI behavior !
The inductor prevents the source from seeing the pulse currents – less conducted emissions.

3.4 Bode Plot

Figures below shows the loop response with 20A load and 28V input – fco=20kHz



The crossover frequency 20kHz fits exactly to the first calculation by hand, the phase margin is more than 60 degrees. Slope at crossover is close to -1.

REMEMBER:

This analysis is a small signal analysis, shows the small signal behavior of the power supply.

The only true analysis is a large signal analysis, the system response on a load transient!

3.5 Load Transients

The Figure 9 shows the response to load transients. The load is switching from 10A to 20A. The input voltage was set to 28V

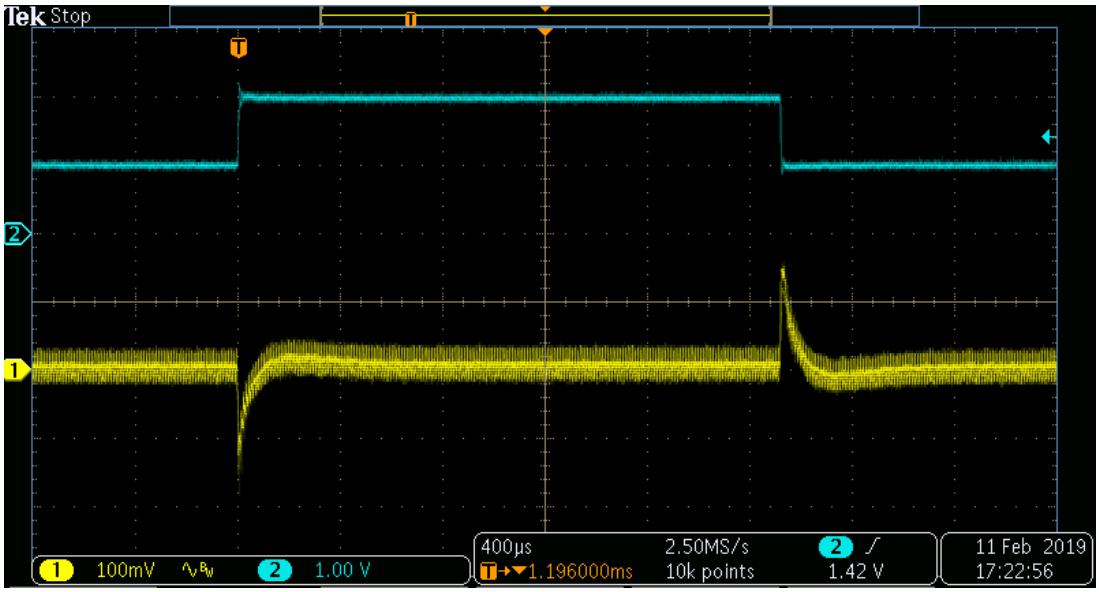


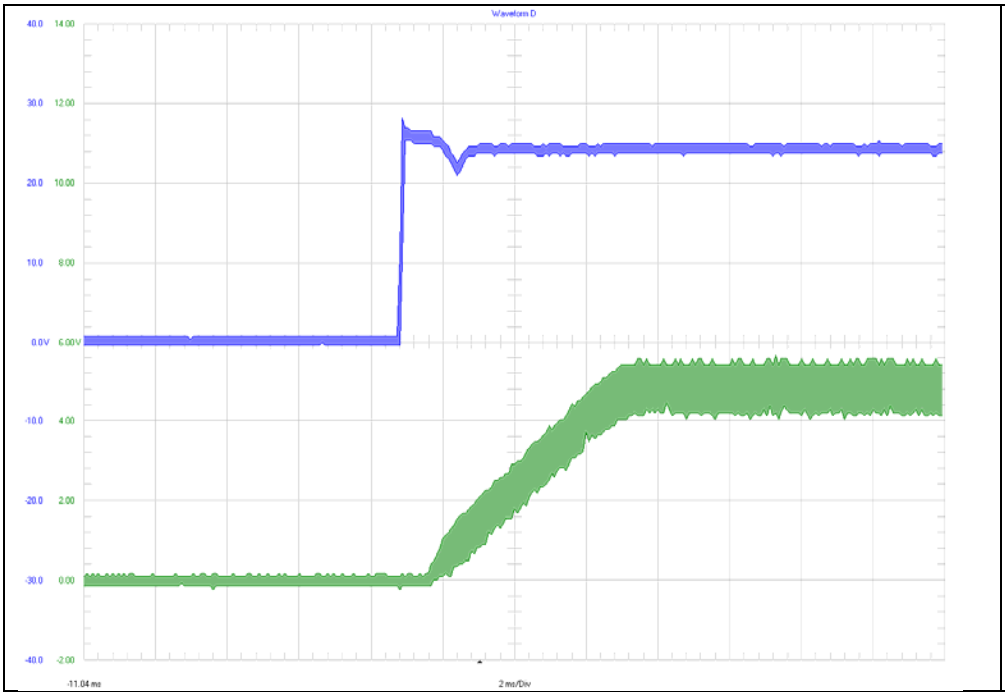
Figure 9

The voltage drop caused by 10A is around 150mV, so around 3% of the output voltage 5V;
The combination output capacitor to loop bandwidth matches.

A proper calculation of the error amplifier compensation results in a stable design. For series production a phase margin >60 degrees and a gain margin <-15dB is recommended.

3.6 Start-up Sequence

The startup waveform is shown in the Figure 10. The input voltage was set at 24 V, with 20 A load at the output. The power supply was connected.



Ch1=> input voltage
10V/div

Ch2=> output voltage
2V/div

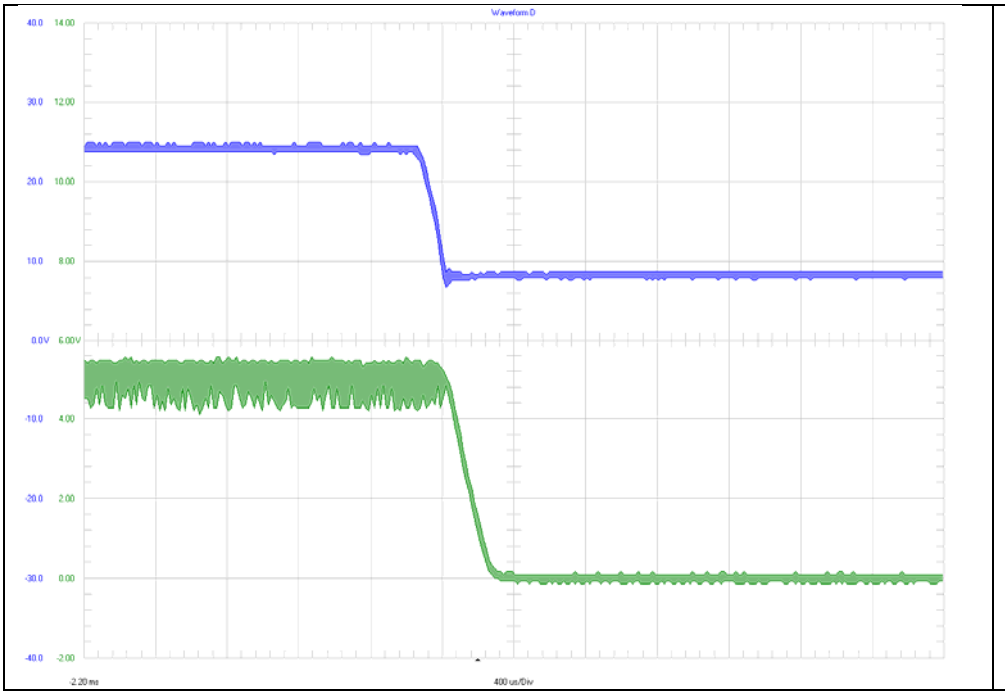
20 MHz bandwidth

2ms/div

Figure 10

3.7 Shutdown Sequence

The shutdown waveform is shown in the Figure 11. The input voltage was set at 24 V, with 20 A load at the output. The power supply was disconnected.



Ch1=> input voltage
10V/div

Ch2=> output voltage
2V/div

20 MHz bandwidth

400 µs/div

Figure 11

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