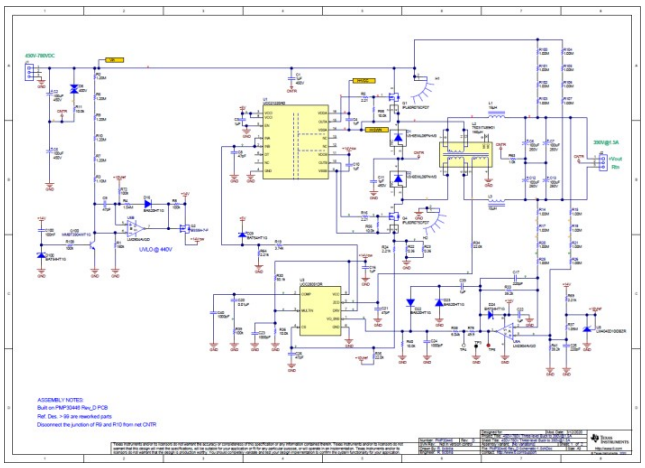
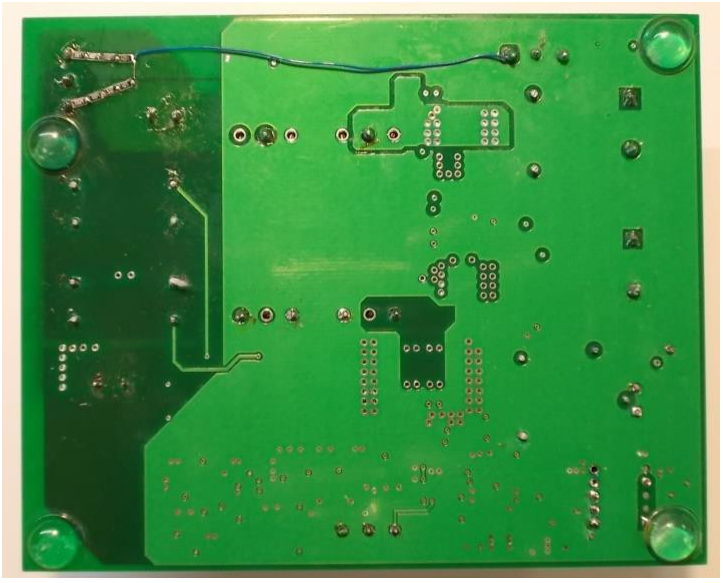
Test Report

Peak Efficiency at 99%, 585-W High-Voltage Buck Reference Design With Standard Si-MOSFETs

Description

This reference design converts a DC-input source in the range of 450 V to 780 V into non-isolated 390 V at 1.5 A. This is an alternative solution to SiC-FET and SiC-Diode Buck converter, since the actual power stage uses only standard silicon components. In order to employ 600 V rated devices, the input source has been split so that two identical buck stages share the center point. A single coupled inductor (1:1) balances automatically the center point. Two small-series inductors limit the current in each branch in case of voltage imbalance and any small variation in the gate drive delay time of the two FETs. The converter minimizes the switching loss as a result of CRM mode (critical conduction mode), achieving peak efficiency of 99% at 450 V input voltage and full load.





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1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Input Voltage	450 VDC – 780 VDC
Output, Voltage:	390 VDC
Output, Current:	1.5 A

1.2 Required Equipment

- 0…800 VDC constant voltage source (VS1)
- Floating electronic load (constant resistance) or variable load resistor
- Oscilloscope (min. 100 MHz bandwidth) with high voltage isolated probes
- HF Current probe
- Infrared camera

1.3 Testing Conditions

1. Connect the source VS1 to J1-1 and J1-3
2. Connect the load to terminals J2-1 (“+Vout”) and J2-3 (“Rtn”); please consider that the load is floating, intended to supply an isolated converter
3. Attach a current probe in series to L1 to measure the output current in one branch
4. Turn on VS1 (accepted range: 450 VDC…780 VDC). The converter will start at Vin > 460 VDC and shut down at 440 VDC
5. Increase the load on the output
6. After turn off, wait ~ 5 minutes until C2 and C5 are completely discharged (warning: HIGH VOLTAGE). If the converter is unloaded, wait also for C6, C7, C12 and C13

2 Testing and Results

2.1 Efficiency Graph and Data

2.1.1 Efficiency Graphs

The efficiency graph versus output load current is shown below. The input voltage has been set to 450 VDC, 620 VDC and 780 VDC.

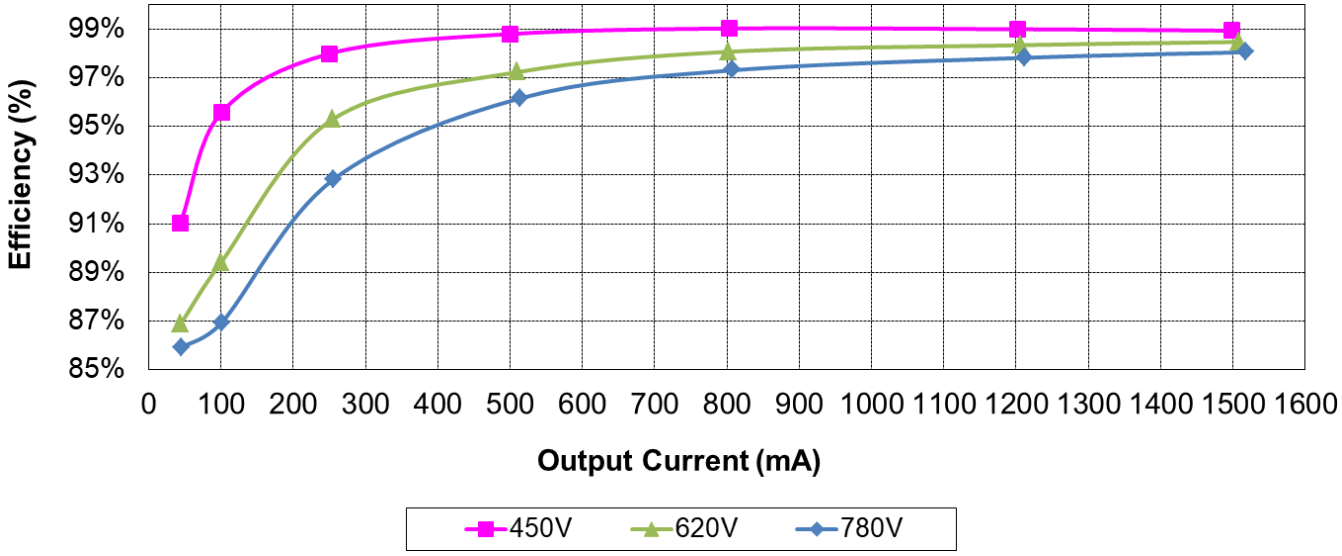

Figure 2-1.

2.1.2 Efficiency Data

The efficiency graph reports the data from the tables shown below.

Vin (V)	Iin (mA)	Pin (W)	Vout (V)	Iout (mA)	Pout (W)	Efficiency (%)
450.6	1.3	0.581	386.7	0.0	0.00	0.00%
450.0	41.5	18.675	386.4	44.0	17.00	91.04%
450.0	90.3	40.635	386.4	100.5	38.83	95.57%
450.2	219.5	98.819	386.4	250.6	96.83	97.99%
450.6	433.4	195.290	386.4	499.3	192.93	98.79%
450.6	696.1	313.663	386.4	803.8	310.59	99.02%
450.5	1041.5	469.196	386.4	1202	464.45	98.99%
451.4	1297	585.466	386.4	1499	579.21	98.93%

Vin (V)	Iin (mA)	Pin (W)	Vout (V)	Iout (mA)	Pout (W)	Efficiency (%)
620.9	1.5	0.900	389.0	0.0	0.00	0.00%
620.6	32.0	19.859	389.5	44.3	17.25	86.89%
620.3	70.1	43.483	389.5	99.8	38.87	89.40%

Vin (V)	Iin (mA)	Pin (W)	Vout (V)	Iout (mA)	Pout (W)	Efficiency (%)
620.0	167.3	103.726	389.4	253.8	98.83	95.28%
620.0	328.9	203.918	389.2	509.4	198.26	97.22%
622.1	511.9	318.453	389.3	802.2	312.30	98.07%
620.7	768.8	477.194	389.1	1206	469.25	98.34%
620.6	960.2	595.900	389.1	1508	586.76	98.47%

Vin (V)	Iin (mA)	Pin (W)	Vout (V)	Iout (mA)	Pout (W)	Efficiency (%)
780.0	1.5	1.154	391.4	0.0	0.00	0.00%
780.1	26.1	20.361	392.2	44.6	17.49	85.91%
780.1	58.2	45.402	392.3	100.6	39.47	86.92%
780.6	138.2	107.879	392.2	255.3	100.13	92.82%
780.2	268.3	209.328	392.1	513.3	201.26	96.15%
780.3	416.6	325.073	391.9	807.1	316.30	97.30%
782.0	620.3	485.075	391.8	1211	474.47	97.81%
780.5	776.9	606.370	391.9	1517	594.51	98.04%

2.2 Static Output Voltage Variation versus Load

The output voltage regulation versus load current and input voltage is shown in the graph below.

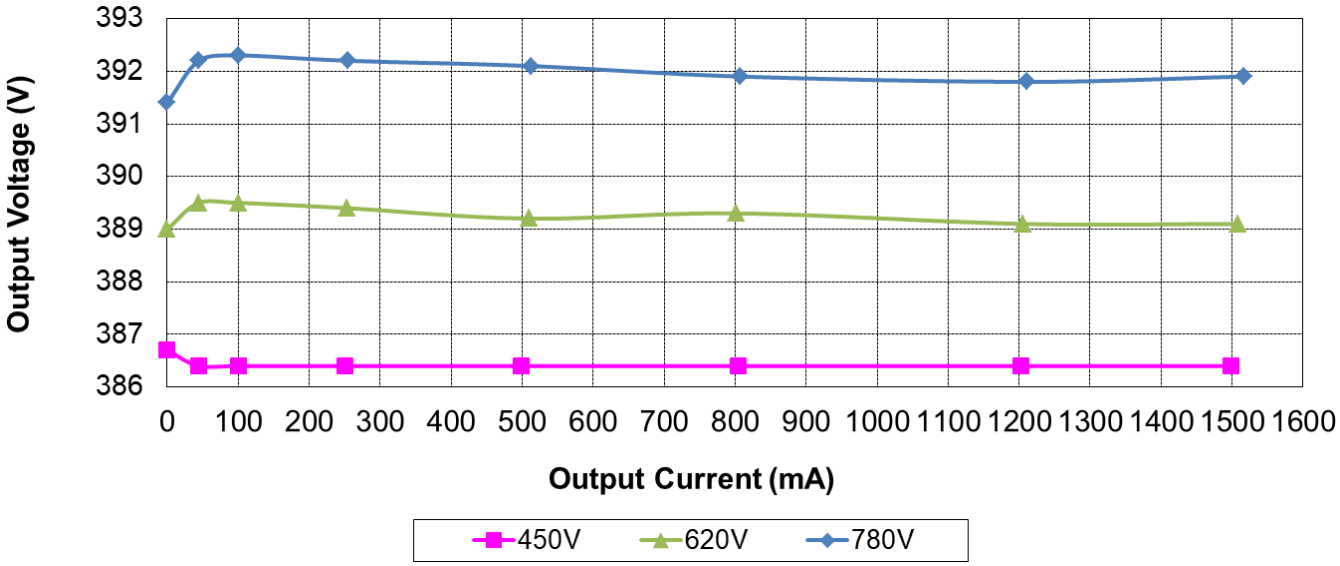

Figure 2-2.

2.3 Thermal Image

The graph and table below are referred to the thermal picture of the converter supplied at 620 VDC while fully loaded. This shot has been taken after the board was running for 1 hour at ambient temperature of 25.5°C in still air condition.

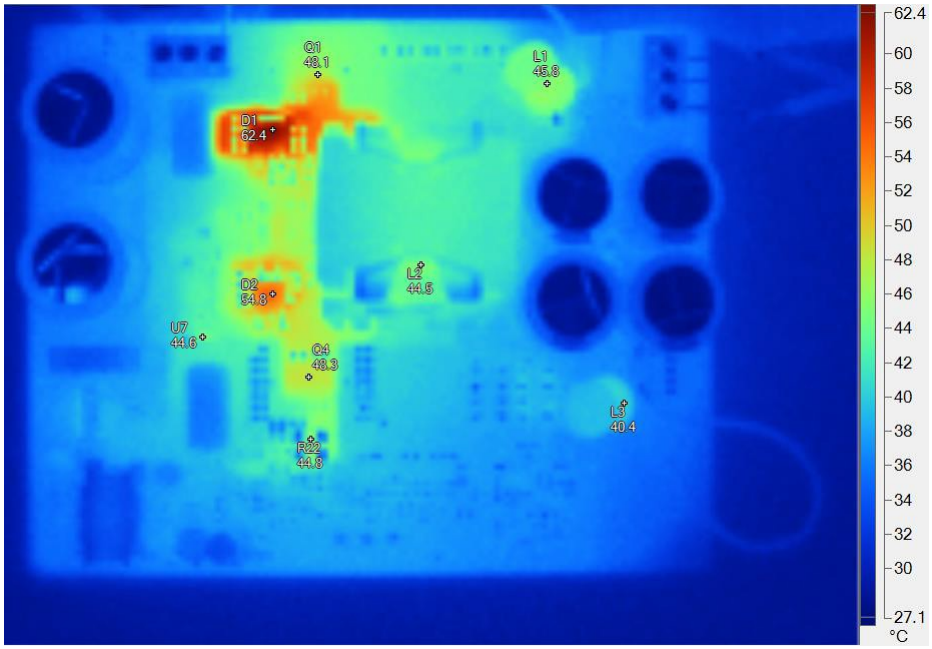

Figure 2-3. Thermal picture 620Vin FL.is2

Table 2-1. Main Image Markers

Name	Temperature	Emissivity	Background
Q1	48.1°C	0.96	25.5°C
D1	62.4°C	0.96	25.5°C
D2	54.8°C	0.96	25.5°C
Q4	48.3°C	0.96	25.5°C
R22	44.8°C	0.96	25.5°C
L2	44.5°C	0.96	25.5°C
L1	45.8°C	0.96	25.5°C
L3	40.4°C	0.96	25.5°C
U7	44.6°C	0.96	25.5°C

2.4 Dimensions

The board dimensions are 135.4 mm x 108 mm, height 39.5 mm

3 Waveforms

3.1 Switching Waveforms on Q1, Q4 and I(L1) at Full Load

The switching waveforms have been measured by supplying the converter between 440 VDC, 780 VDC and full load. Both switch-node waveforms have been superimposed showing there is no unbalance.

At Vin(UVLO) = 440 VDC, the minimum switching frequency was 17.01514 KHz.

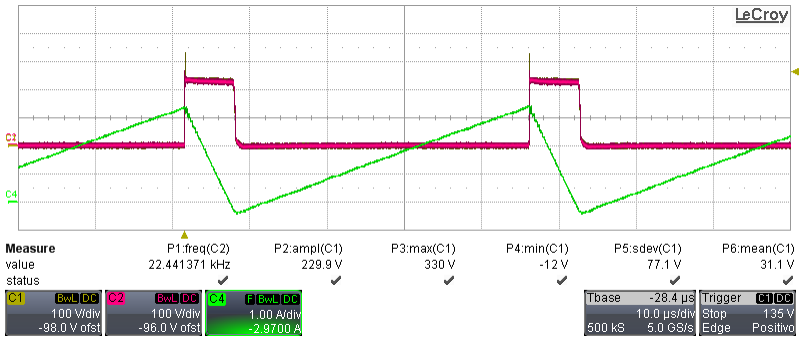

Figure 3-1. C1: Q1-Vds (100 V/div, 10 usec/div, 100 MHz BWL), C2: Q4-Vds (100 V/div, 100 MHz BWL) C4: I(L1) (1 A/div, 100 MHz BWL), Vin = 450 VDC

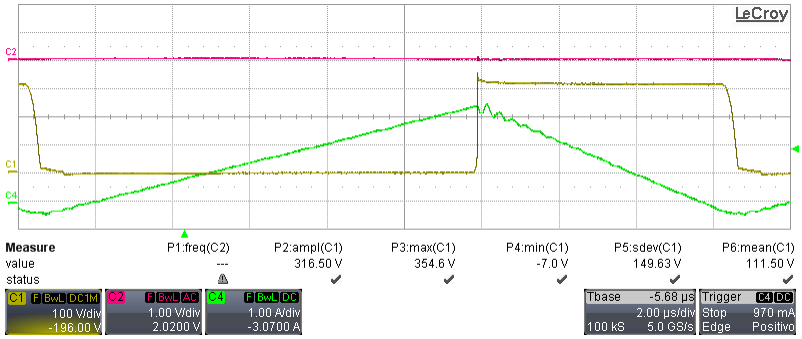

Figure 3-2. C1: Q1-Vds (100 V/div, 2 usec/div, 100 MHz BWL), C2: Vout (1 V/div, AC Coupling, 20 MHz BWL) C4: I(L1) (1 A/div, 100 MHz BWL), Vin = 620 VDC

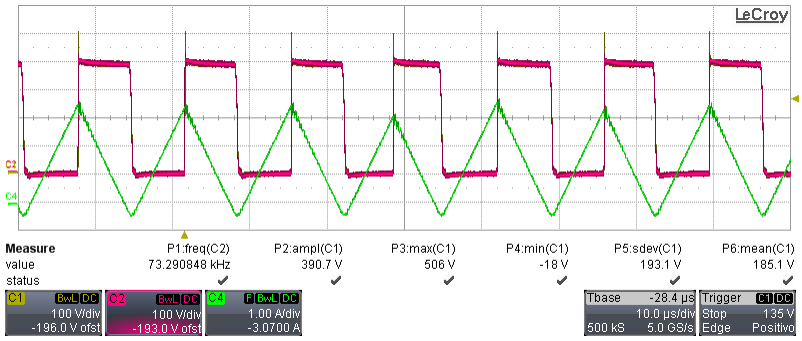

Figure 3-3. C1: Q1-Vds (100 V/div, 10 usec/div, 100 MHz BWL), C2: Q4-Vds (100 V/div, 100 MHz BWL) C4: I(L1) (1 A/div, 100 MHz BWL) , Vin = 780 VDC

3.2 Output Voltage Ripple

The output voltage ripple has been measured by supplying the converter at 620 VDC and full load.

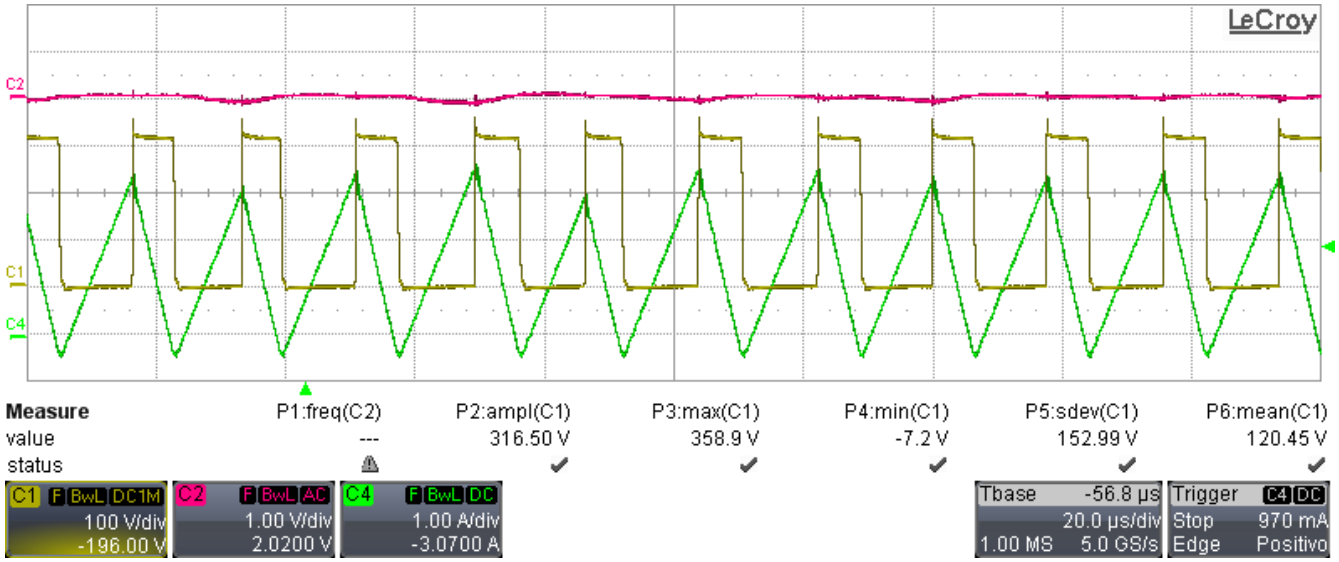

Figure 3-4. C1: Q1-Vds (100 V/div, 20 usec/div, 100 MHz BWL), C2: Output voltage (1 V/div, AC coupling, 20 MHz BWL) C4: I(L1) (1 A/div, 100 MHz BWL)

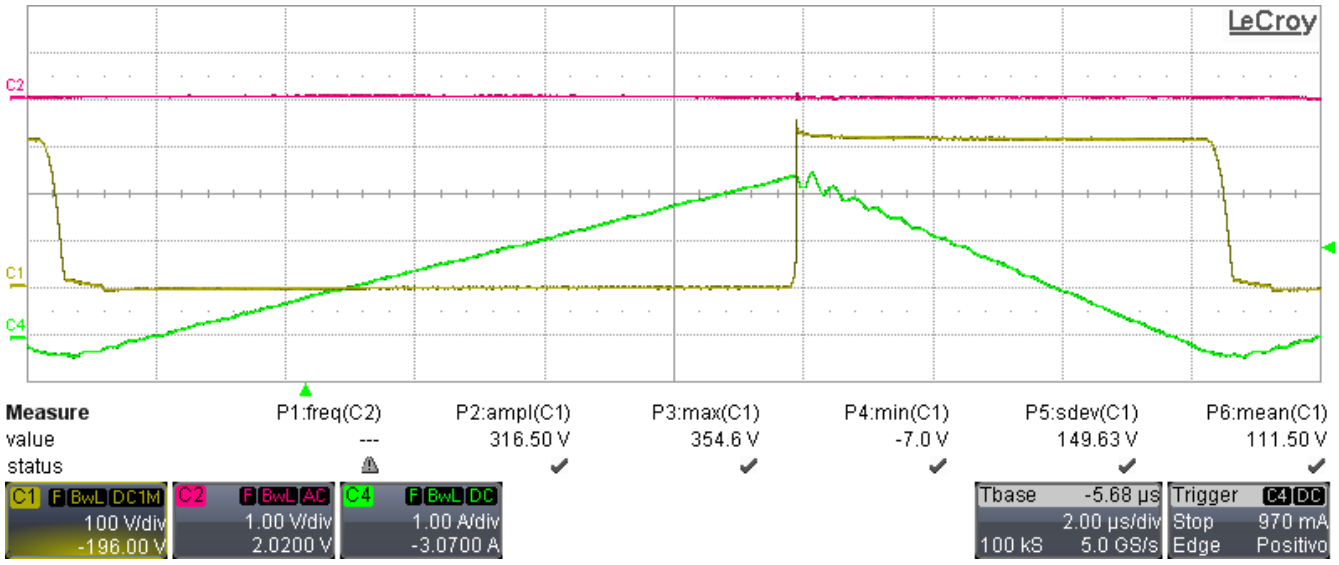

Figure 3-5. Same waveform but smaller time division (2us/div)

3.3 Load Transients

The output voltage variation, during load transients, has been measured by supplying the converter at 450 VDC and 620 VDC, while the load current has been switched between 0.5 A (33.3%) and 1.5 A (100%).

For all waveforms the bandwidth limit of the oscilloscope has been set to 20 MHz.

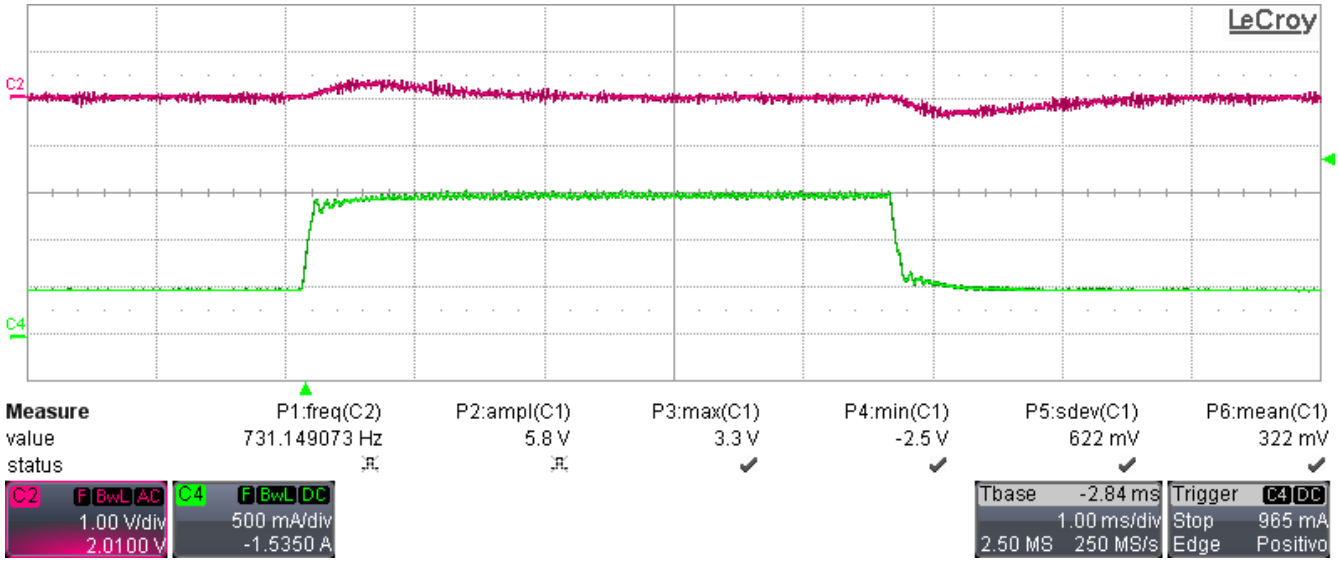

Figure 3-6. C1: Output voltage (1 V/div, 1 msec/div, AC coupling) C4: Output current (500 mA/div, DC coupling) Vin = 450 VDC

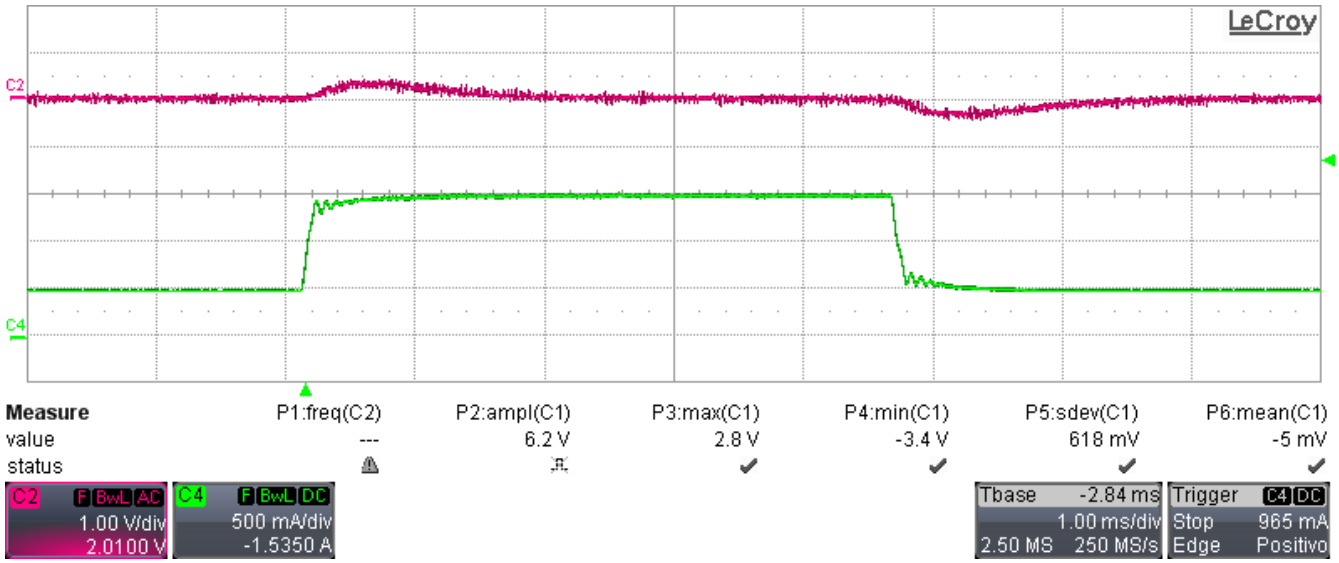

Figure 3-7. C1: Output voltage (1 V/div, 1 msec/div, AC coupling) C4: Output current (500 mA/div, DC coupling) Vin = 620 VDC

3.4 Startup

The screenshots below show the current through the inductor L1 and the output voltage of the converter during startup, respectively fully loaded and with zero current. The input voltage has been set to 620 VDC.

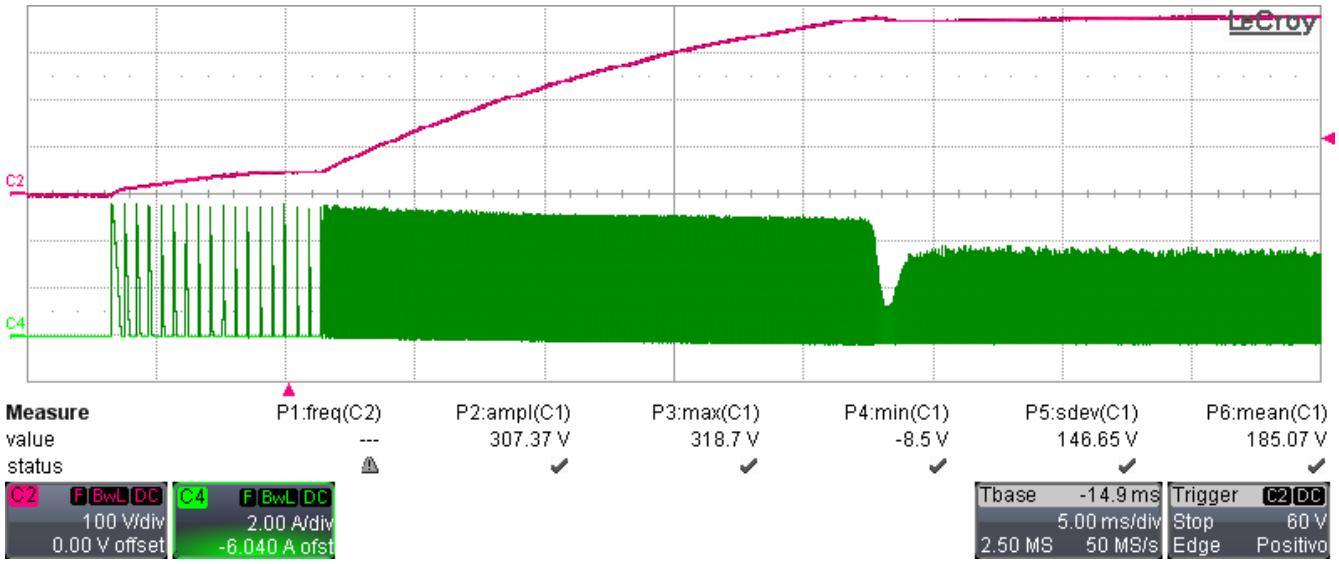

Figure 3-8. C2: Output voltage (100 V/div, 5 msec/div, 20 MHz BWL) C4: I(L1) (2 A/div, 100 MHz BWL) Output current = 1.5 A

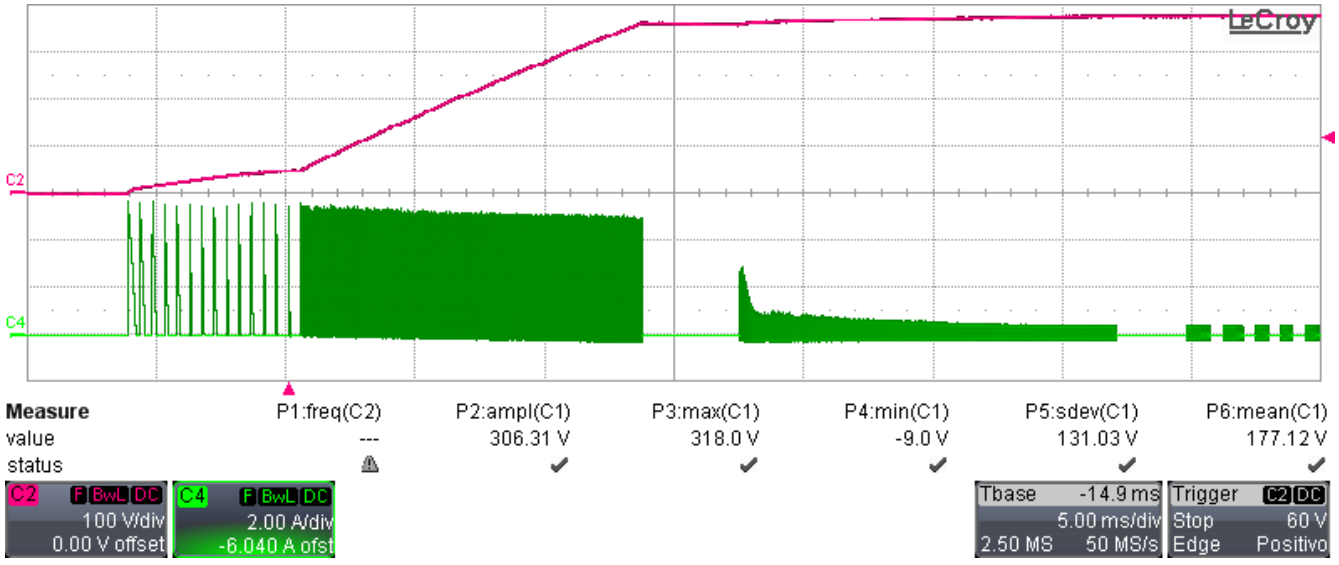

Figure 3-9. C2: Output voltage (100 V/div, 5 msec/div, 20 MHz BWL) C4: I(L1) (2 A/div, 100 MHz BWL) Output current = 0 A

4 Isolated gate driver

The UCC2122x family is a dual-channel 3kVrms basic and functional isolated gate driver in narrow-body D

(SOIC-16) package. These devices are designed to drive power MOSFET and GaN transistors with fast switching performance and high noise immunity. High gate drive strength enables better efficiency and higher power density in power systems.

Device Options	UVLO	Peak Current	Features	Isolation
UCC21220D	8V	4A/6A	Disable	Basic and Functional
UCC21220AD	5V	4A/6A	Disable	Basic and Functional
UCC21222D	8V	4A/6A	Disable, Deadtime	Basic and Functional

The UCC2154x family are dual-channel 5.7kVrms reinforced isolated gate drivers in wide-body SOIC-16 (DW) and SOIC-14 (DWK) packages. The DW package stands as a drop-in replacement for existing sockets and provides enhanced performance. The DWK package facilitates higher bus voltage applications with 3.3mm Ch-to- Ch spacing.

Device Options	UVLO	Peak Current	Max Ch-Ch Voltage	Isolation
UCC21540DW	8V	4A/6A	1500V	Reinforced
UCC21540DWK	8V	4A/6A	1850V	Reinforced
UCC21541DW	8V	1.5A/2.5A	1500V	Reinforced

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