Test Report: PMP30951

Isolated 10-W PSR DCM Flyback Reference Design

Description

This design introduces a tiny isolated auxiliary power supply used to supply automotive IGBT drive. The three isolated outputs support three gate controls, each output delivers +15 V and –5 V. An additional +10-V output is provided on the primary side. To simplify transformer windings, a virtual ground by ZENER diodes is implemented on the secondary side and well suited for symmetrical loading.

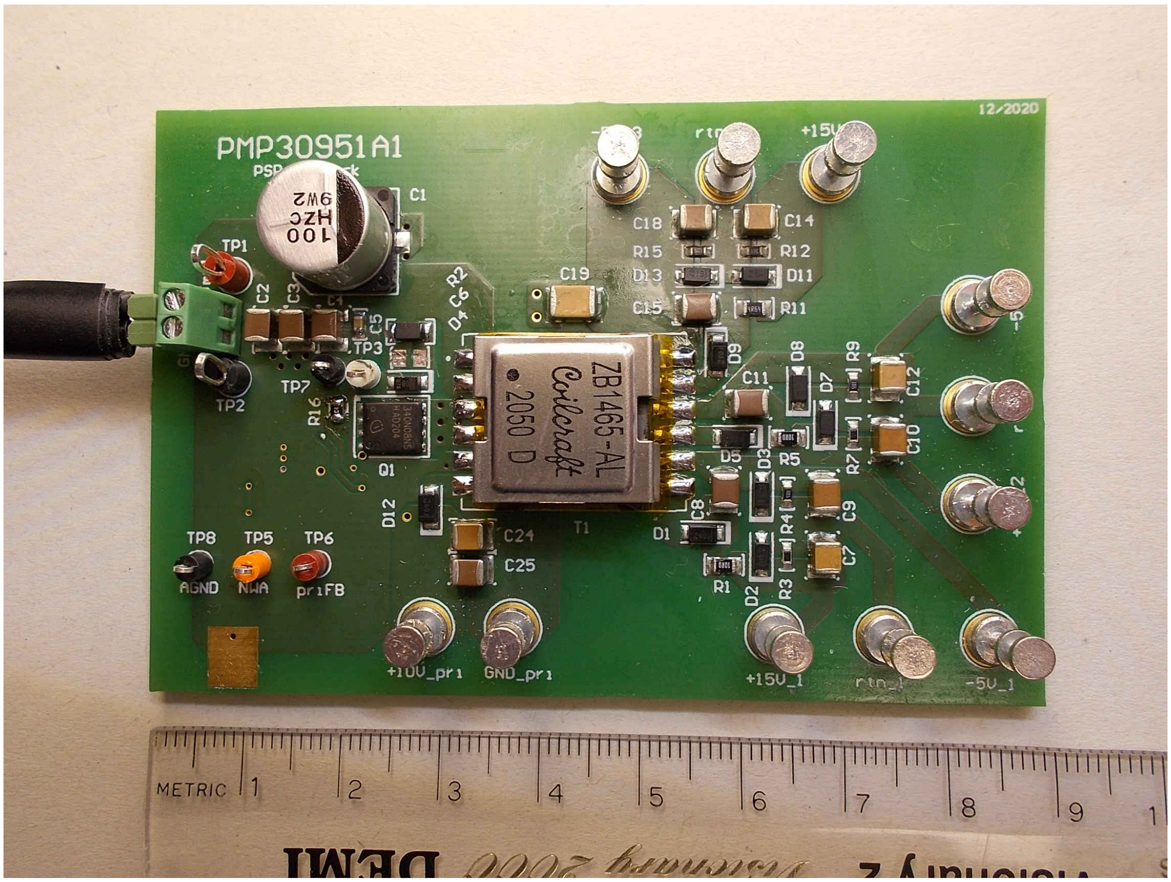
The flyback converter itself supports input voltage cranking as low as 5 V_{min} and load dump up to 42 V_{max}.

Features

- Simple transformer due to virtual ground by ZENER dividers
- Primary side regulation avoids optoisolator
- Three isolated HV outputs plus single LV output, 3-kV isolation voltage
- Wide input voltage range supports cranking to 5 V and load dump 42 V

Applications

- Traction inverter-high voltage



Top Photo

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input Voltage Range	8 V to 16 V typical (5 V_{min}, 42 V_{max})
Primary (Non-Isolated) Output Voltage	+10 V at 0.2 A_{max}
Secondary Positive Output Channel 1 and 2	+15 V at 0.075 A_{max}
Secondary Negative Output Channel 1 and 2	–5 V at 0.075 A_{max}
Secondary Positive Output Channel 3	+15 V at 0.15 A_{max}
Secondary Negative Output Channel 3	–5 V at 0.15 A_{max}
Switching Frequency	200 kHz

1.2 Considerations

Keep the following considerations in mind while working with this design:

- Unless otherwise indicated, input voltage was set to 12 V
- Resistors were used as load
- Output currents were set to full load
- Cut the PCG trace to insert diode D101
- Measured switching frequency ⇒ 200 kHz
- Undervoltage lockout ON ⇒ 7 V
- Undervoltage lockout OFF ⇒ 5 V

1.3 Dimensions

The dimensions of the PCB are 88 mm × 58 mm.

2 Testing and Results

2.1 Efficiency Graphs

The following graph shows efficiency and loss versus percentage of load.

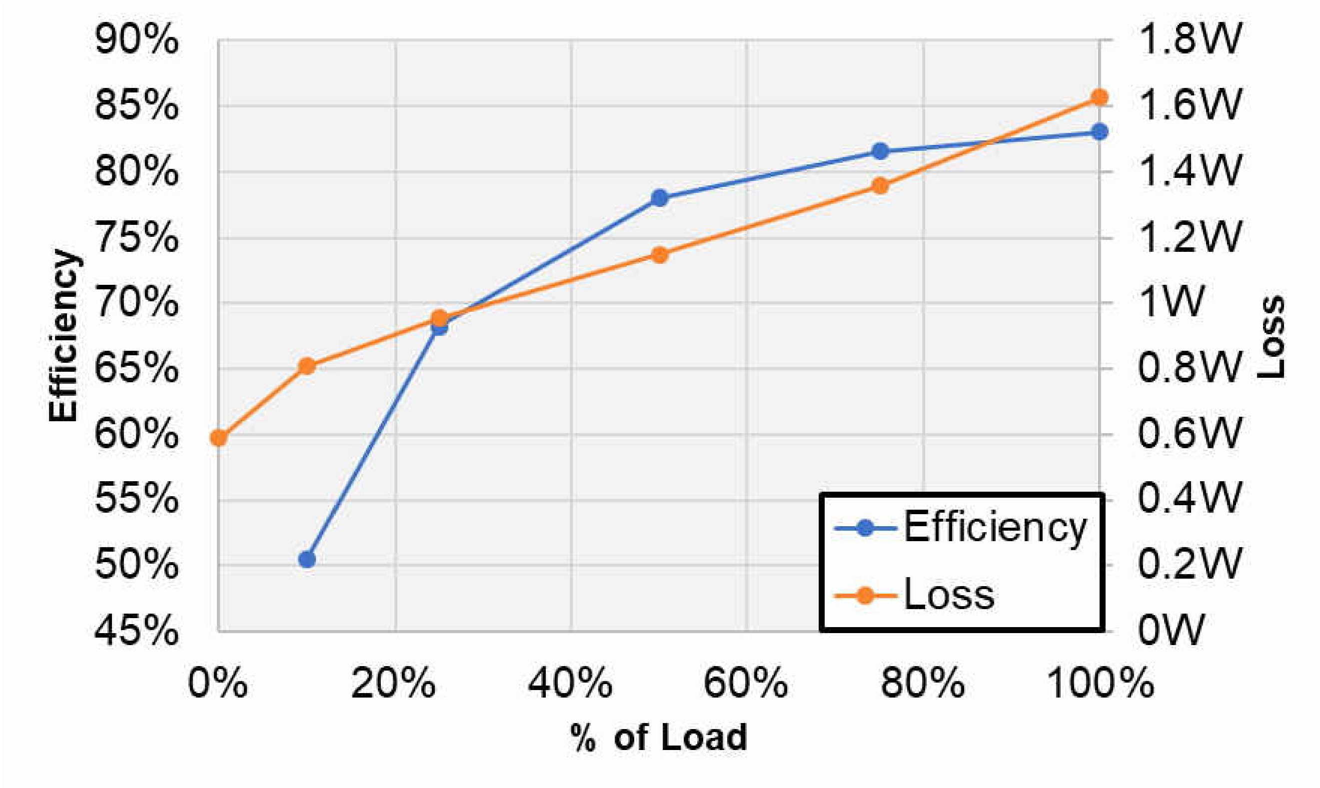


Figure 2-1. Efficiency Graph

2.2 Efficiency Data

Efficiency data for special cases (cross regulation) is shown in the following table.

Table 2-1. Efficiency Data for Special Cases (Cross Regulation)

	Case A	Case B
V_{IN}	12.004	12.018
I_{IN}	0.5626	0.456
V_{OP}	10.122	10.1224
I_{OP}	0.2007	0.2007
U_{Os1}+	15.14	15.16
I_{Os1}+	0.0751	0.0752
U_{Os1}–	4.841	4.847
I_{Os1}–	0.0733	0.0732
U_{Os2}+	15.14	15.75
I_{Os2}+	0.0756	0.008
U_{Os2}–	4.86	5.06
I_{Os2}–	0.0726	0.0076
U_{Os3}+	15.74	15.76
I_{Os3}+	0.0152	0.0152
U_{Os3}–	5.061	5.065
I_{Os3}–	0.0146	0.0147
$P_{IN} = U_{IN} \times I_{IN}$	6.753	5.480
$P_{op} = V_{OP} \times I_{OP}$	2.031	2.032
POs1+ = (U_{OS1}+) × (I_{OS1}+)	1.137	1.140
POs1– = (U_{OS1}–) × (I_{OS1}–)	0.355	0.355
POs2+= (U_{OS2}+) × (I_{OS2}+)	1.145	0.126
POs2– = (U_{OS2}–) × (I_{OS2}–)	0.353	0.038
POs3+ = (U_{OS3}+) × (I_{OS3}+)	0.239	0.240
POs3– = (U_{OS2}–) × (I_{OS2}-)	0.074	0.074
P_O= POP + (PO_{S1}+) + (PO_{S1}–) + (PO_{S2}+) + (PO_{S2}–) + (PO_{S3}+) + (PO_{S3}–)	5.334	4.005
Eff = P_O / P_{IN}	0.790	0.731
Loss = P_{IN} – P_O	1.420	1.475

Case A ⇒ Primary, Secondary 1 and 2 ⇒ full load; Secondary 3 ⇒ 10%

Case B ⇒ Primary, Secondary 1 ⇒ full load; Secondary 2 and 3 ⇒ 10%

Positive voltage 15 V varies in between 15.14 V to 15.76 V

Negative voltage –5 V varies in between –4.86 V to –5.07 V

2.3 Load Regulation

2.3.1 Primary Output

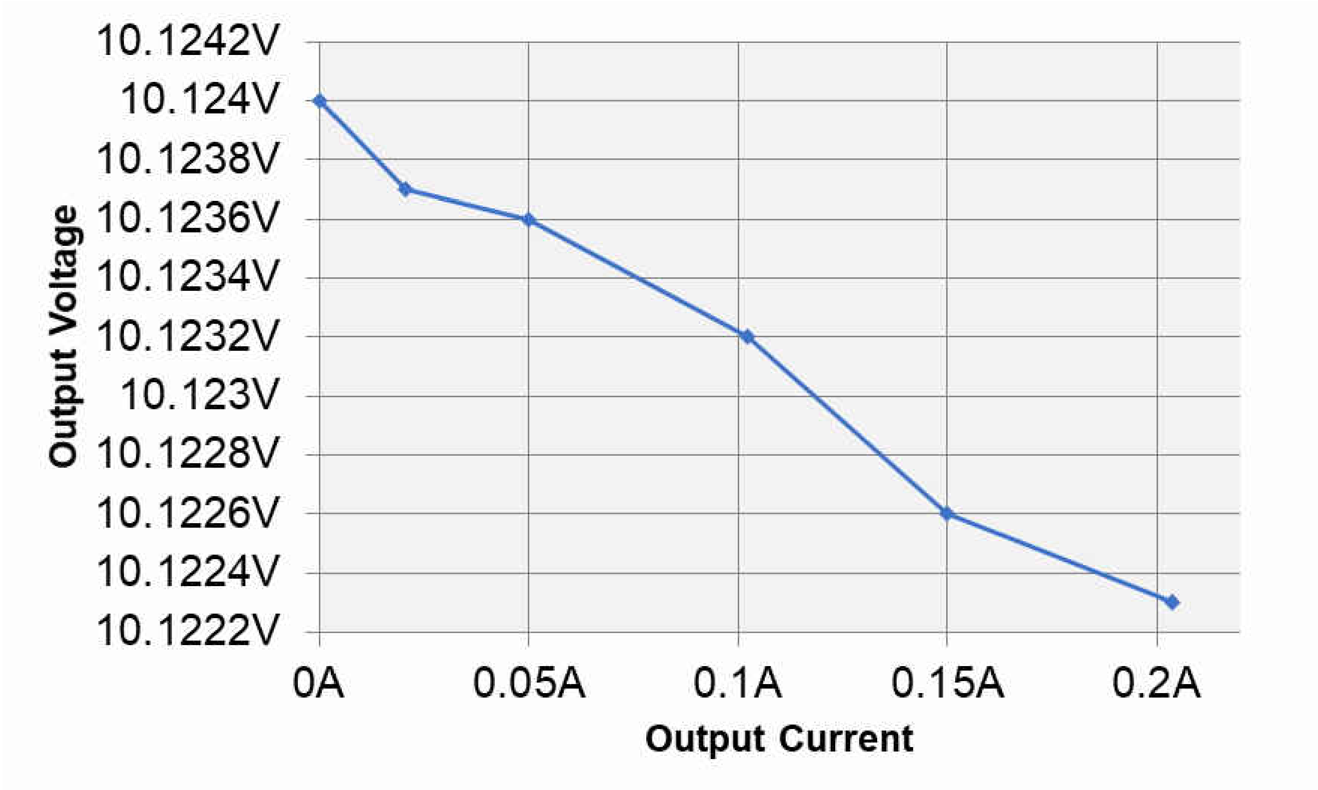


Figure 2-2. Output Voltage vs Output Current (Primary Output)

2.3.2 Secondary Outputs

The following images show the load regulation of the secondary outputs.

2.3.2.1 Positive Outputs

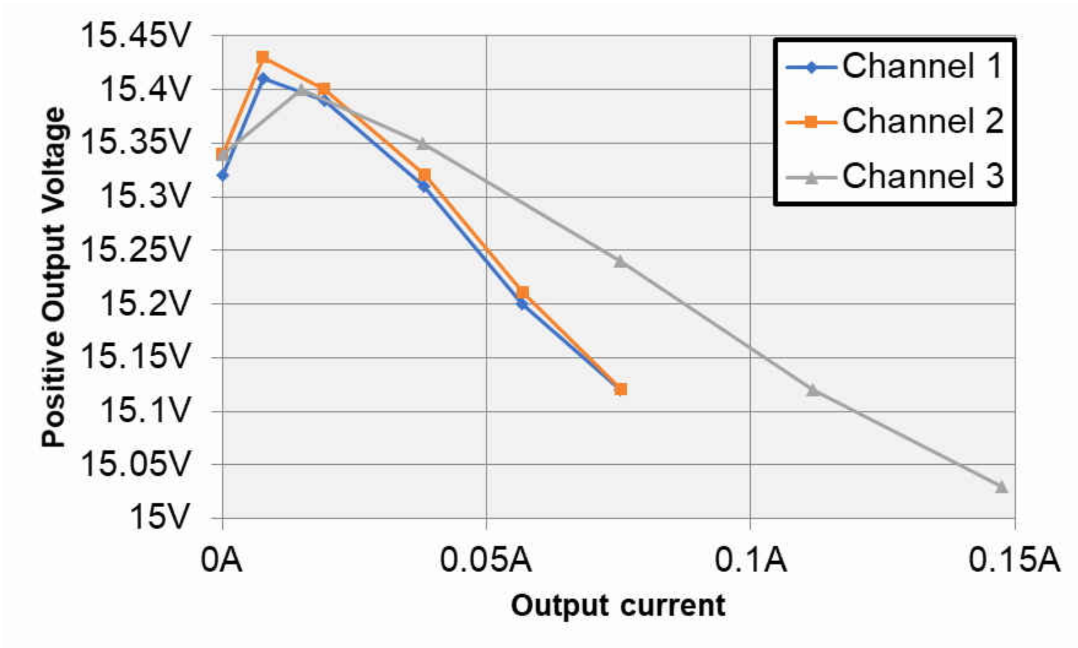


Figure 2-3. Output Voltage vs Output Current (Positive Outputs)

2.3.2.2 Negative Outputs

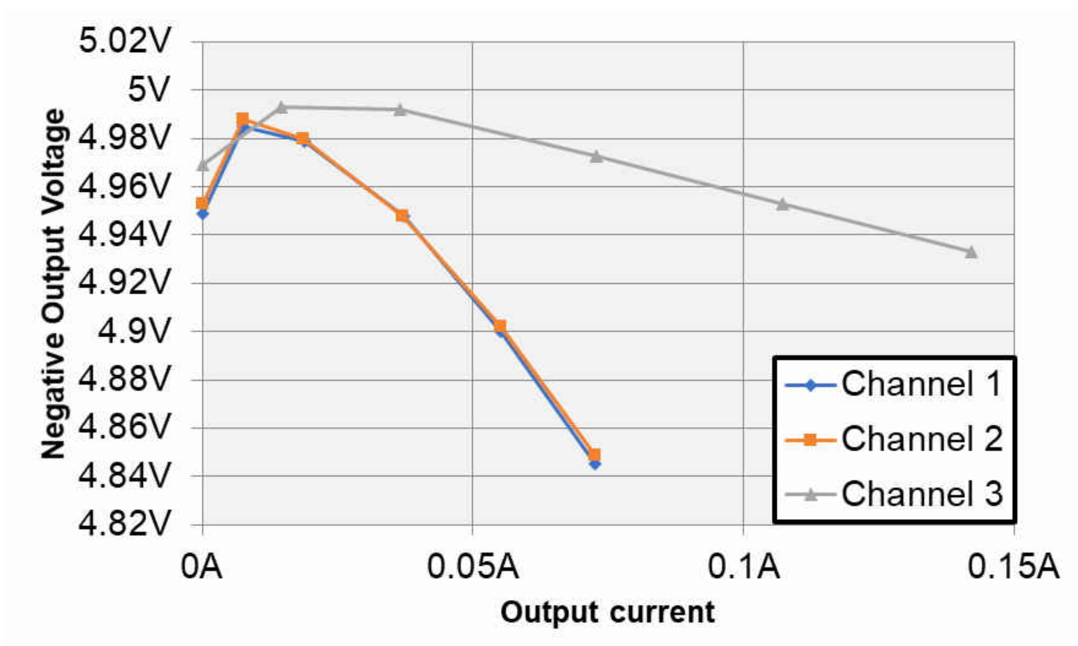


Figure 2-4. Output Voltage vs Output Current (Negative Outputs)

2.4 Line Regulation

2.4.1 Primary Output

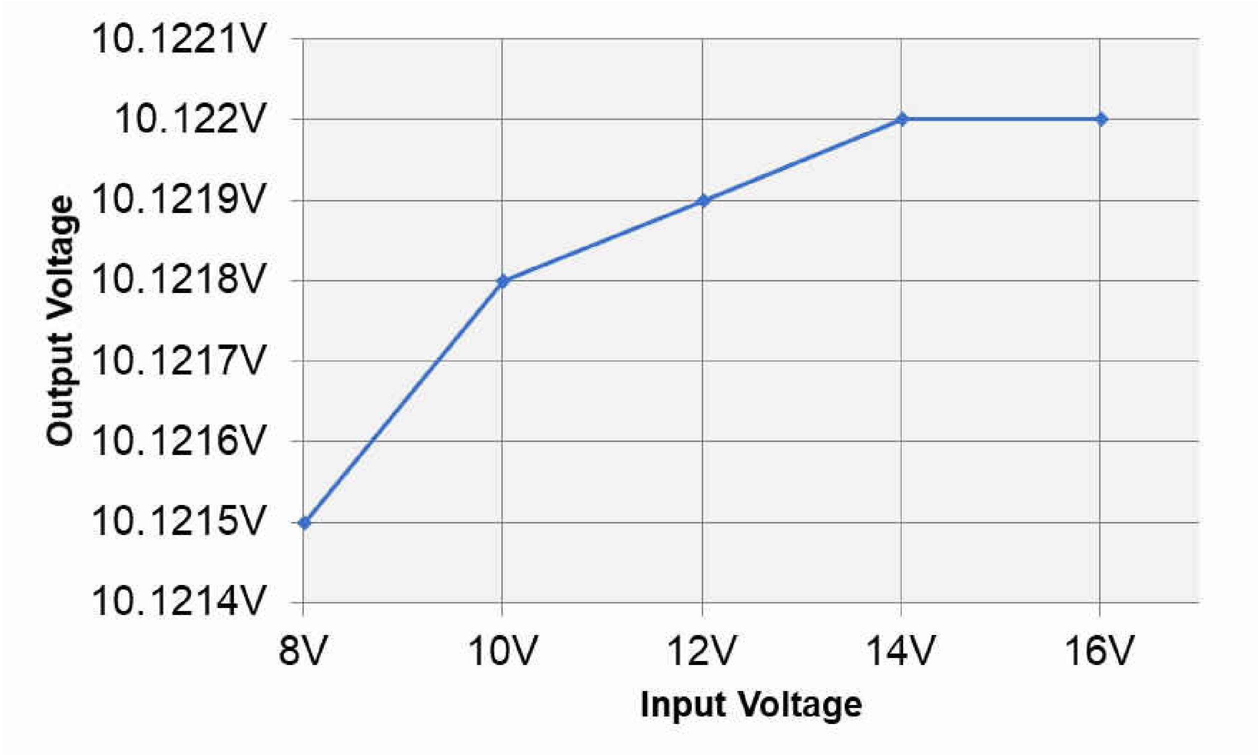


Figure 2-5. Primary Output Voltage vs Input Voltage

2.4.2 Secondary Outputs

The following images show the line regulation of the secondary outputs.

2.4.2.1 Positive Outputs

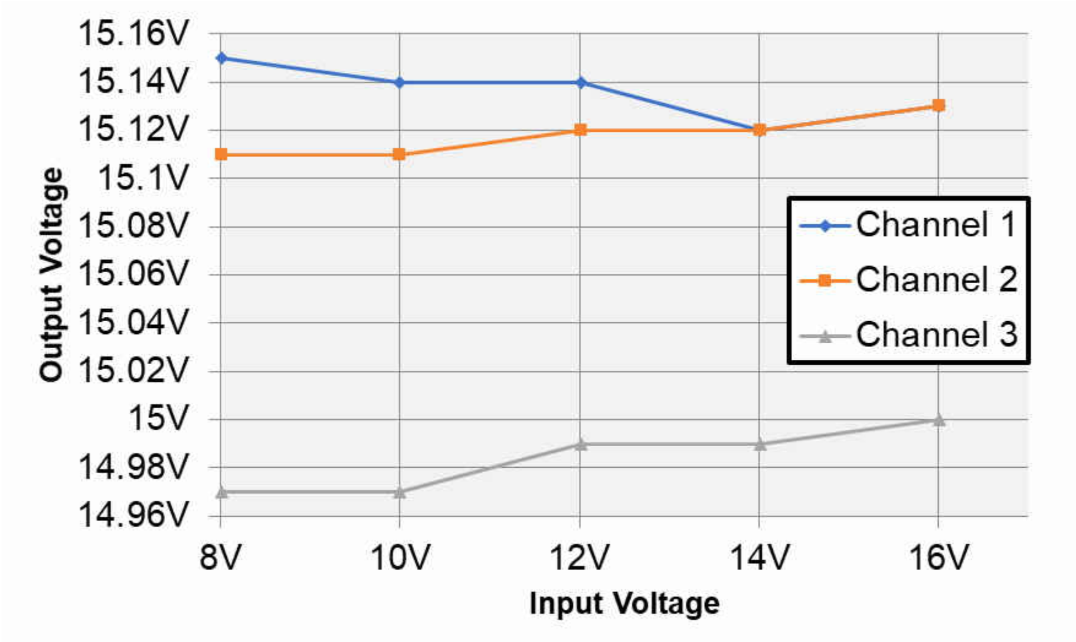


Figure 2-6. Secondary Output Voltages vs Input Voltage (Positive Outputs)

2.4.2.2 Negative Outputs

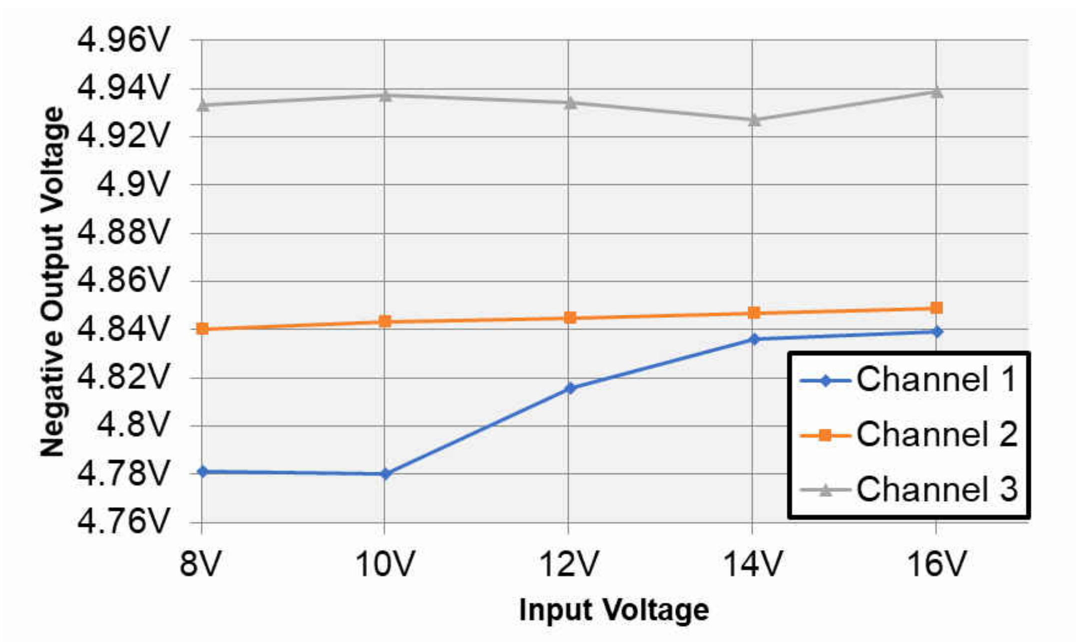


Figure 2-7. Output Voltage vs Input Voltage (Negative Outputs)

2.5 Thermal Images

The thermal image is shown in the following figure. Transformer T1 was painted black.

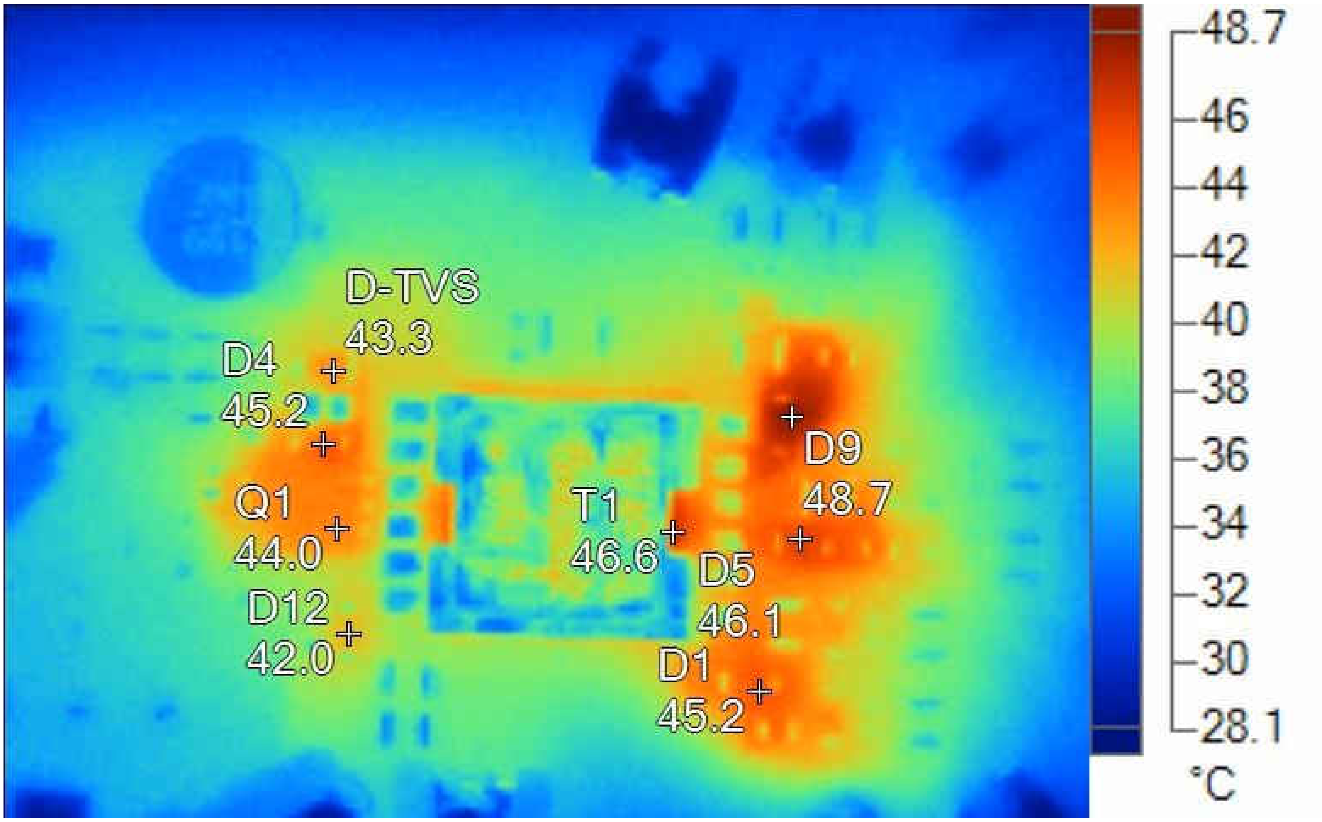


Figure 2-8. Thermal Image, Full Load, Input 12 V at Ambient Temperature 23°C

Name	Temperature
D1	45.2°C
D12	42.0°C
D4	45.2°C
D5	46.1°C
D9	48.7°C
D-TVS	43.3°C
Q1	44.0°C
T1	46.6°C

The maximum temperature rise is below 30 K.

2.6 Bode Plots

The table below summarizes the bode plots in the following figures.

V_{in}	5.5 V	12 V
Bandwidth (kHz)	13	15.6
Phase Margin	84°	83°
Slope (20 dB/decade)	–0.93	-0.98
Gain Margin (dB)	–14.7	–16.4
Slope (20 dB/decade)	–0.92	–1.6
Freq (kHz)	83	83

2.6.1 5.5-V Input Voltage

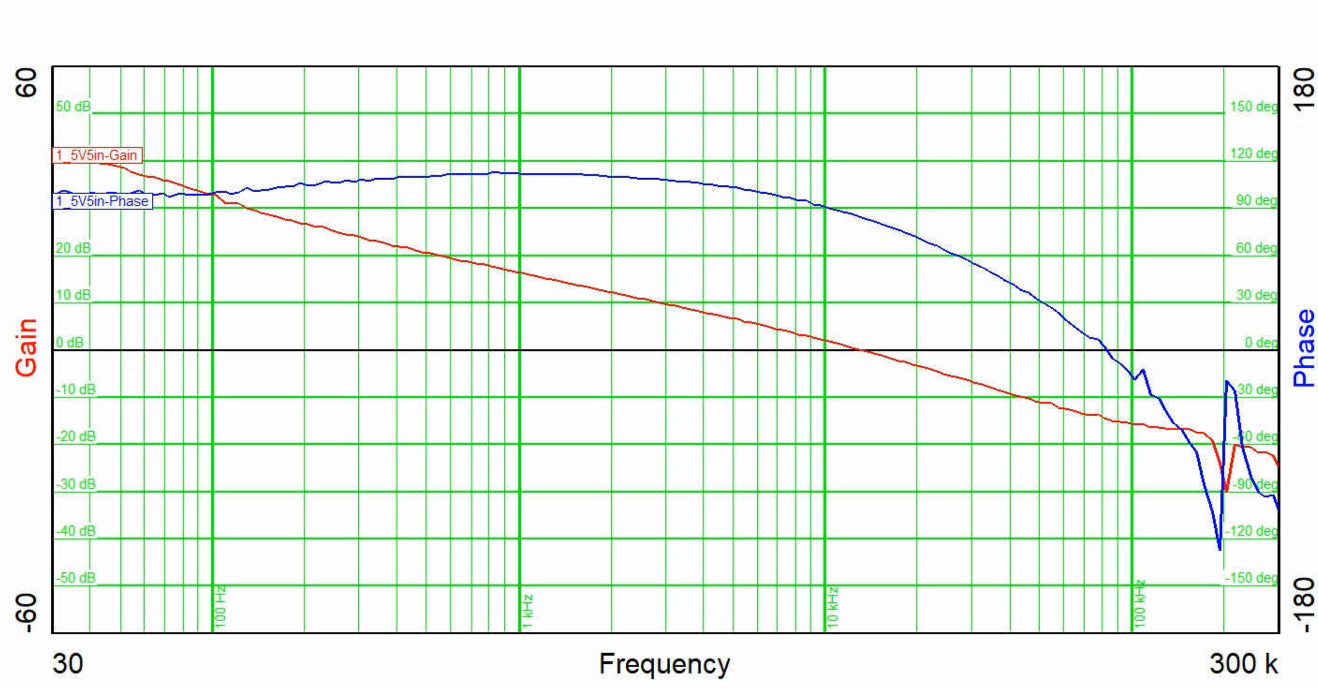


Figure 2-9. Bode Plot at 5.5-V Input Voltage

2.6.2 12-V Input Voltage

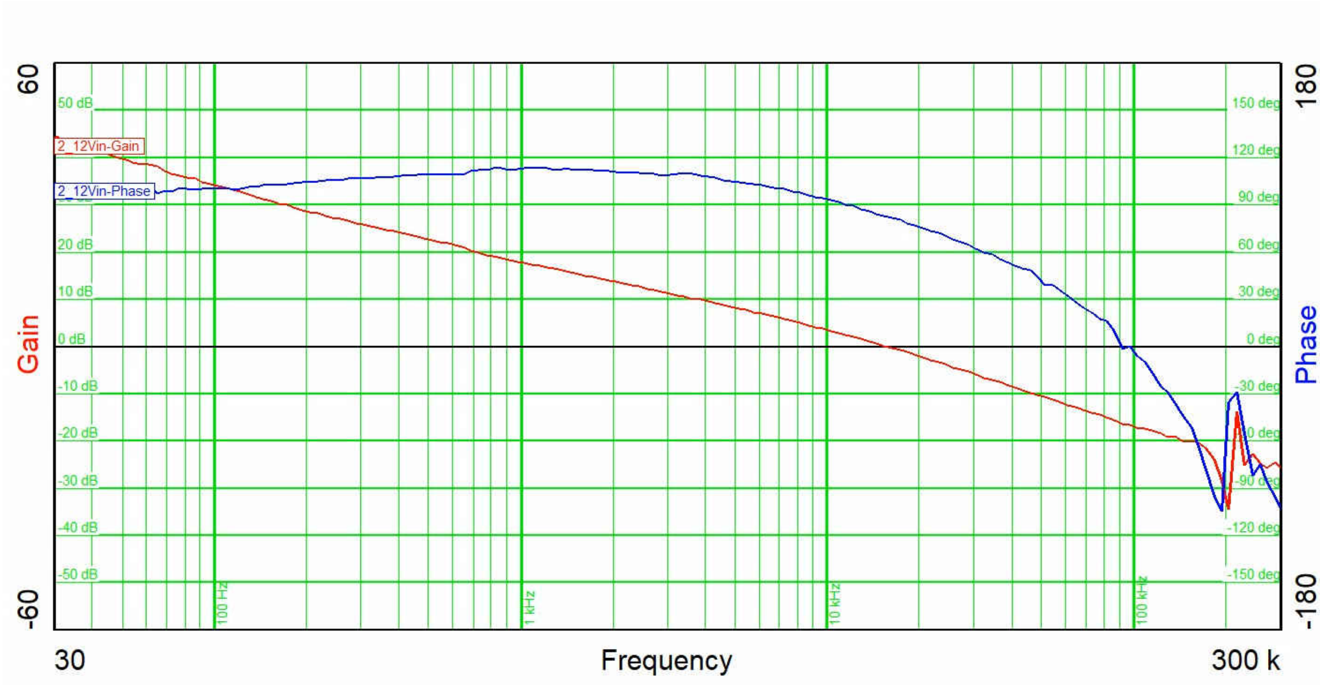


Figure 2-10. Bode Plot at 12-V Input Voltage

3 Waveforms

3.1 Switching

3.1.1 Q1 Drain to GND

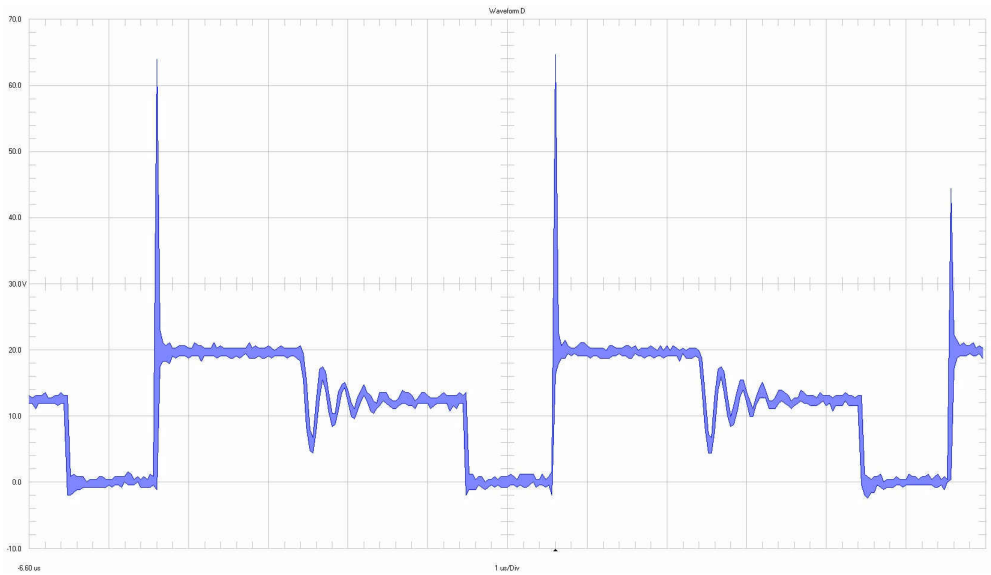
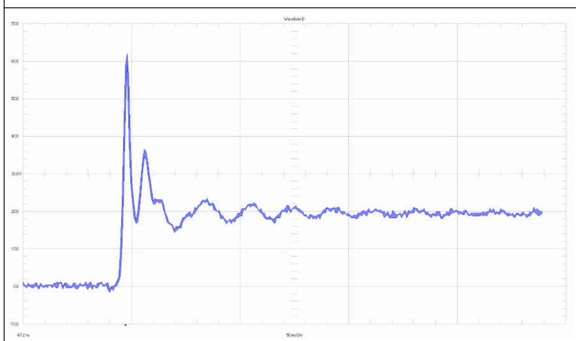
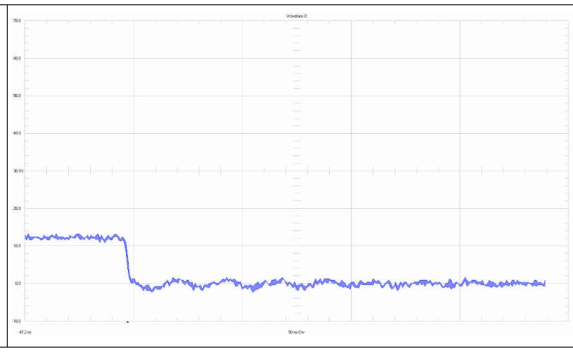
<table>
<tr><td colspan="2">
</td><td>10 V / div
1 µs / div
full bandwidth</td></tr>
<tr><td></td><td></td><td>10 V / div
50 ns / major div
full bandwidth</td></tr>
</table>

Figure 3-1. Switchnode to GND

3.1.2 Q1 Gate to GND

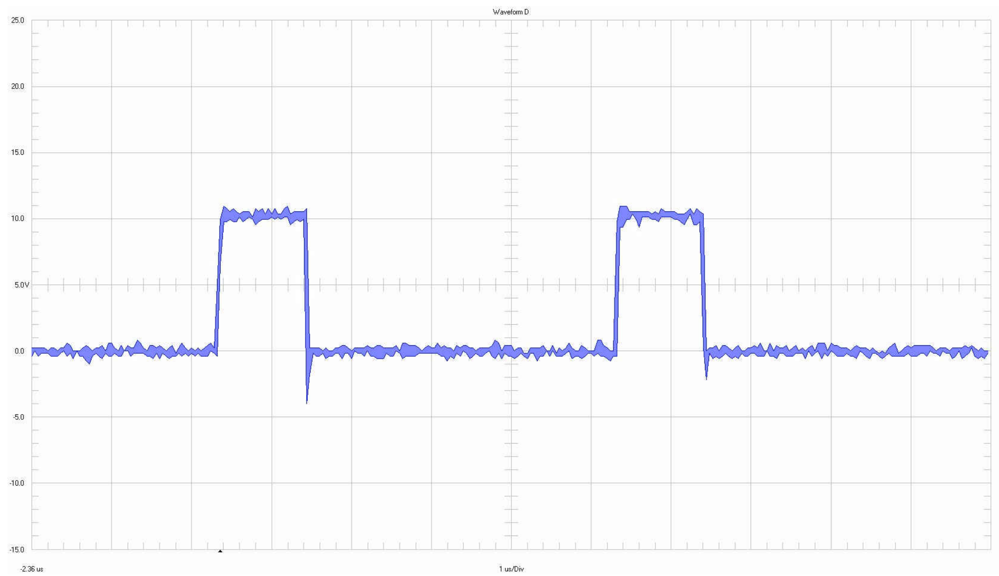
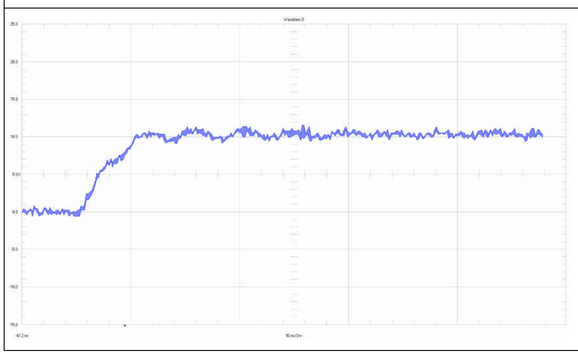
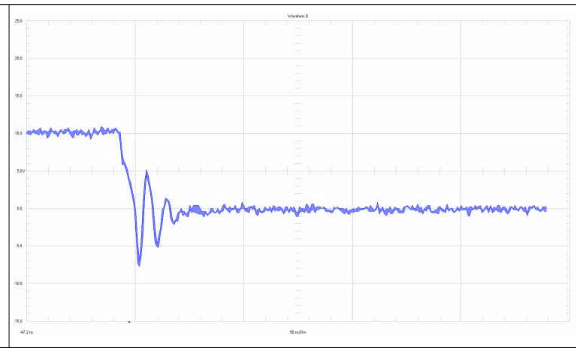
<table>
<tr><td colspan="2">
</td><td>5 V / div
1 µs /div
full bandwidth</td></tr>
<tr><td></td><td></td><td>5 V / div
50 ns / major div
full bandwidth</td></tr>
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Figure 3-2. Waveform Gate Q1 to GND

3.1.3 Diode D12

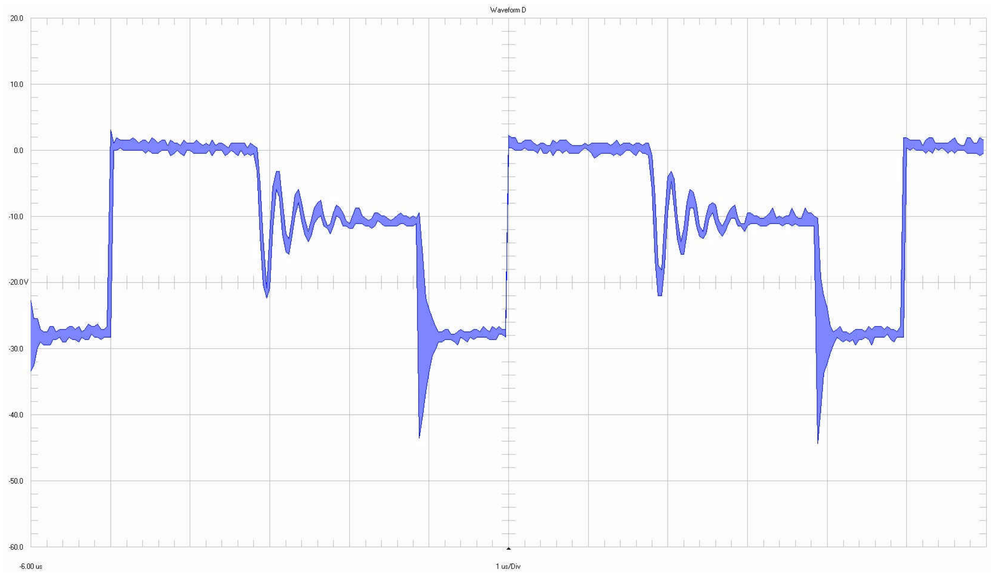
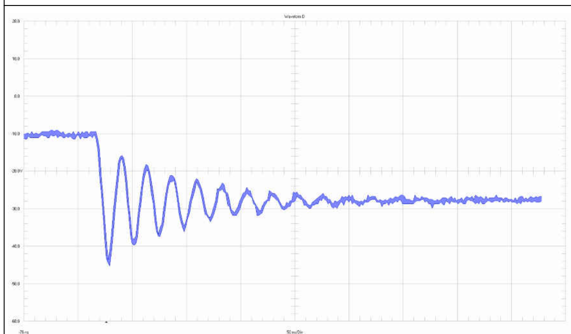
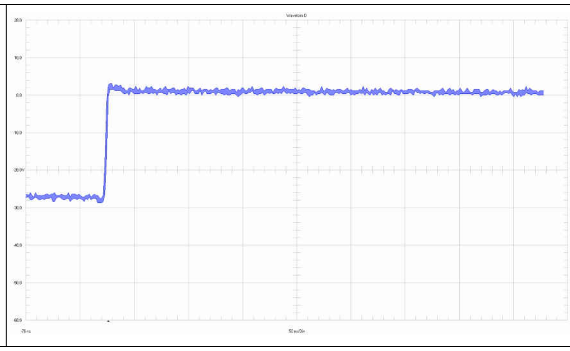
		10 V / div 1 µs / div full bandwidth
		10 V / div 50 ns / major div full bandwidth

Figure 3-3. Diode D12 to +10 V_{pri}

3.1.4 Diode D9

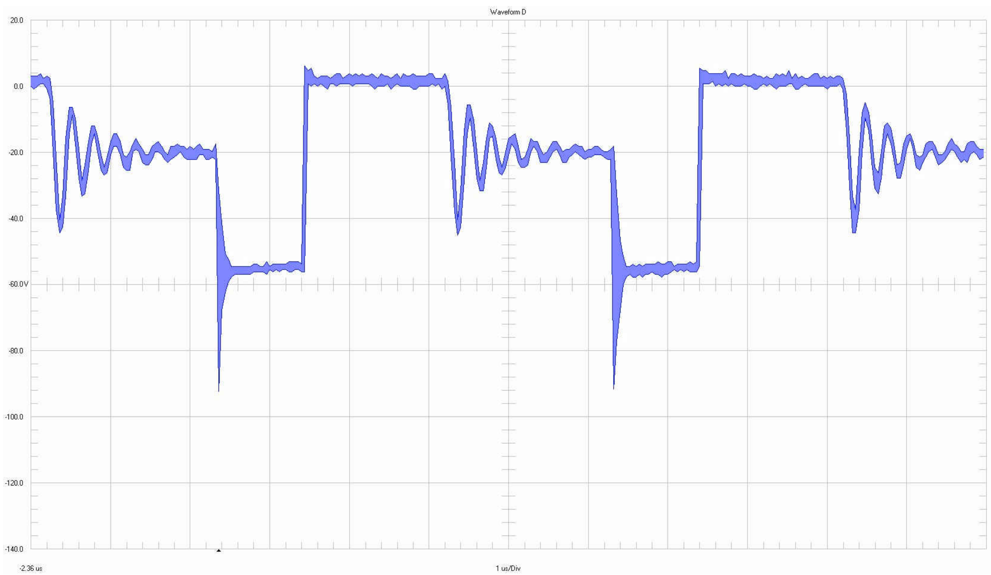
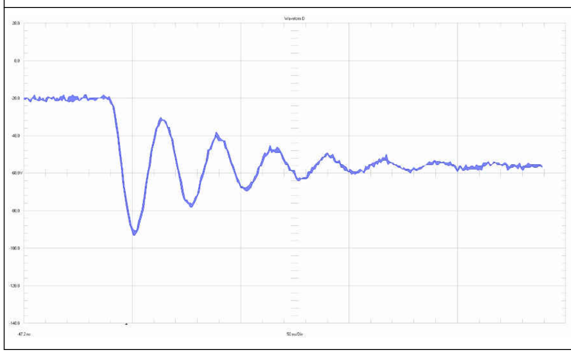
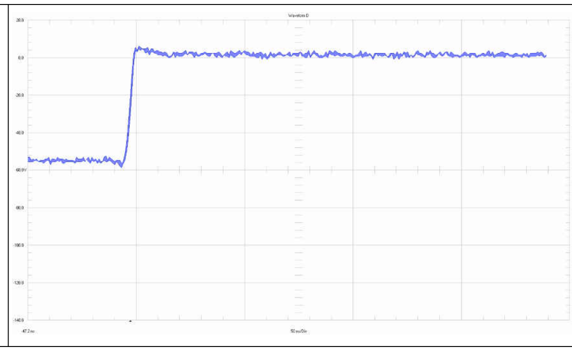
<table>
<tr><td colspan="2">
</td><td>20 V / div
1 µs / div
full bandwidth</td></tr>
<tr><td></td><td></td><td>20 V / div
50 ns / major div
full bandwidth</td></tr>
</table>

Figure 3-4. Diode D9 to +15V_3

3.2 Output Voltage Ripple

Output voltage ripple is shown in the following figures.

3.2.1 Primary 10 V (Auxiliary)

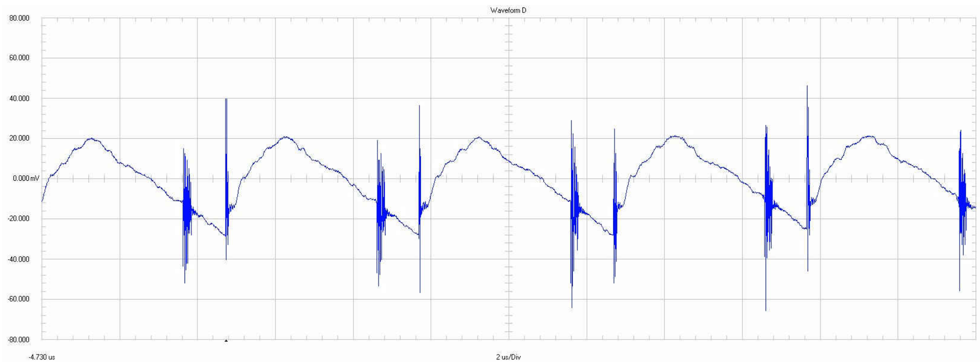
	20 mV / div 2 µs / div 20 MHz bandwidth

Figure 3-5. +10 V_{aux} Output

3.2.2 Secondary +15 V

The following three waveforms show the output voltage ripple of the three secondary +15-V outputs.

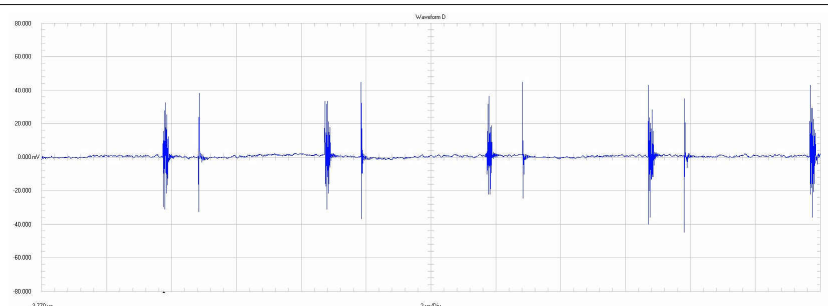
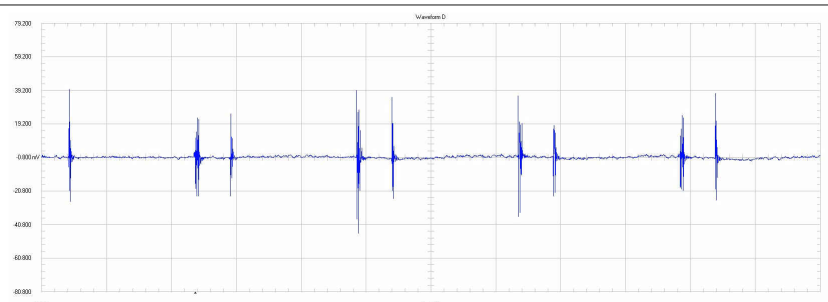
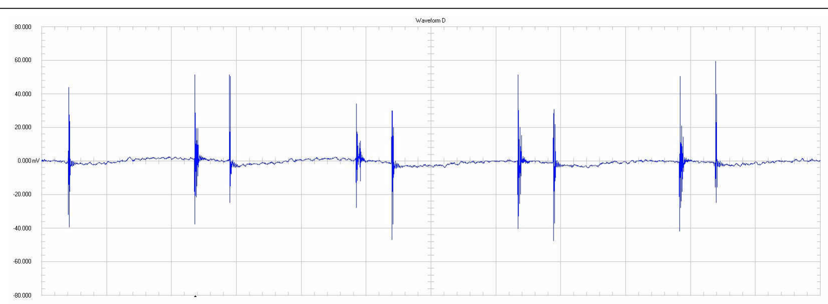
	1 20 mV / div 2 µs / div 20 MHz bandwidth
	2 20 mV / div 2 µs / div 20 MHz bandwidth
	3 20 mV / div 2 µs / div 20 MHz bandwidth

Figure 3-6. +15-V Output

3.2.3 Secondary –5 V

The following three waveforms show the output voltage ripple of the three secondary –5 V outputs.

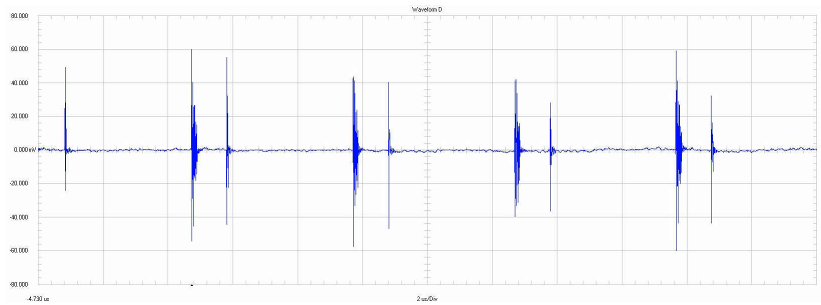
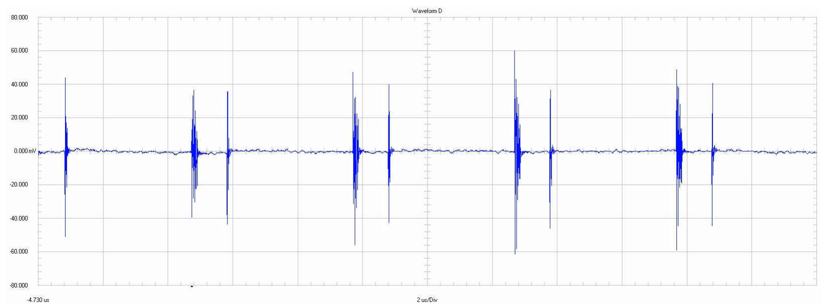
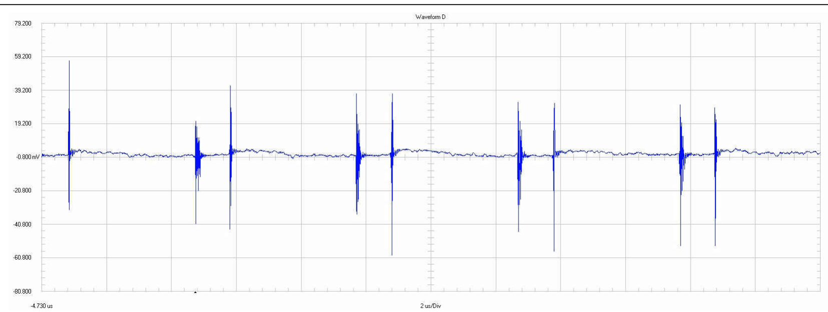
	1 20 mV / div 2 µs / div 20 MHz bandwidth
	2 20 mV / div 2 µs / div 20 MHz bandwidth
	20 mV / div 2 µs / div 20 MHz bandwidth

Figure 3-7. –5-V Output

3.3 Input Voltage Ripple

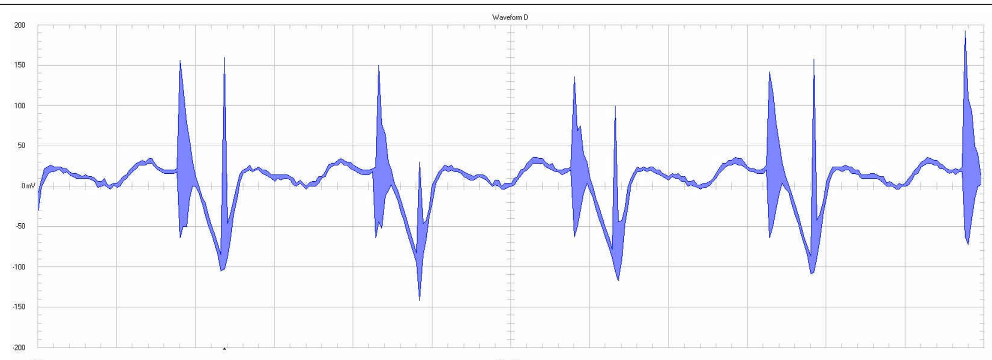
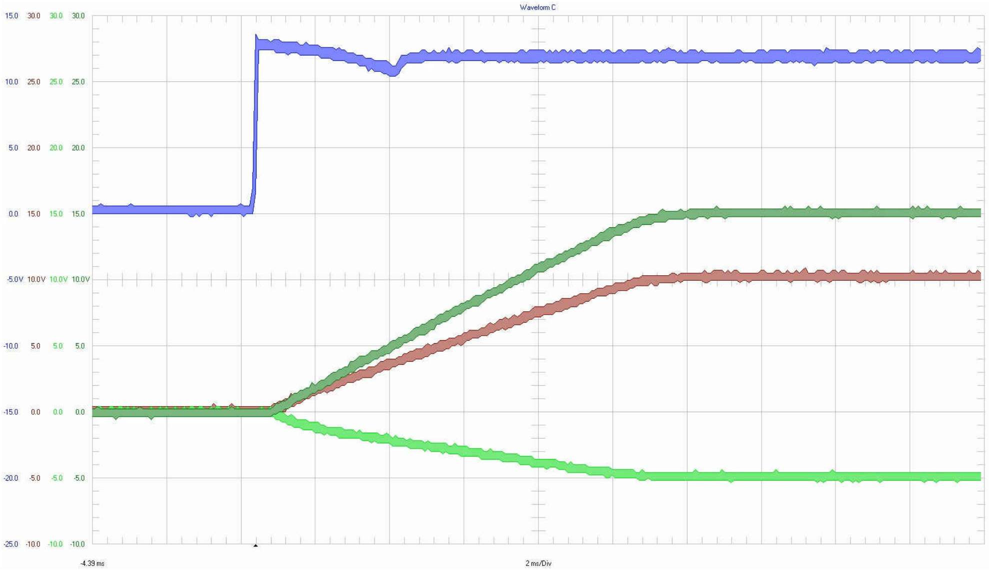
	50 mV / div 2 µs / div 20 MHz bandwidth

Figure 3-8. Input Voltage Ripple

3.4 Start-Up Sequence

Start-up behavior is shown in the following figure. An oscilloscope with isolated channels was used.



5 V / div

Ch1 ⇒ Input

Ch2 ⇒ +15 V_{out} (3)

Ch3 ⇒ +10 V_{out} (aux)

Ch4 ⇒ -5 V_{out} (3)

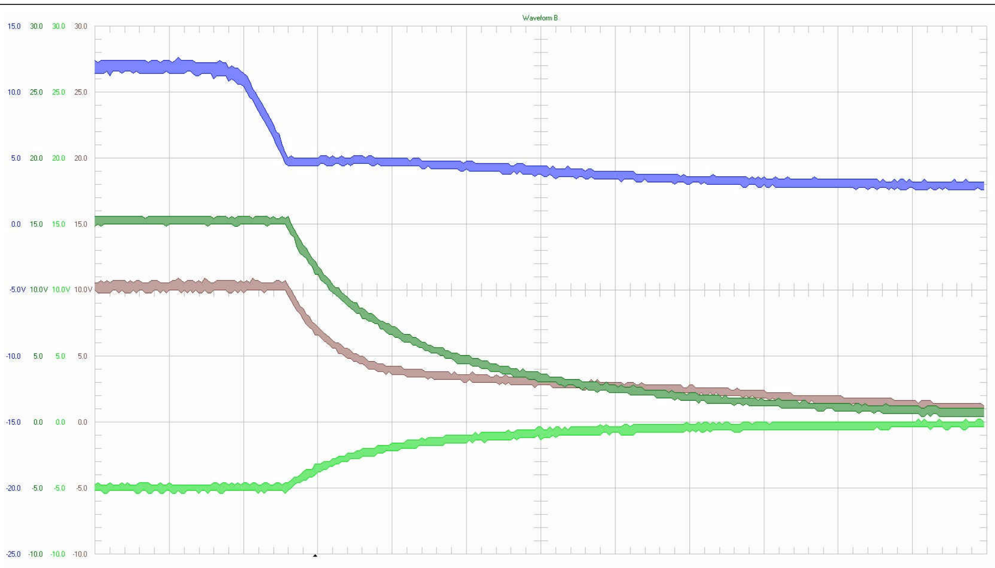
20 MHz bandwidth

2 ms / div

Figure 3-9. Start-up

3.5 Shutdown Sequence

Shutdown behavior is shown in the following figure. An oscilloscope with isolated channels was used.



5 V / div

Ch1 ⇒ Input

Ch2 ⇒ +15 V_{out} (3)

Ch3 ⇒ +10 V_{out} (aux)

Ch4 ⇒ -5 V_{out} (3)

20 MHz bandwidth

1 ms / div

Figure 3-10. Shutdown

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265