Test Report: PMP30934

IGBT and SiC Gate Drive Auxiliary PSU Reference Design

Description

This reference design introduces a tiny auxiliary power supply unit (PSU) used to supply automotive insulated-gate bipolar transistor (IGBT) or automotive silicon carbide (SiC) drive. The isolated outputs support three gate controls, each supplied with +17 V and –4 V. To simplify transformer windings, a virtual ground Zener diode which works for symmetrical loading, is implemented.

The LM25184 controller supports primary-side regulation just by controlling the flyback voltage from secondary side and there is no need for an additional auxiliary winding. Furthermore, valley switching is beneficial for efficiency.

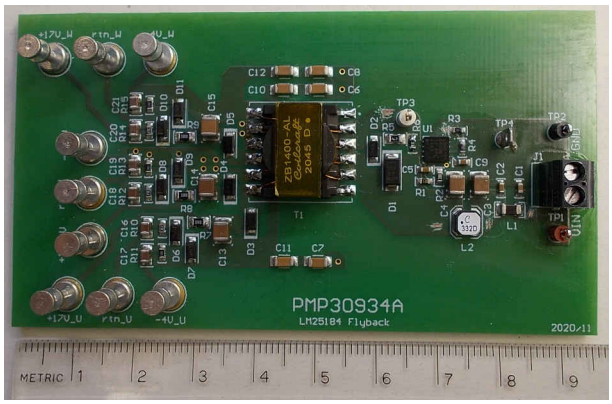
To reduce reflected ripple-to-source, a differential input filter is added to this PSR flyback converter.

Features

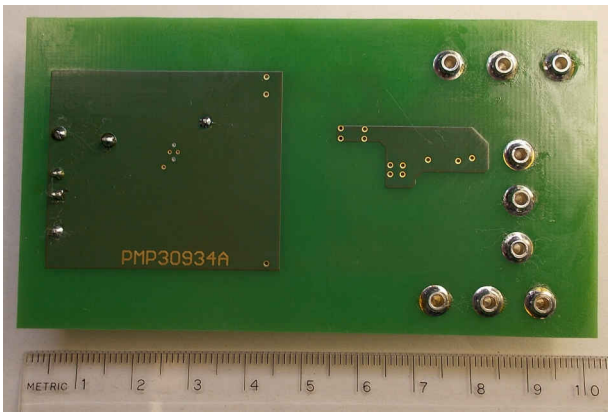
- Two-stage differential input filter to prevent from conducted emissions
- Three outputs (+17 V and –4 V) with efficiency 86% at full load, temperature rise only +15 K at full load
- Simple transformer windings by using virtual output return provides isolation voltage 2500 V_{RMS}
- No optoisolator design, primary-side regulation
- Two-layer board, single-side assembly, high-power density by using integrated FET, circuit geometry 70 mm × 35 mm
- Maximum height 7.4 mm (by low profile transformer)

Applications

- Bidirectional 400 V and 800 V to LV
- Unidirectional 400 V and 800 V to LV
- Unidirectional HV-to-LV digital loop



Board Photo (Top)



Board Photo (Bottom)

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input Voltage Range	6 V to 27 V (13.5 V nominal)
Positive Output U, V and W	+17 V at 0.05 A_{max}
Negative Output U, V and W	–4 V at 0.05 A_{max}
IC	LM25184QNGURQ1

1.2 Considerations

Keep the following considerations in mind while working with this design:

- Unless otherwise indicated, input voltage was set to 13.5 V. Resistors were used as load.
- Output currents were set to full load (around 0.05 A, each output)
- For lowest cost, the PCB has been routed with two layers and single side assembly

1.3 Dimensions

The size of the board is 95.3 mm × 52 mm with 35-µm copper thickness (both layers).

2 Testing and Results

2.1 Efficiency Graphs, all Outputs Similar Loaded

Efficiency is shown in the following figure.

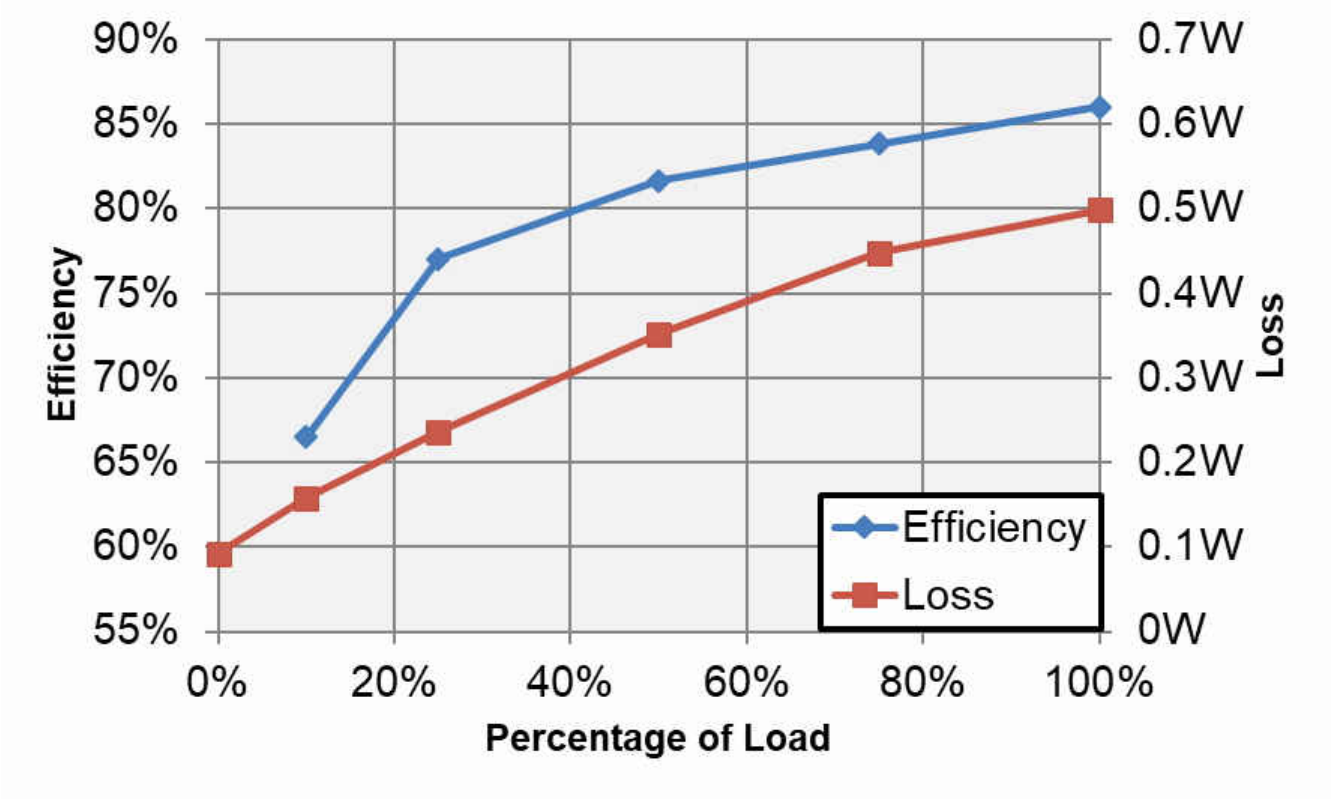


Figure 2-1. Efficiency and Loss vs Percentage of Load, 100% = 50 mA

2.2 Load Regulation

The load regulation graphs are shown in the following images.

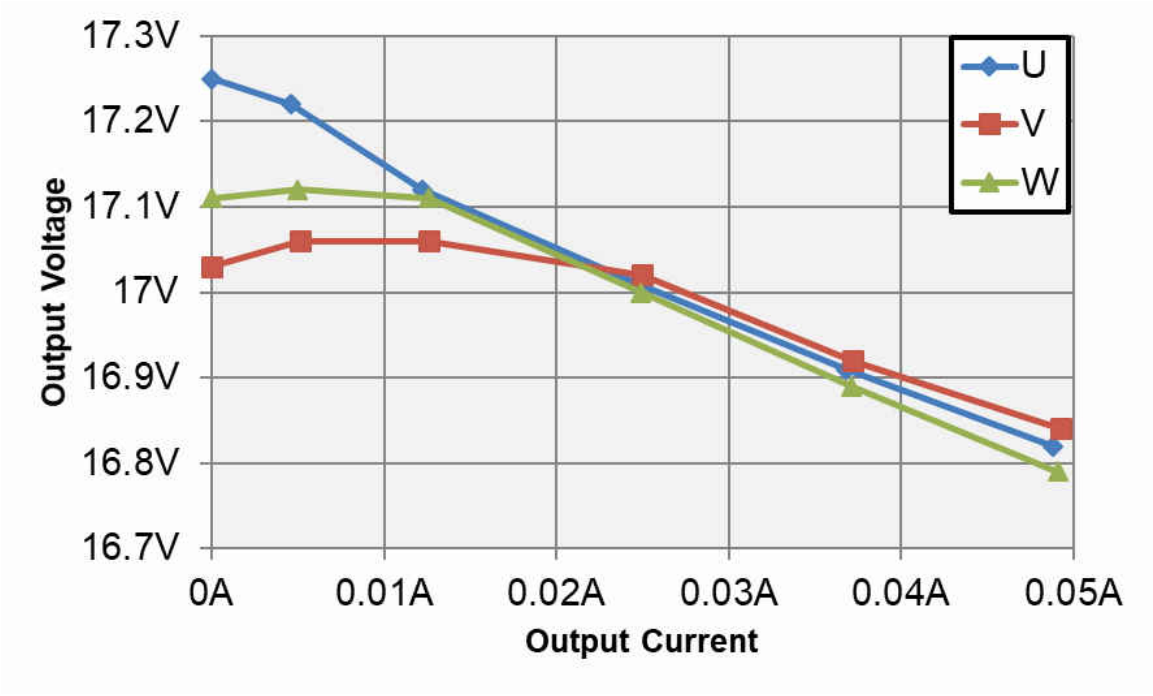


Figure 2-2. Output Voltage vs Output Current (Positive Outputs)

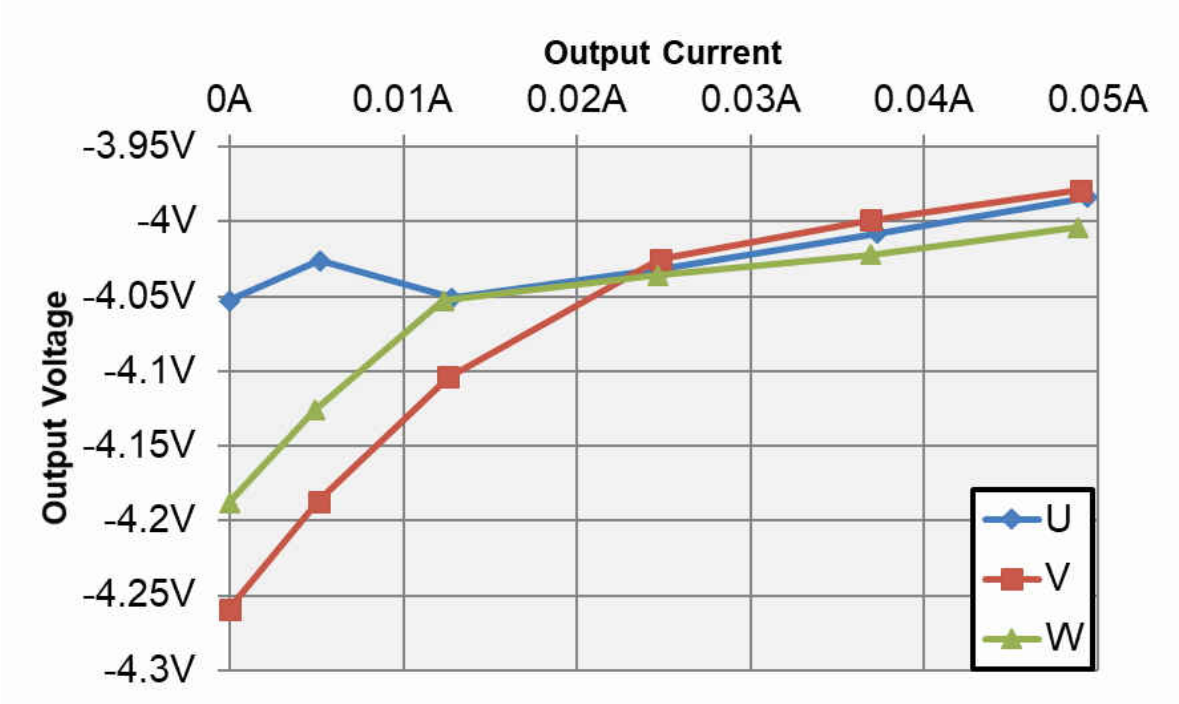


Figure 2-3. Output Voltage vs Output Current (Negative Outputs)

2.3 Cross Regulation and Further Data For Non-Symmetrical Loading

	A	B
V_{IN}	13.5	13.506
I_{IN}	0.1158	0.1909
+VoutU	**17.27**	**17.29**
+IoutU	0.0046	0.0045
–VoutU	–4.133	**–4.134**
–IoutU	0.0052	0.0052
+VoutV	17.11	16.8
+IoutV	0.005	0.049
–VoutV	**–4.292**	**–3.974**
–IoutV	0.0052	0.0489
+VoutW	**16.74**	**16.78**
+IoutW	0.049	0.0491
–VoutW	**–3.975**	–3.983
–IoutW	0.0487	0.0488
PIN	1.563	2.578
Pout	1.223	2.135
Eff	0.782	0.828
Loss	0.341	0.443

A ⇒ output W full load 50 mA; output V and U 10% load, so 5 mA (one channel fully loaded).

B ⇒ output W and V full load 50 mA; output U just 10% load, so 5 mA (two channels fully loaded).

Non-symmetrical loading 10% and 100% of channels results in voltage deviation 16.74 V to 17.29 V and –3.974 V to –4.292 V.

Non-symmetrical loading **individually** at a channel, so different loading at + voltage and – voltage could be a problem for a virtual ground using this Zener solution. Here the load at + and – output is almost similar.

If needed, this could be improved: by increasing the voltage drop across shunt resistors R7, R8, and R9 ⇒ needs rework on R6, try 73.2 kΩ.

2.4 Line Regulation at Full Load to all Outputs

The images in this section illustrate the line regulation graphs at full load to all outputs.

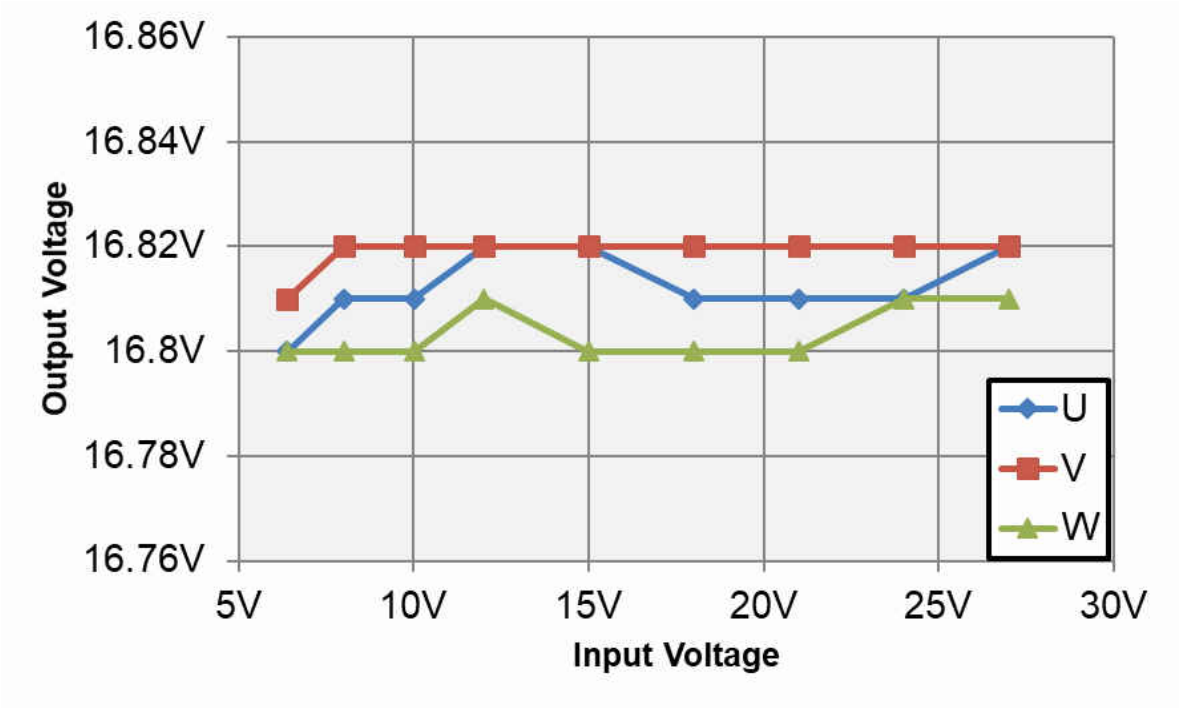


Figure 2-4. Output Voltage vs Input Voltage

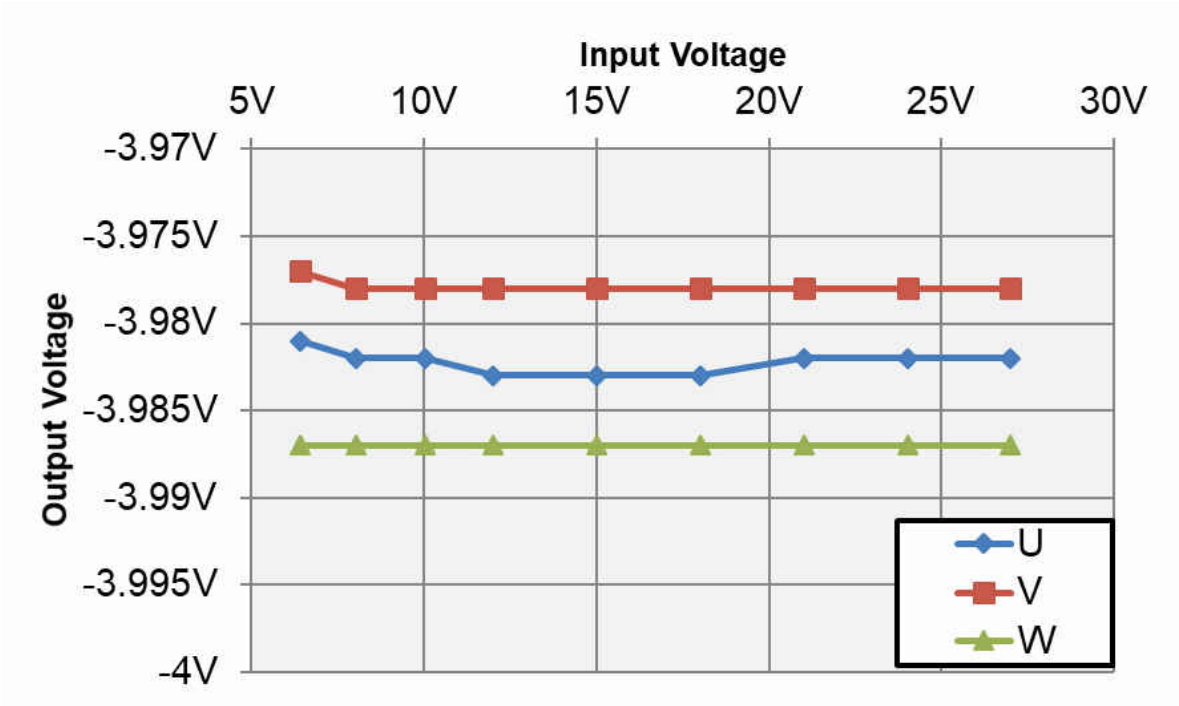


Figure 2-5. Output Voltage vs Input Voltage (Negative Outputs)

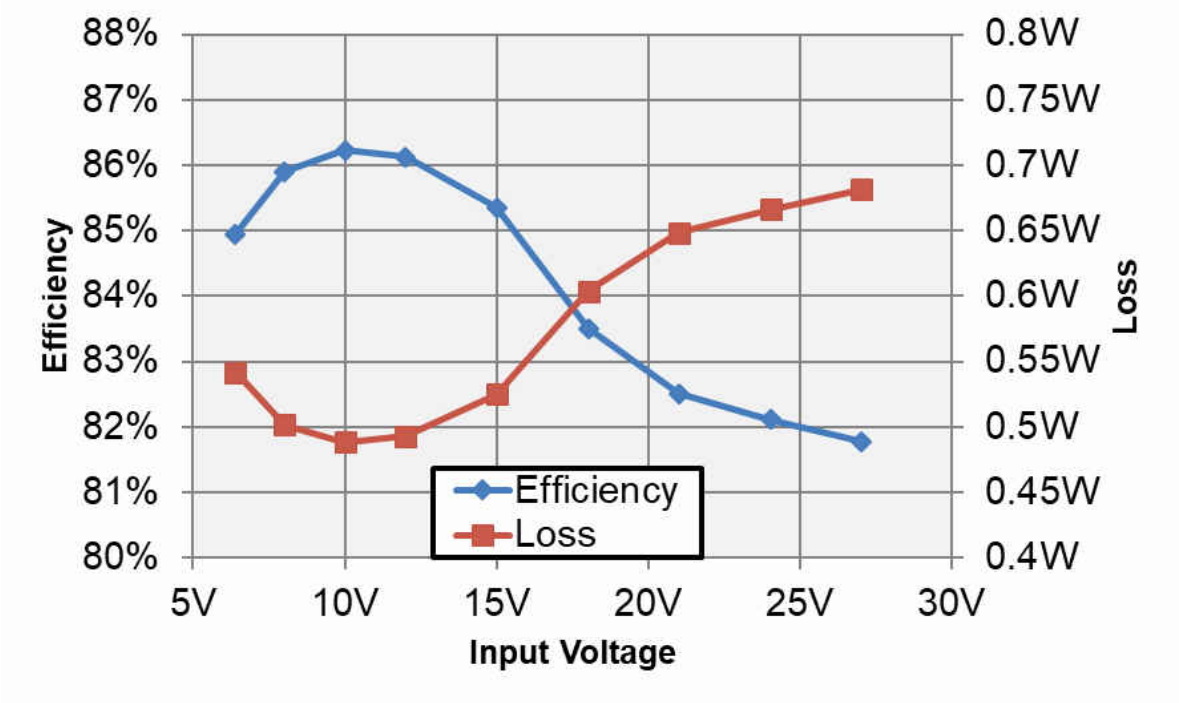


Figure 2-6. Efficiency and Loss vs Input Voltage

2.5 Thermal Images

The thermal image is shown in the following figure.

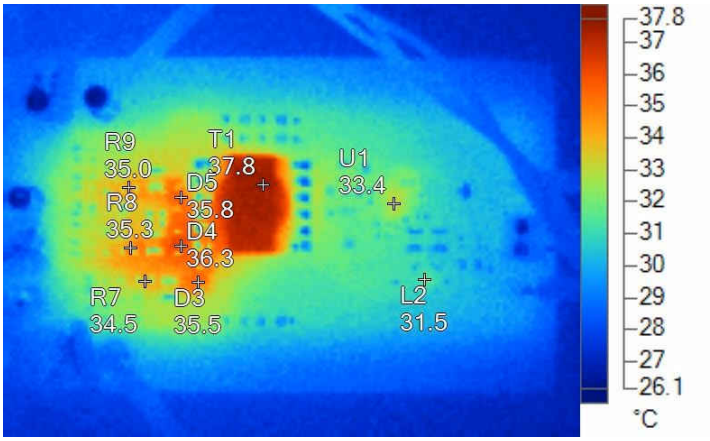


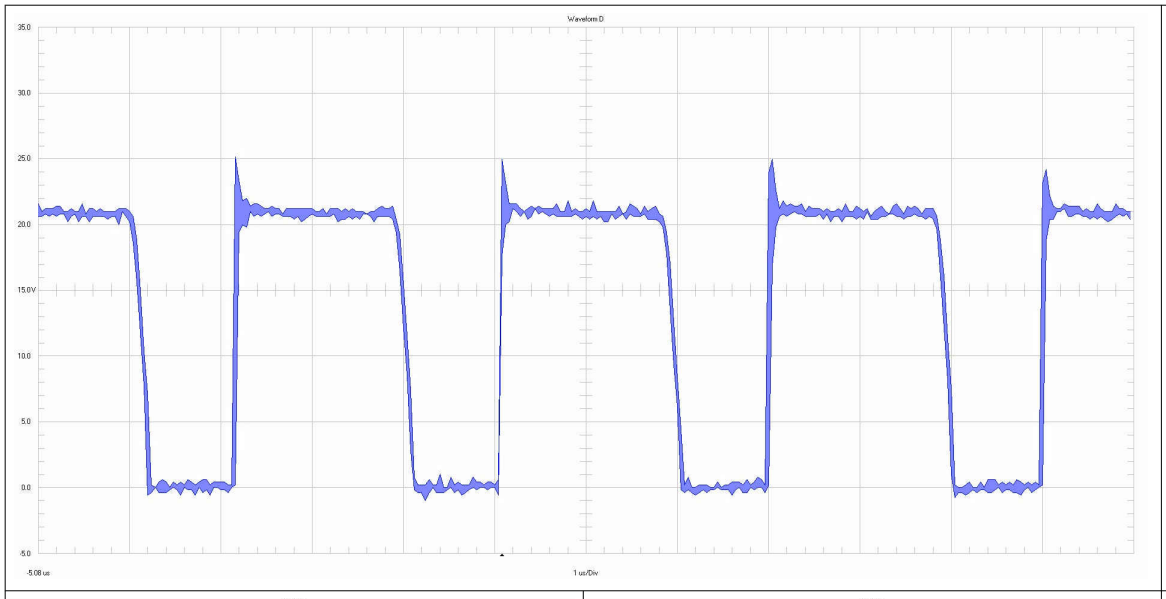
Figure 2-7. Thermal Image at Full Load and 13.5 V, dT +15 K

Name	Temperature
D3	35.5°C
D4	36.3°C
D5	35.8°C
L2	31.5°C
R7	34.5°C
R8	35.3°C
R9	35.0°C
T1	37.8°C
U1	33.4°C

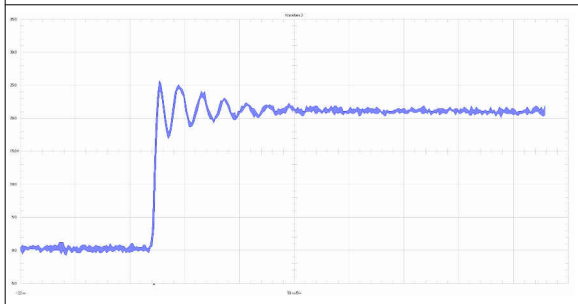
3 Waveforms

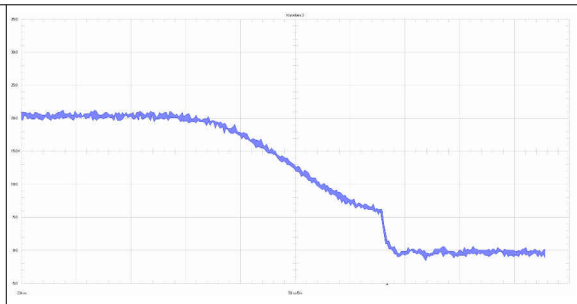
3.1 Switching

3.1.1 Switchnode to GND



5 V / div
1 µs / div
full bandwidth





The falling edge shows effective valley switching.

5 V / div
50 ns / div
full bandwidth

Figure 3-1. Switch Node to GND

3.1.2 Diode D3

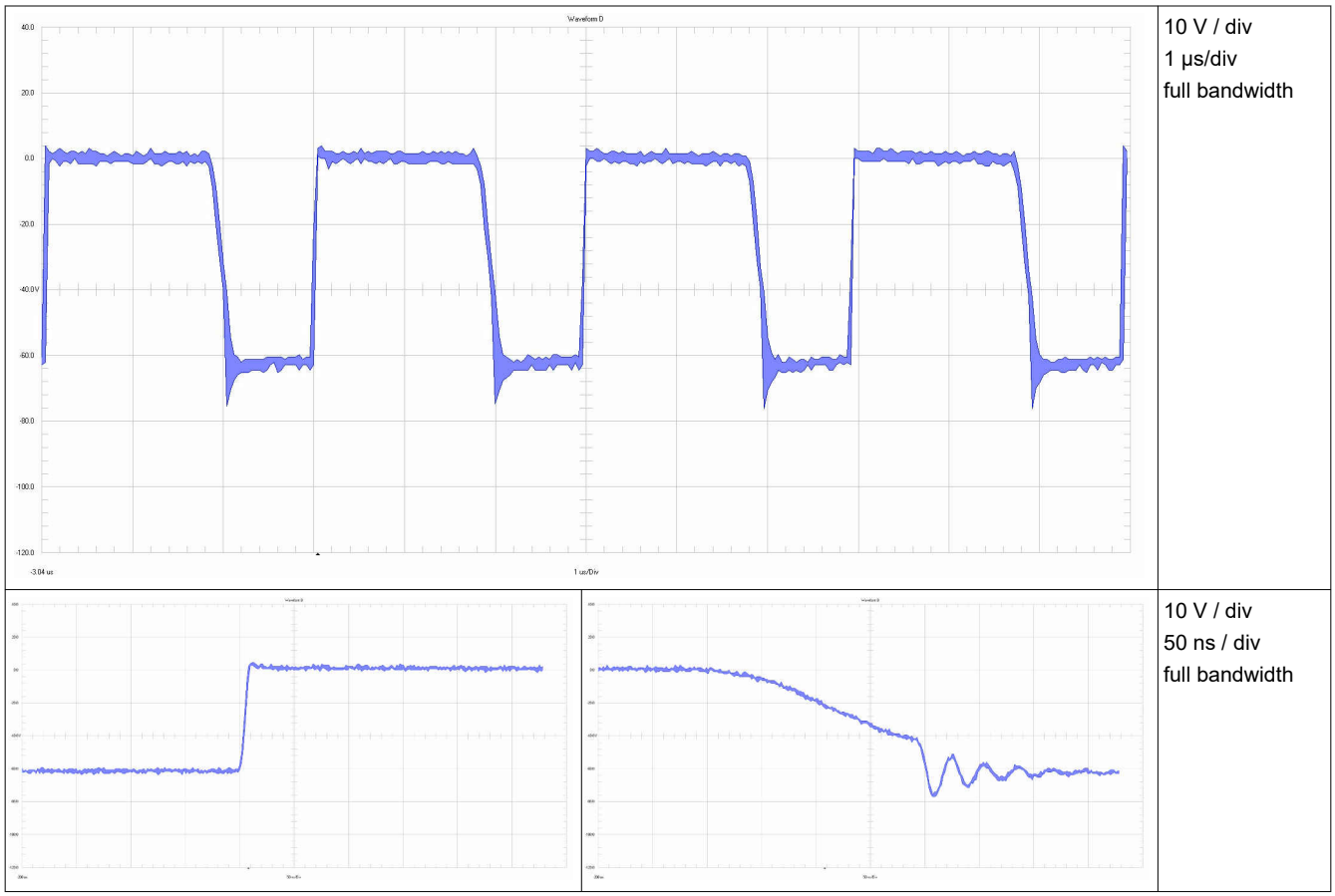


Figure 3-2. Diode D3

3.2 Output Voltage Ripple

Figure 3-3 displays the positive +17-V output of channel U.

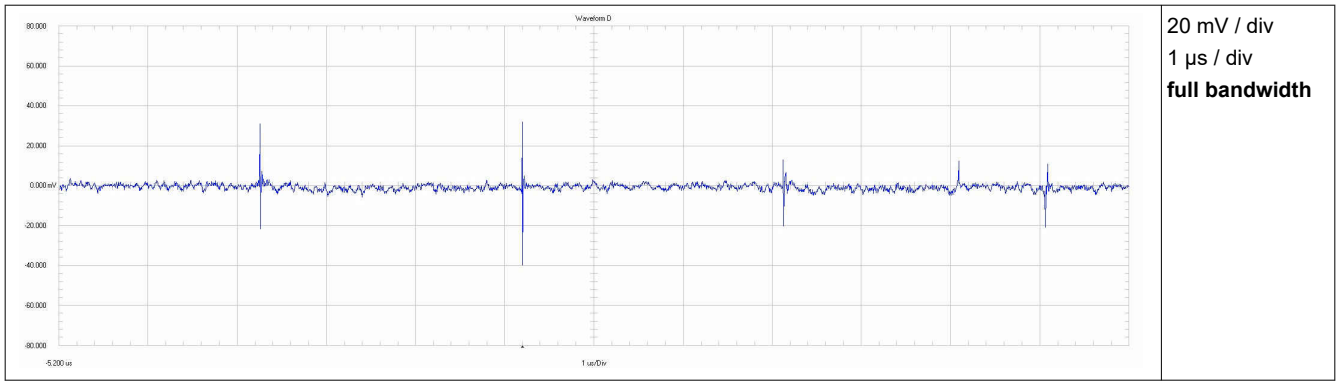


Figure 3-3. +17-V Output U

Figure 3-4 shows the negative –4-V output of channel U.

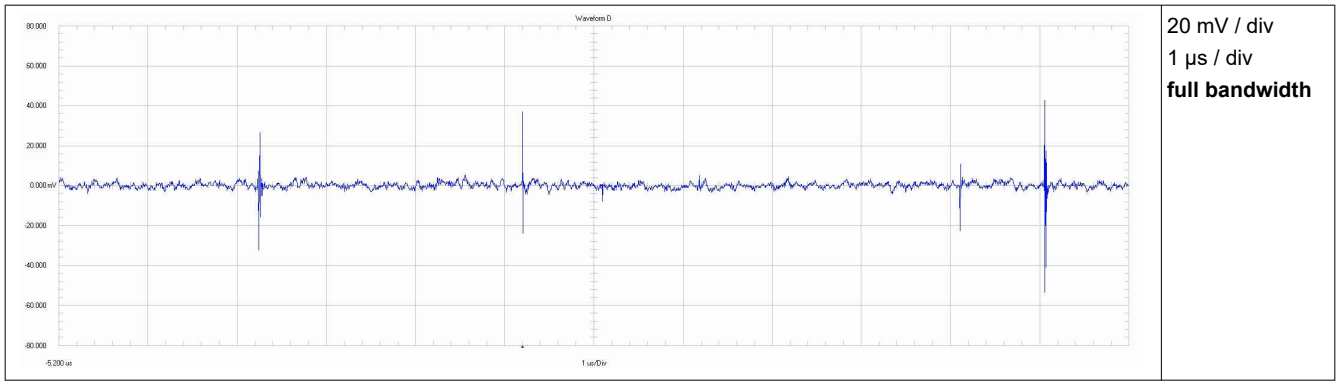
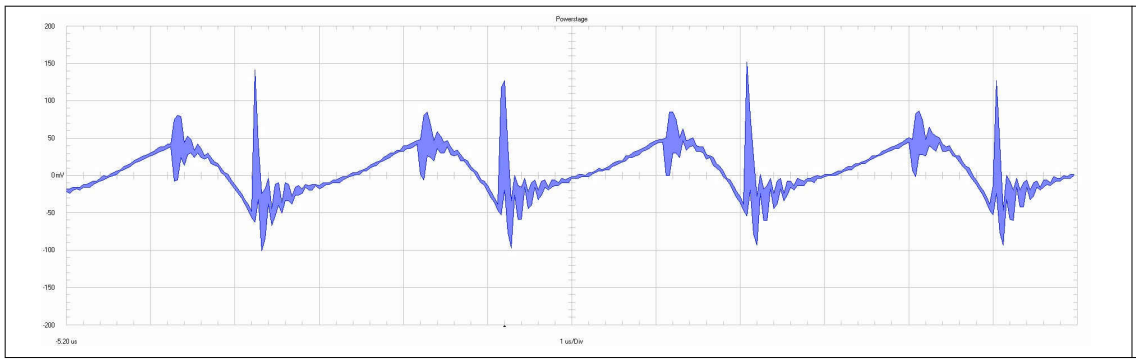


Figure 3-4. –4-V Output U

3.3 Input Voltage Ripple

The input voltage ripple was measured at different locations on this reference design.

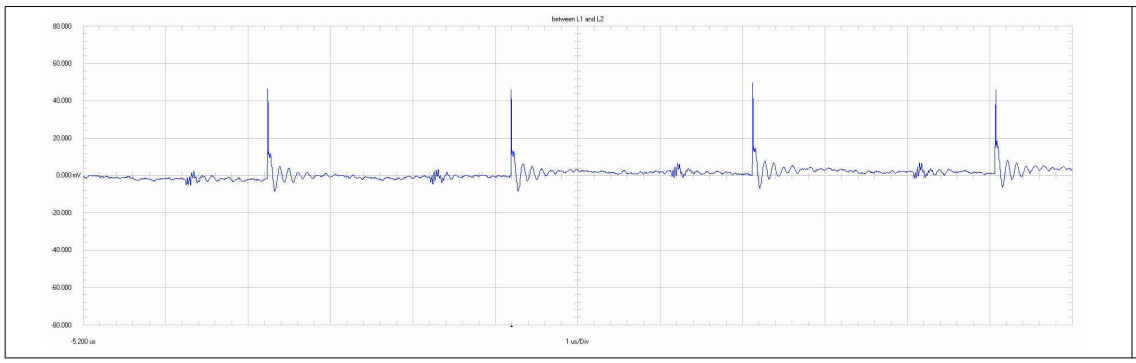
3.3.1 Power Stage Input



50 mV / div
1 µs / div
20 MHz bandwidth

Figure 3-5. Voltage Ripple Power Stage Input

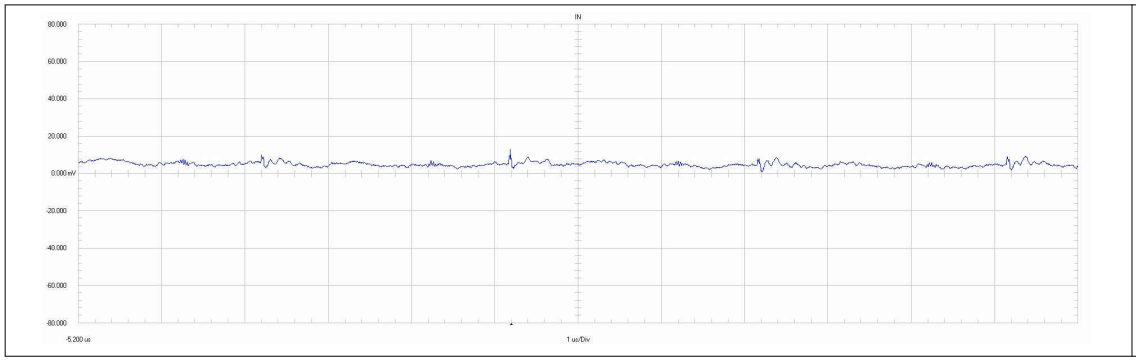
3.3.2 Between L1 and L2



20 mV / div
1 µs / div
20 MHz bandwidth

Figure 3-6. Voltage Ripple Between L1 and L2, Ripple Attenuation by Differential LC Filter

3.3.3 Input Terminal



20 mV / div
1 µs / div
20 MHz bandwidth

Figure 3-7. Voltage Ripple at J1, RF Noise Reduction by Ferrite Bead

3.4 Start-Up Sequence

Start-up behavior of channel U is shown in the following figure.

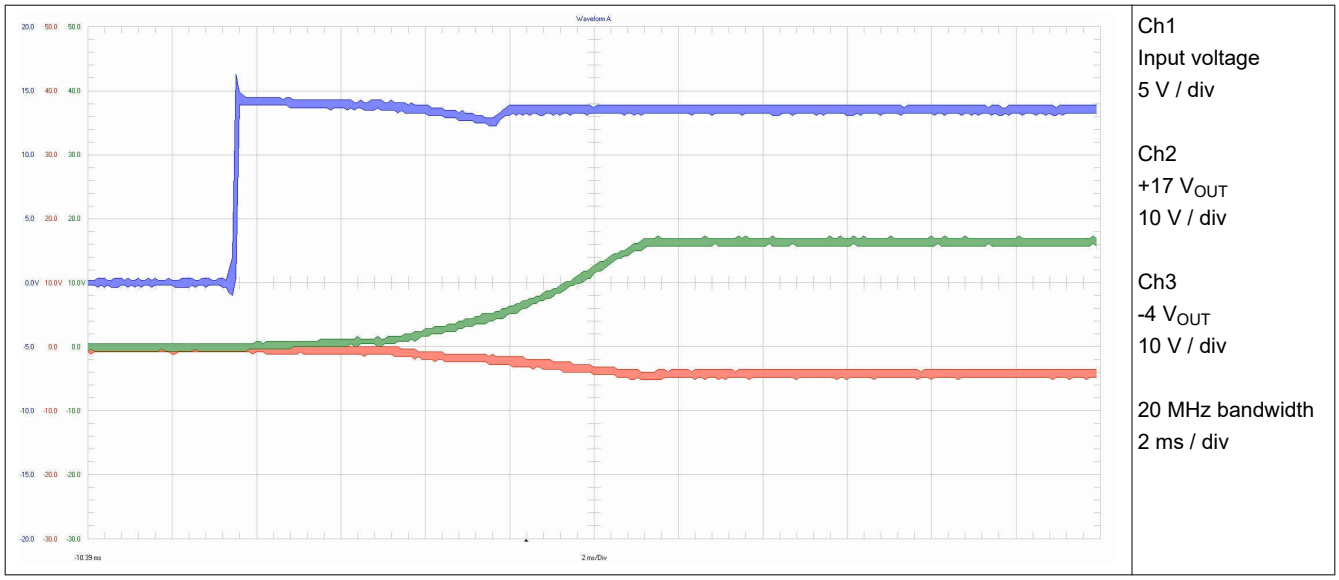


Figure 3-8. Start-up Channel U

3.5 Shutdown Sequence

Shutdown behavior of channel U is shown in the following figure.

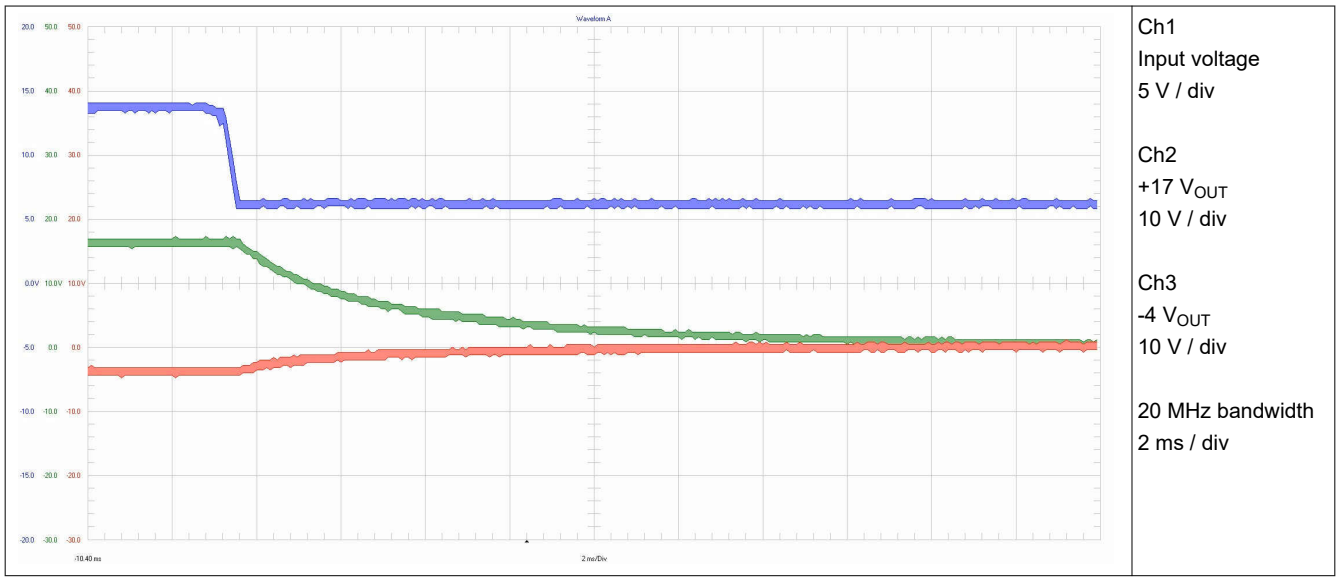


Figure 3-9. Shutdown Channel U

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