Synchronous Inverting Buck-Boost Converter Reference Design for Communications Equipment

Description

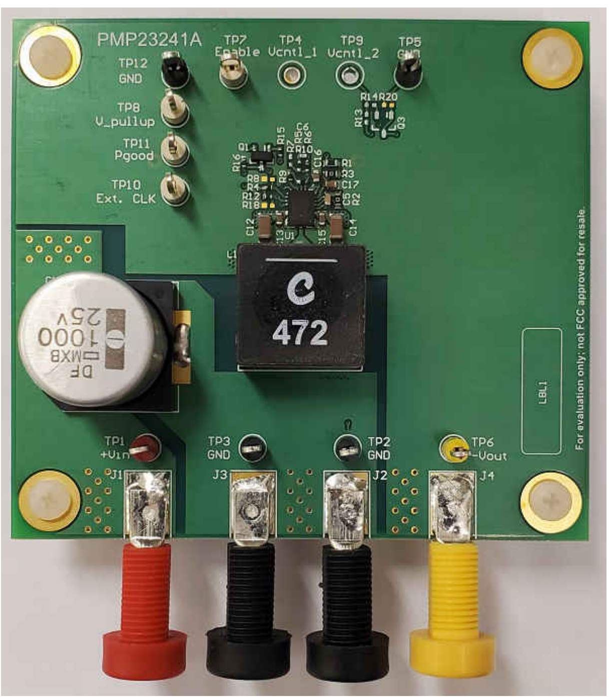
This reference design utilizes the LM61495 synchronous buck regulator, with internal top and bottom FETs, which is configured as a synchronous inverting buck-boost converter. The design generates an output of –8 V, capable of delivering 2.7-A continuous (4-A peak) of current to the load, from a +12 V, ±10% input. The design is built on the PMP23241A PCB, which is a 4-layer board with 1-oz copper for each of the four layers. The board is 76.2 mm × 68.6 mm. The actual design size is approximately 17.0 mm × 30.5 mm, *excluding* the input bulk capacitor, C1.

Features

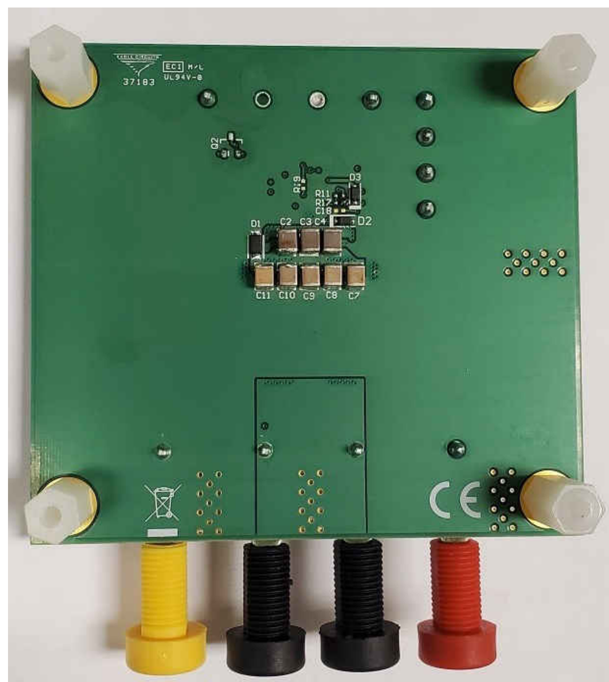
- Very small design size
- Regulator includes integrated FETs
- High efficiency
- Regulator features spread-spectrum switching (dithering) for improved EMI performance
- Converter generates a negative output voltage from a positive input voltage

Applications

- Active antenna system mMIMO (AAS)
- Macro remote radio unit (RRU)



Top of Board



Bottom of Board

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
V_{IN}	12 VDC ±10%
V_{OUT}	–8 VDC
I_{OUT}	2.7-A continuous (4-A peak)
F_{SW}	400-kHz nominal

1.2 Required Equipment

- Power supplies (one to provide the main converter power)
- Electronic Load (isolated or floating)
- DMMs
- Oscilloscope

1.3 Considerations

All voltage measurements were made relative to the 0-V common *GND*. When taking measurements, make sure to connect the GND clips of the oscilloscope to the GND (that is, 0-V) connection. Do *not* connect the oscilloscope GND clips to the –V_{OUT} node. Though this –V_{OUT} is the reference for the GND pins of the regulator IC, the output is no longer considered 0-V common GND.

In the inverting buck-boost topology, the voltage potential between the *VIN* and *GND* pins of the converter or regulator is the sum of the magnitudes of V_{IN} and V_{OUT} voltages. For example, with a nominal input voltage of +12 V, the total voltage potential exhibited by the LM61495 is: |+12 V| + |–8 V| = 20 V. The LM61495 has a maximum recommended supply voltage of 36 V. Therefore, do *not* apply an input voltage greater than 28 V_{IN} to the converter, preferably lower, to provide an extra buffer to accommodate for switching voltage spikes.

2 Testing and Results

2.1 Efficiency Graphs

Figure 2-1 shows the converter efficiency for a 12-V input and –8-V output with the load current being swept from 0.3 A to 4 A.

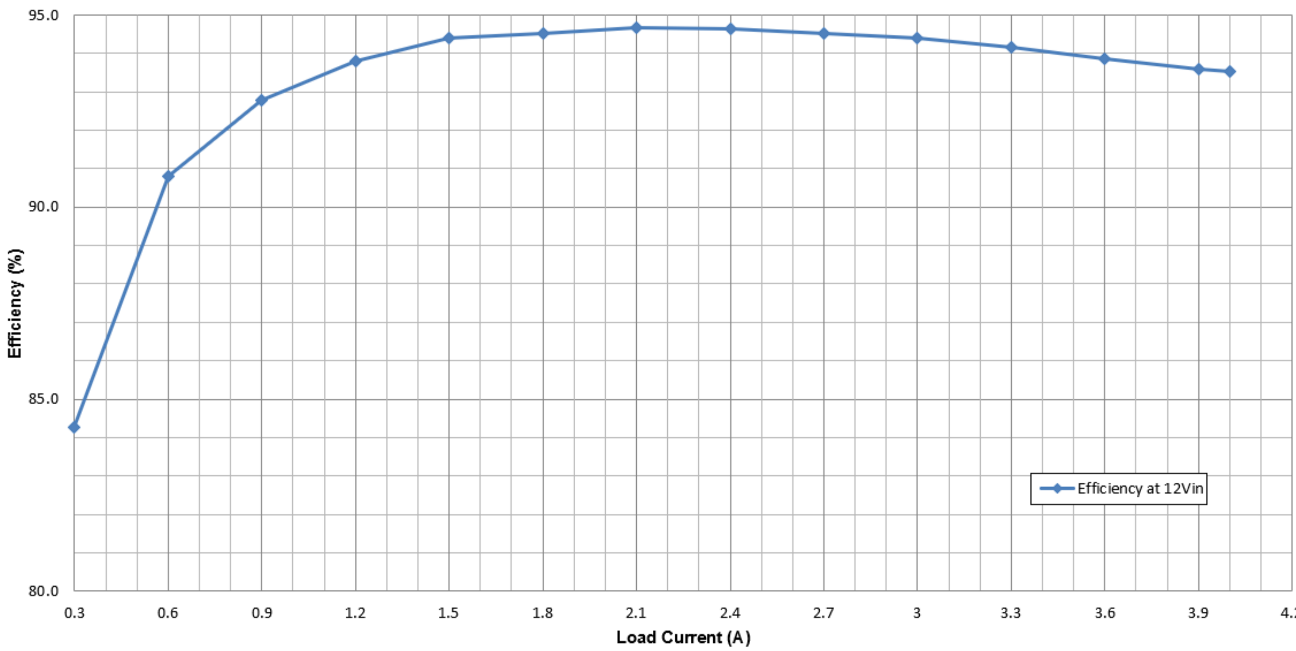


Figure 2-1. Efficiency Graph

2.2 Efficiency Data

Table 2-1 shows the efficiency data for –8-V outputs with a 12-V input.

Table 2-1. Efficiency Data 12-V input, –8-V Output

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	P_{loss} (W)	Efficiency (%)
12	0.035	–7.955	0	0.4200	0.0000	0.4200	0.0
12	0.236	–7.9545	0.3	2.8320	2.3864	0.4457	84.3
12	0.438	–7.9541	0.6	5.2560	4.7725	0.4835	90.8
12	0.643	–7.9535	0.9	7.7160	7.1582	0.5579	92.8
12	0.848	–7.953	1.2	10.1760	9.5436	0.6324	93.8
12	1.053	–7.9524	1.5	12.6360	11.9286	0.7074	94.4
12	1.262	–7.9517	1.8	15.1440	14.3131	0.8309	94.5
12	1.47	–7.9508	2.1	17.6400	16.6967	0.9433	94.7
12	1.68	–7.95	2.4	20.1600	19.0800	1.0800	94.6
12	1.892	–7.9489	2.7	22.7040	21.4620	1.2420	94.5
12	2.105	–7.9477	3	25.2600	23.8431	1.4169	94.4
12	2.321	–7.9464	3.3	27.8520	26.2231	1.6289	94.2
12	2.539	–7.9446	3.6	30.4680	28.6006	1.8674	93.9
12	2.758	–7.943	3.9	33.0960	30.9777	2.1183	93.6
12	2.831	–7.9428	4	33.9720	31.7712	2.2008	93.5

2.3 Thermal Images

The thermal images in Figure 2-2 and Figure 2-3 show operation at 12-V input and –8-V output at 2.7-A and 4-A loads, respectively, with no airflow. Thermals images were taken after the board had reached thermal equilibrium.

Figure 2-2. Top Side of Board, 12-V Input, –8-V Output at 2.7-A Load; $T_{ambient}$ ≈ 22°C

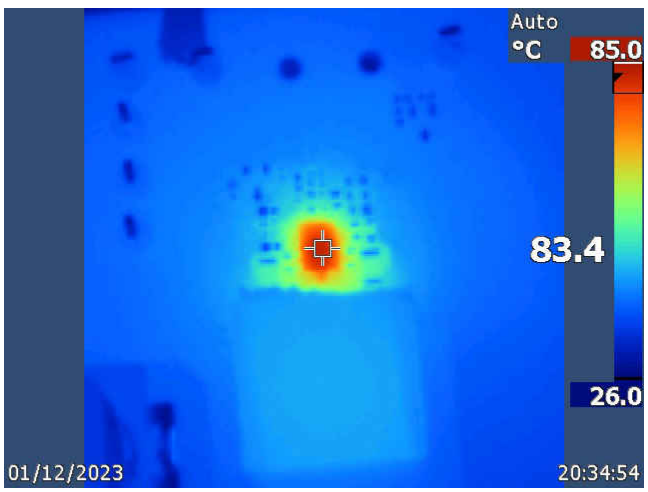


Figure 2-3. Bottom Side of Board, 12-V Input, –8-V Output at 4-A Load; $T_{ambient}$ ≈ 26°C

2.4 Dimensions

Figure 2-4 and Figure 2-5 show the top and bottom photos of the PMP23333 design which is built on the PMP23241A PCB. This board is a 4-layer board with 1-oz copper for each of the four layers. The board dimensions are 3.0 in × 2.7 in (76.2 mm × 68.58 mm). The actual design is approximately 0.67 in × 1.2 in (17.02 mm × 30.48 mm), *excluding* the input bulk capacitor, C1.

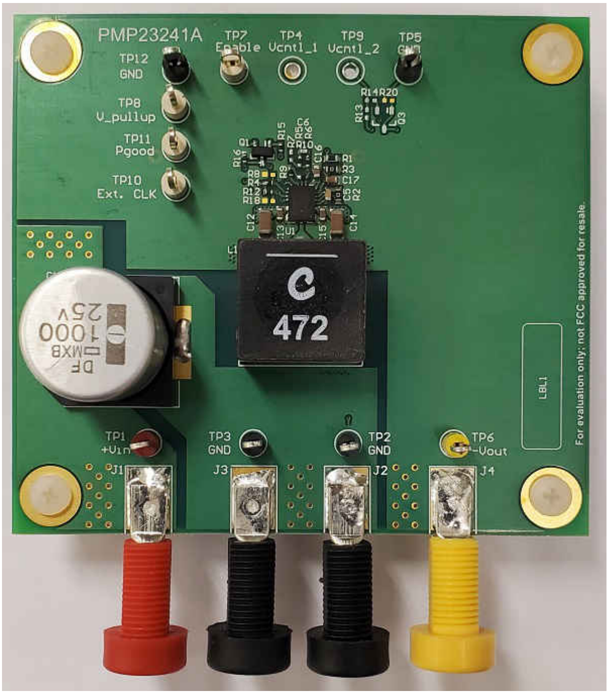


Figure 2-4. Top of PMP23333 Board

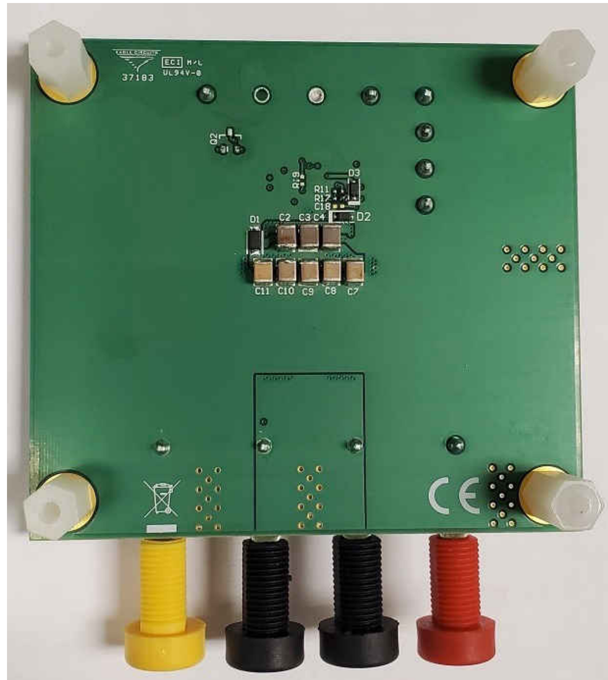


Figure 2-5. Bottom of PMP23333 Board

3 Waveforms

3.1 Switching

Figure 3-1 to Figure 3-3 show the switch node voltage of the converter at 12-V input and –0.8-V output at no load, 2.7-A load, and 4-A load conditions.

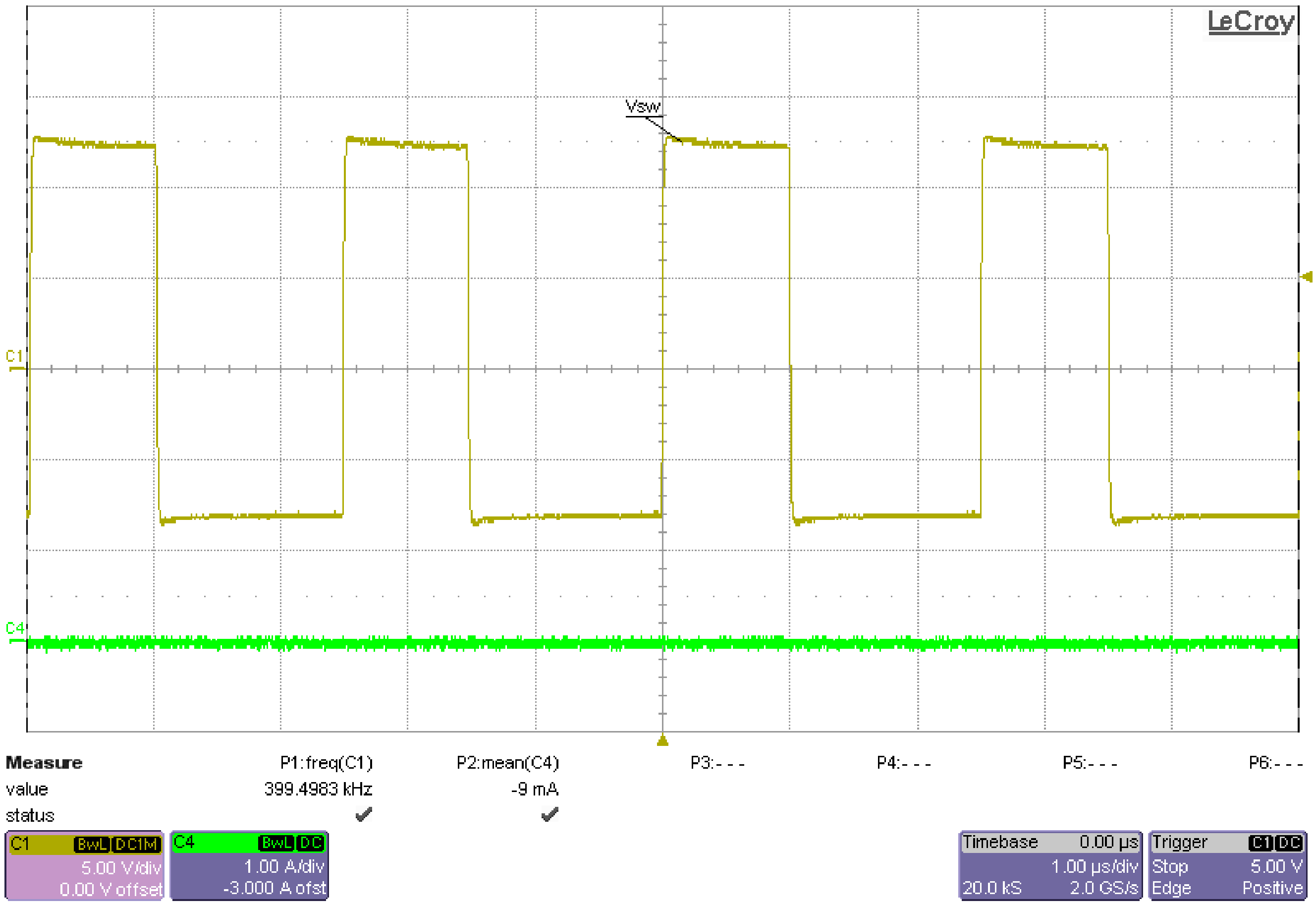


Figure 3-1. Switch Node Voltage, 12-V Input, –8-V Output, No Load

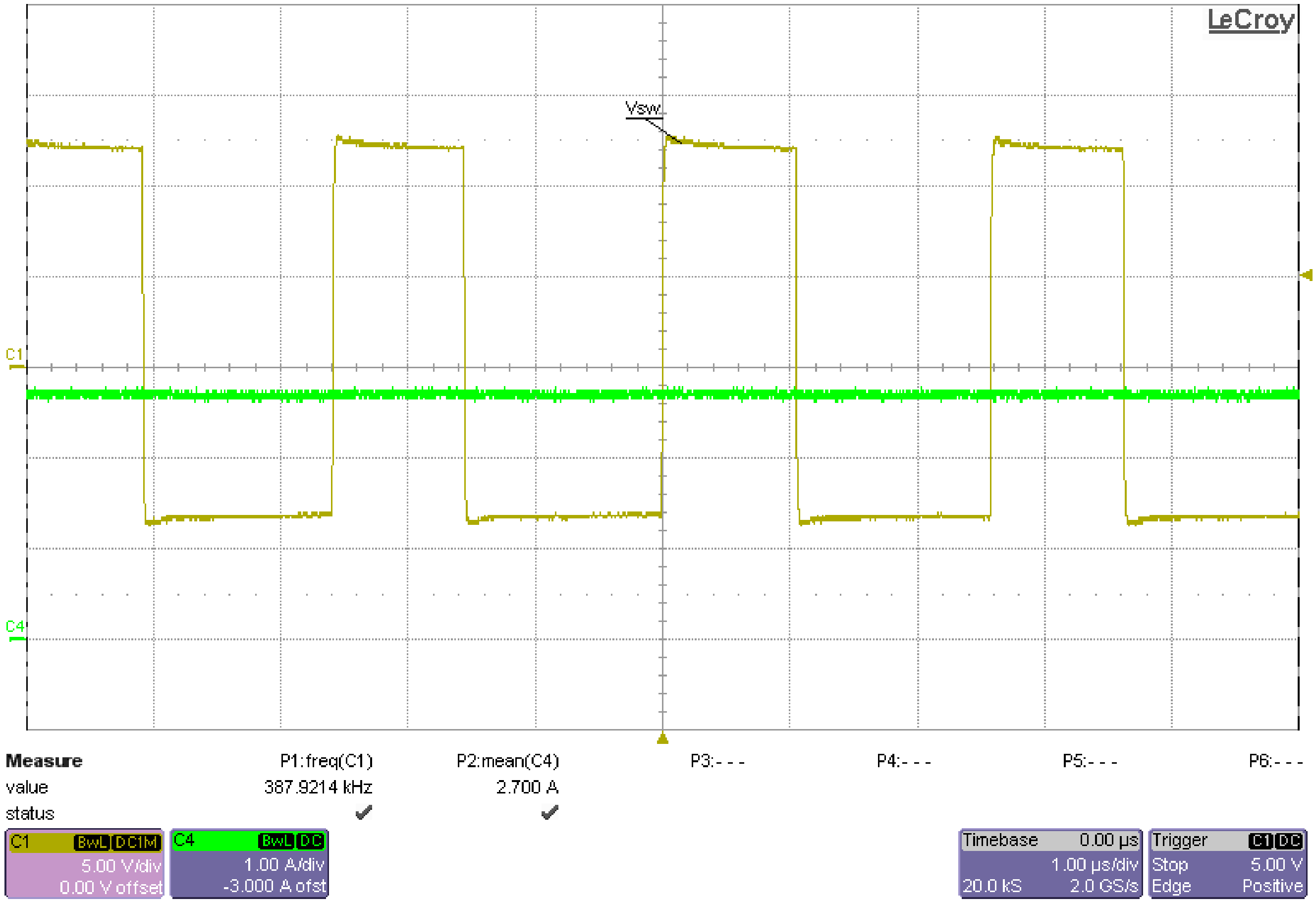


Figure 3-2. Switch Node Voltage, 12-V Input, –8-V Output, 2.7-A Load

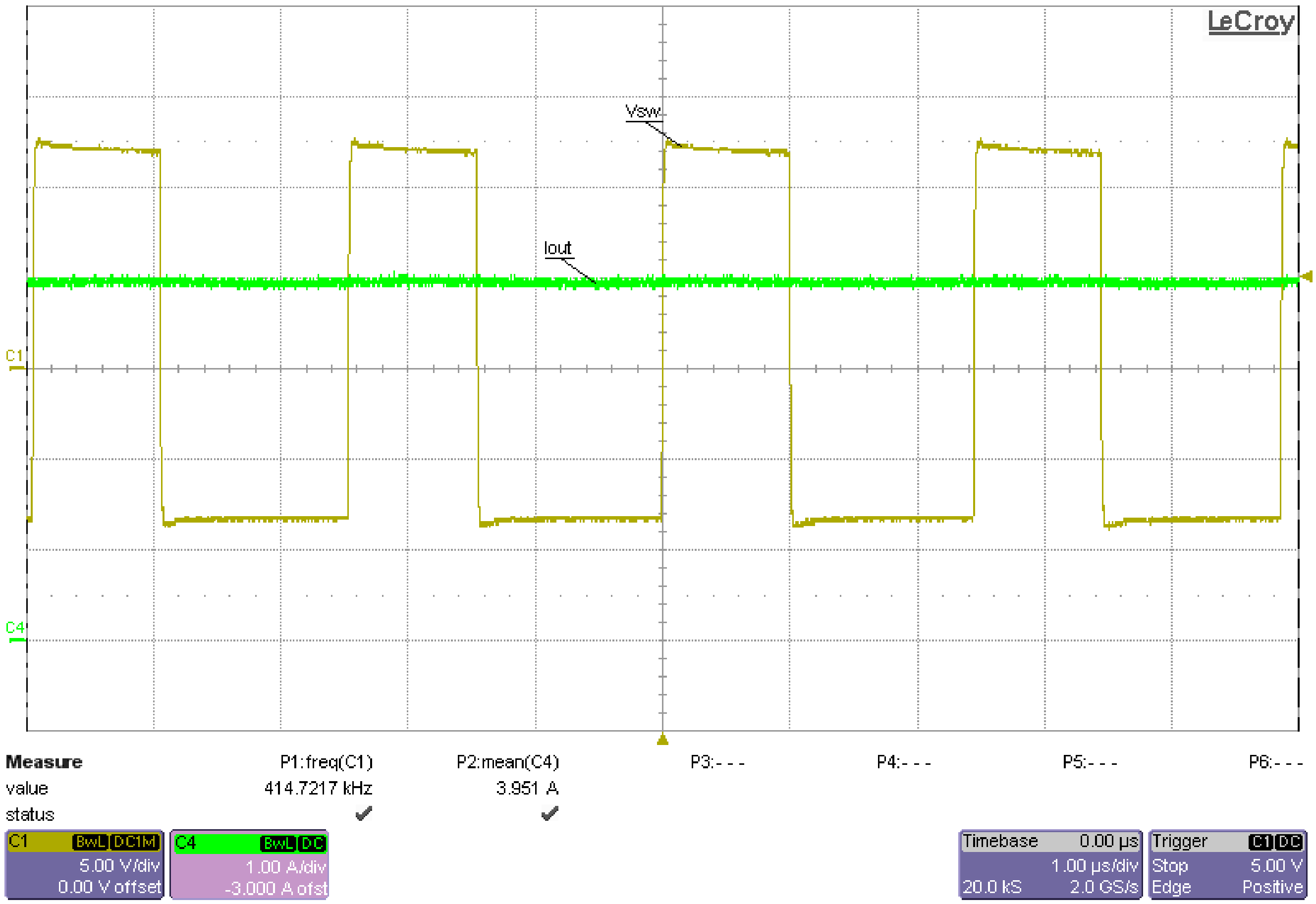


Figure 3-3. Switch Node Voltage, 12-V Input, –8-V Output, 4-A Load

3.2 Output Voltage Ripple

Figure 3-4 to Figure 3-6 show the output voltage ripple waveforms. The waveforms were captured at 12-V input, –0.8-V output at no load, 2.7-A load, and 4-A load conditions.

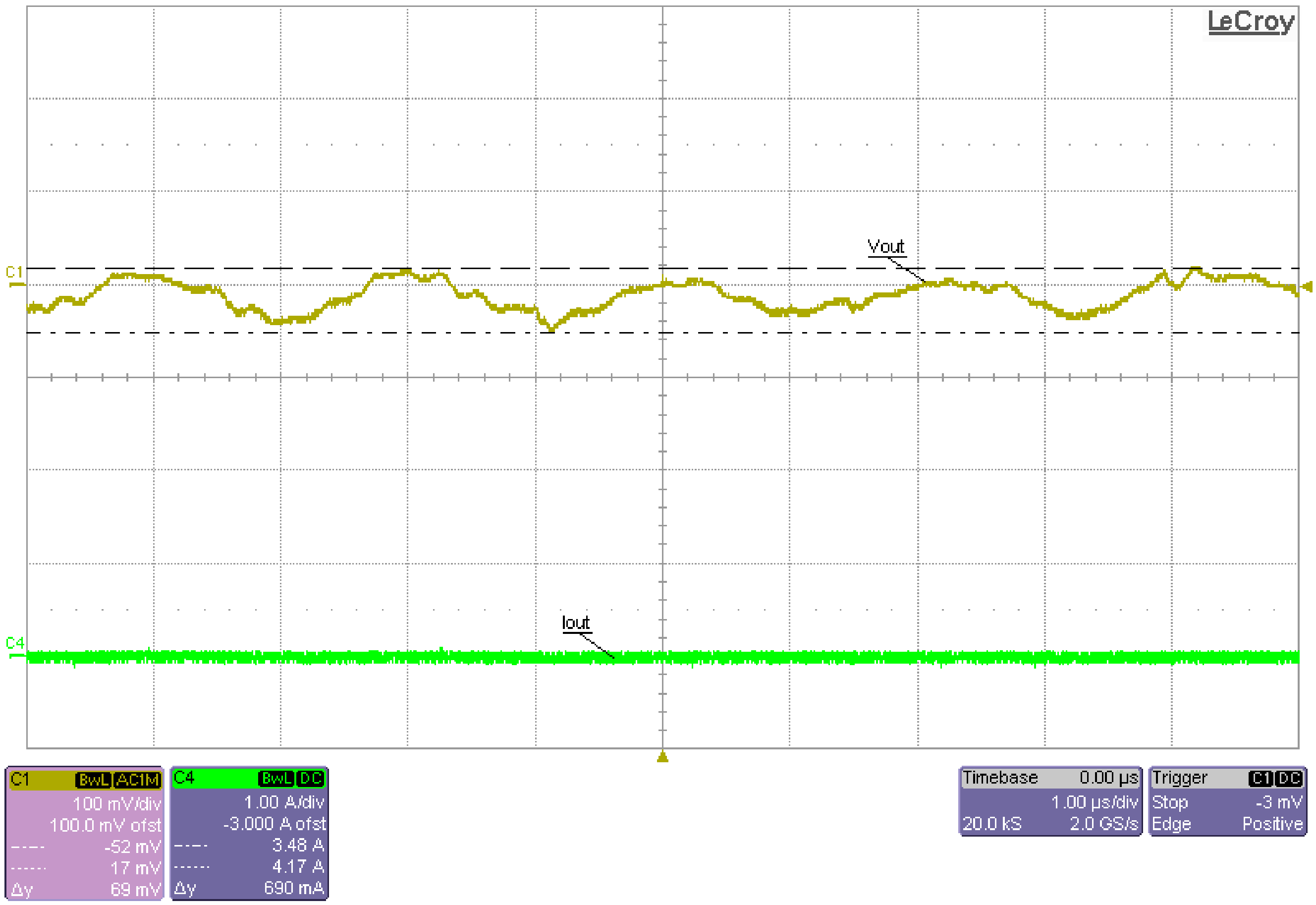


Figure 3-4. Output Voltage Ripple, 12-V Input, –8-V Output, No Load

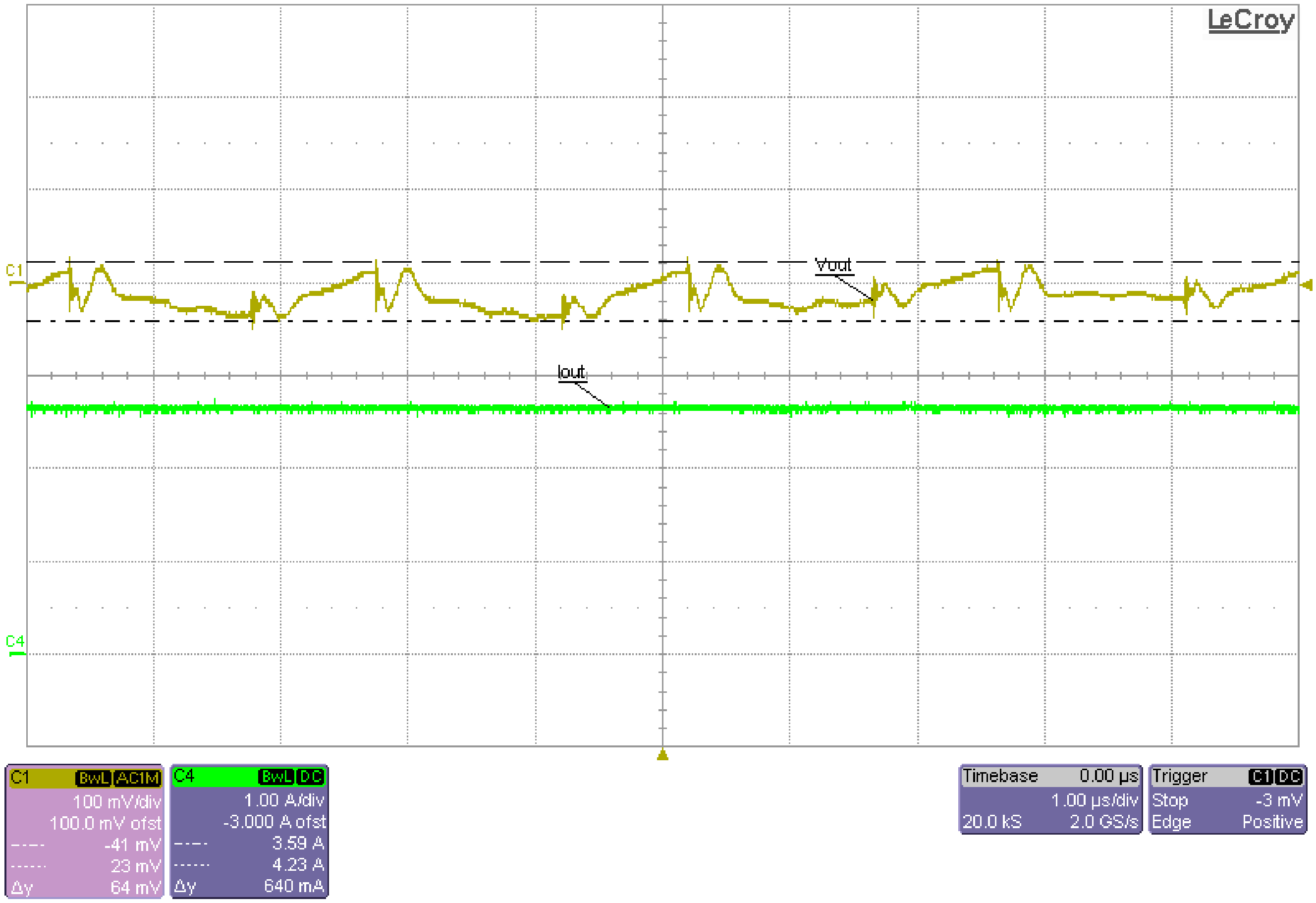


Figure 3-5. Output Voltage Ripple, 12-V Input, –8-V Output, 2.7-A Load

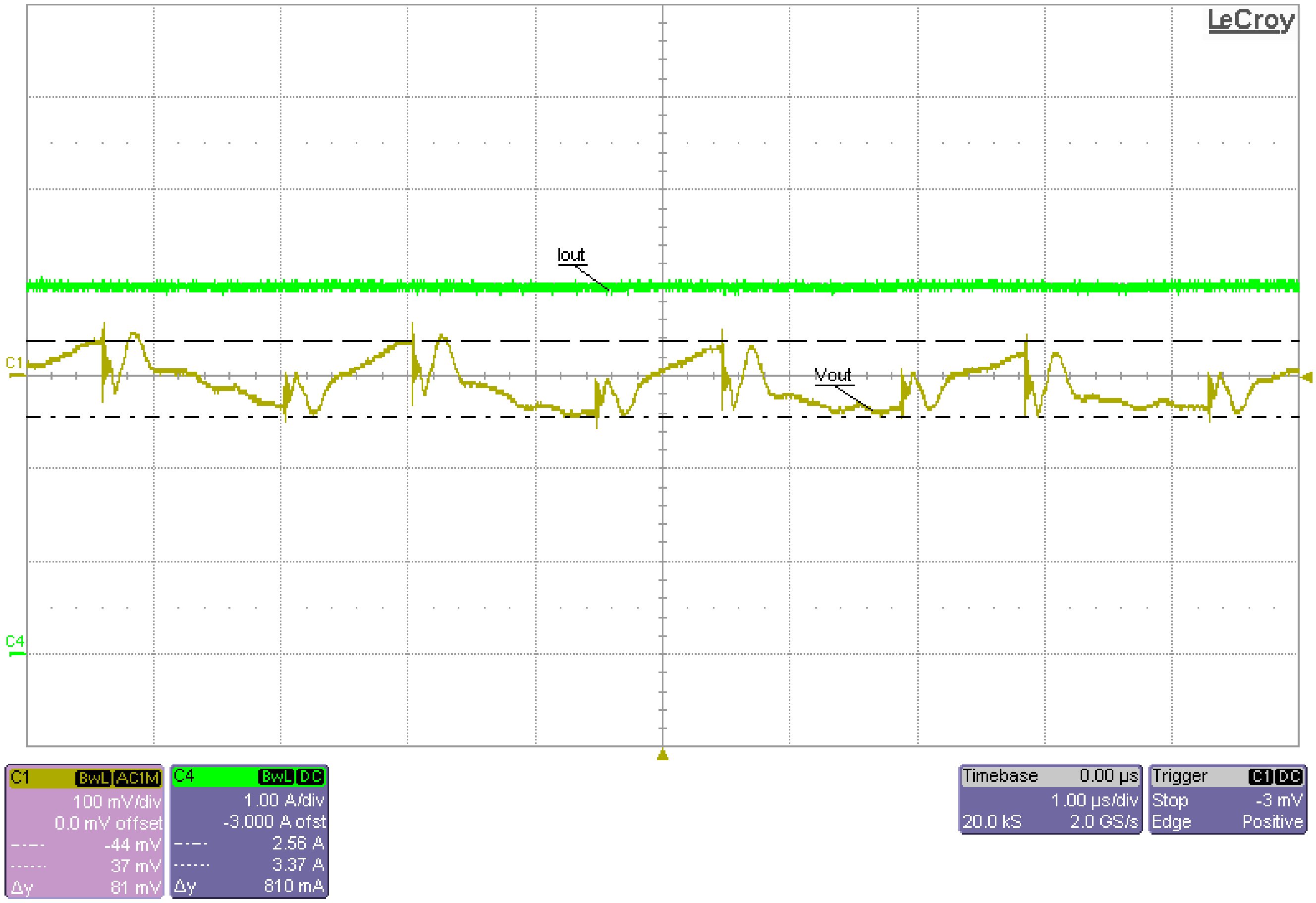


Figure 3-6. Output Voltage Ripple, 12-V Input, –8-V Output, 4-A Load

3.3 Load Transient

Figure 3-7 shows the load transient response of the converter at 12-V input and –0.8-V output undergoing a 1-A to 3-A load step.

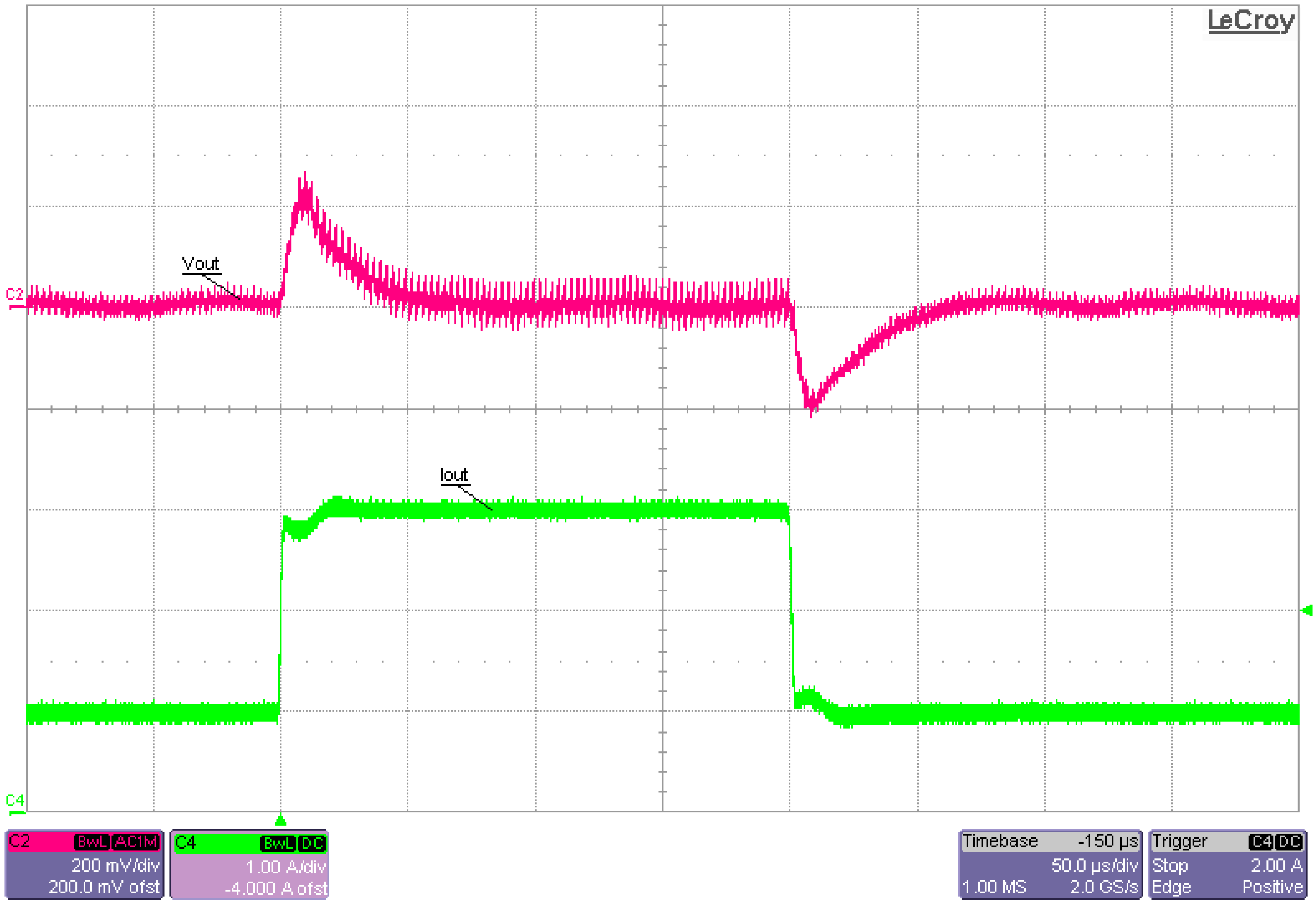


Figure 3-7. Load Transient Response, 12-V Input, –8-V Output, 1-A to 3-A Load Step

3.4 Start-Up

Figure 3-8 to Figure 3-11 show the output voltage start-up waveforms at 12-V input and –8-V output with the converter starting up into no load and into 2.7-A constant-current load using the electronic load. Two methods of enabling the converter were exercised and captured: one where the input voltage is already turned *ON* and the converter waits for the enable signal to go HIGH; the other where the enable signal is tied to V_{IN} and the converter waits for the main power supply to be turned ON.

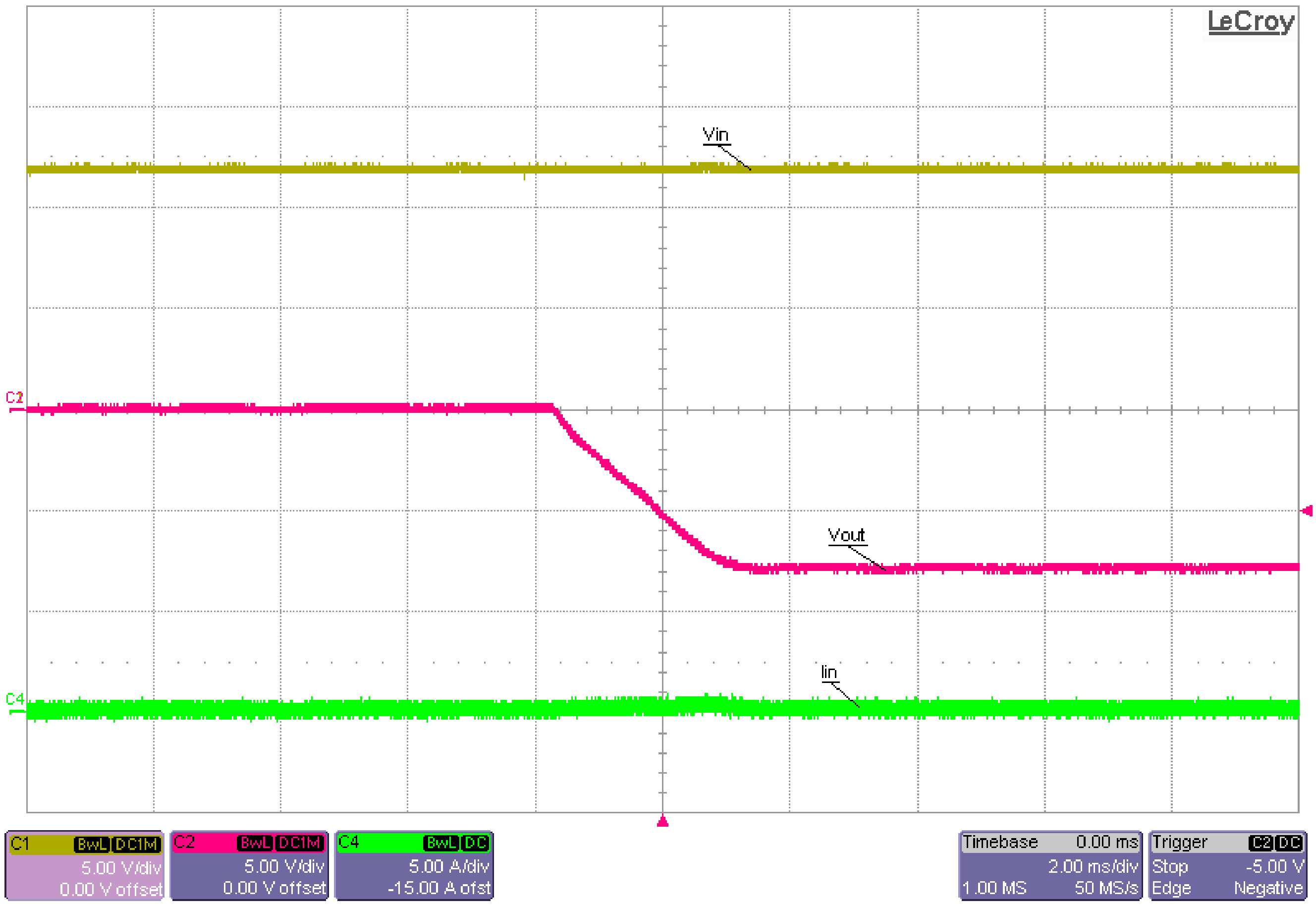


Figure 3-8. Start-Up Into No Load, 12-V Input, –8-V Output, Start-Up Initiated via the Enable Connection (input Supply Already Turned ON)

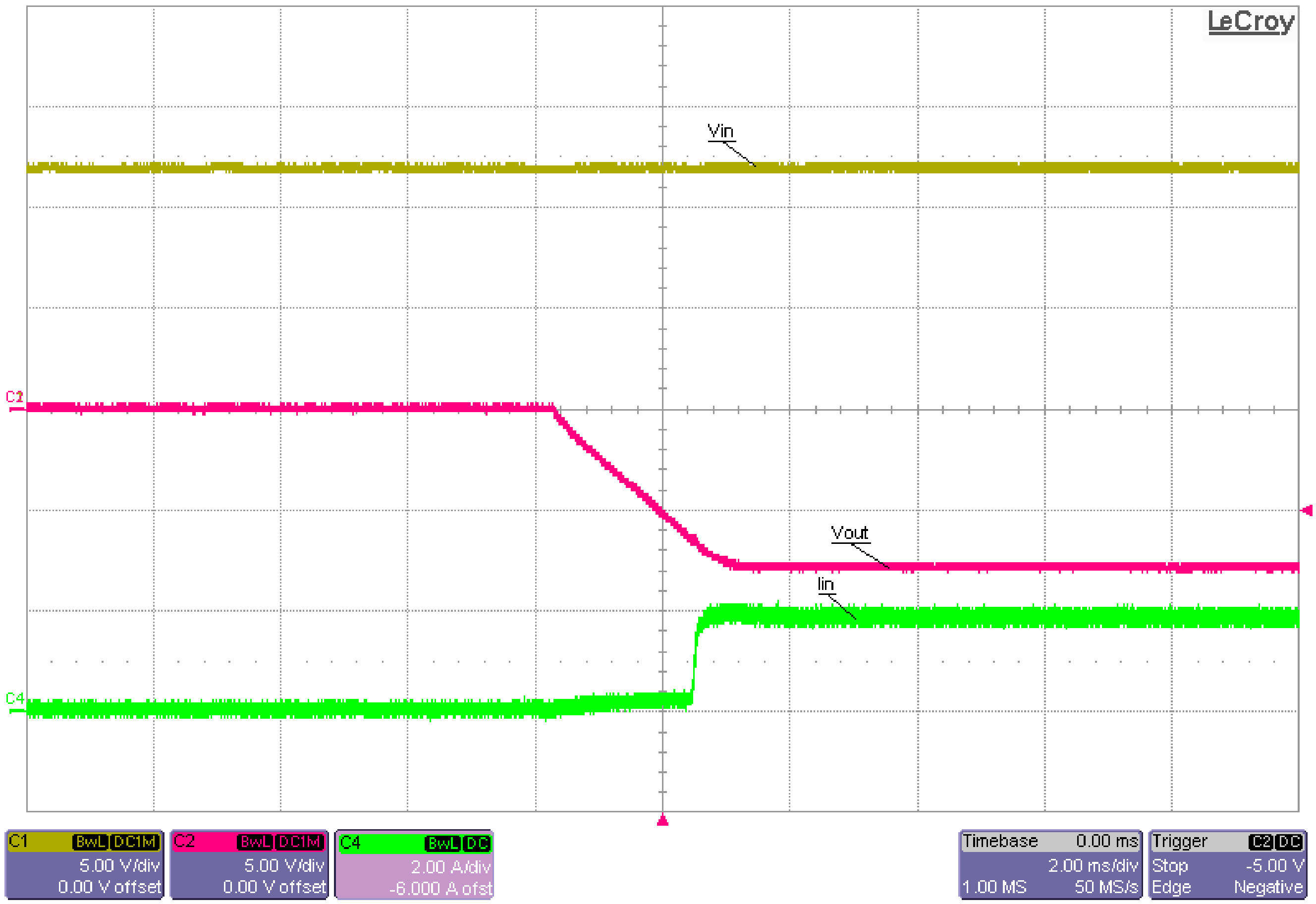


Figure 3-9. Start-Up Into 2.7-A Constant-Current Load, 12-V Input, –8-V Output Start-Up Initiated via the Enable Connection (input Supply Already Turned ON)

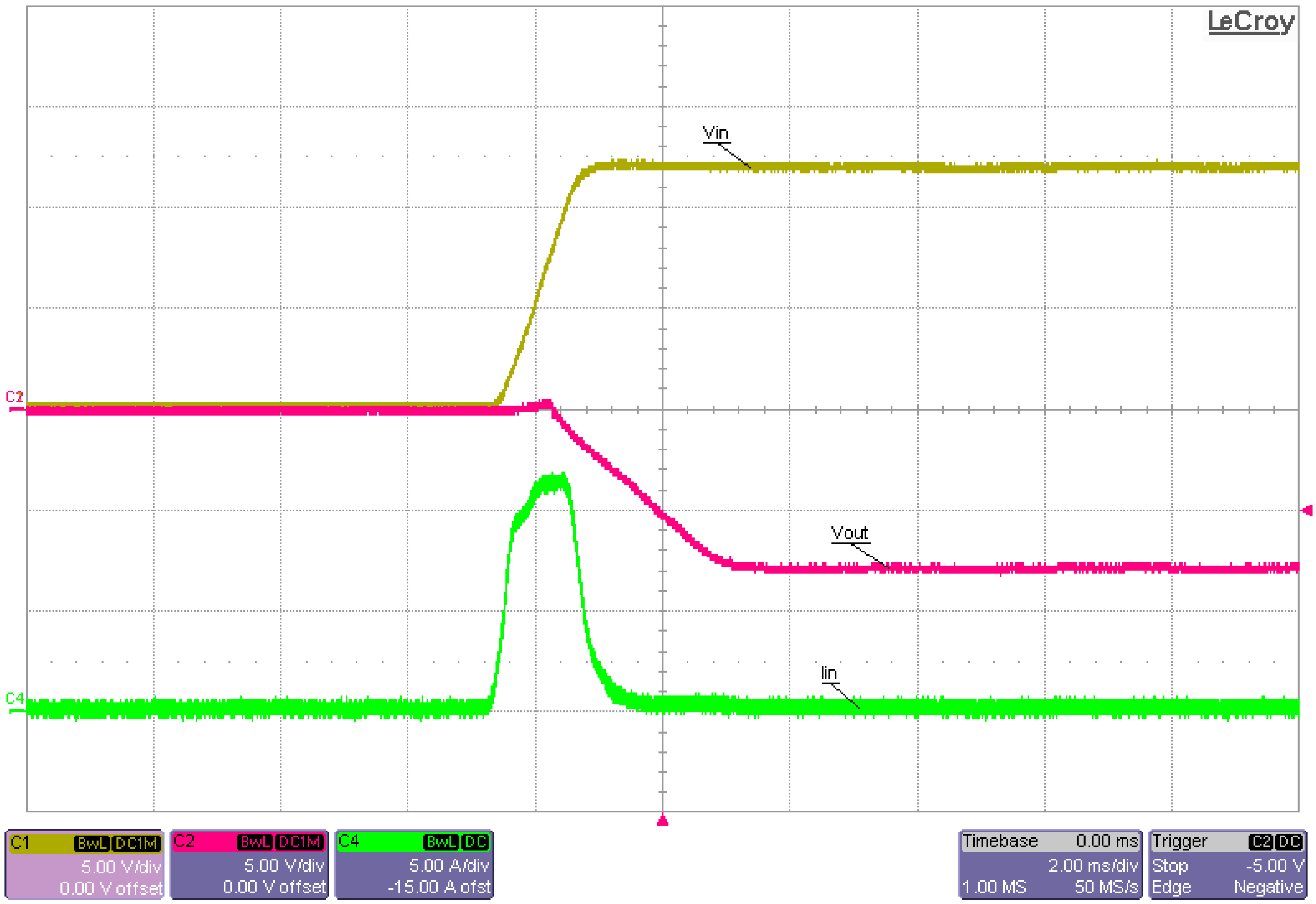


Figure 3-10. Start-Up Into No Load, 12-V Input, –8-V Output, Start-Up Initiated via Input Supply (Enable Signal Already Set HIGH)

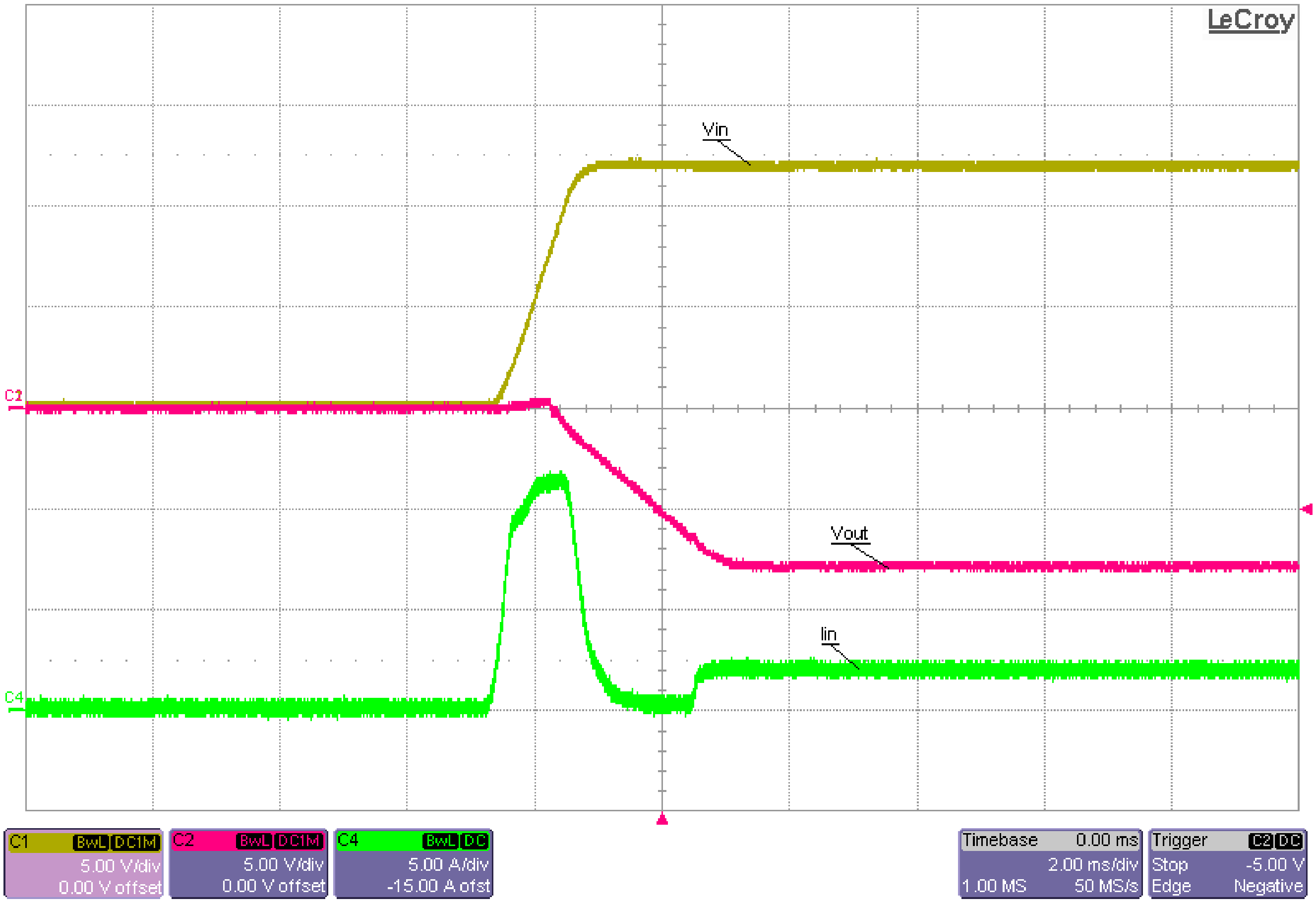


Figure 3-11. Start-Up Into 2.7-A Constant-Current Load, 12-V Input, –8-V Output, Start-Up Initiated via Input Supply (Enable Signal Already Set HIGH)

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