Test Report: PMP23193

50- to 150-V_{IN}, 28-V 5-A Synchronous Buck Converter Reference Design for 100-kRad Space Applications

Description

This reference design is a 28-V output, 5-A synchronous buck converter for space applications operating from a 50-V to 150-V input range. The TPS7H5001-SP PWM controller controls the power stage. The INA901-SP senses the inductor current and provides current feedback to the controller enabling both average current-mode control and output short-circuit protection. If these features are not needed, the INA901-SP can be removed and the TPS7H5001-SP can be operated with voltage-mode control. The adjustable dead time of the TPS7H5001-SP allows the timing of the switching MOSFETs to be optimized and results in over 94% efficiency with a 100-V input and over 96% efficiency with a 50-V input. A self-biasing circuit is included to power the control circuits directly from the output. If an external 12-V bias is provided, the self-biasing circuit can be removed, and results in higher efficiency.

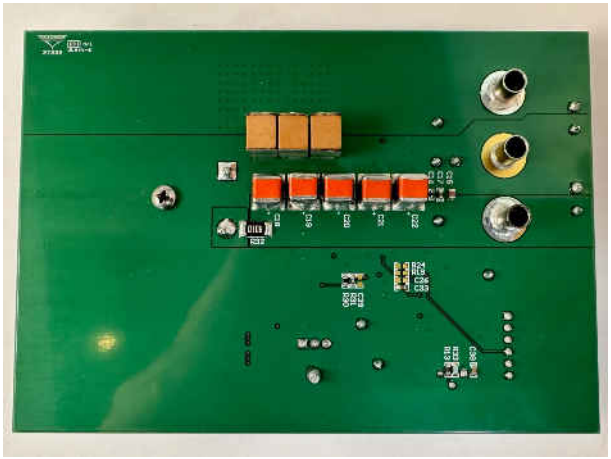
Features

- Radiation: TID 100-kRad (Si), SEL, SEB, SEGR immune up to 75 MeV-cm^2/mg
- Space-grade MOSFET based
- > 94% efficiency at 100 V V_{IN}
- Overcurrent protection
- Synchronizable
- Optional self-bias circuit (higher efficiency with external bias)

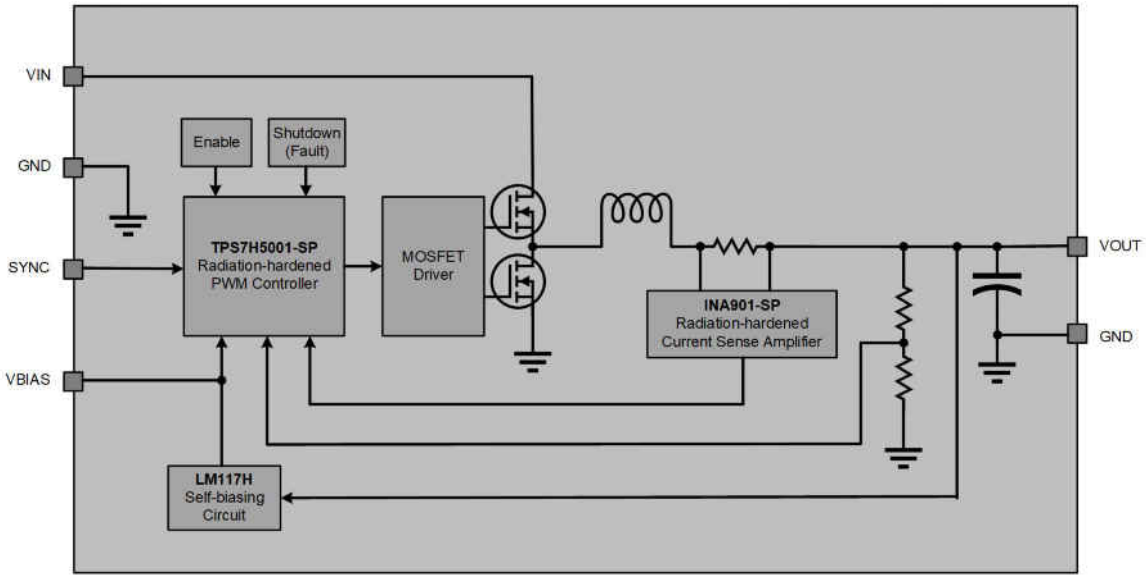
Applications

- Command and data handling (C and DH)
- Radar imaging payload

Top Photo



Bottom Photo



Block Diagram

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input Voltage Range	50 VDC–150 VDC
Output Voltage	28 V
Maximum Load Current (thermally limited)(1)	5 A
Switching Frequency	100 kHz

(1) Load currents above 5 A are permissible, but verify the thermal performance

1.2 Input and Output Signals

Table 1-2. Signals and Functions

Signal	Function
GND	Return path for VIN and VOUT.
SYNC	External synchronization signal. Refer to the *TPS7H500x-SP Radiation-Hardness-Assured 2-MHz Current Mode PWM Controllers* data sheet for signal requirements.
VBIAS	Bias power for TPS7H5001. The LM117H self-bias circuit generates a 13.2-V rail to power internal circuitry. Alternatively, an external 12-V rail can be provided and the self-biasing circuit can then be removed.
VIN	Main power input. Operating range is 50 V to 150 V.
VOUT	Main 28-V power output. Designed to power loads up to 5 A.

2 Testing and Results

2.1 Efficiency Graphs

Efficiency and power loss are shown in the following figures.

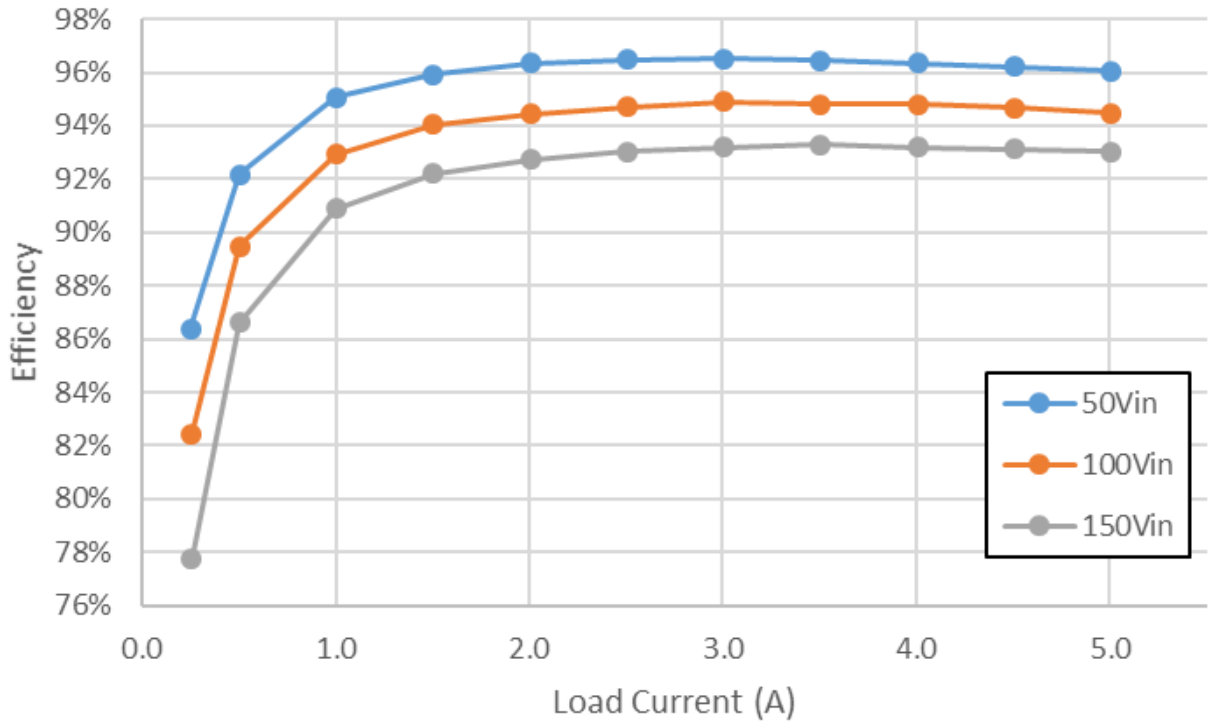


Figure 2-1. Efficiency Graph

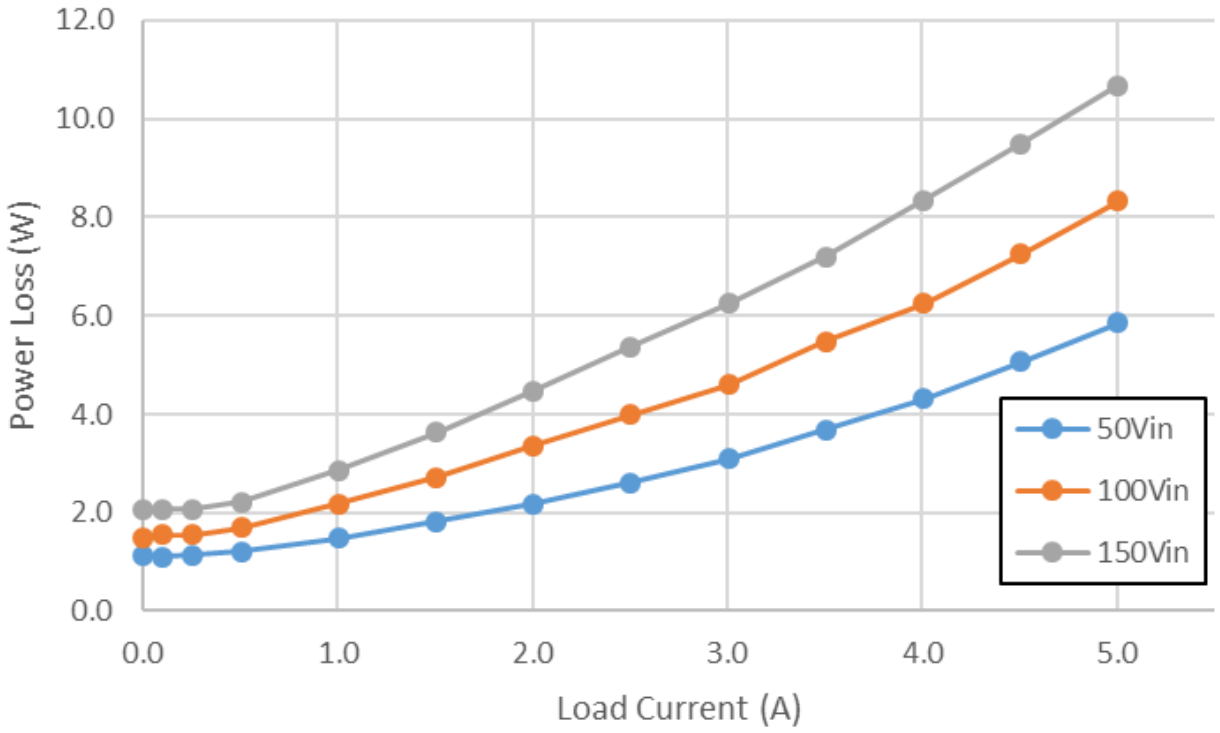


Figure 2-2. Power Loss Graph

2.2 Efficiency Data

Efficiency data is shown in the following tables.

Table 2-1. Efficiency Data for 50-V Input

I_{OUT} (A)	V_{OUT} (V)	V_{IN} (V)	I_{IN} (A)	P_{OUT} (W)	P_{IN} (W)	Loss (W)	Efficiency
0.000	28.49	49.99	0.0224	0.00	1.12	1.12	0.0%
0.103	28.49	49.98	0.0808	2.93	4.04	1.10	72.7%
0.253	28.49	49.96	0.167	7.21	8.34	1.14	86.4%
0.504	28.49	49.93	0.312	14.36	15.58	1.22	92.2%
1.003	28.50	49.87	0.603	28.59	30.07	1.49	95.1%
1.504	28.50	49.82	0.897	42.86	44.69	1.82	95.9%
2.005	28.50	49.76	1.192	57.14	59.31	2.17	96.3%
2.505	28.50	50.00	1.480	71.39	74.00	2.61	96.5%
3.005	28.50	49.94	1.777	85.64	88.74	3.10	96.5%
3.504	28.50	50.00	2.071	99.86	103.55	3.69	96.4%
4.005	28.50	49.94	2.372	114.14	118.46	4.32	96.4%
4.505	28.51	50.00	2.670	128.44	133.50	5.06	96.2%
5.004	28.51	49.94	2.974	142.66	148.52	5.86	96.1%

Table 2-2. Efficiency Data for 100-V Input

I_{OUT} (A)	V_{OUT} (V)	V_{IN} (V)	I_{IN} (A)	P_{OUT} (W)	P_{IN} (W)	Loss (W)	Efficiency
0.000	28.50	100.00	0.015	0.00	1.50	1.50	0.0%
0.103	28.50	99.98	0.0448	2.94	4.48	1.54	65.5%
0.254	28.50	100.02	0.0878	7.24	8.78	1.54	82.4%
0.504	28.50	100.01	0.161	14.36	16.05	1.69	89.5%
1.004	28.50	99.98	0.308	28.61	30.79	2.18	92.9%
1.504	28.50	99.95	0.456	42.86	45.58	2.71	94.0%
2.005	28.50	100.00	0.605	57.14	60.50	3.36	94.5%
2.505	28.50	99.97	0.754	71.39	75.38	3.98	94.7%
3.006	28.51	100.01	0.903	85.70	90.31	4.61	94.9%
3.504	28.51	99.98	1.054	99.90	105.38	5.48	94.8%
4.005	28.51	99.95	1.205	114.18	120.44	6.26	94.8%
4.505	28.51	99.92	1.358	128.44	135.69	7.25	94.7%
5.004	28.51	100.00	1.510	142.66	151.00	8.34	94.5%

Table 2-3. Efficiency Data for 150-V Input

I_{OUT} (A)	V_{OUT} (V)	V_{IN} (V)	I_{IN} (A)	P_{OUT} (W)	P_{IN} (W)	Loss (W)	Efficiency
0.000	28.51	149.99	0.0137	0.00	2.05	2.05	0.0%
0.103	28.51	149.99	0.0334	2.94	5.01	2.07	58.6%
0.254	28.51	149.98	0.0621	7.24	9.31	2.07	77.8%
0.504	28.51	149.97	0.1106	14.37	16.59	2.22	86.6%
1.004	28.51	149.96	0.210	28.62	31.49	2.87	90.9%
1.504	28.51	150.01	0.310	42.88	46.50	3.62	92.2%
2.005	28.51	149.98	0.411	57.16	61.64	4.48	92.7%

Table 2-3. Efficiency Data for 150-V Input (continued)

I_{OUT} (A)	V_{OUT} (V)	V_{IN} (V)	I_{IN} (A)	P_{OUT} (W)	P_{IN} (W)	Loss (W)	Efficiency
2.505	28.51	149.97	0.512	71.42	76.78	5.37	93.0%
3.005	28.51	149.95	0.613	85.67	91.92	6.25	93.2%
3.504	28.51	150.00	0.714	99.90	107.10	7.20	93.3%
4.005	28.51	149.98	0.817	114.18	122.53	8.35	93.2%
4.505	28.52	149.97	0.920	128.48	137.97	9.49	93.1%
5.004	28.52	149.94	1.023	142.71	153.39	10.67	93.0%

2.3 Thermal Images

All images captured with the unit under test (UUT) enclosed in a 30 m × 45 cm × 20 cm Plexiglas box, 25ºC ambient, after a 30-minute warm up, and no forced airflow. The unit was tested with a 5-A load and at various input voltages. Black electrical tap was placed on top of U for increased emissivity.

Reference Designator	Description	50 V_{IN} Maximum Temperature (°C)	100 V_{IN} Maximum Temperature (°C)	150 V_{IN} Maximum Temperature (°C)
Q1 and Q2	High-side FETs	69.8	92.1	116.4
Q3 and Q4	Low-side FETs	63.7	82.9	82.9
U2	TPS7H5001-SP controller	42.5	49.9	56.1
U1	MOSFET driver	53.5	64.5	75.0
L1	Output inductor	43.4	52.5	60.1
U3	INA901-SP current sense amplifier	45.7	56.5	66.2
U4	LM117H linear regulator	60.6	65.6	69.1

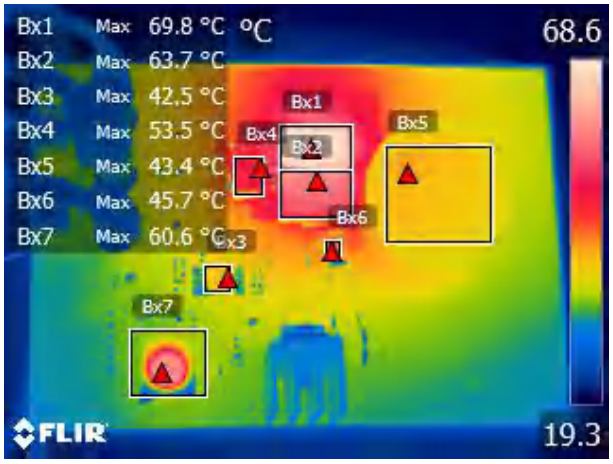


Figure 2-3. Thermal Image, 50 V_{IN}

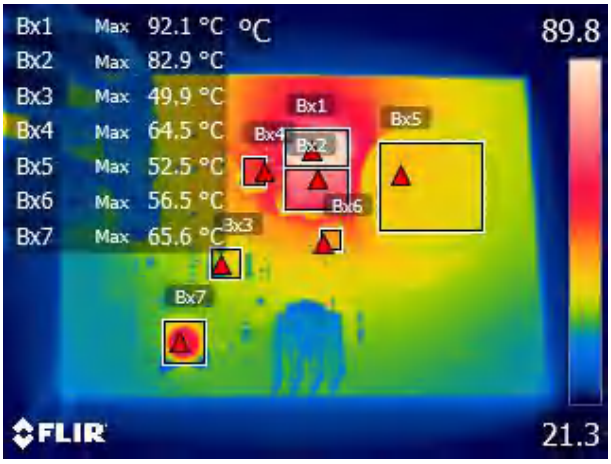


Figure 2-4. Thermal Image, 100 V_{IN}

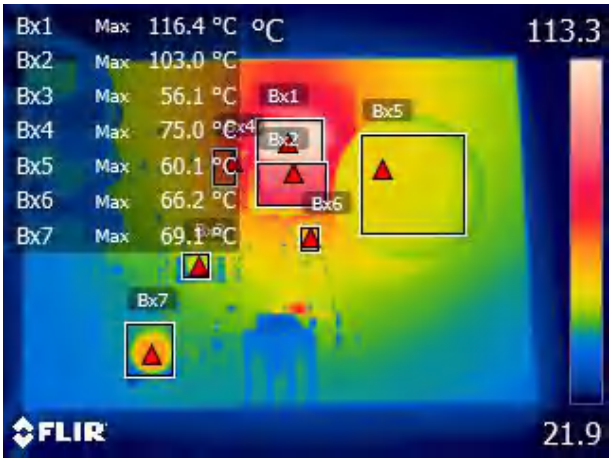


Figure 2-5. Thermal Image, 150 V_{IN}

2.4 Bode Plots

The feedback loop frequency response was measured with a 5-A load at different input voltage conditions and is shown in the following figures.

Table 2-4. Feedback Loop Frequency Response

Condition	Unity Gain Bandwidth (kHz)	Phase Margin (°)	Gain Margin (dB)
50 V_{IN}, 5-A load	6.9	80	22.5
100 V_{IN}, 5-A load	15.6	69	17.7
150 V_{IN}, 5-A load	27	46	9.4

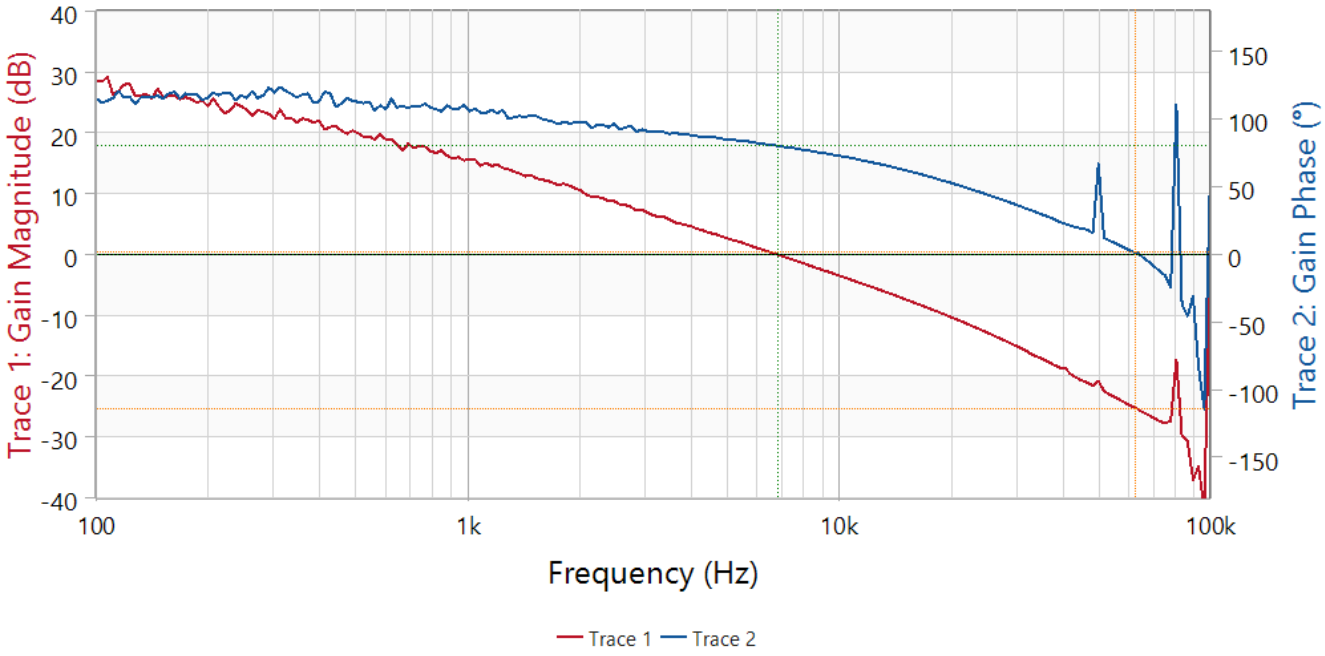


Figure 2-6. Bode Plot, 50 V_{IN}, 5-A Load

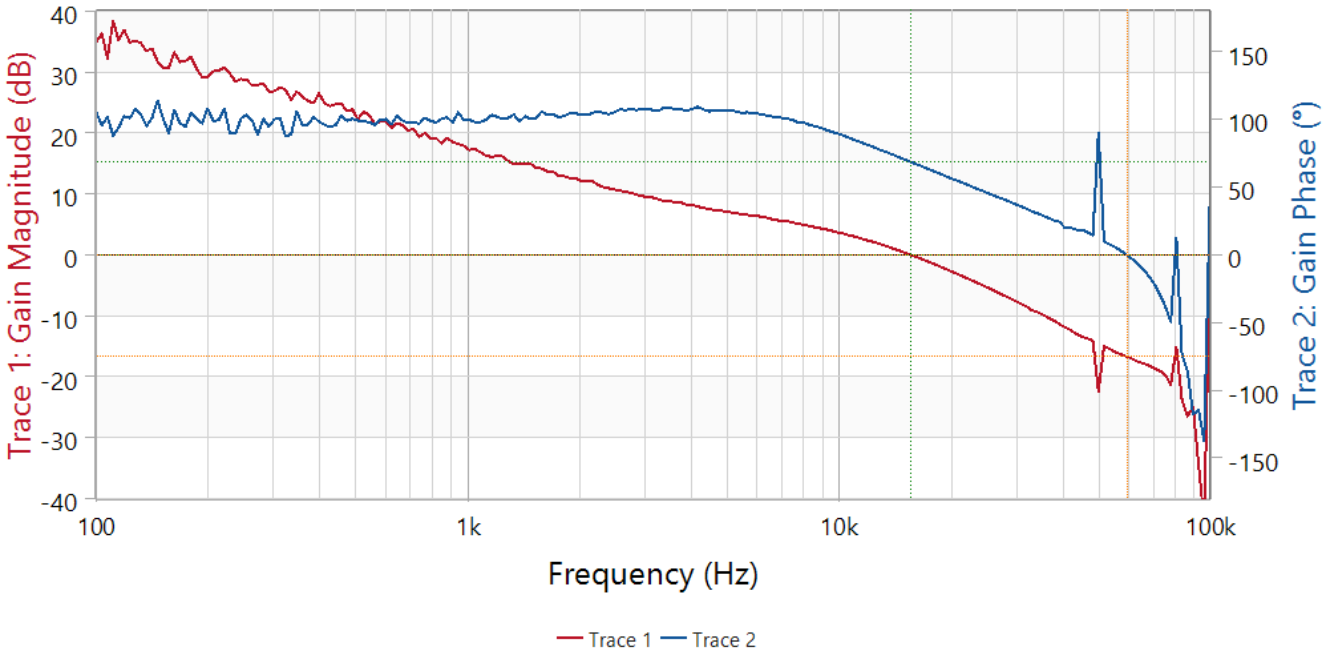


Figure 2-7. Bode Plot, 100 V_{IN}, 5-A Load

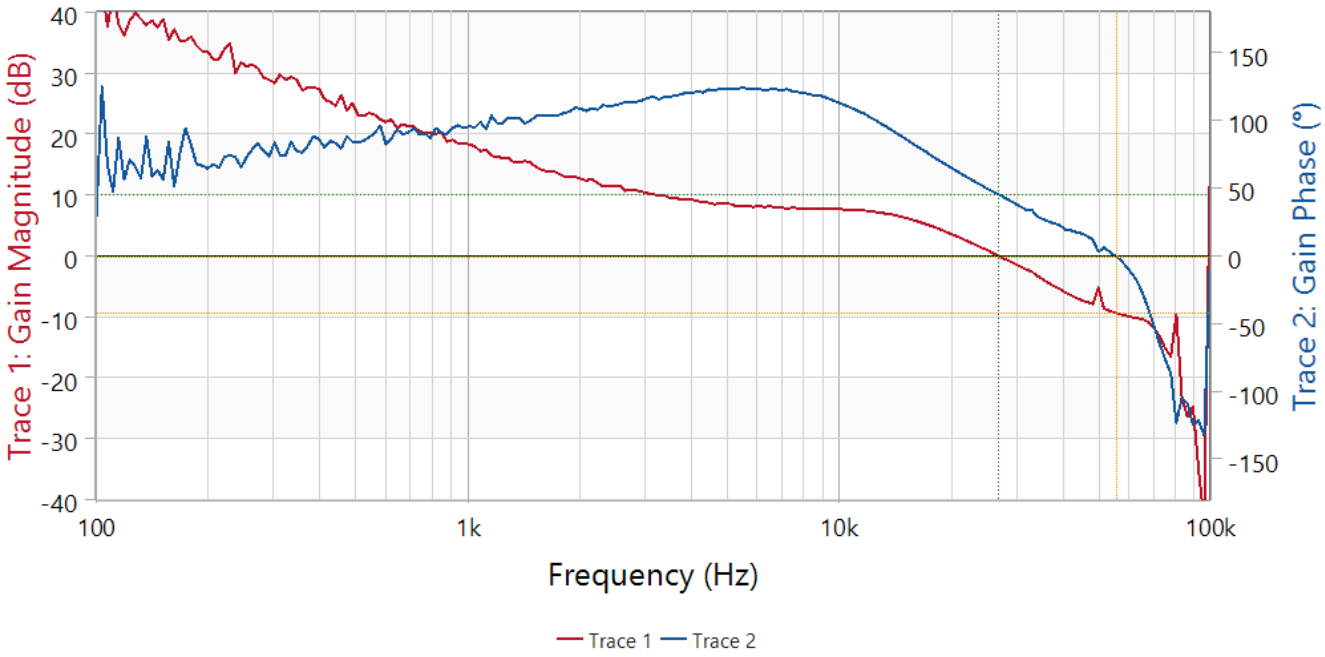


Figure 2-8. Bode Plot, 150 V_{IN}, 5-A Load

3 Waveforms

3.1 Switching

The maximum voltage stress on the drain of the low-side FETs (Q3 and Q4) occurs with 150-V input and 5-A load. This was recorded as 178 Vpk, as shown in the following figure.

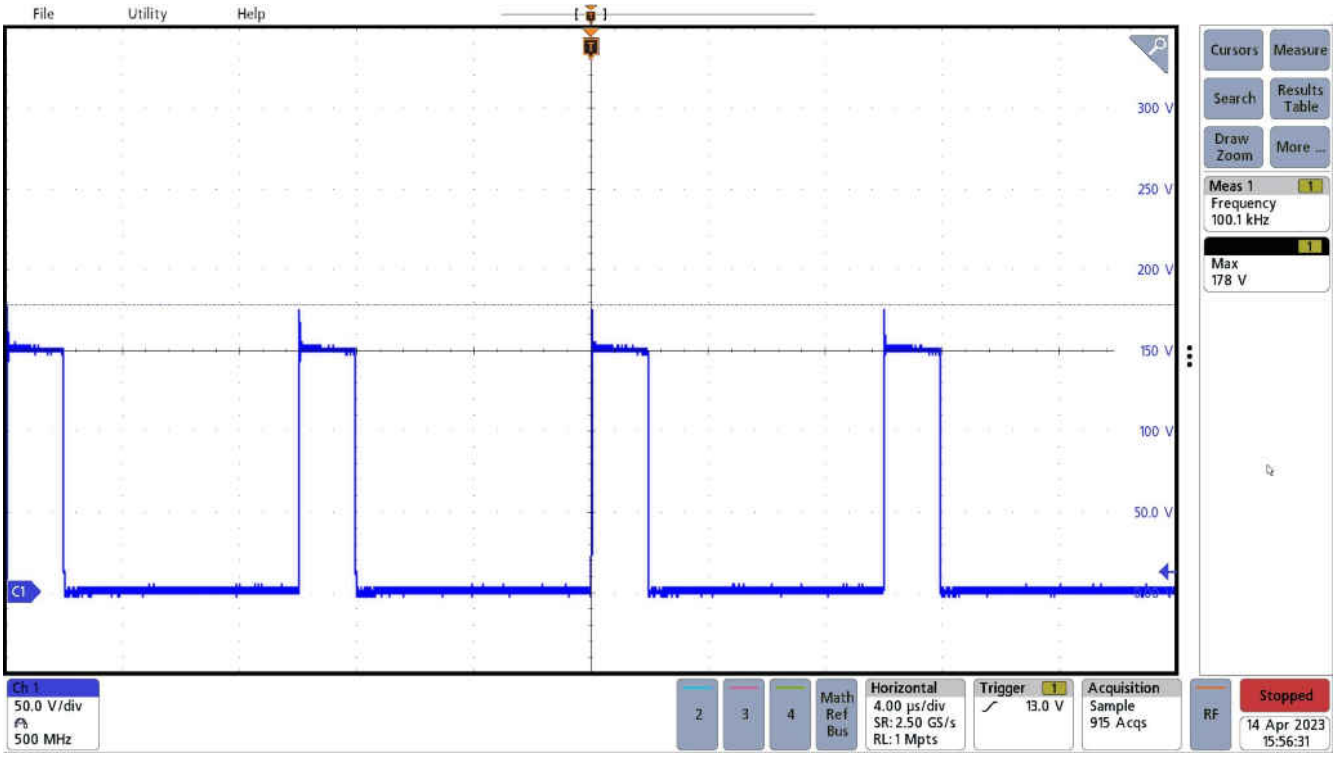


Figure 3-1. Maximum Voltage Stress

3.2 Output Voltage Ripple

The output ripple voltage was measured using a tip and barrel technique across output capacitor C17. The following figures show the output ripple with a 5-A load at different input voltages.

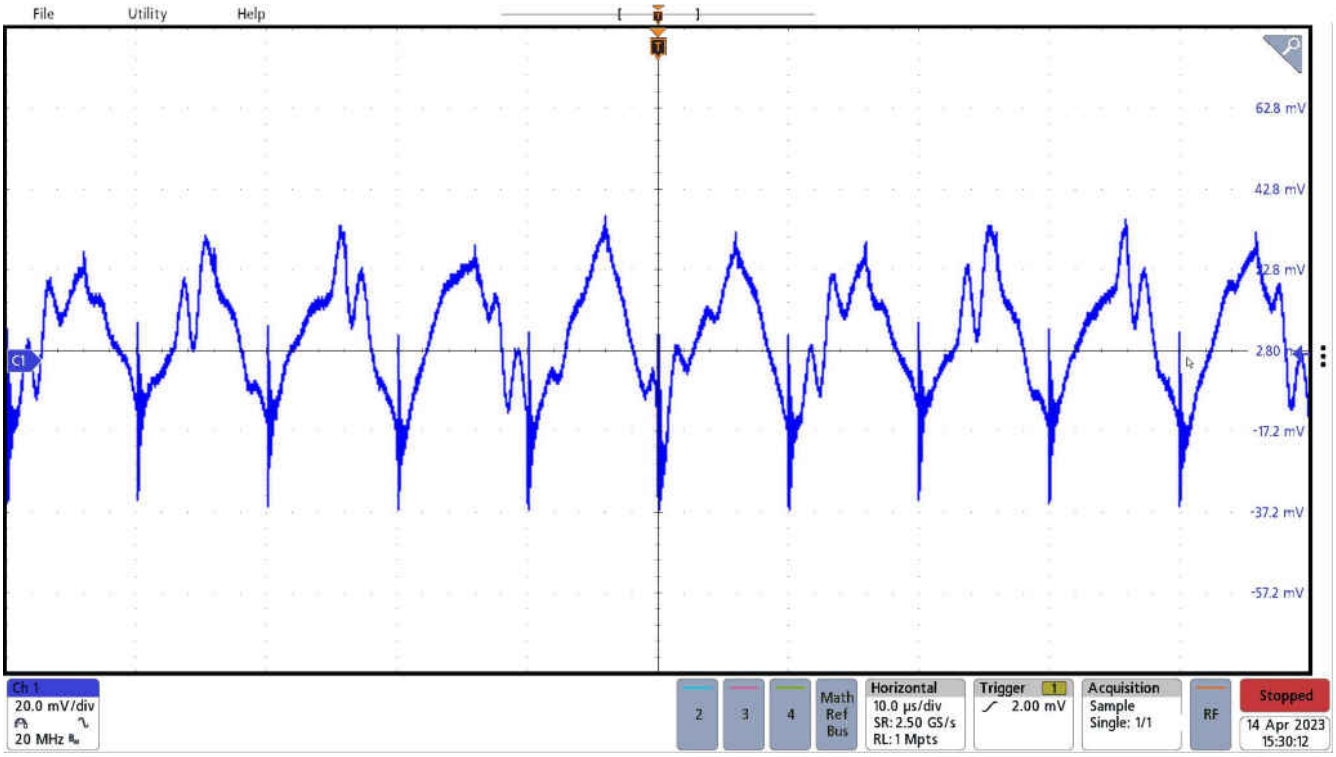


Figure 3-2. Output Voltage Ripple, 50 V_{IN}, 5-A Load

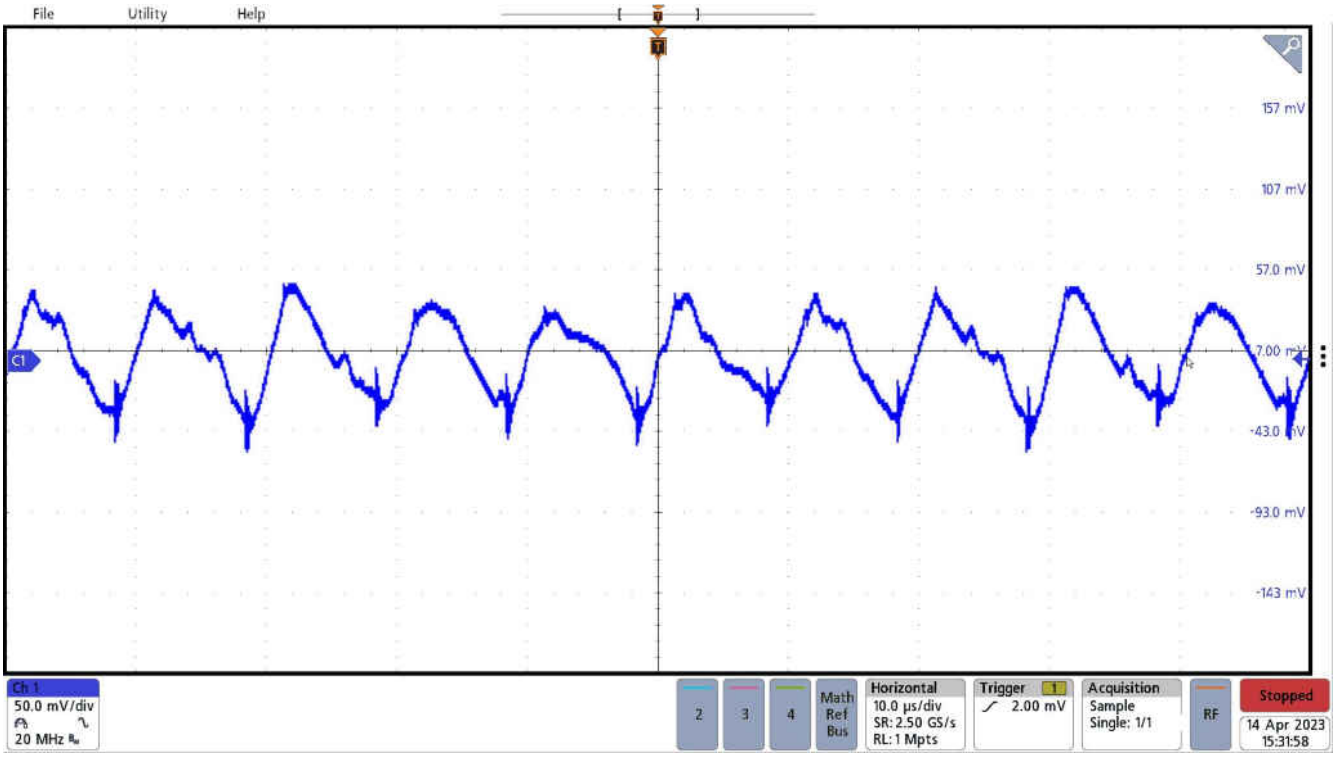


Figure 3-3. Output Voltage Ripple, 100 V_{IN}, 5-A Load

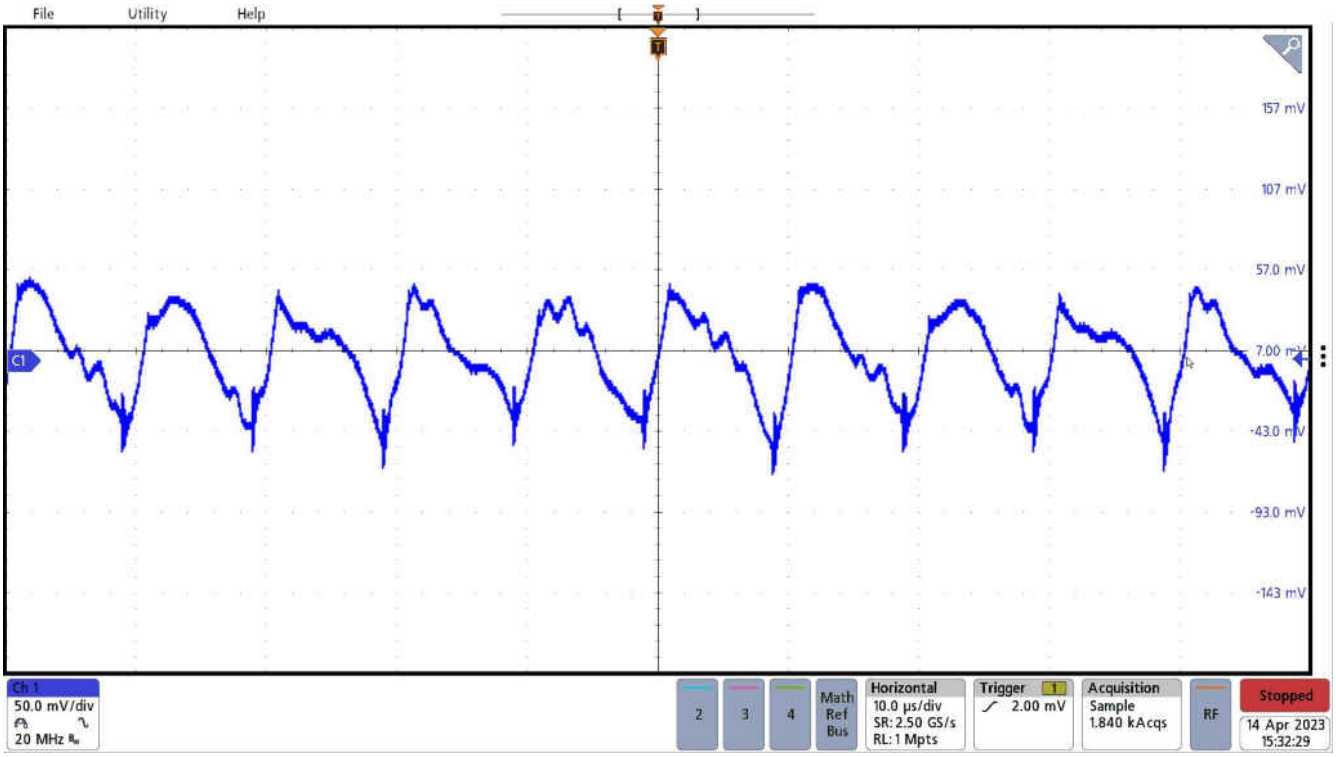


Figure 3-4. Output Voltage Ripple, 150 V_{IN}, 5-A Load

3.3 Short-Circuit Protection

The following figures show the output voltage and current during a short-circuit event. The input voltage was 100 V for both figures. Channel 1 shows the output voltage. Channel 4 shows the output current.

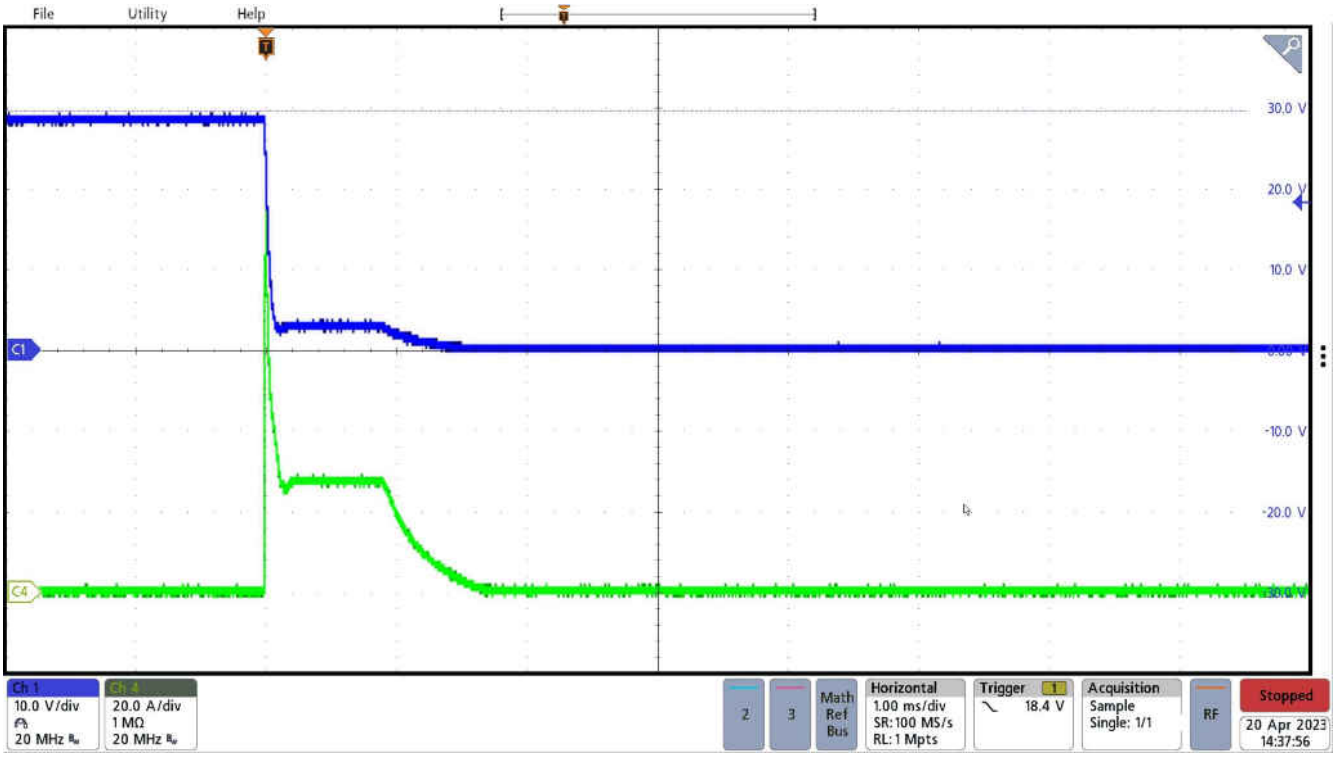


Figure 3-5. Operation Upon Application of Short Circuit

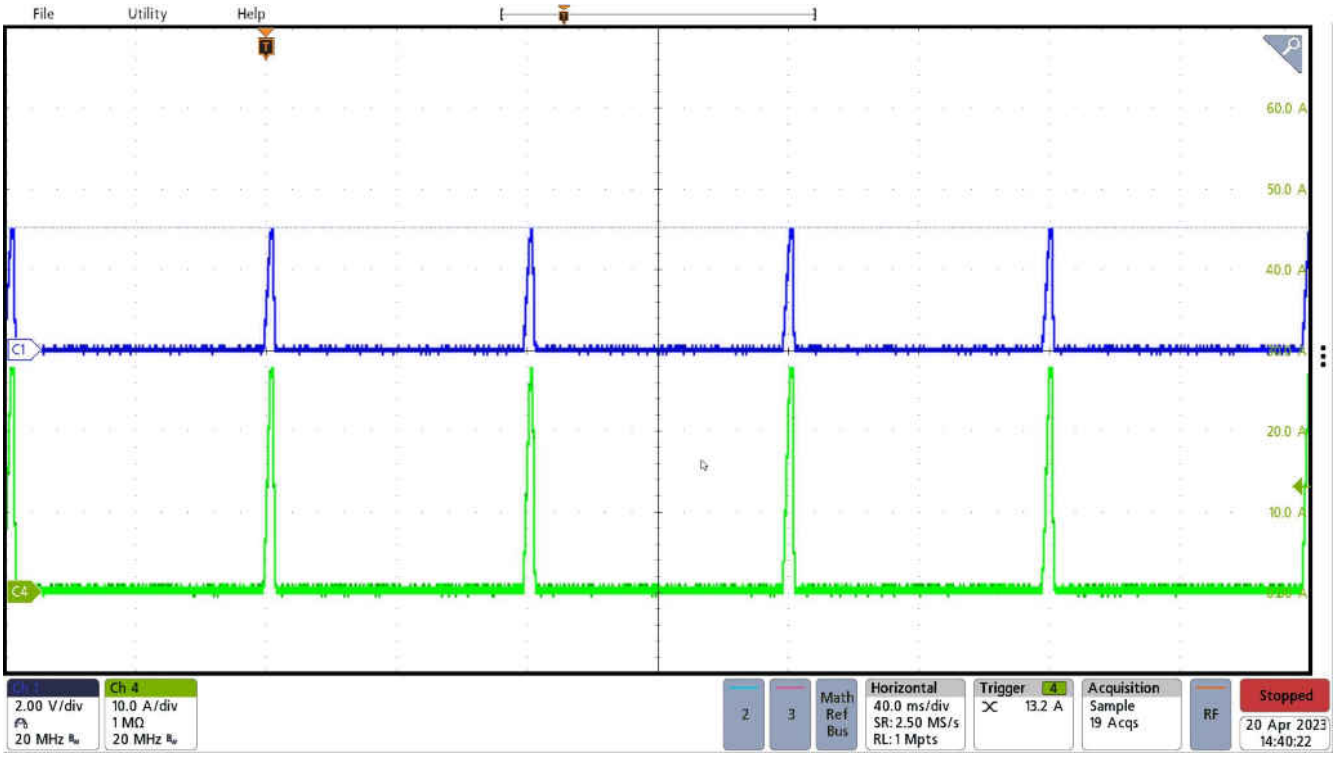


Figure 3-6. Operation During Sustained Short Circuit

3.4 Load Transients

Load transient response is shown in the following figures. The load was stepped between 1 A and 5 A at different input voltages.

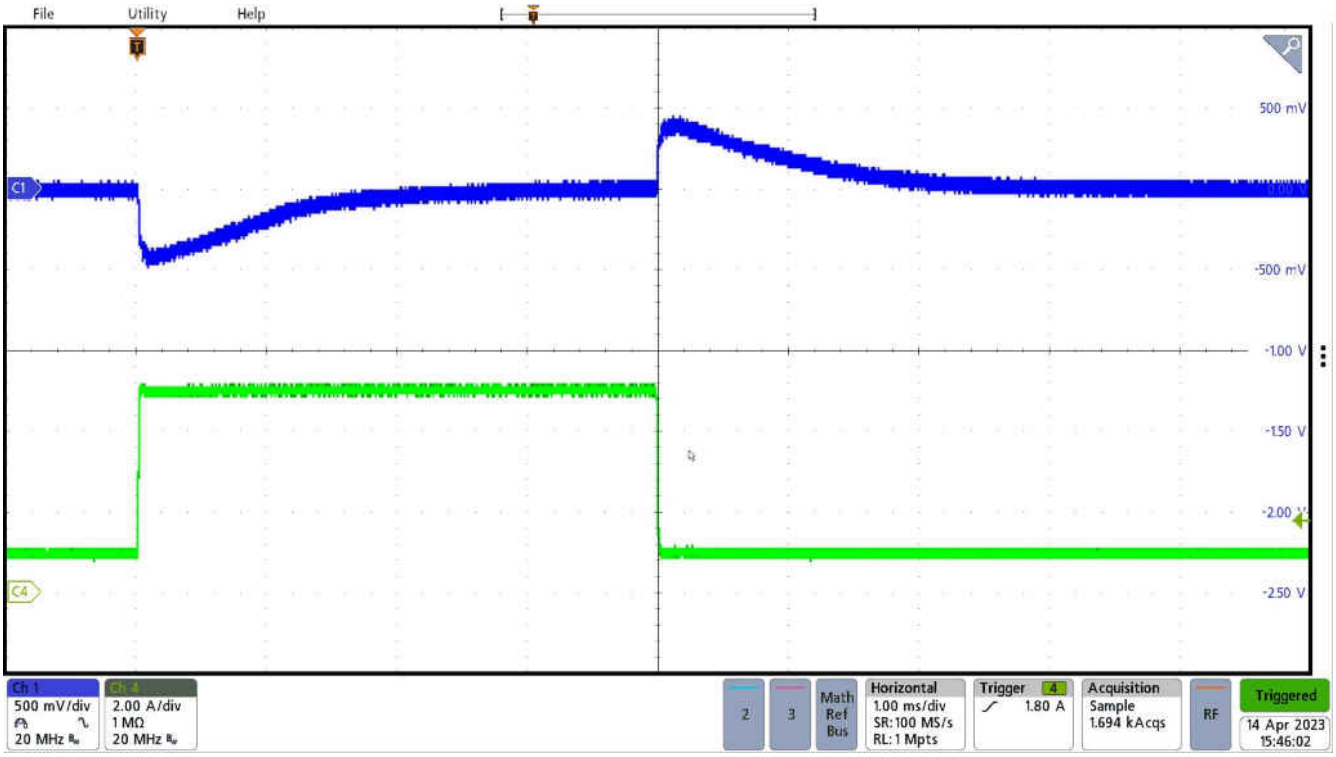


Figure 3-7. Load Transient, 50 V_{IN}

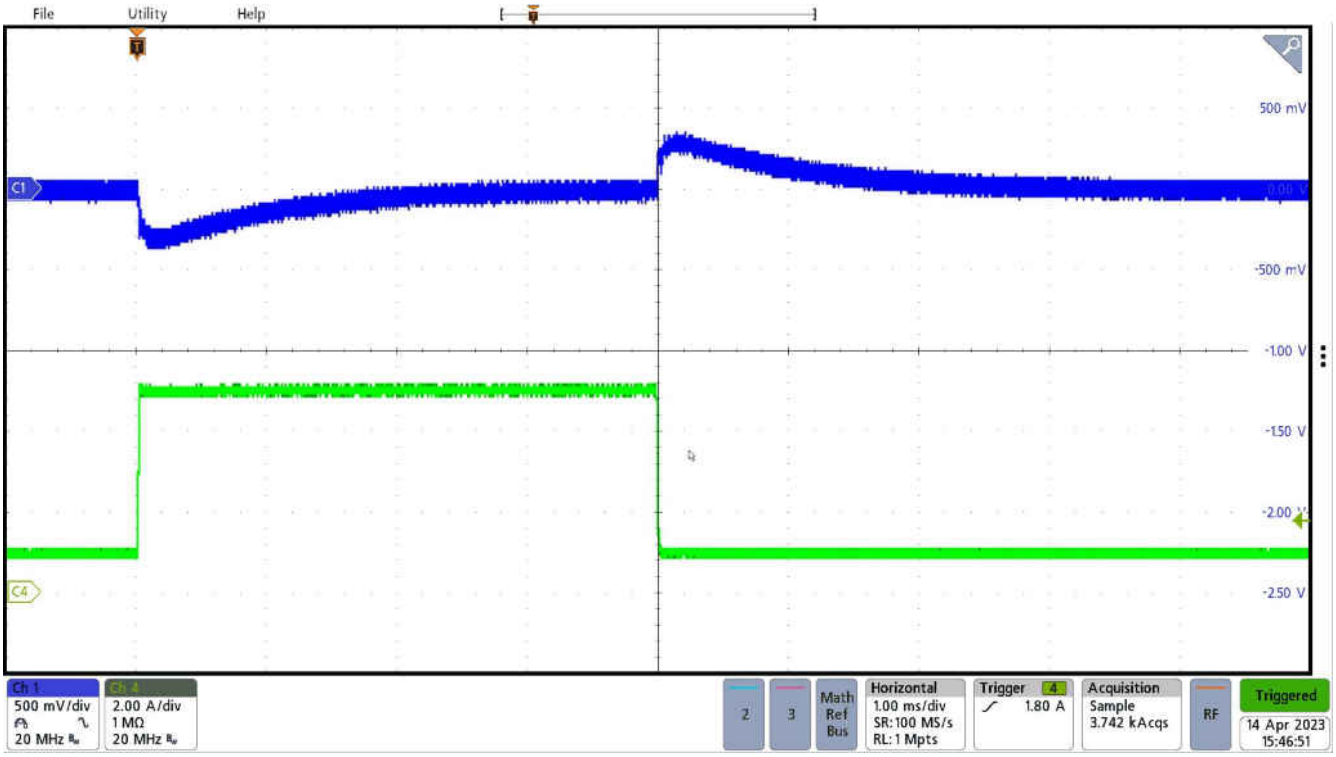


Figure 3-8. Load Transient , 100 V_{IN}

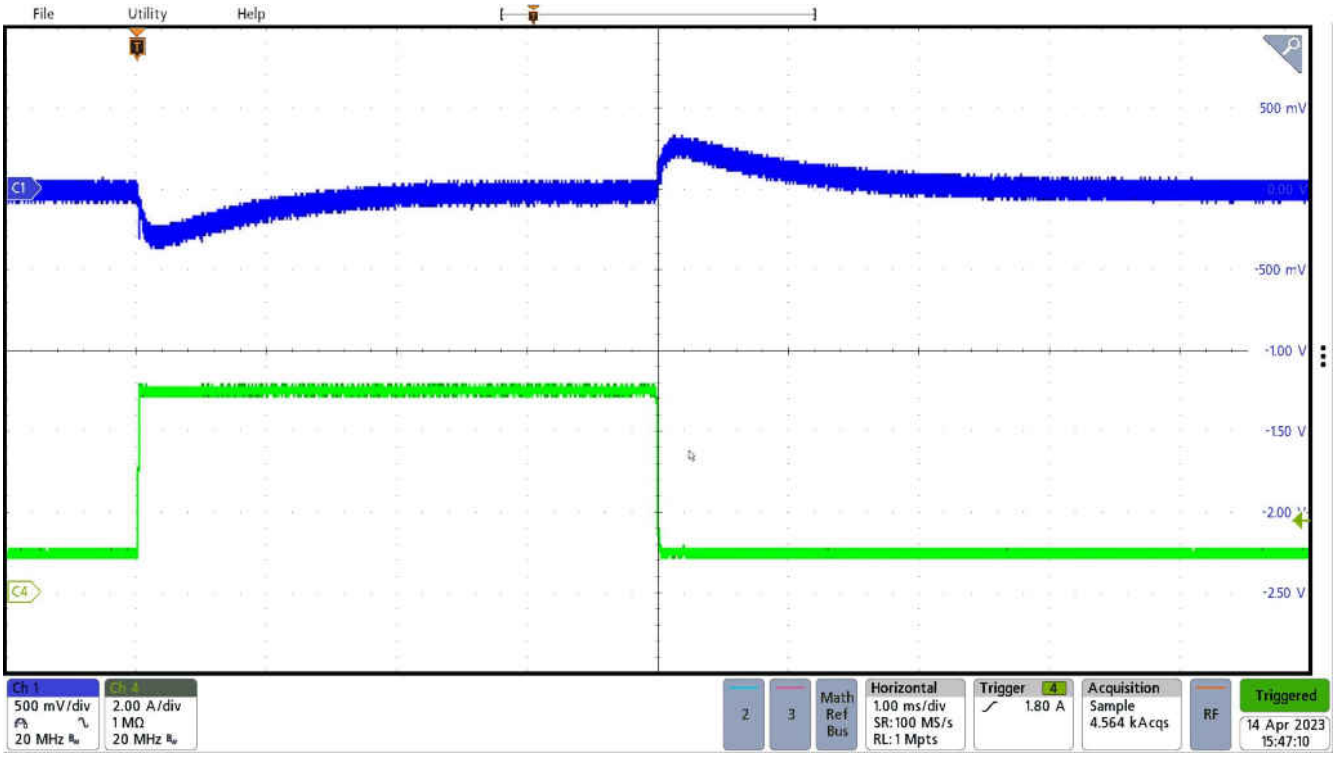


Figure 3-9. Load Transient , 150 V_{IN}

3.5 Start-Up

Start-up behavior with no load is shown in the following figures.

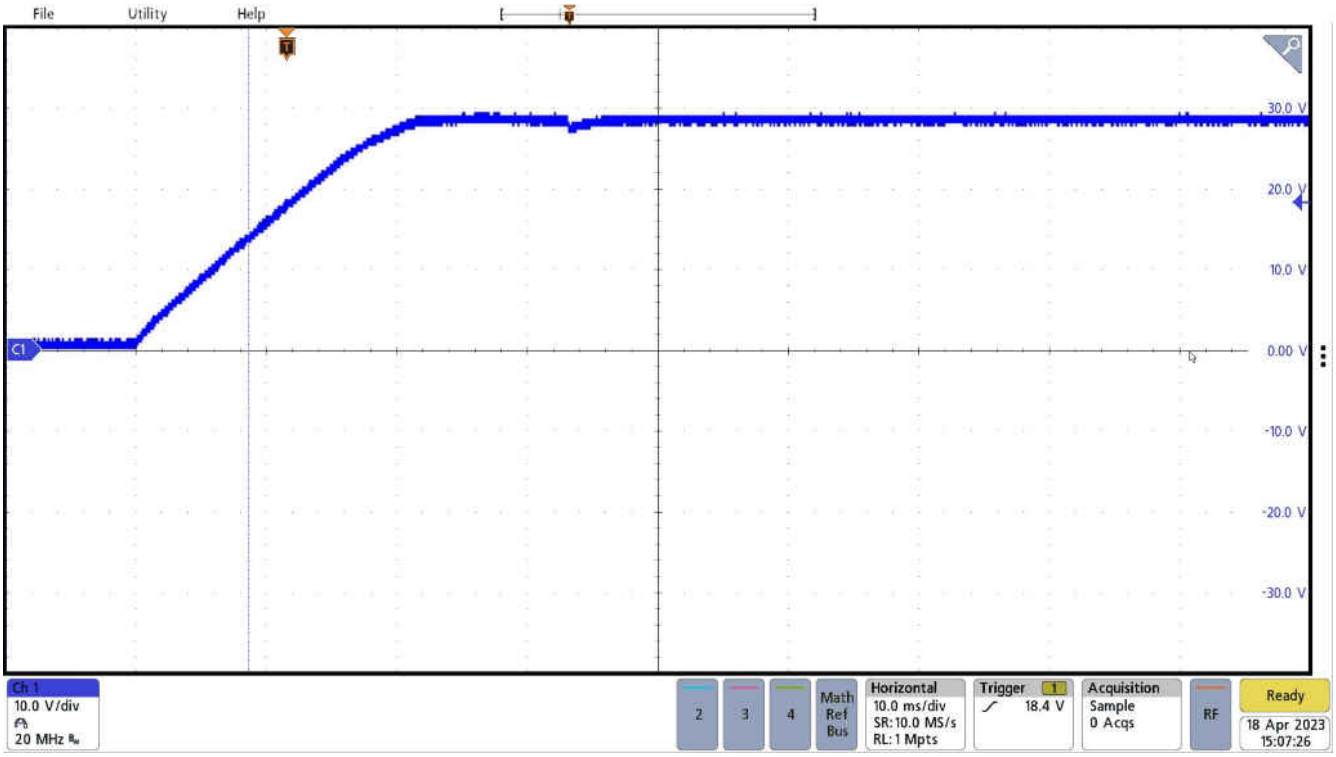


Figure 3-10. Start-Up, 50 V_{IN}

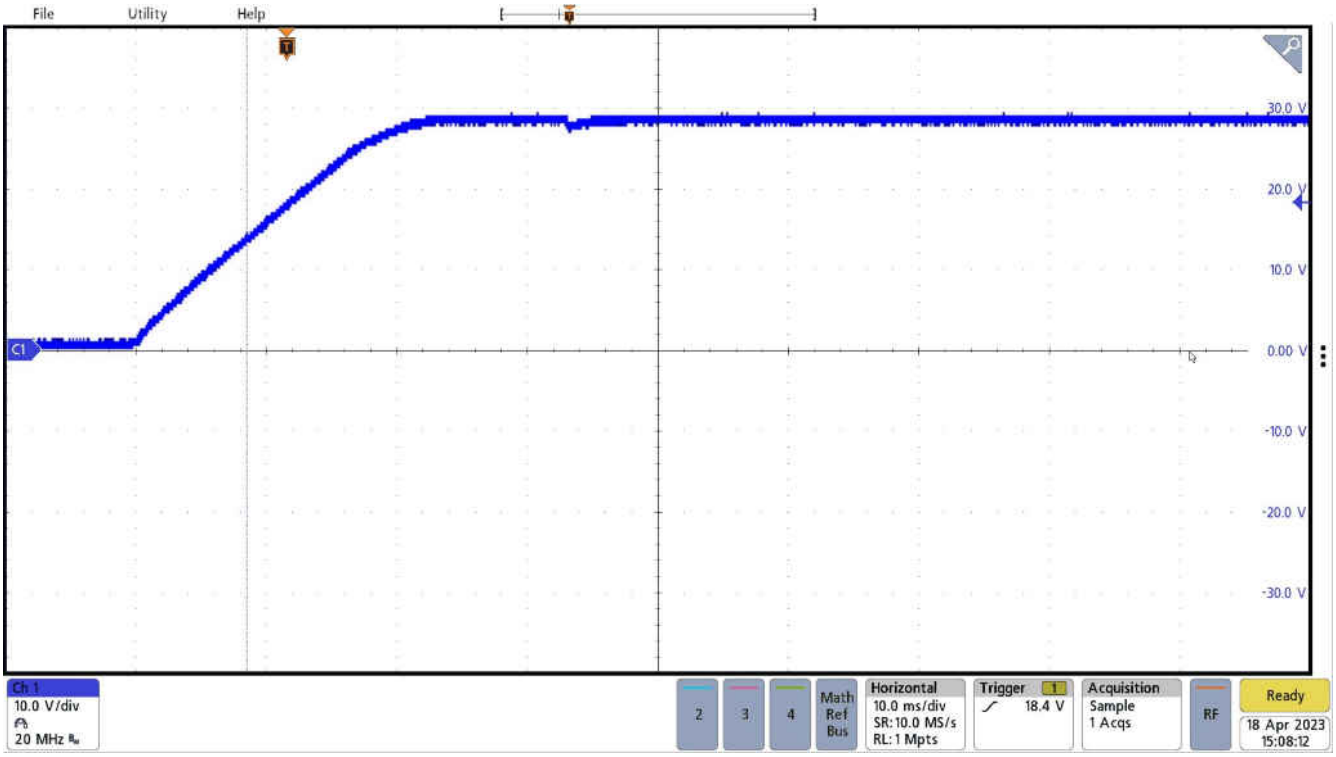


Figure 3-11. Start-Up, 100 V_{IN}

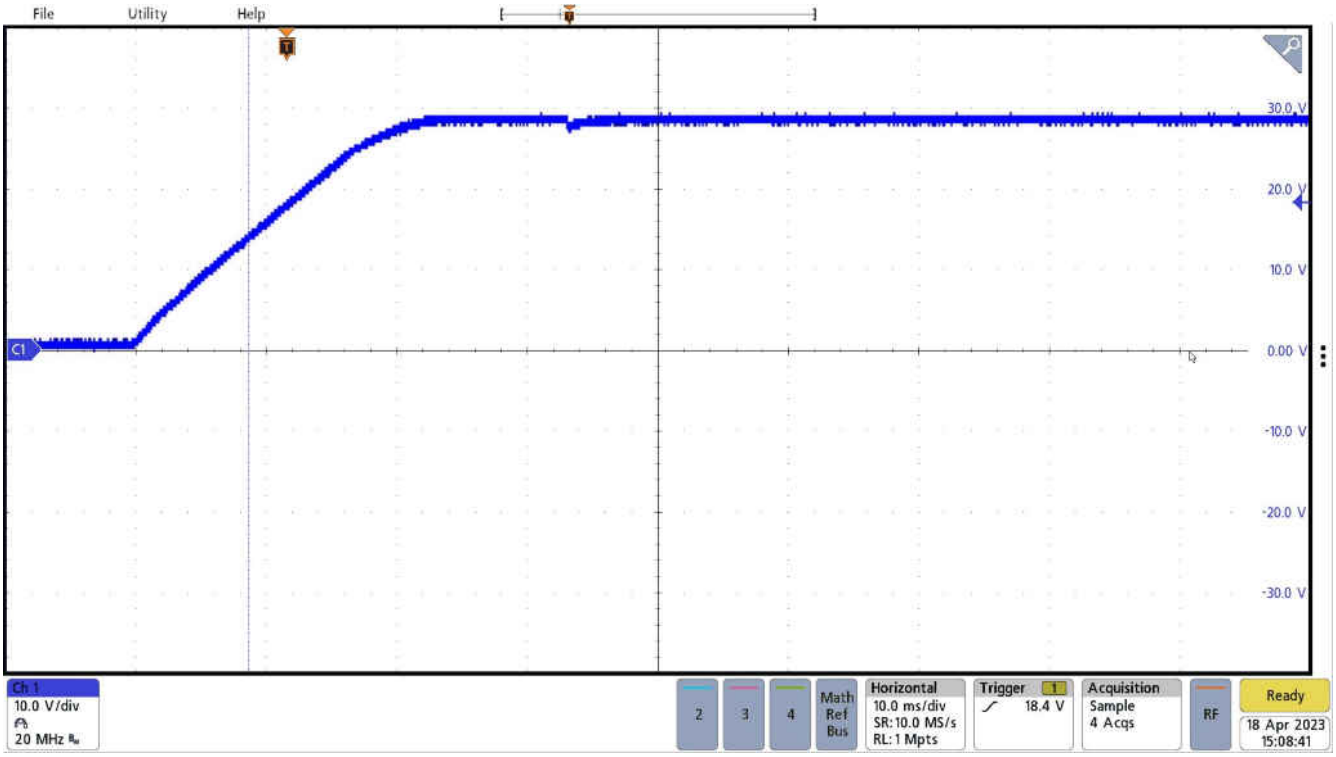


Figure 3-12. Start-Up, 150 V_{IN}

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