Test Report: PMP41063

300-V to 1,000-V Input 48-W Isolated Auxiliary Power Reference Design With Low Standby Power

Description

This reference design provides an isolated 12-V, 48-W output power conversion with cascaded flyback topology. The power supply can be powered from the 300-V to 1,000-V DC (direct current) input. This design uses valley switching fly-back controller UCC28730 to achieve less than 70-mW low standby power loss at 1000-V input voltage to extend the battery lifetime.

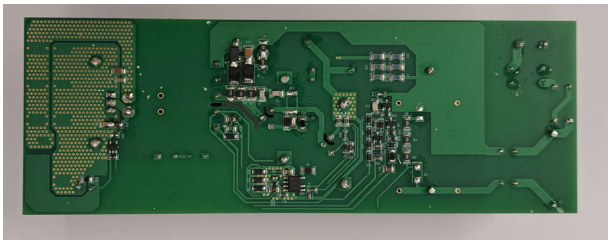
Features

- Wide input voltage range from 300-V to 1,000-V DC
- Less than 70-mW no load power consumption at 1000-V input
- Primary-side regulation design (no optocoupler) extends product lifetime
- Minimized output undershoot and overshoot during load transient
- Uniform start-up time across input voltage range
- 86.14% efficiency at 1,000-V input and 48-W output

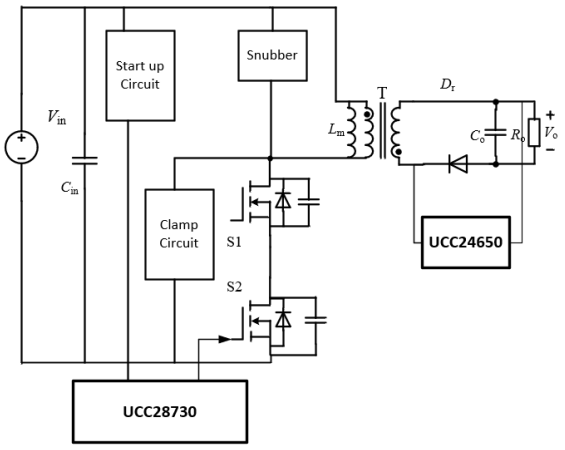
Applications

- Battery energy storage system
- Power conversion system (PCS)
- String inverter

Top of Board



Bottom of Board



Block Diagram

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input voltage range	300-V to 1,000-V
Output Voltage, Current	12 V at 4 A
Maximum power	48 W

1.2 Required Equipment

- DC Source: IT-M3906D-1500-12
- Chroma DC Source 62024P-600-8
- Electronic load: Chroma, 6314A
- Oscilloscope: Tektronix, DPO 3054
- Infrared Thermal Camera: Fluke, TiS55
- Ture-RMS-Multimeter: Fluke, 287C
- Digital Power Meter: Yokogawa WT310

1.3 Dimensions

Board size: 173 mm × 60.7 mm × 37 mm (open frame)

2 Testing and Results

2.1 Efficiency and Regulation Graphs

Efficiency is shown in the following figure.

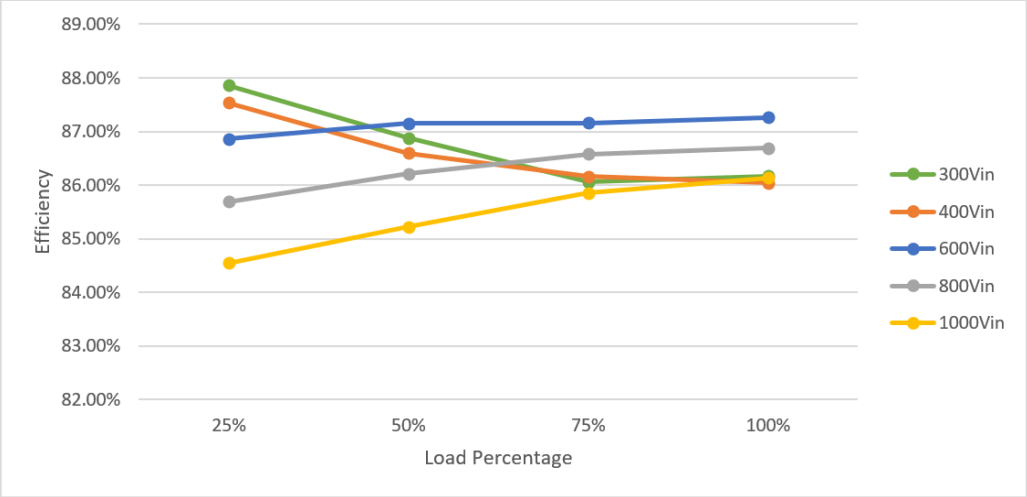


Figure 2-1. Efficiency versus Input Voltage and Load

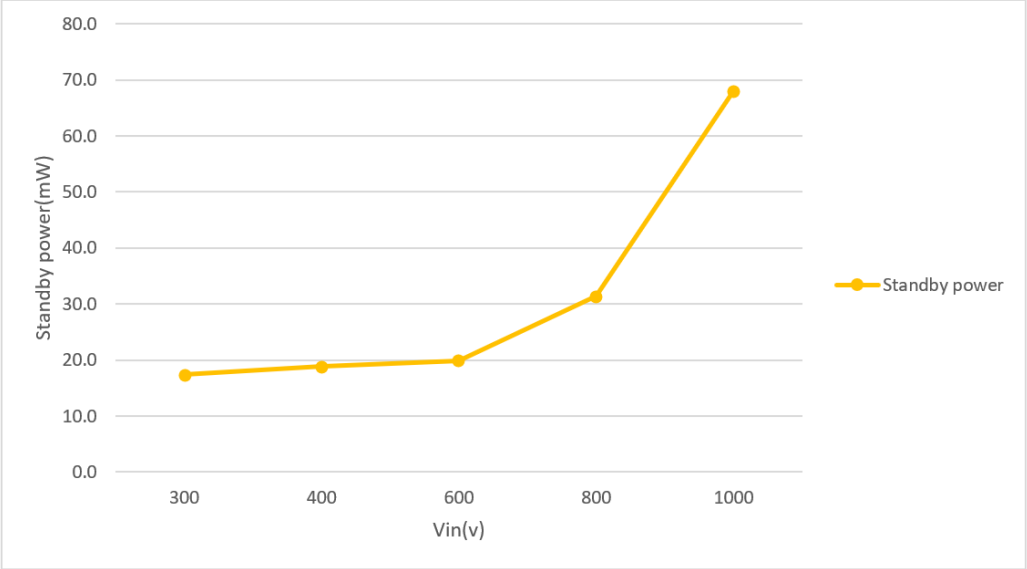


Figure 2-2. No Load Power Consumption

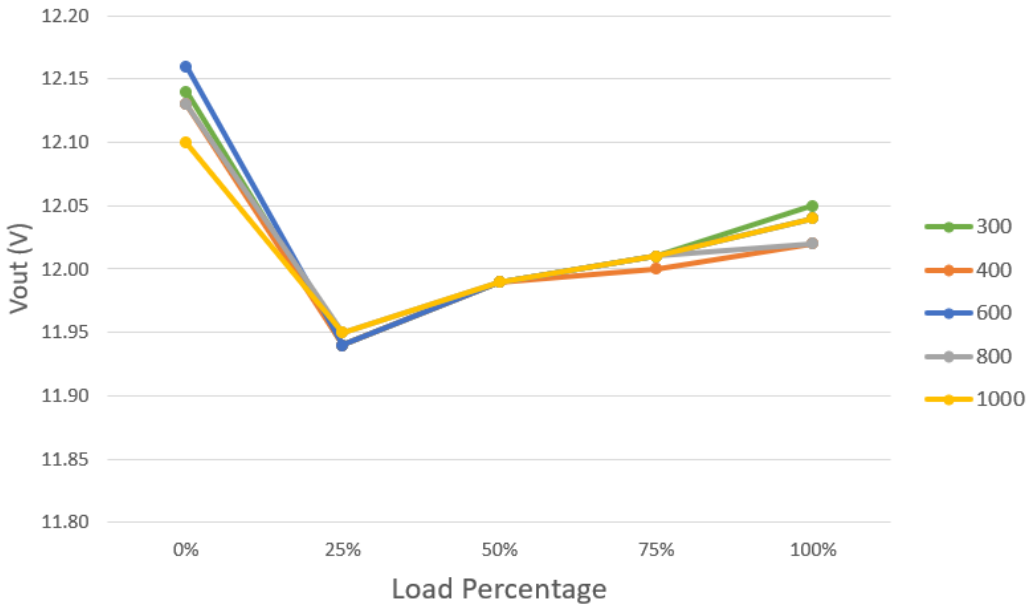


Figure 2-3. Output Voltage Regulation

2.2 Efficiency Data

Efficiency data is shown in the following table.

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
300	0.0000581	12.14	0.000	0.0174	0	–
300	0.0453	11.94	1.000	13.59	11.94	87.86%
300	0.09201	11.99	2.000	27.6	23.98	86.87%
300	0.13955	12.01	3.000	41.87	36.03	86.06%
300	0.18645	12.05	4.000	55.94	48.2	86.17%
400	0.0000471	12.13	0.000	0.0188	0	–
400	0.0341	11.94	1.000	13.64	11.94	87.54%
400	0.06923	11.99	2.000	27.69	23.98	86.60%
400	0.10446	12.00	3.000	41.78	36.00	86.16%
400	0.1397	12.02	4.000	55.88	48.08	86.04%
600	0.0000332	12.16	0.000	0.0199	0	–
600	0.022911	11.94	1.000	13.75	11.94	86.86%
600	0.045861	11.99	2.000	27.52	23.98	87.15%
600	0.0689	12.01	3.000	41.34	36.03	87.16%
600	0.09198	12.04	4.000	55.19	48.16	87.27%
800	0.0000392	12.13	0.000	0.0314	0	–
800	0.017631	11.95	1.000	14.10	11.95	85.70%
800	0.034767	11.99	2.000	27.81	23.98	86.22%
800	0.052021	12.01	3.000	41.62	36.03	86.58%
800	0.06933	12.02	4.000	55.46	48.08	86.69%
1000	0.000068	12.10	0.000	0.0680	0	–
1000	0.014464	11.95	1.000	14.46	11.95	84.55%
1000	0.02814	11.99	2.000	28.14	23.98	85.22%
1000	0.041968	12.01	3.000	41.97	36.03	85.85%
1000	0.05591	12.04	4.000	55.91	48.16	86.14%

2.3 Thermal Images

Table 2-1 shows the thermal images, all images were captured with 25ºC ambient, after 30-minute warm up

Table 2-1. Thermal Image Data

Temperature (°C)	300 V_{IN}	600 V_{IN}	800 V_{IN}	1000 V_{IN}
High-side switch Q1	61.8	56.7	54.5	55.1
Low-side switch Q2	50.1	47.5	46.3	47.5
Transformer	Core: 56.8 Winding: 64.3	Core: 58.2 Winding: 65.3	Core: 58.9 Winding: 66.2	Core: 60.2 Winding: 67.4
Snubber circuit resistor R16, R17, R18	65	64.7	65.2	67.6
Snubber circuit clamp diode D1 and D2	60.8	61.4	62.3	63.4
Snubber circuit clamp diode D1 and D2	60.8	61.4	62.3	63.4
Snubber circuit Clamp TVS D22	53.5	55.6	57.6	58.9
TVS diode D6 and D10	40.5	46.2	54.5	61.5
Secondary diode D7	77.9	78.5	78.8	79.2
UCC28730	40.5	40.6	40.6	40.8
UCC24650	50.3	53.4	54.5	56.3

Figure 2-4 through Figure 2-11 show the thermal image data.

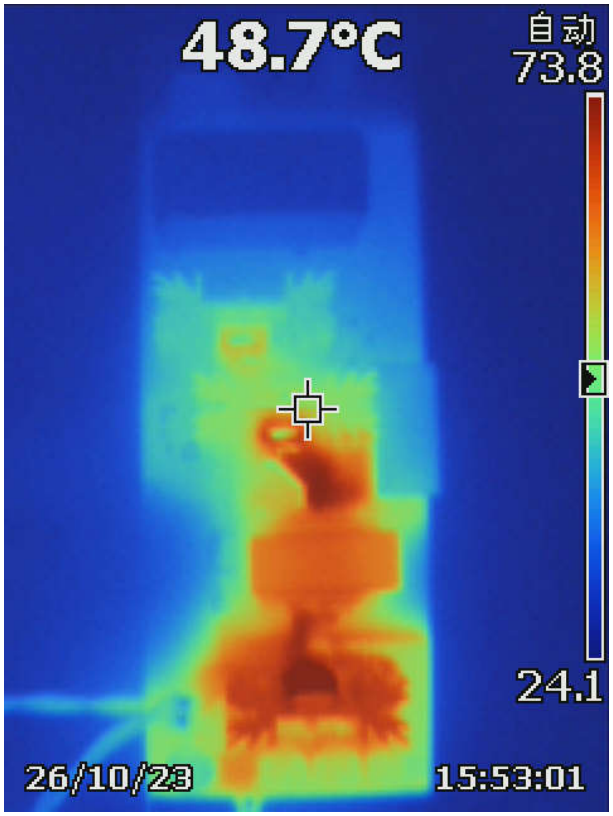


Figure 2-4. Thermal Image 300 V_{IN} 12 V, 4-A Load Top View

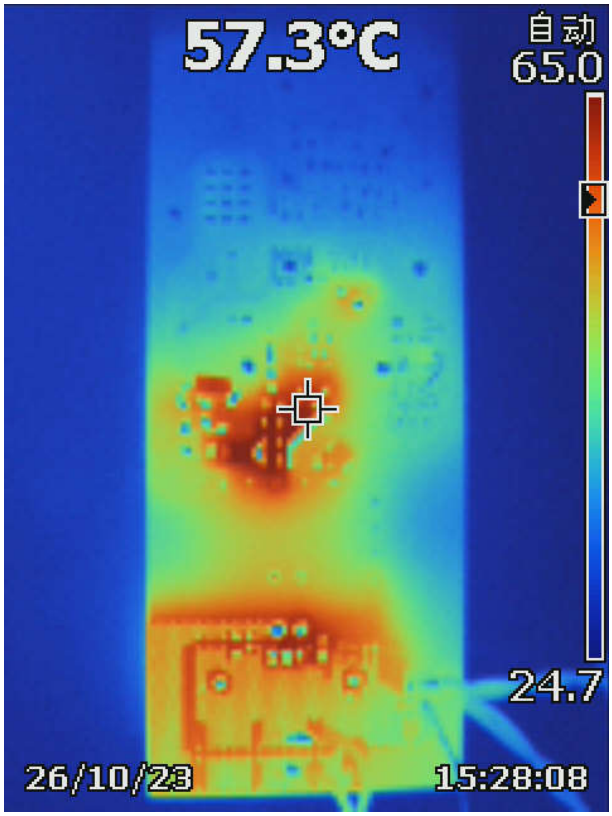


Figure 2-5. Thermal Image 300 V_{IN} 12 V, 4-A Load Bottom View

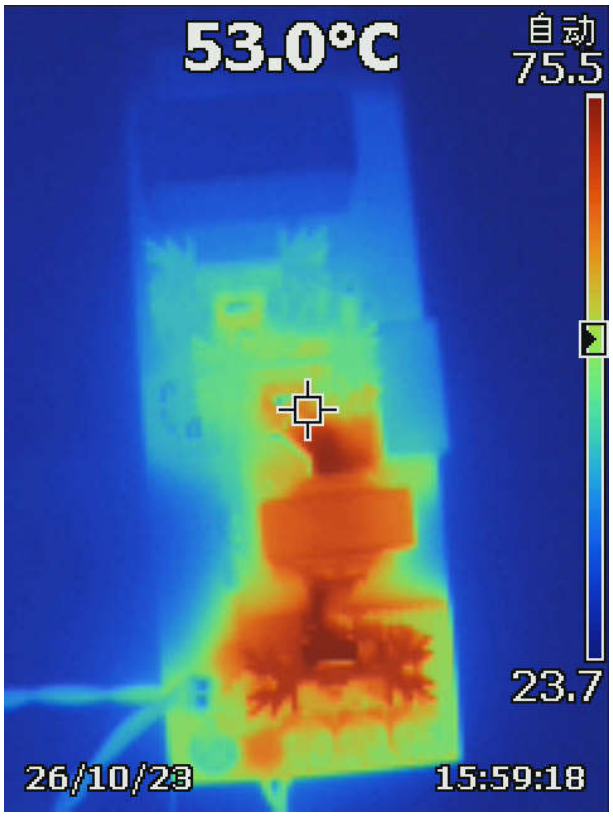


Figure 2-6. Thermal Image 600 V_{IN} 12 V, 4-A Load Top View

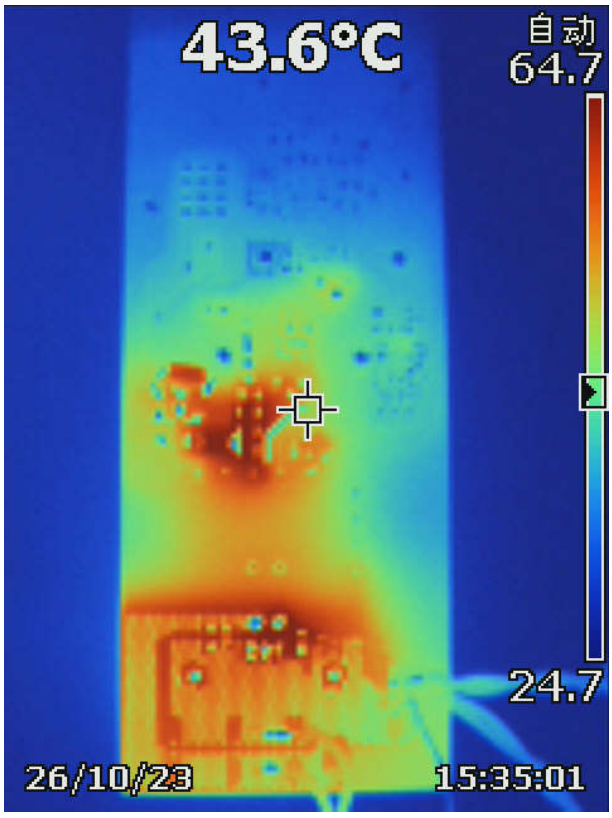


Figure 2-7. Thermal Image 600 V_{IN} 12 V, 4-A Load Bottom View

Figure 2-8. Thermal Image 800 V_{IN} 12 V, 4-A Load Top View

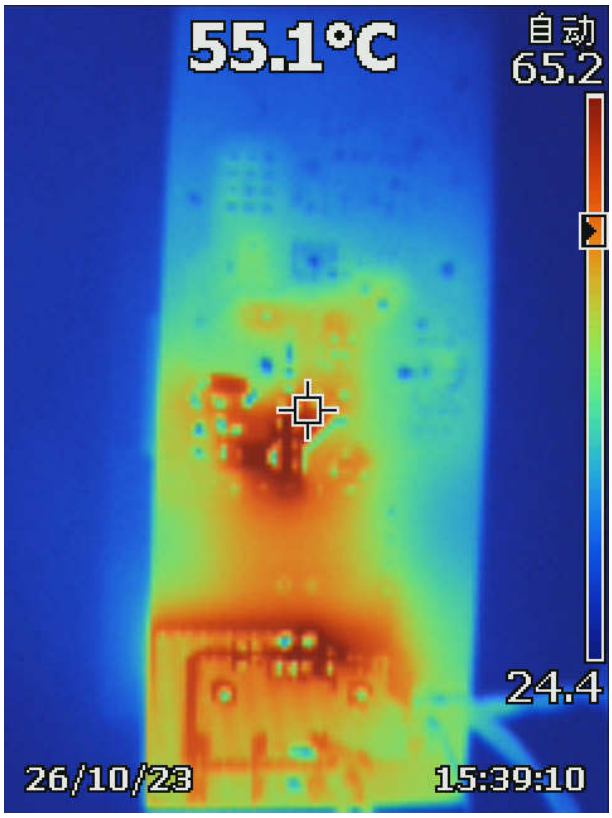


Figure 2-9. Thermal Image 800 V_{IN} 12 V, 4-A Load Bottom View

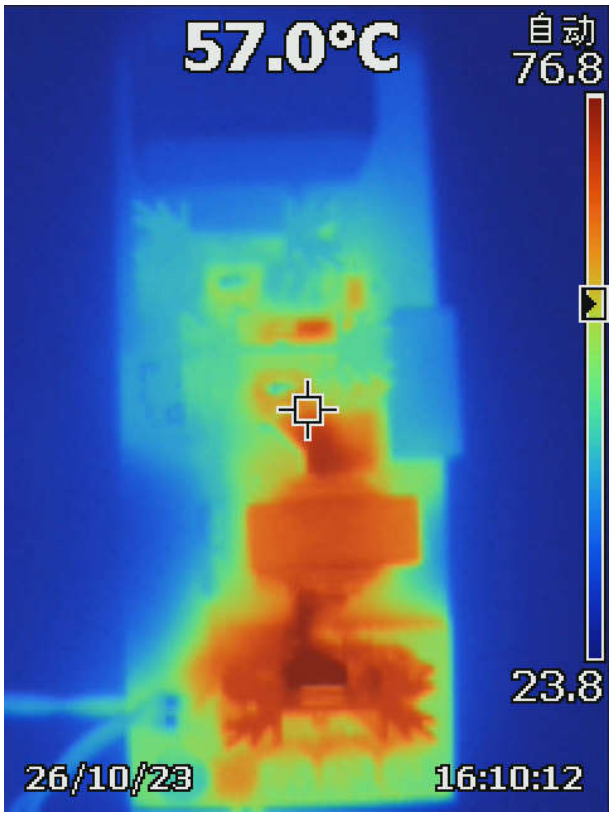


Figure 2-10. Thermal Image 1000 V_{IN} 12 V,4-A Load Top View

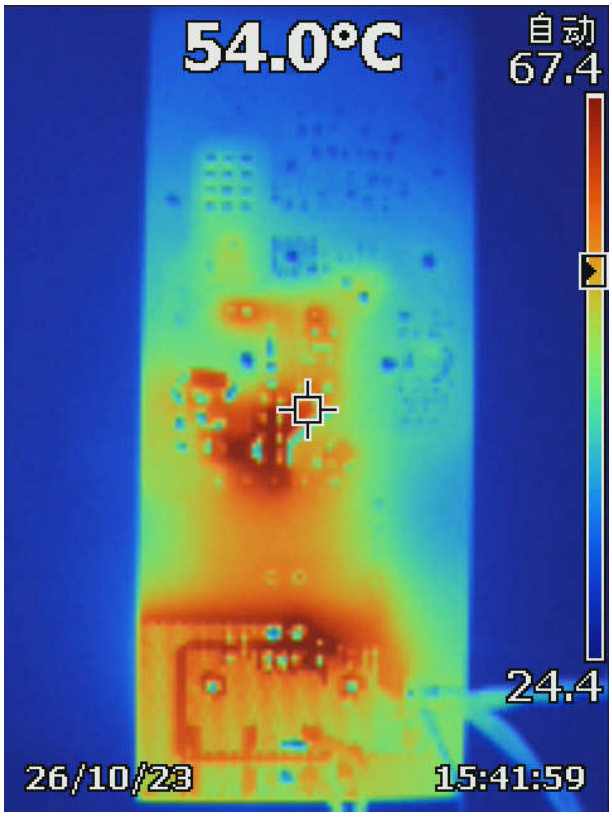


Figure 2-11. Thermal Image 1000 V_{IN} 12 V, 4-A Load Bottom View

3 Waveforms

3.1 Switching

Switching behavior is shown in the following figures. Each waveform reflects the following parameters:

- Vds_low side: drain source voltage of low-side switch Q2
- Vsw: switching node voltage connecting to Q1 drain refer to primary ground
- Vds_high side: drain source voltage of high-side switch Q1

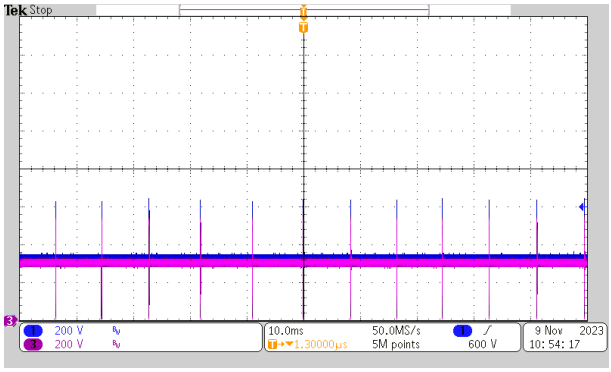


Figure 3-1. 300 V_{IN} Open Load, Vds_low Side (Purple), Vsw (Blue)

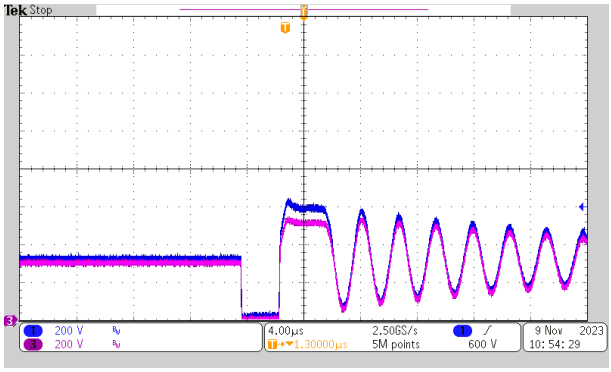


Figure 3-2. 300 V_{IN} Open Load, Zoom of Vds_low Side (Purple), Vsw (Blue)

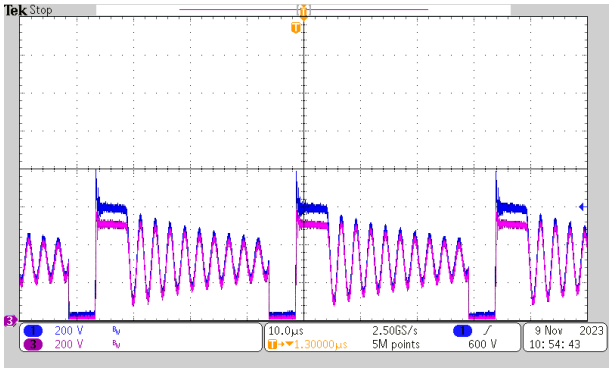


Figure 3-3. 300 V_{IN} 1-A Load, Vds_low Side (Purple), Vsw (Blue)

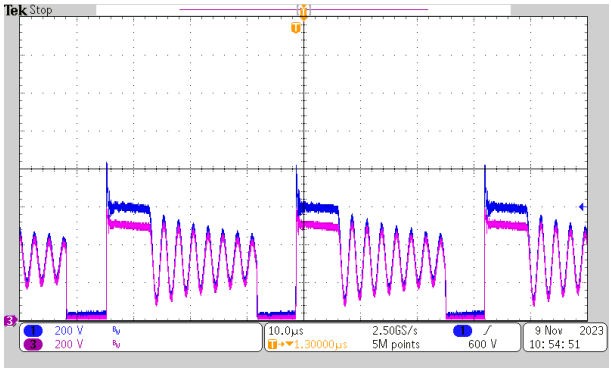


Figure 3-4. 300 V_{IN} 2-A Load, Vds_low Side (Purple), Vsw (Blue)

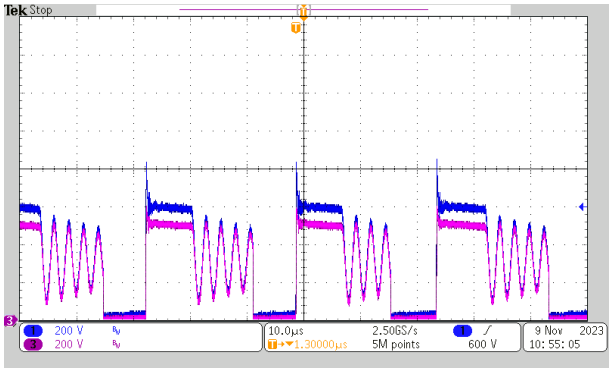


Figure 3-5. 300 V_{IN} 3-A Load, Vds_low Side (Purple), Vsw (Blue)

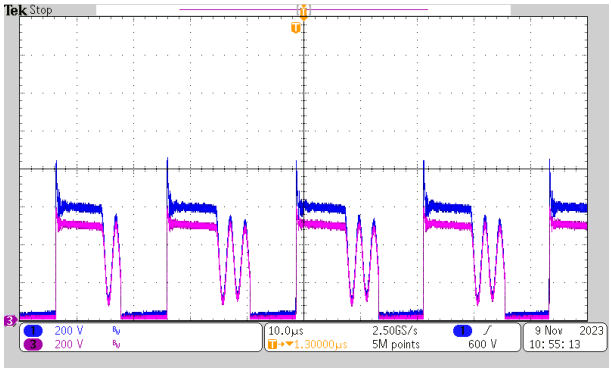


Figure 3-6. 300 V_{IN} 4-A Load, Vds_low Side (Purple), Vsw (Blue)

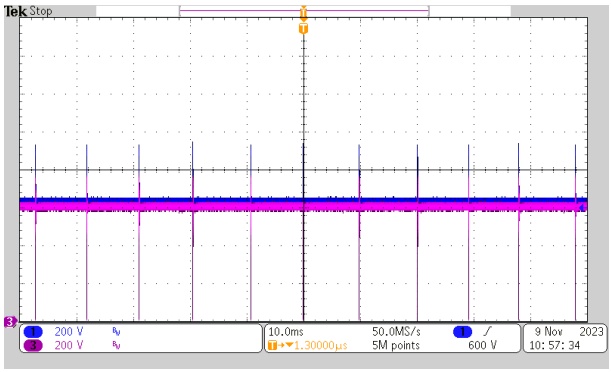


Figure 3-7. 600 V_{IN} Open Load, Vds_low Side (Purple), Vsw (Blue)

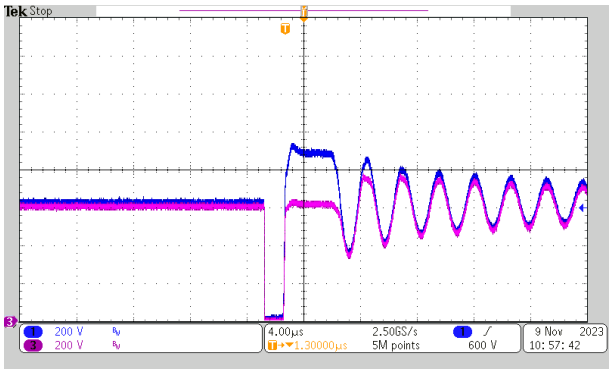


Figure 3-8. 600 V_{IN} Open Load, Zoom of Vds_low Side (Purple), Vsw (Blue)

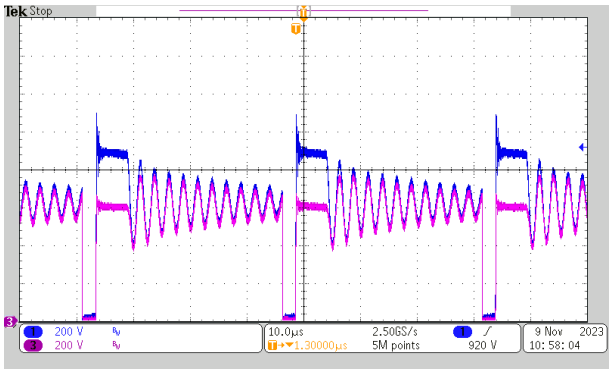


Figure 3-9. 600 V_{IN} 1-A Load, Vds_low Side (Purple), Vsw (Blue)

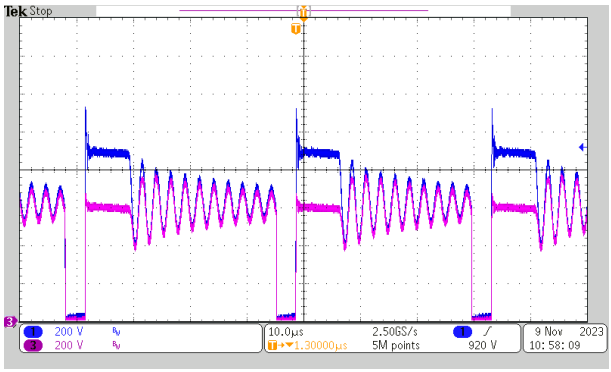


Figure 3-10. 600 V_{IN} 2-A Load, Vds_low Side (Purple), Vsw (Blue)

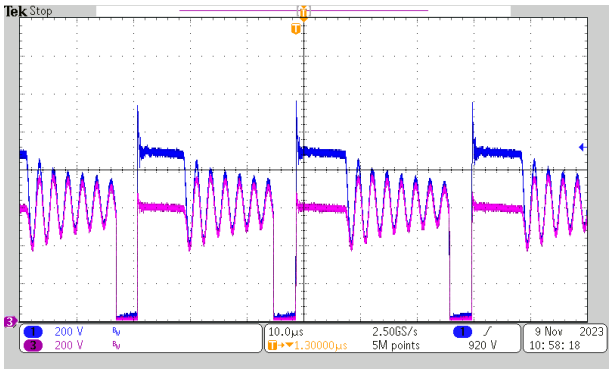


Figure 3-11. 600 V_{IN} 3-A Load, Vds_low Side (Purple), Vsw (Blue)

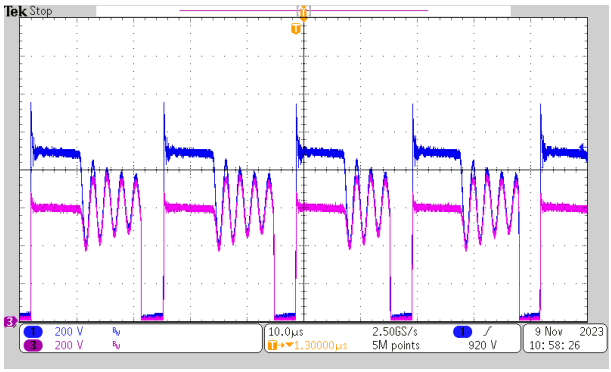


Figure 3-12. 600 V_{IN} 4-A Load, Vds_low Side (Purple), Vsw (Blue)

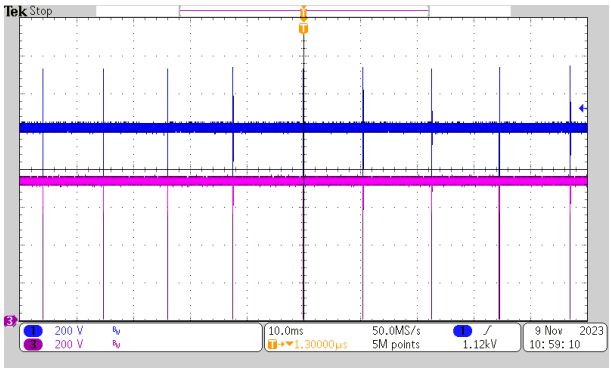


Figure 3-13. 1000 V_{IN} Open Load, Vds_low Side (Purple), Vsw (Blue)

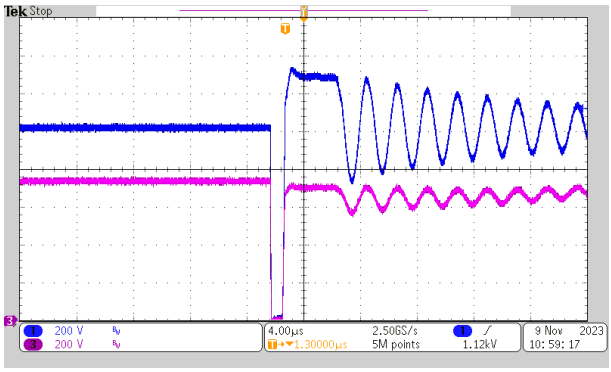


Figure 3-14. 1000 V_{IN} Open Load, Zoom of Vds_low Side (Purple), Vsw (Blue)

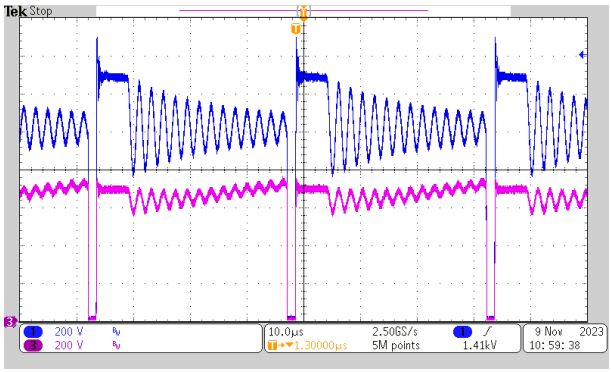


Figure 3-15. 1000 V_{IN} 1-A Load, Vds_low Side (Purple), Vsw (Blue)

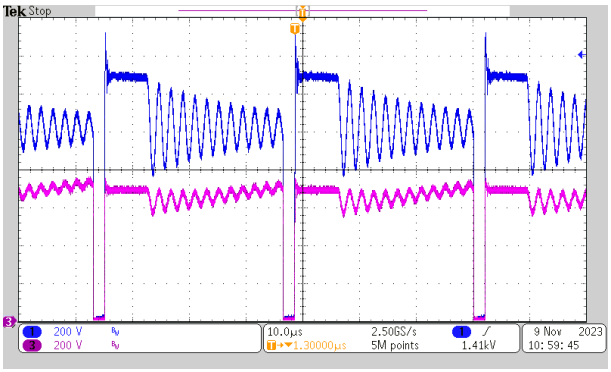


Figure 3-16. 1000 V_{IN} 2-A Load, Vds_low Side (Purple), Vsw (Blue)

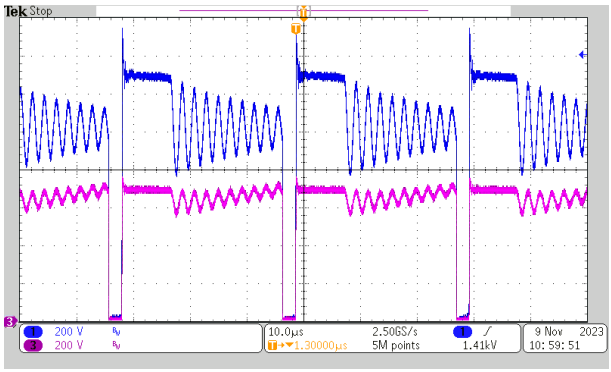


Figure 3-17. 1000 V_{IN} 3-A Load, Vds_low Side (Purple), Vsw (Blue)

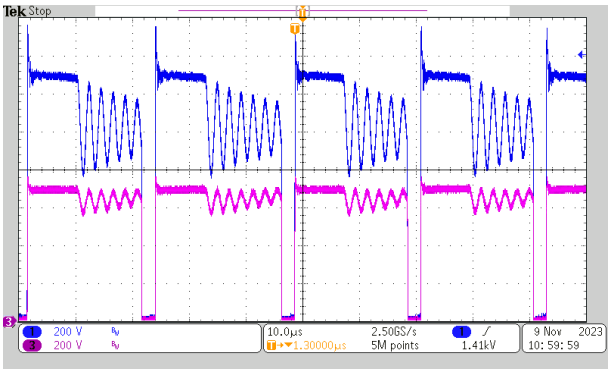


Figure 3-18. 1000 V_{IN} 4-A Load, Vds_low Side (Purple), Vsw (Blue)

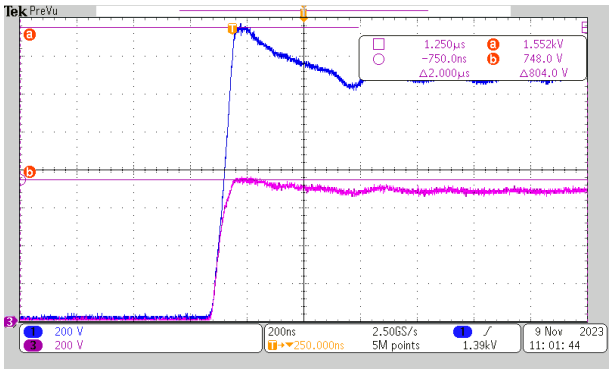


Figure 3-19. 1000 V_{IN} 4-A Load, Zoom of Vds_low Side (Purple), Vsw (Blue)

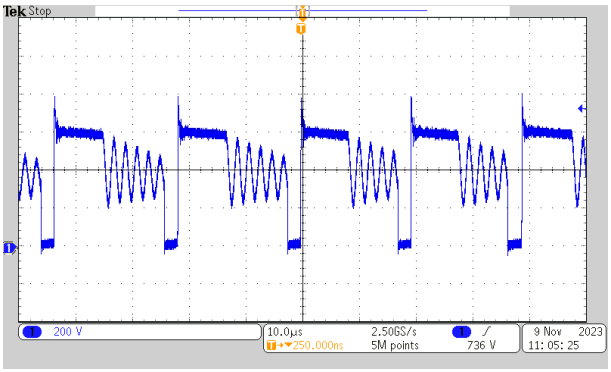


Figure 3-20. 1000 V_{IN} 4-A Load, Vds_high Side

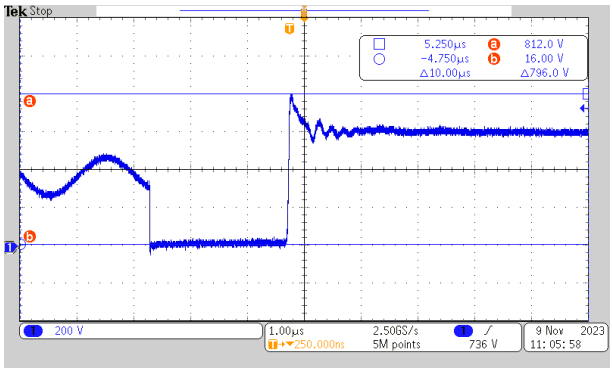


Figure 3-21. 1000 V_{IN} 4-A Load Zoom of Vds_high Side

3.2 Output Voltage Ripple

Output voltage ripple is shown in the following figures.

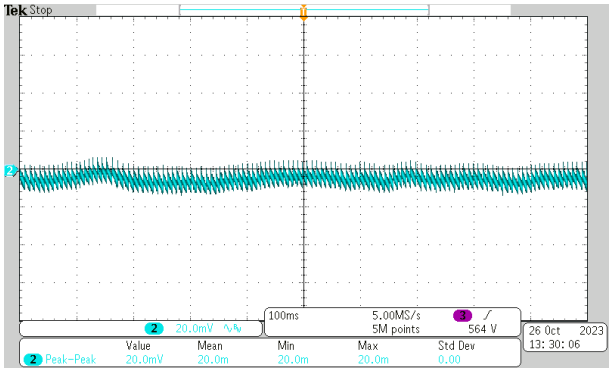


Figure 3-22. 300 V_{IN} Open-Load Output Voltage Ripple

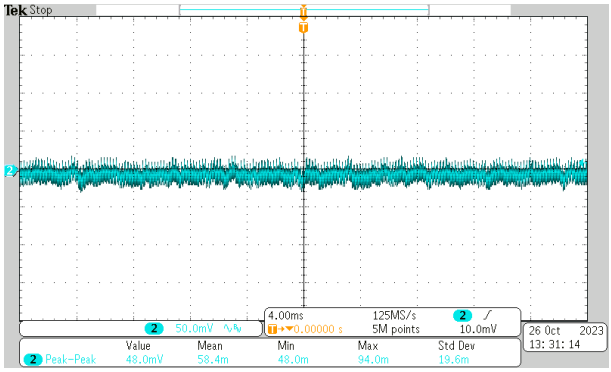


Figure 3-23. 300 V_{IN} 2-A Load Output Voltage Ripple

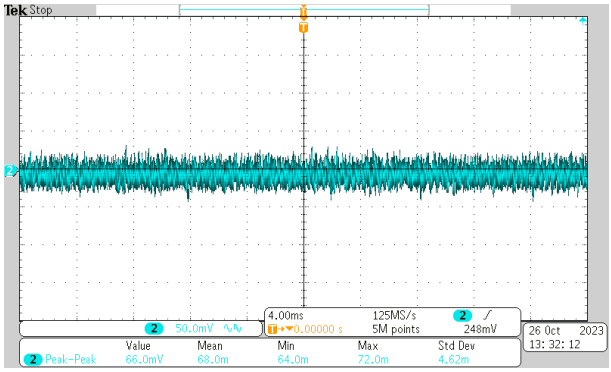


Figure 3-24. 300 V_{IN} 4-A Load Output Voltage Ripple

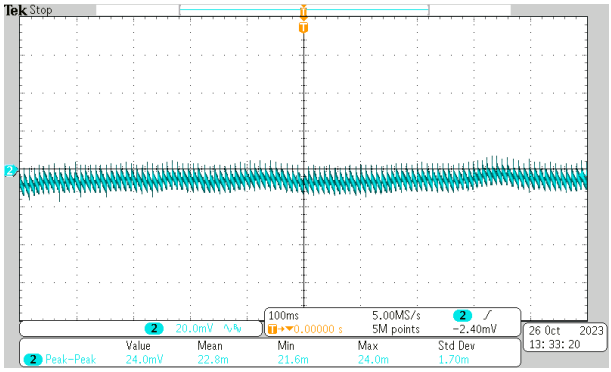


Figure 3-25. 600 V_{IN} Open-Load Output Voltage Ripple

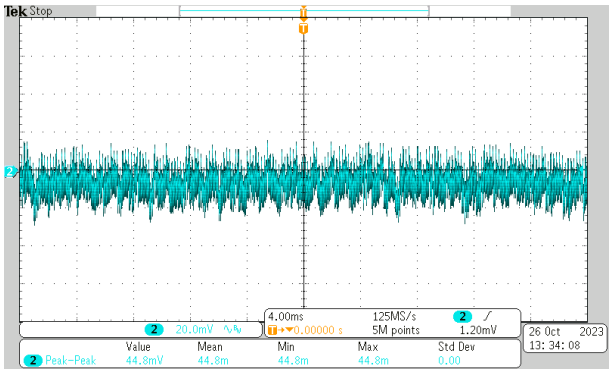


Figure 3-26. 600 V_{IN} 2-A Load Output Voltage Ripple

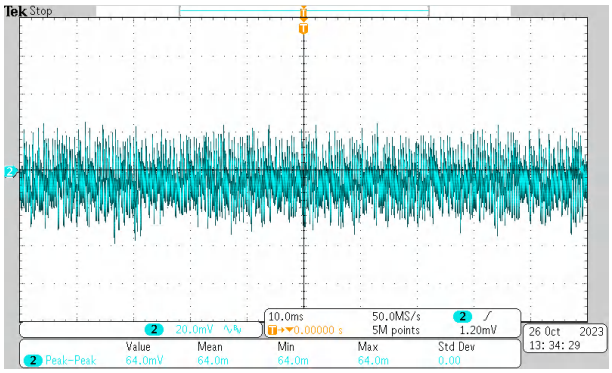


Figure 3-27. 600 V_{IN} 4-A Load Output Voltage Ripple

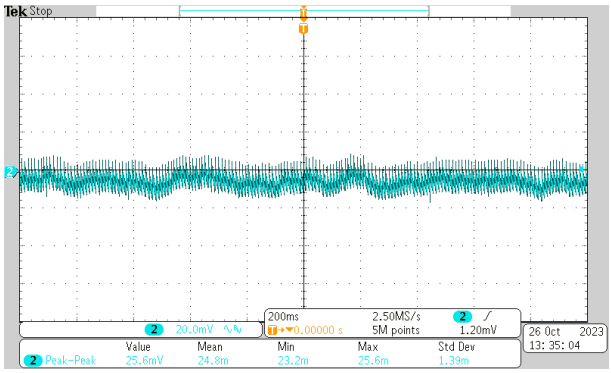


Figure 3-28. 1000 V_{IN} Open-Load Output Voltage Ripple

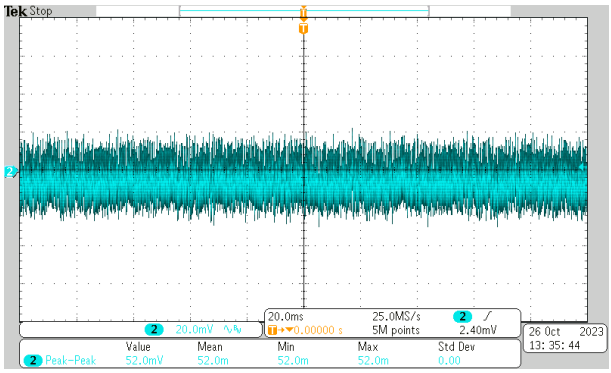


Figure 3-29. 1000 V_{IN} 2-A Load Output Voltage Ripple

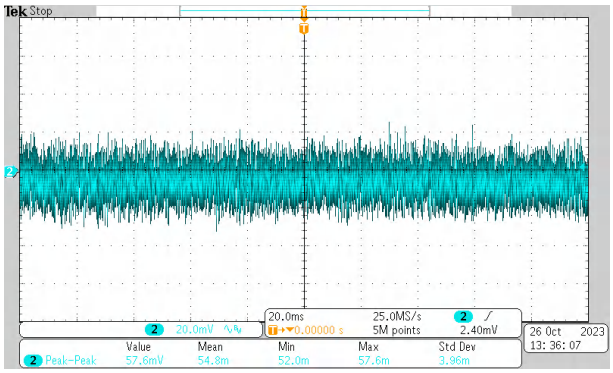


Figure 3-30. 1000 V_{IN} 4-A Load Output Voltage Ripple

3.3 Load Transients

The following images show the load transient waveforms, when performing open load to full load tests. The open load on time was set to 400 ms to make sure the time is sufficient for output voltage settle back to normal regulation voltage, and full load on time was set to 40 ms.

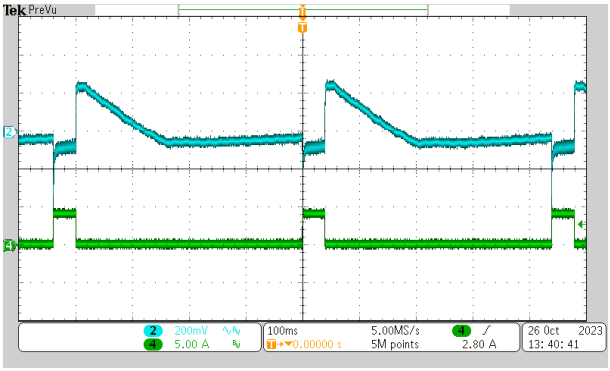


Figure 3-31. Open Load to 4-A Load Dynamic at 300 V_{IN}, V_{OUT} (Blue), I_{OUT} (Green)

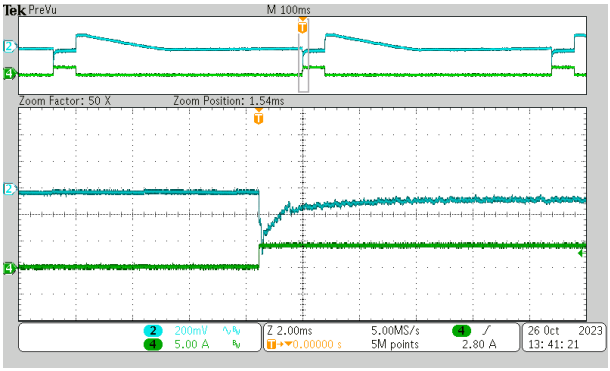


Figure 3-32. Open Load to 4-A Load Dynamic at 300 V_{IN}, Zoom of Undershoot V_{OUT} (Blue), I_{OUT} (Green)

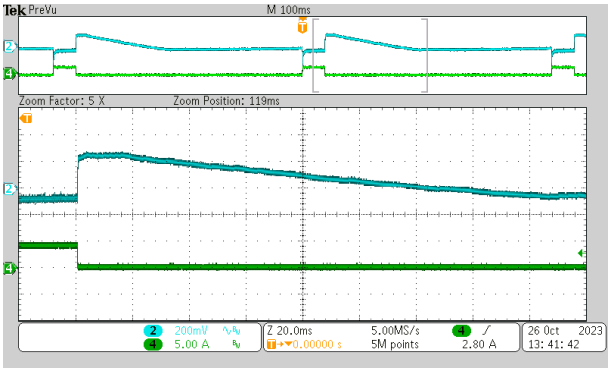


Figure 3-33. Open Load to 4-A Load Dynamic at 300 V_{IN}, Zoom of Overshoot V_{OUT} (Blue), I_{OUT} (Green)

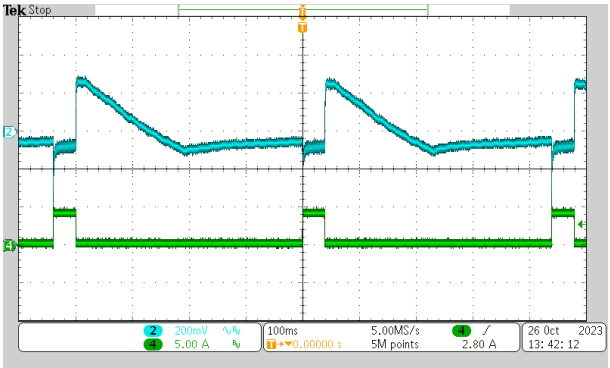


Figure 3-34. Open Load to 4-A Load Dynamic at 600 V_{IN}, V_{OUT} (Blue), I_{OUT} (Green)

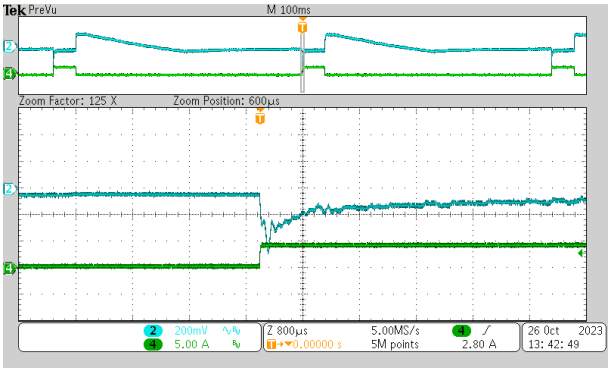


Figure 3-35. Open Load to 4-A Load Dynamic at 600 V_{IN}, Zoom of Undershoot V_{OUT} (Blue), I_{OUT} (Green)

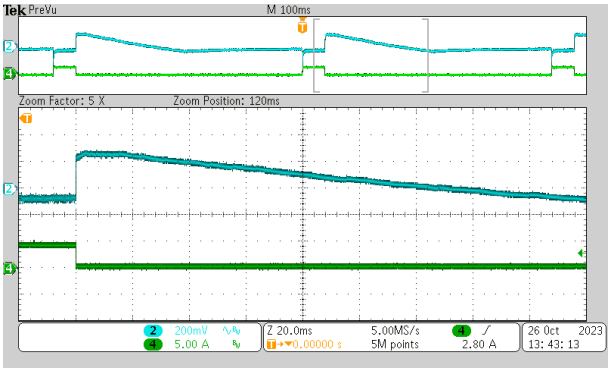


Figure 3-36. Open Load to 4-A Load Dynamic at 600 V_{IN}, Zoom of Overshoot V_{OUT} (Blue), I_{OUT} (Green)

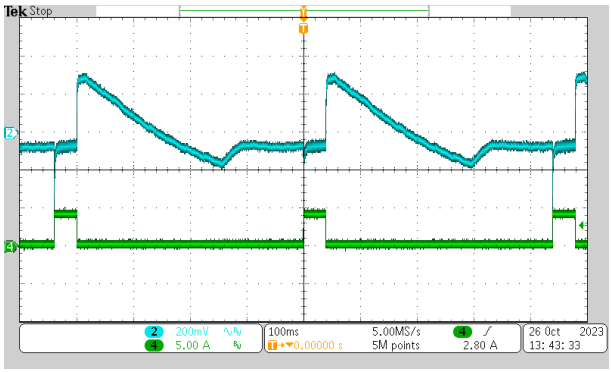


Figure 3-37. Open Load to 4-A Load Dynamic at 1000 V_{IN}, V_{OUT} (Blue), I_{OUT} (Green)

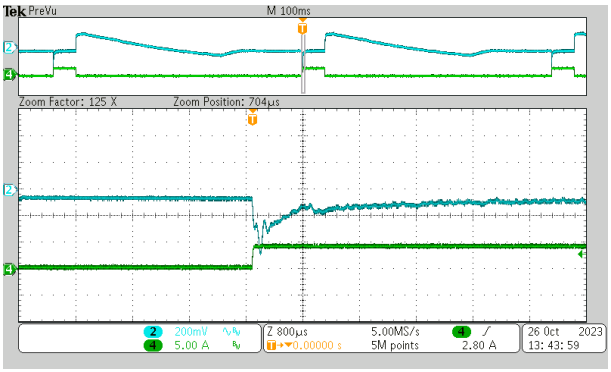


Figure 3-38. Open Load to 4-A Load Dynamic at 1000 V_{IN}, Zoom of Undershoot V_{OUT} (Blue), I_{OUT} (Green)

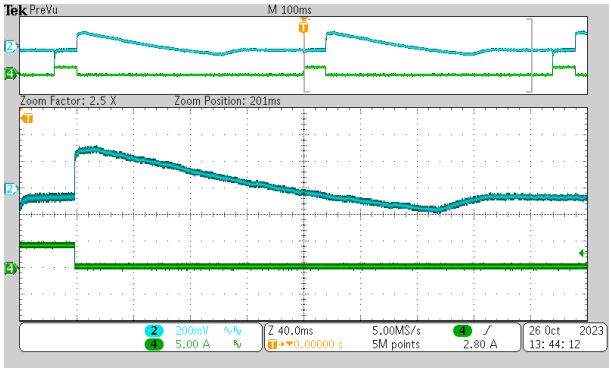


Figure 3-39. Open Load to 4-A Load Dynamic at 1000 V_{IN}, Zoom of Overshoot V_{OUT} (Blue), I_{OUT} (Green)

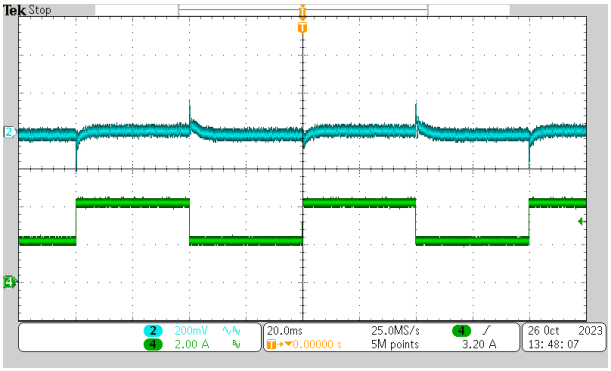


Figure 3-40. 2-A to 4-A Load Dynamic at 1000 V_{IN}, V_{OUT} (Blue), I_{OUT} (Green)

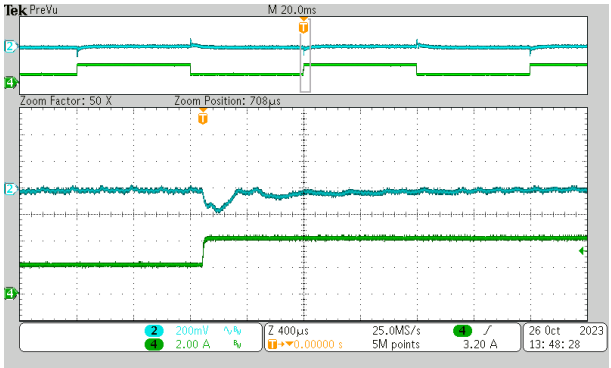


Figure 3-41. 2-A to 4-A Load Dynamic at 1000 V_{IN}, Zoom of Undershoot V_{OUT} (Blue), I_{OUT} (Green)

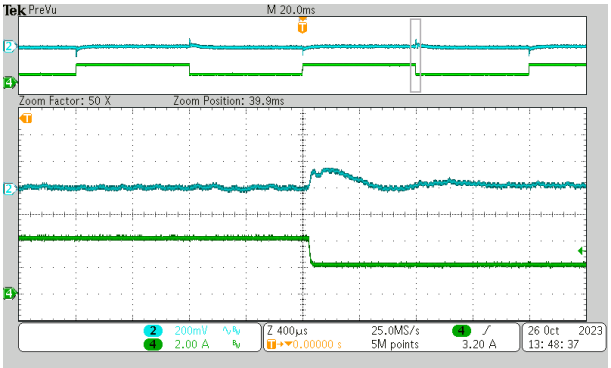


Figure 3-42. 2-A to 4-A Load Dynamic at 1000 V_{IN}, Zoom of Overshoot V_{OUT} (Blue), I_{OUT} (Green)

3.4 Start-Up Sequence

Figure 3-43 through Figure 3-49 show the output voltage start-up and power-down waveforms.

Table 3-1. Start-Up Sequence Timing

Start-Up Time (ms)	300 V_{IN}	600 V_{IN}	1000 V_{IN}
Open load	578	550	542
Full load	610	586	583

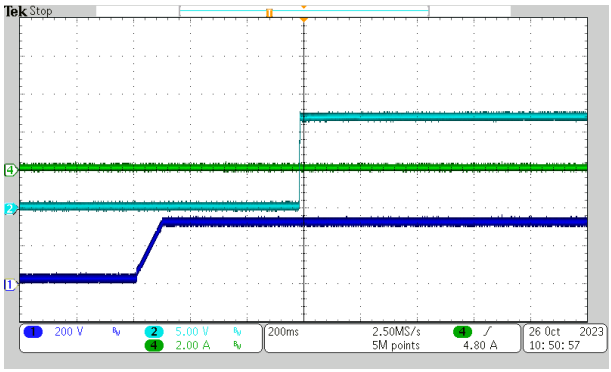


Figure 3-43. 300 V_{IN} Start Up, Open Load V_{IN} (CH1), V_{OUT} (CH2), I_{OUT} (CH4)

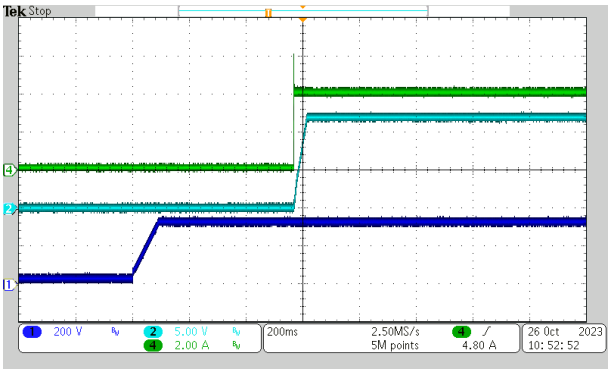


Figure 3-44. 300 V_{IN} Start Up, 4-A Load V_{IN} (CH1), V_{OUT} (CH2), I_{OUT} (CH4)

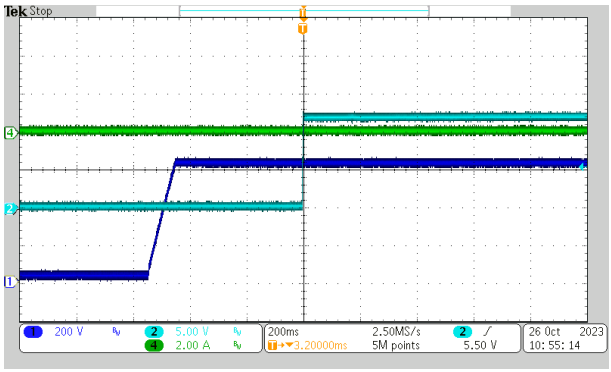


Figure 3-45. 600 V_{IN} Start Up, Open Load V_{IN} (CH1), V_{OUT} (CH2), I_{OUT} (CH4)

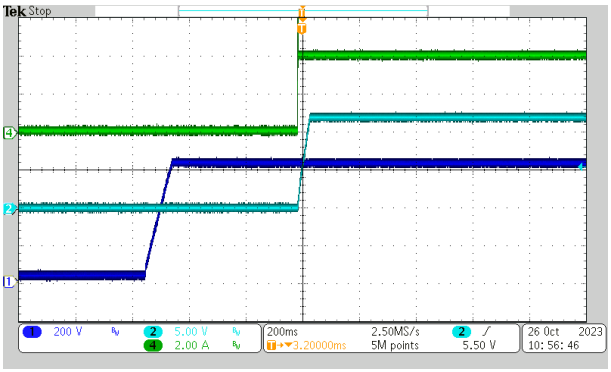


Figure 3-46. 600 V_{IN} Start Up, 4-A Load V_{IN} (CH1), V_{OUT} (CH2), I_{OUT} (CH4)

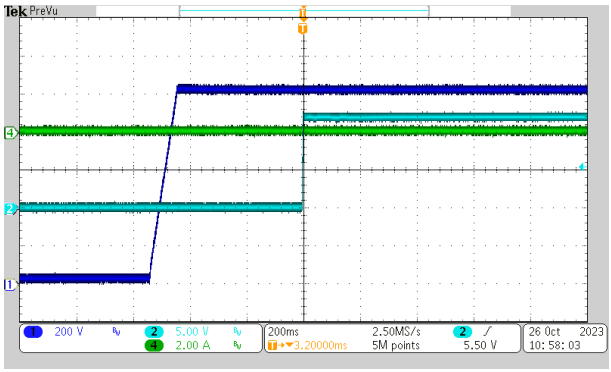


Figure 3-47. 1000 V_{IN} Start Up, Open Load V_{IN} (CH1), V_{OUT} (CH2), I_{OUT} (CH4)

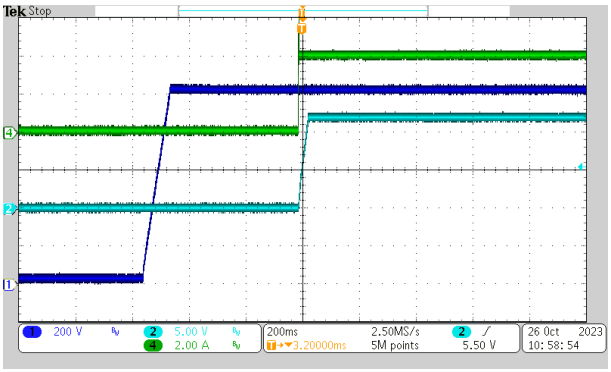


Figure 3-48. 1000 V_{IN} Start Up, 4-A Load V_{IN} (CH1), V_{OUT} (CH2), I_{OUT} (CH4)

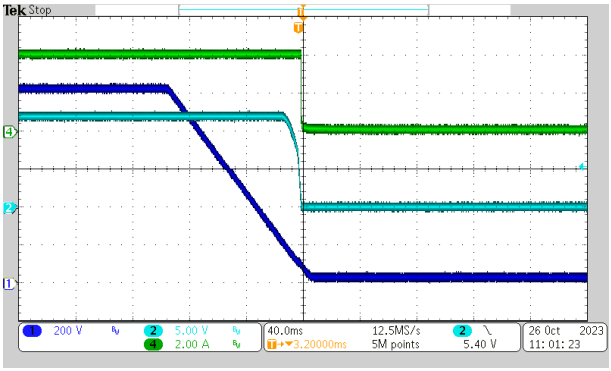


Figure 3-49. 1000 V_{IN} Power Down, 4-A Load V_{IN} (CH1), V_{OUT} (CH2), I_{OUT} (CH4)

3.5 Overcurrent Protection (OCP)

Overcurrent protection (OCP) was performed at the electrical load side, Table 3-2 shows OCP at different input voltage.

Table 3-2. OCP at Various Input Voltages

Parameter	300 V_{IN}	600 V_{IN}	1000 V_{IN}
OCP (A)	4.307	4.338	4.417

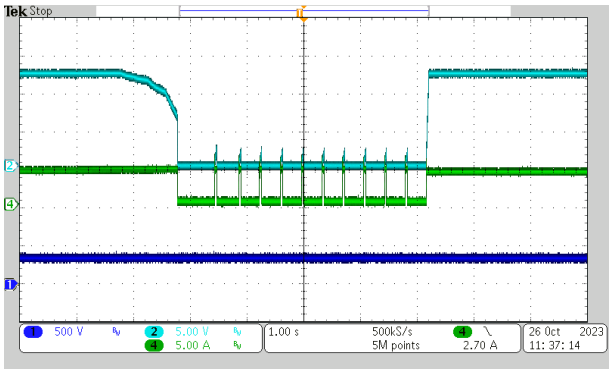


Figure 3-50. OCP at 300 V_{IN}

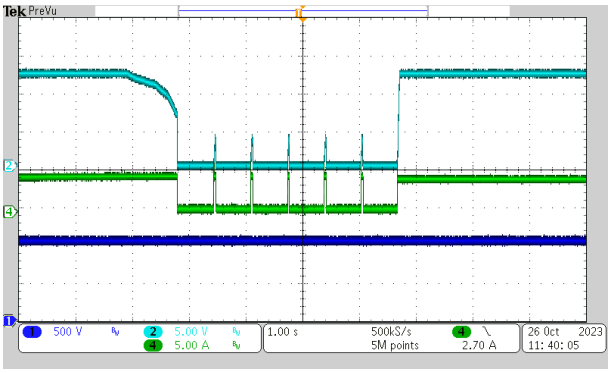


Figure 3-51. OCP at 600 V_{IN}

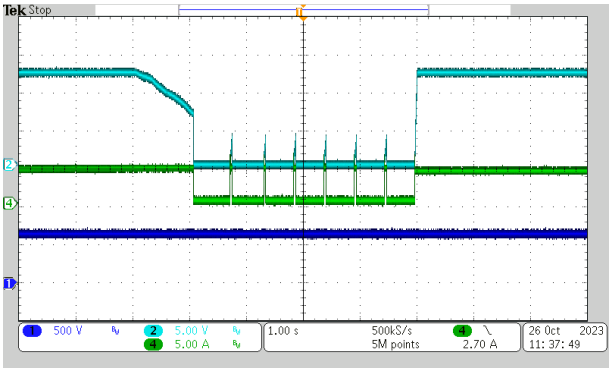


Figure 3-52. OCP at 1000 V_{IN}

3.6 Short-Circuit Protection

Figure 3-53 through Figure 3-55 show the short-circuit protection (SCP) tests performed at the PCB end.

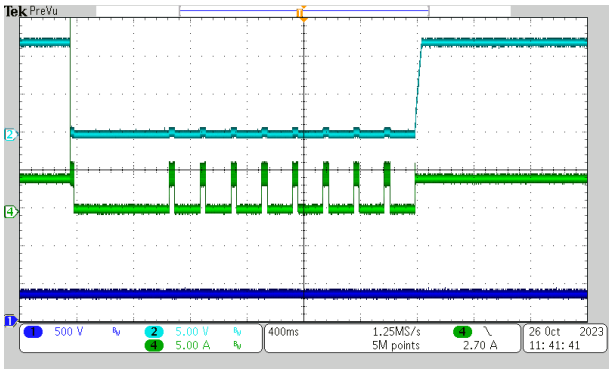


Figure 3-53. SCP at 300 V_{IN}

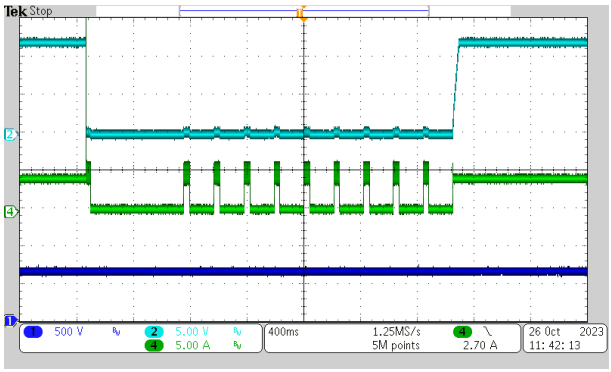


Figure 3-54. SCP at 600 V_{IN}

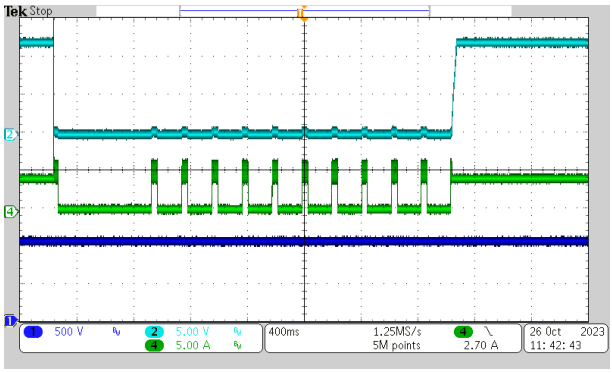


Figure 3-55. SCP at 1000 V_{IN}

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265