Collin Wells, Ting Ye

TI Designs – Precision: Verified Design

Single-Supply Low-Input Voltage Optimized Precision Full-Wave Rectifier Reference Design

TEXAS INSTRUMENTS

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Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
OPA350	Product Folder
LM7705	Product Folder

Circuit Description

This small-signal optimized single-supply precision absolute value circuit can turn low-level alternating current (ac) signals to positive polarity signals. The circuit is designed to function up to 50 kHz and has excellent linearity at signal levels as low as 5 mVpp. The circuit can be used in sensor acquisition or signal strength indication applications that need to quantify values of low-level input signals which have positive and negative polarities.

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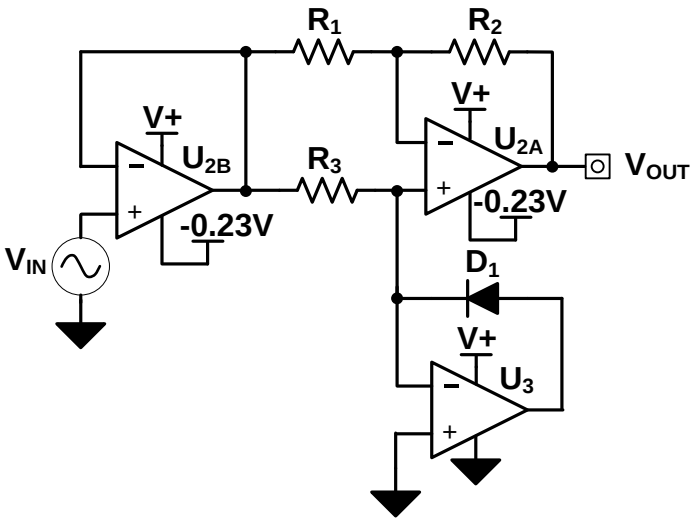
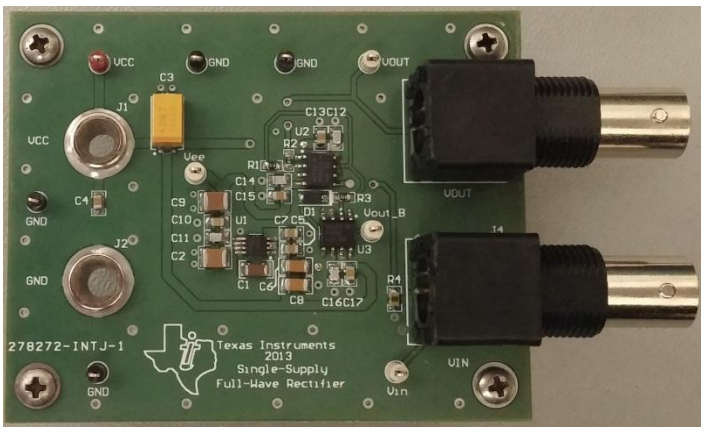




1 Design Summary

The design requirements are as follows:

- Supply Voltage: 5 V
- Input: +/- 2.5 mV to +/- 200 mV
- Output: 2.5 mV to 200 mV Full-Wave Rectified Signal

The goals of this design are to achieve accurate full-wave rectification of low-level signals at frequencies of 50 kHz and less. Figure 1 displays the measured input and output signals with a 1 kHz, 100 mVpp sine-wave input. Channel 2 is the input voltage, Vin and Channel 1 is the output voltage, Vout

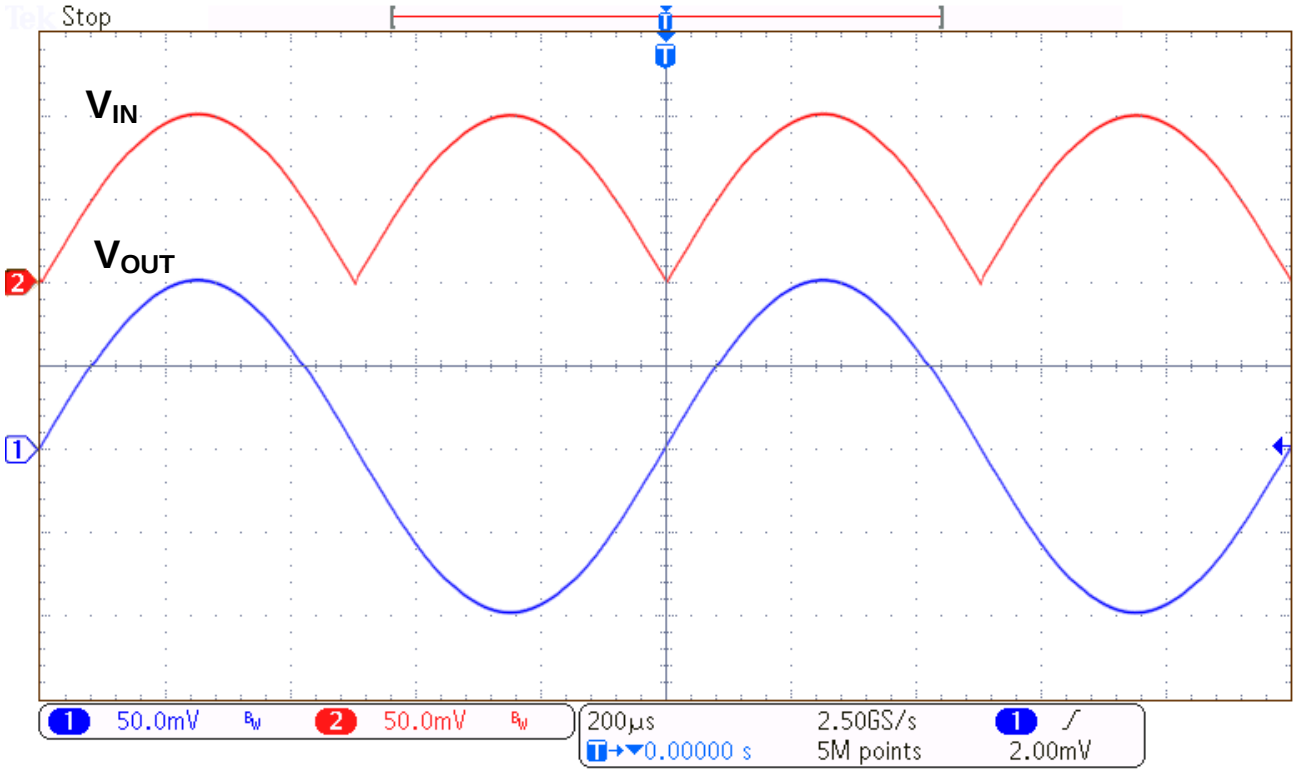


Figure 1: Measured output transient waveform with 1 kHz, 100 mVpp input signal

2 Theory of Operation

A more complete schematic for the single supply full wave rectifier circuit is shown in Figure 2. This topology was chosen to meet the design goals for signal levels as small as 5 mVpp. U_{2B} is used to buffer the input signal and prevents gain interactions between the feedback impedance of U_{2A} and the source resistance of the signal source. With U_{2B} in the circuit, the input impedance is set by R_4, the source termination resistor. U_{2B} can be removed to allow bipolar input signals with a peak-to-peak voltage twice as large as the supply voltage at the expense of decreased input impedance as described in Section 7.

This design differs from traditional single-supply rectifiers and allows for excellent linearity at low-level signals by using the LM7705 negative bias generator. The LM7705 generates a -0.23 V output from the +5V supply that is connected to negative supply pin of U_{2A} and U_{2B}. This allows a rail-to-rail input/output op amp to accept signals and create outputs that are below the circuit ground (GND) potential of 0 V.

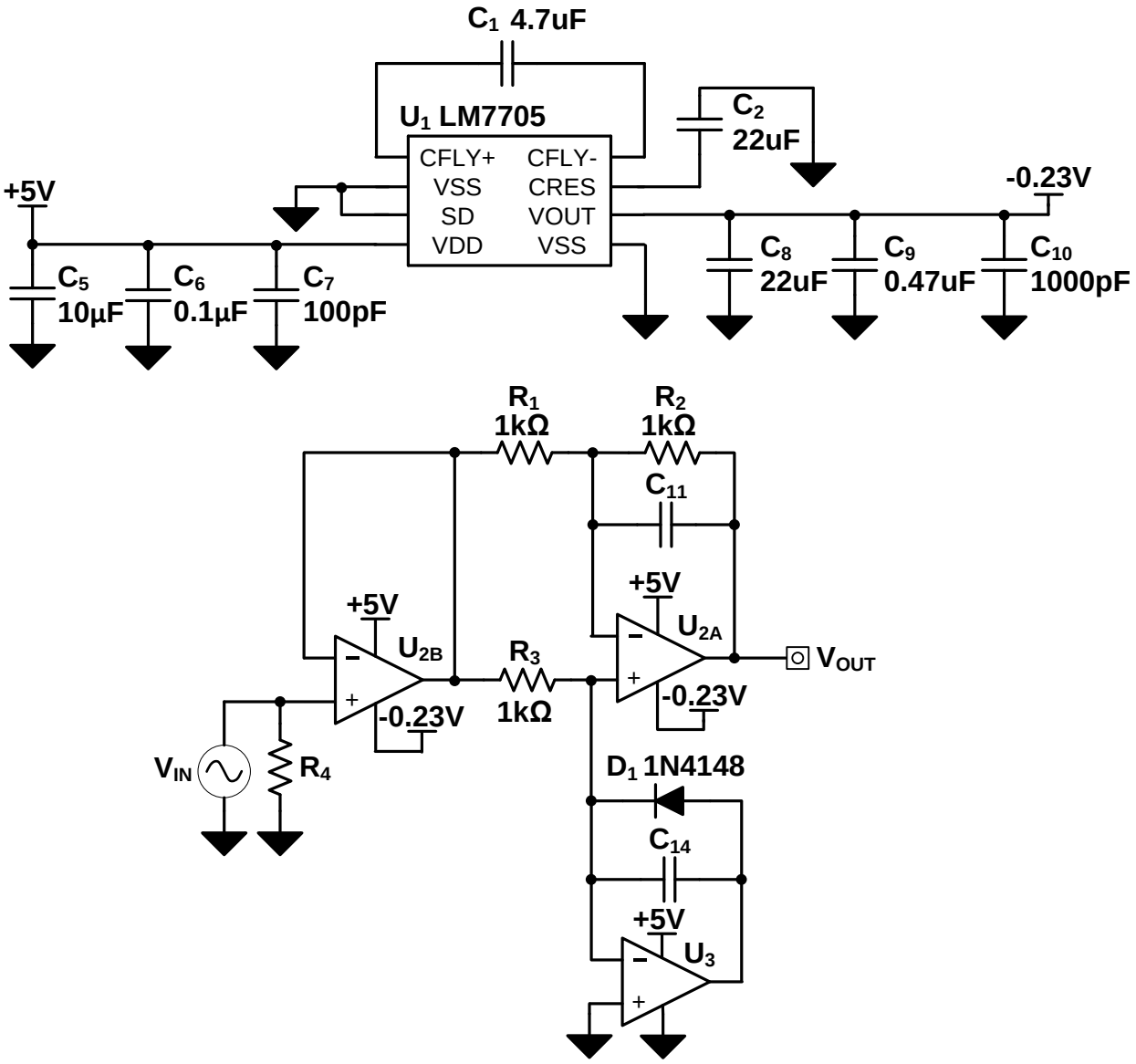


Figure 2: Circuit schematic

2.1 Simplified Circuit for Positive Input Signals

The circuit schematic and transfer function for positive input signals is shown in Figure 3 and (1. When the input is positive, D_1 becomes reverse biased and acts as an open circuit. This effectively removes U_3 from the circuit. In this configuration, U_{2B} buffers the input signal into both the non-inverting and inverting nodes of U_{2A} making it act as a summing amplifier. The transfer function for positive inputs can be solved using superposition and is simply the sum of the inverting and non-inverting gains. This creates a unity gain output regardless of the values of R_1 and R_2.

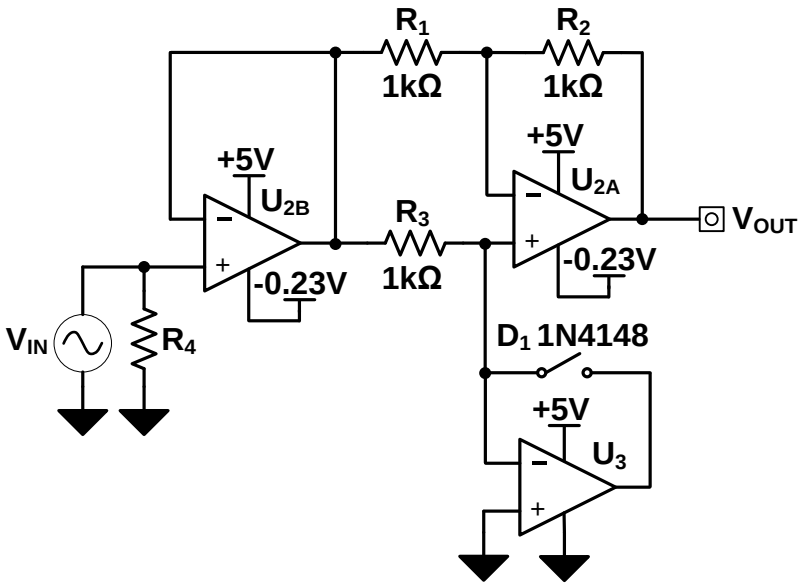


Figure 3: Simplified circuit with a positive input signal

$$\frac{V_{OUT}}{V_{IN}} = \left(-\frac{R_2}{R_1}\right) + \left(1 + \frac{R_2}{R_1}\right)$$
$$V_{OUT} = V_{IN} \quad (1)$$

2.2 Simplified Circuit for Negative Input Signals

The circuit and transfer function for negative inputs are shown in Figure 4 and Equation 2. Negative input signals forward bias D_1 providing a closed-loop unity-gain feedback path for U_3. Therefore, U_3 will buffer the GND voltage applied to its non-inverting input. With the non-inverting input of U_{2A} set to GND, it acts as a standard inverting amplifier. Setting R_1 and R_2 to equal values results in an exact inversion of the negative input signals, achieving the full-wave rectified output.

R_3 should be sized such that the current flowing through it while U_3 is holding the non-inverting input of U_{2A} to GND is not significant to cause output errors of either U_{2B} or U_3 due to current draw.

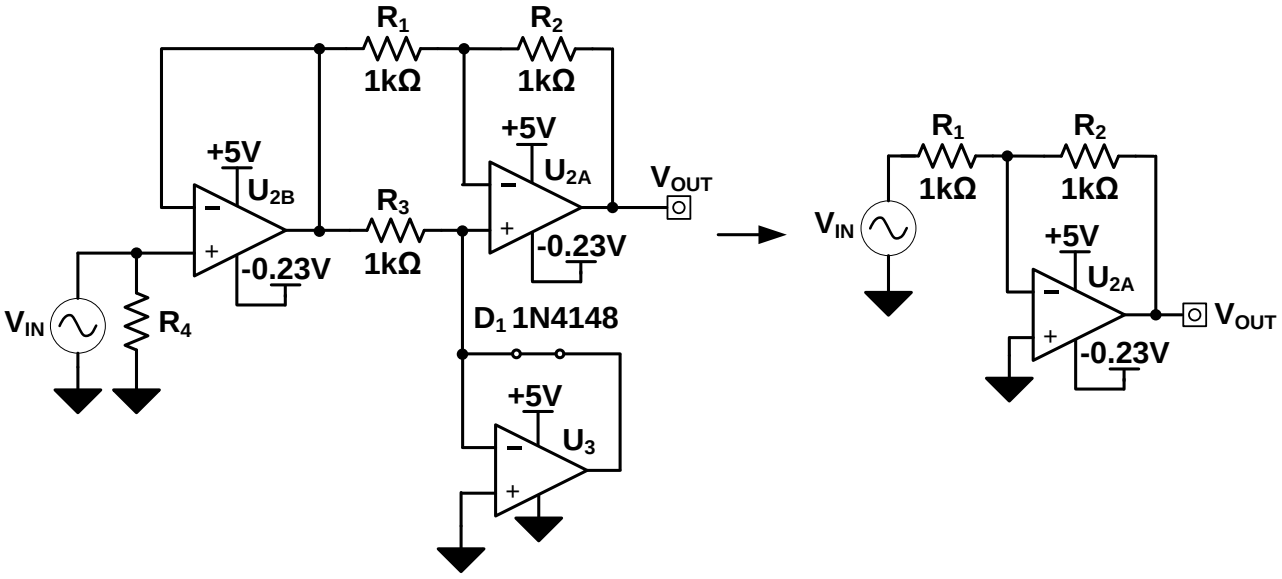


Figure 4: Simplified circuit with a negative input signal

$$\frac{V_{OUT}}{V_{IN}} = \left(-\frac{R_2}{R_1}\right)$$
$$\text{If } R1 = R2$$
$$V_{OUT} = -V_{IN} \quad (2)$$

3 Component Selection

3.1 Operational Amplifier

Since transient waveform integrity is the primary concerns in this circuit, choose operational amplifiers (op amps) with key specifications including **low total-harmonic-distortion (THD), wide bandwidths, high slew rate, high open-loop gain (A_{OL}), and low noise.** Rail-to-rail input (RRI) and rail-to-rail outputs (RRO) are advantageous because they increase the circuit dynamic range. The OPA350 high-speed rail-to-rail op amp has 0.0006% THD+N at 1 kHz, 38 MHz unity-gain bandwidth, slew rate of 22 V/µs, 122 dB of open-loop gain, and 7 nV/ √Hz input noise at 10 kHz making it an excellent choice for a high performance version of this circuit. Other amplifier options for this application include the OPA320, OPA322, OPA354 or OPA356 as further discussed in Section 7.

3.2 Diode

Important specifications of the D_1 diode are low forward voltage (VF), fast switching speed (TT), low diode capacitance (CD), and low leakage current (IR). Schottky diodes usually have fast transition time but lager leakage current. Standard diodes have low reverse current. The diode used in this design is fast switching diode 1N4148 based on its performance and cost. Table 1 compares several diode candidates.

Table 1. Diode Selection Parameters

	1N4148	BAT42W	BAS70
VF	720mV at IF=5mA	400mV at IF=10mA	410mV at IF=1mA
TT	4ns(max)	5ns(max)	5ns(max)
CD	4pF(max) at 1MHz, VR=0V	7pF(typ) at 1MHz, VR=1V	2pF(max) at 1MHz, VR=0V
IR	25nA at VR=20V	500nA at VR=25V	100nA at VR=50V

3.3 Passive Components

Resistors R_1 and R_2, which set the gain, are the most crucial passive components to ensure precise full-wave rectification. The resistors were selected for 0.1% tolerance to achieve good gain accuracy. Resistors R_1 and R_2 were chosen to be 1 kΩ to limit thermal noise and to prevent the leakage current of the diodes from causing errors.

While they were not required for this version of the design with the OPA350, the compensation capacitors, C_{18} and C_{19}, should be selected as C0G/NP0 dielectrics with the proper voltage rating.

The tolerance of the other passive components in this circuit can be selected for 1% or above since the components will not directly affect accuracy of this circuit.

4 Simulation

The TINA-TI™ schematic shown in Figure 5 includes the circuit values obtained in the design process. Since currently there is no macro model for LM7705, it is not included and has been replaced with a -0.23 V voltage source, Vee. DC analysis displays a dc offset voltage of -219.06 µV and dc quiescent current of 5.2 mA per OPA350 channel.

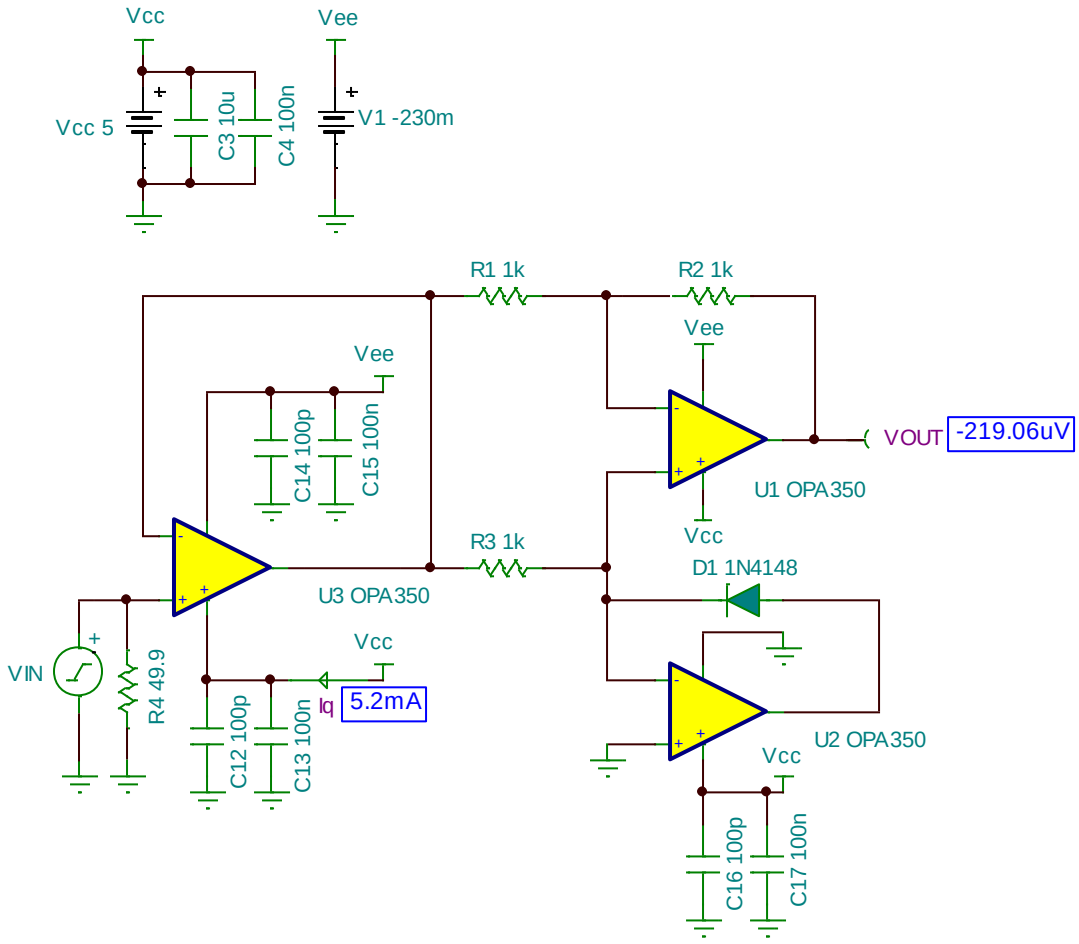
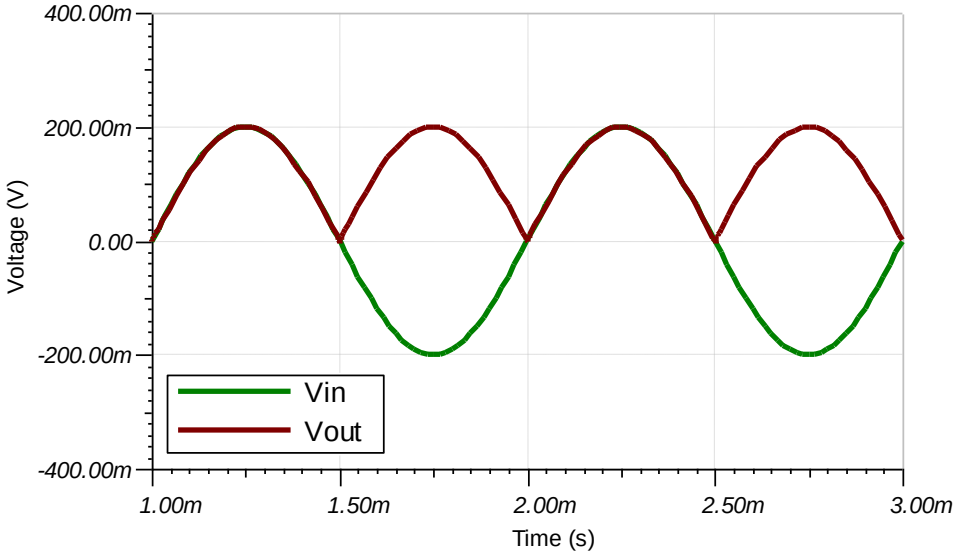


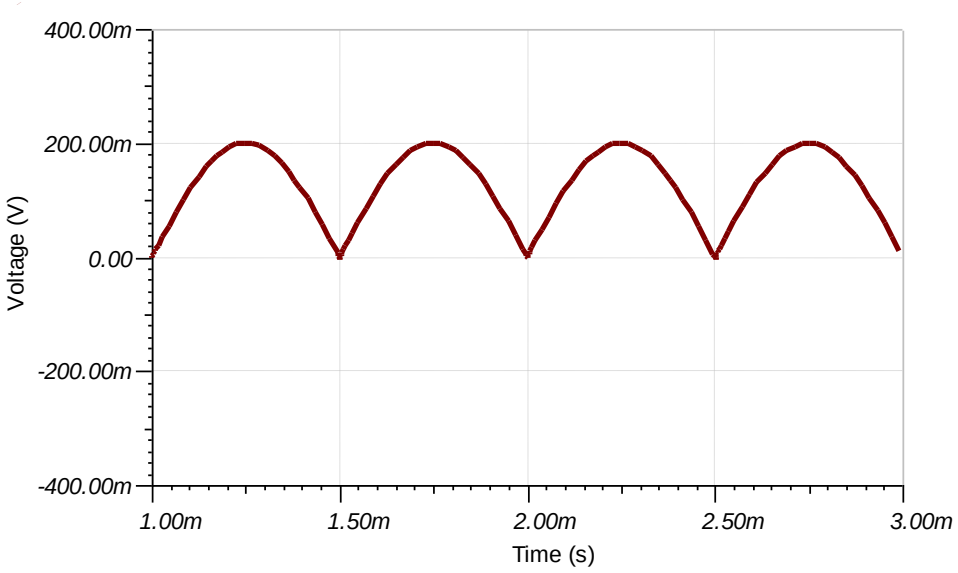
Figure 5: TINA-TI™ simulation schematic showing dc output offset and quiescent current

4.1 Transient Response

The transient response of the design with a 400 mVpp, 1 kHz sine-wave input signal is shown in Figure 6. The output is precisely full-wave rectified.



A. Transient simulation with +/- 200 mV at 1 kHz sinusoid wave input

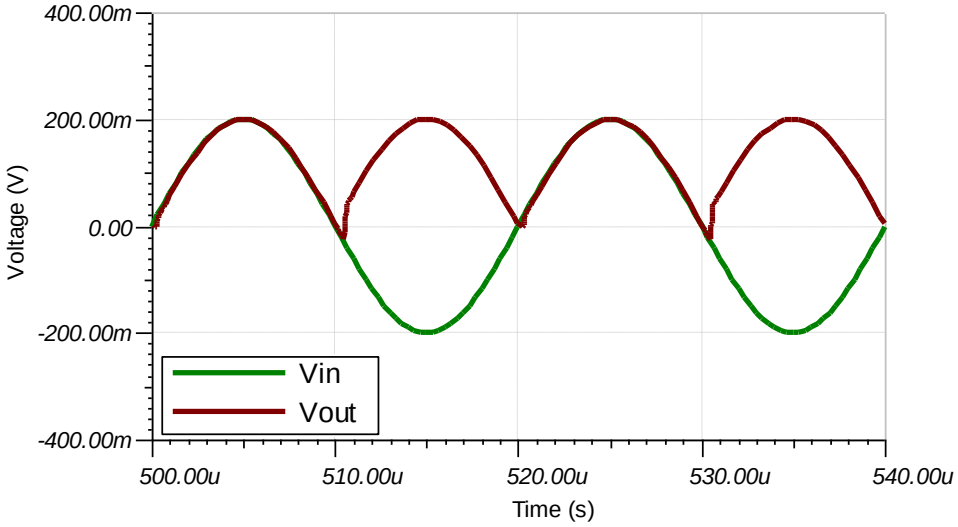


B. Simulated output with +/- 200 mV at 1 kHz sinusoid wave input

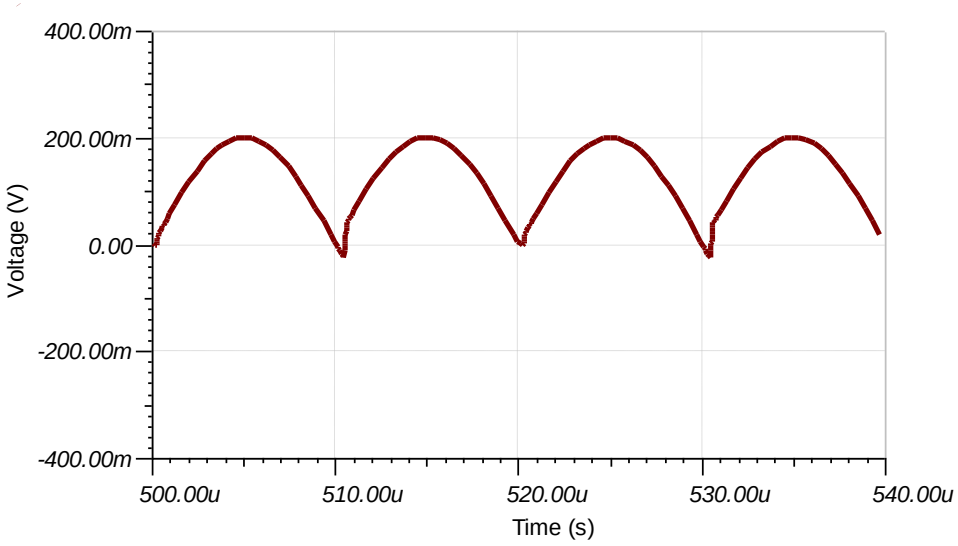
Figure 6: TINA-TI™ simulated transient waveform at 1 kHz with +/- 200 mV sine-wave input

As the input signal frequency increases, the transition edges of the full-wave rectified output begin to get distorted. This design was created to allow for minimal distortion at the maximum input frequency of approximately 50 kHz as shown in the simulation in Figure 7. The distortion is caused by the time it takes to transition from forward biasing to reverse biasing D_1. The limitations are caused by the junction capacitance (CJ) and transition time (TT)

of the diodes, as well as the slew rate and output current limits of U_{2B}.



A. Transient simulation with +/- 200 mV at 50 kHz sinusoid wave input



B. Simulated output with +/- 200 mV at 50 kHz sinusoid wave input

Figure 7: TINA-TITM simulated transient waveform at 50 kHz with +/- 200 mV sine-wave input

The circuit performance with a low-level 5 mVpp, 1 kHz input signal is shown in Figure 8. Low-level input signals have a limited useful bandwidth compared to larger amplitude signals because the distortion dominates the output waveform easier at the low signal levels. Figure 9 shows how the distortion begins to dominate the output with a low-level 5 mVpp input at just 5 kHz.

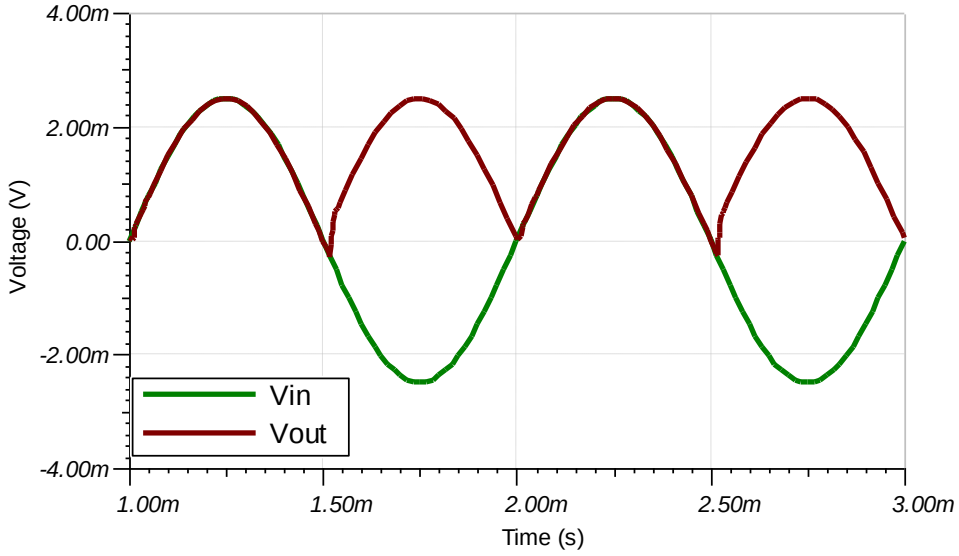


Figure 8: TINA-TITM simulated output at 1 kHz with 5mVpp sine-wave input

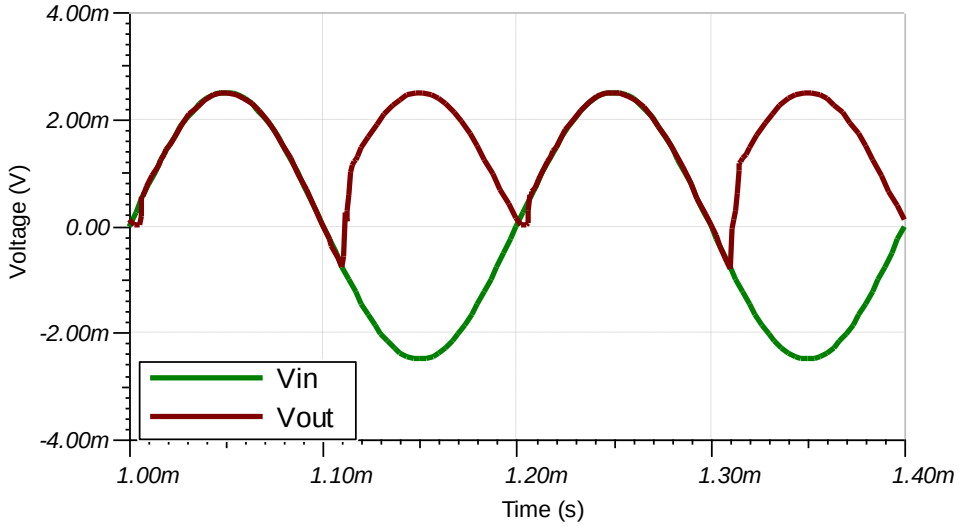


Figure 9: TINA-TITM simulated output at 5 kHz with 5mVpp sine-wave input

4.2 Small-Signal Transitions

The small-signal transition time of the circuit was tested by applying a step response to the input that caused the output changed by approximately 50 mV. Figure 10 shows that it takes a little over 1 µs for the output to transition. The output will be distorted and not properly rectified during this transition time. Smaller level input signals result in less overdrive of the input stage and will result in longer transition times. The results in Figure 10 also indicate the design should suffer from limited overshoot or ringing and is stable.

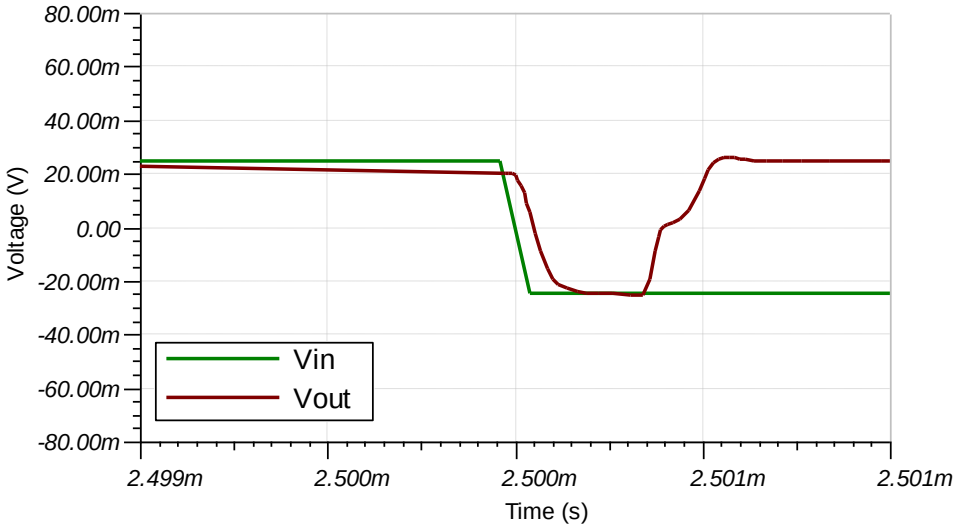


Figure 10: TINA-TI™ simulated output step response at input of 50 mVpp

4.3 Simulated Result Summary

The simulated results show the design functions well at the maximum input signal level up to the maximum frequency of 50 kHz with limited distortion. Full-wave rectification of low-level signals is possible at speeds less than 1 kHz with limited distortion.

5 PCB Design

The PCB schematic and bill of materials can be found in the Appendix A.1 and A.2.

5.1 PCB Layout

An important PCB layout concern for this design is to avoid allowing the LM7705 output to capacitively couple with signal traces. If the traces are routed too close together, the small switching noise of the LM7705 will couple to the inputs and will appear on the output signal. Keeping the LM7705 output traces short and providing good return paths will also help reduce noise. Additionally, follow standard precision PCB layout guidelines including: using ground planes, proper power supply decoupling, keeping the summing node as small as possible, and using short thick traces for sensitive nodes. The layout for the design is shown in Figure 11.

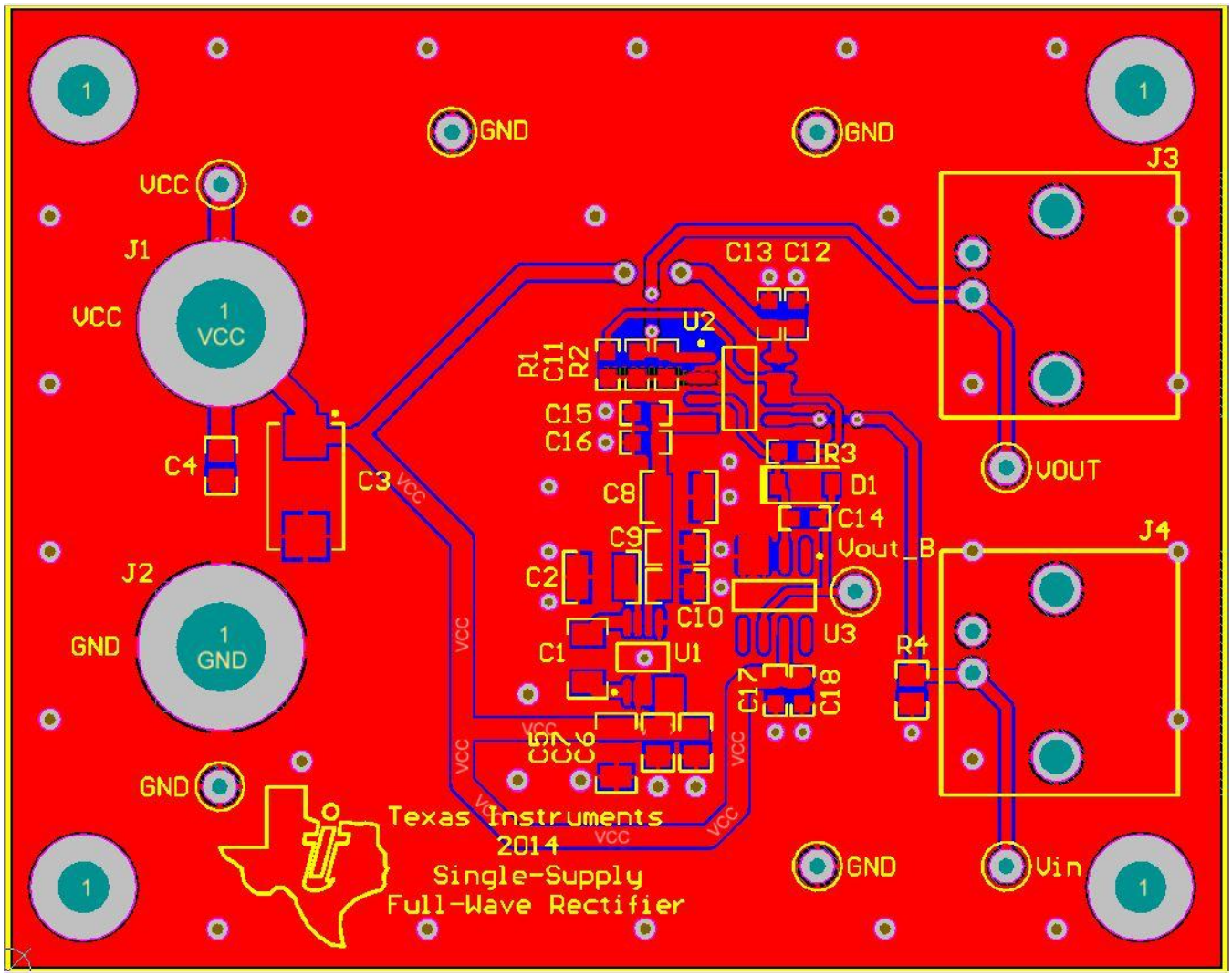


Figure 11: Altium PCB Layout

6 Verification & Measured Performance

6.1 DC Measurements

DC measurements were made for the offset voltage and the quiescent current for five units. The average values are reported in Table 2.

Table 2. Measured DC result summary

	Measured Value
Output Offset Voltage (µV)	68.15
Quiescent Current (mA)	14.17

6.2 Transient Measurements

The transient response of the design with a 400 mVpp, 1 kHz sine-wave input signal is shown in Figure 12. The design creates a very accurate full-wave rectified output with minimal distortion.

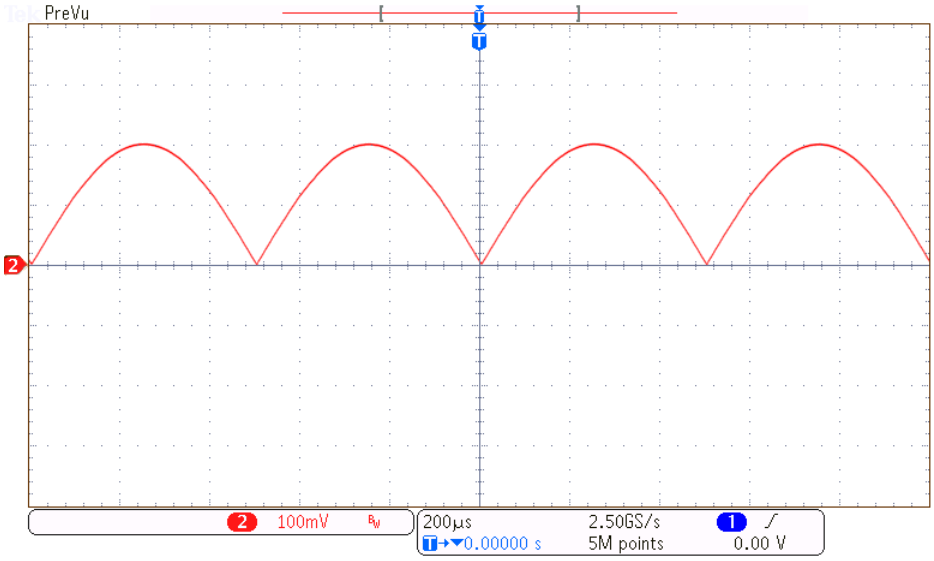


Figure 12: Measured output with 400 mVpp at 1 kHz sine-wave input

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Figure 13 displays the measured transient response with a 50 kHz, 400 mVpp input. The output waveform achieves good performance with only slight distortion, conforming to the design goals.

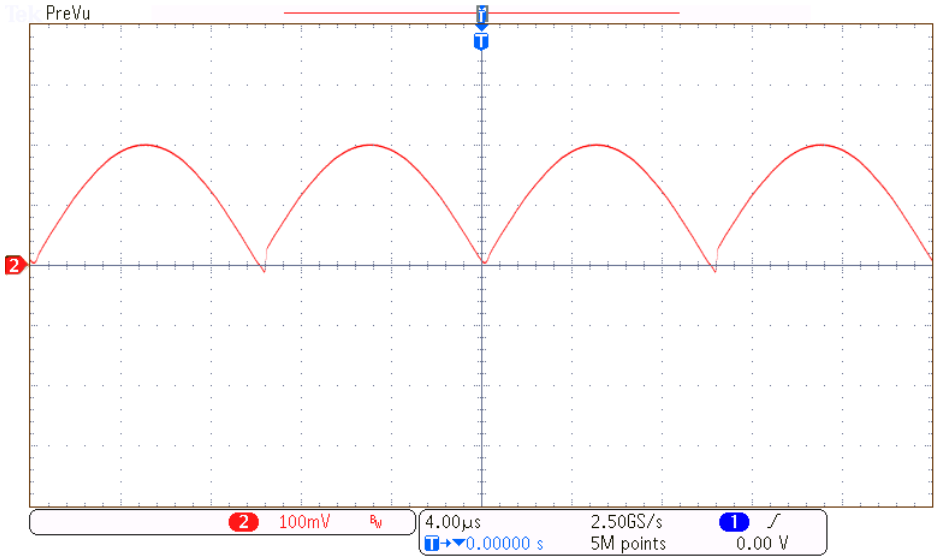


Figure 13: Measured output with 400 mVpp at 50 kHz sine-wave input

Figure 14 and Figure 15 display the performance with low-level 5 mVpp signals at 1 kHz and 5 kHz respectively. The distortion is minimal at 1 kHz but increases quickly as the input frequency increases. The output waveforms match simulation results shown in Figure 8 and Figure 9.

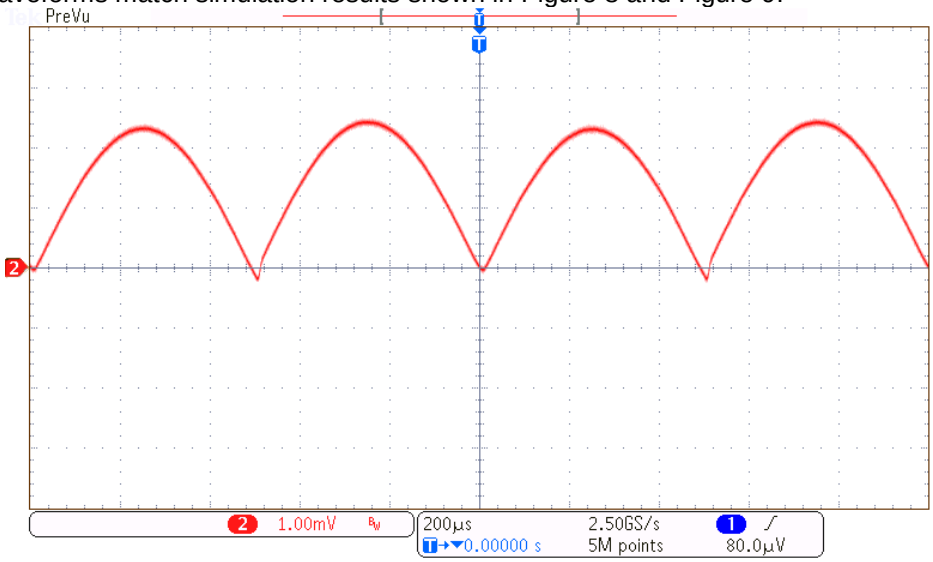


Figure 14: Measured output with 5 mVpp at 1 kHz sine-wave input

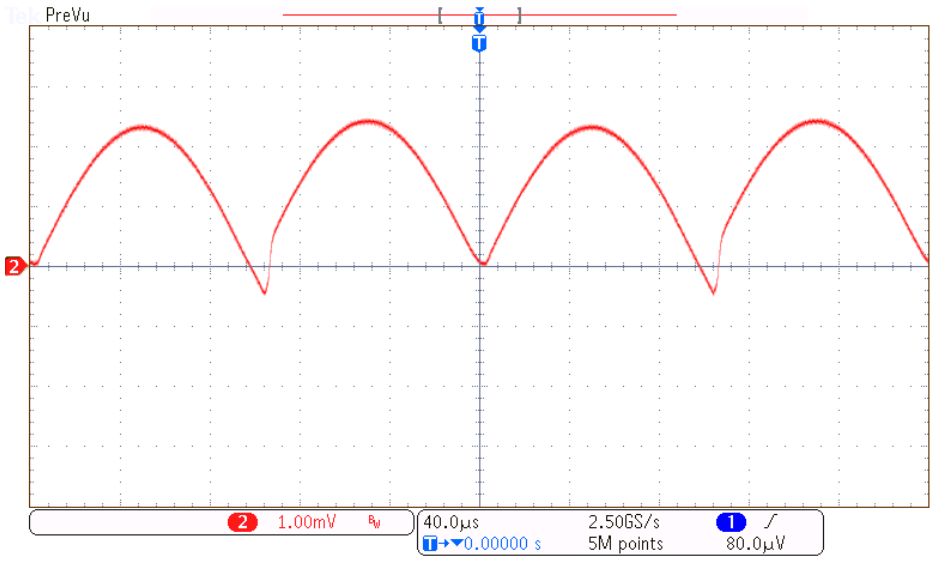


Figure 15: Measured output with 5 mVpp at 5 kHz sine-wave input

6.3 Small Signal Transition

The small-signal transition of the circuit was tested by applying a step response to the input that caused the output changed by approximately 50 mV. The results are shown in Figure 16. The overshoot and ringing can be reduced by increasing the values of the capacitors across R2 and the diode or using smaller values for the resistors. Smaller values for R_1 and R_2 will also help improve the small-signal response but the required output current will begin to cause the output voltage to decrease creating an offset between the output and the desired rectified output.

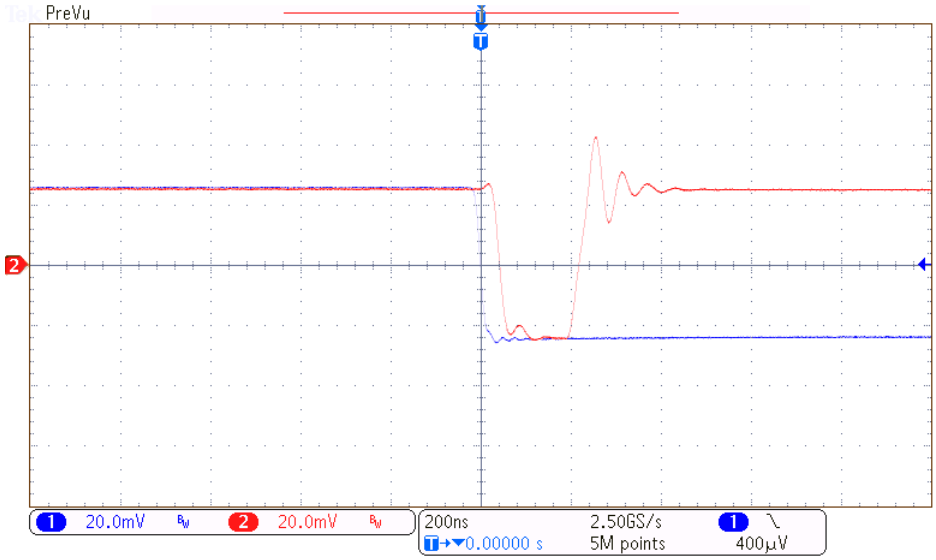


Figure 16: Measured output step response at input 50 mVpp and 1 kHz

6.4 Output Fast Fourier Transform (FFT)

The FFT shown in Figure 17 was taken from 20 Hz to 10 kHz to view the output spectrum of the circuit with a 400 mVpp and 1 kHz input signal. Since harmonics of a full wave rectifier are the double of base frequency, the harmonic tones are even harmonics at 2, 4, 6, 8, and 10 kHz with a 1 kHz, 400 mVpp input signal.

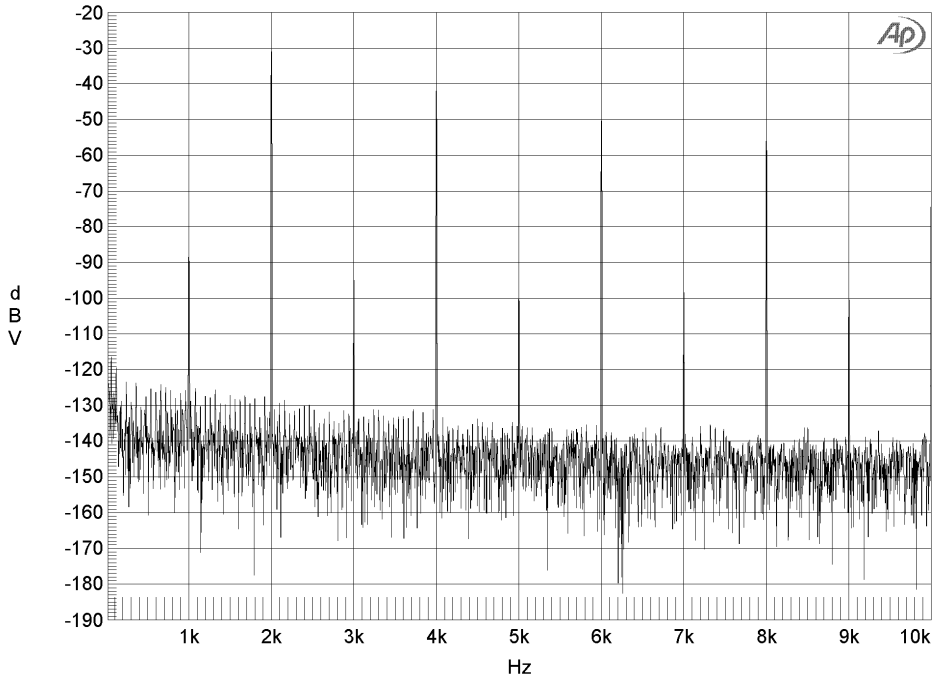


Figure 17: FFT of output at 1 kHz with 400 mVpp sine-wave input

6.5 Measured Result Summary

The measured transient results show the maximum frequency is approximately 50 kHz with a +/- 200 mV input sine-wave before distortion begins to affect the signal integrity. The design also succeeds in achieving a low distortion full-wave rectified output with a 5 mVpp low-level input signal at frequencies below 1 kHz with minimal distortion.

7 Modifications

An absolute circuit can be implemented by many op amps provided they have the proper bandwidth and slew rate for the input signals. However, as mentioned in the component selection section, this circuit will work best with a low noise, low THD, wide bandwidth, high slew rate, and high A_{OL} op amp. Other single supply amplifiers suitable for this design are described as follows. OPA320 and OPA322 are other precision amplifiers with modest bandwidths but better low frequency performance. The OPA353, OPA354, and OPA356 are high speed op amps which have high bandwidth and slew rate; however, due to their offset and to obtain a higher dynamic range, they should be applied in the design without input buffer and LM7705. These op amps' performance is summarized in Table 3.

Table 3. Alternate Single Supply Amplifiers

Amplifier	Channel	GBW (MHz)	SR (V/us)	Aol (dB)	Noise at 1kHz (nV/rtHz)	THD+N (%)	Vos, Max (mV)	Vos Drift(uV/C)	IB, Max (pA)	Iq per Channel, Max (mA)
OPA320	1	20	10	132	8.5	0.0005 at	0.15	1.5	0.9	1.75

						fin=10kHz				
OPA322	1	20	10	130	8.5	0.0005 at fin=10kHz	2	1.8	10	1.9
OPA350	1	38	22	122	15	0.0006 at fin=1kHz	0.5	4	10	7.5
OPA353	1	44	22	122	15	0.0006 at fin=1kHz	8	5	10	8
OPA354	1	250	150	106	70	0.0178 at fin=1MHz	8	4	50	6
OPA356	1	450	300	92	80	0.0891 at fin=1MHz	9	7	50	11

This circuit was designed to optimize the full-wave rectification performance of low-level signals below 200mVpp. As a result the input buffer, U_{2B}, was included to prevent the source impedance of the input signal from creating a gain error that leads to an unbalanced output for the positive and negative cycles. With a -230 mV negative supply, the output stage of U_{2B} limits the negative input signal magnitude to roughly -200 mV before the output stage begins to saturate. Without the input buffer this topology can accept inputs that are double the supply voltage. So a +5V single-ended supply can handle +/-5V inputs as shown in Figure 18 below.

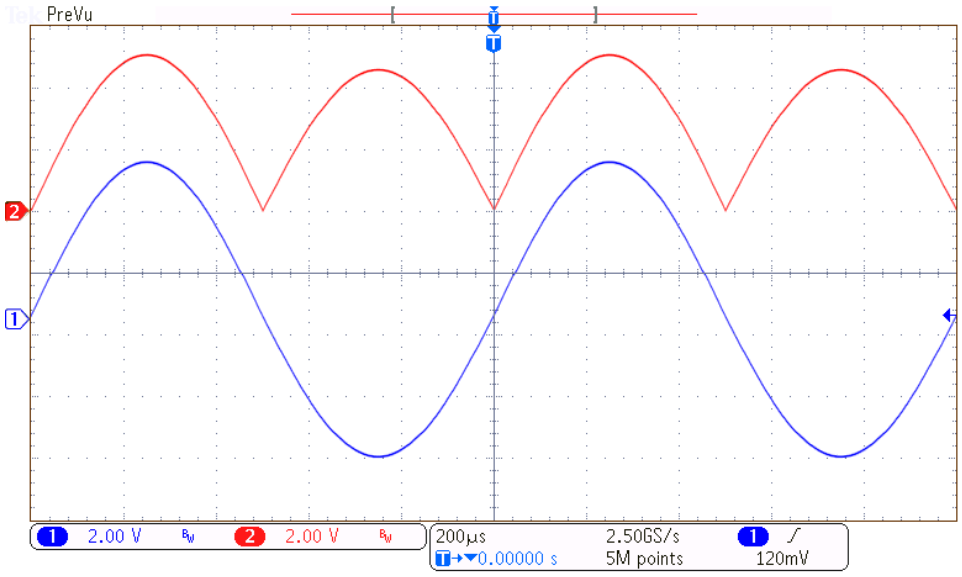


Figure 18: Output at 1 kHz with 4.95 Vp sine-wave input of the circuit without input buffer

8 About the Author

Ting Ye is a field application engineer based in Taipei who supports industrial and precision customers. She performed a six month rotation working with the Precision Linear group where she supported op amp and current loop products for industrial applications.

Collin Wells is an applications engineer in the Precision Linear group at Texas Instruments where he supports industrial products and applications. Collin received his BSEE from the University of Texas, Dallas.

9 Acknowledgements & References

1. *R. Elliott. (2010 Feb. 27) Precision Rectifiers. Available: http://sound.westhost.com/appnotes/an001.htm*

2. *D. Jones and M. Stitt. (1997, Dec.). Precision Absolute Value Circuits. Available: http://www.ti.com/lit/an/sboa068/sboa068.pdf*

Appendix A.

A.1 Electrical Schematic

The Altium electrical schematic for this design can be seen in Figure A.1.

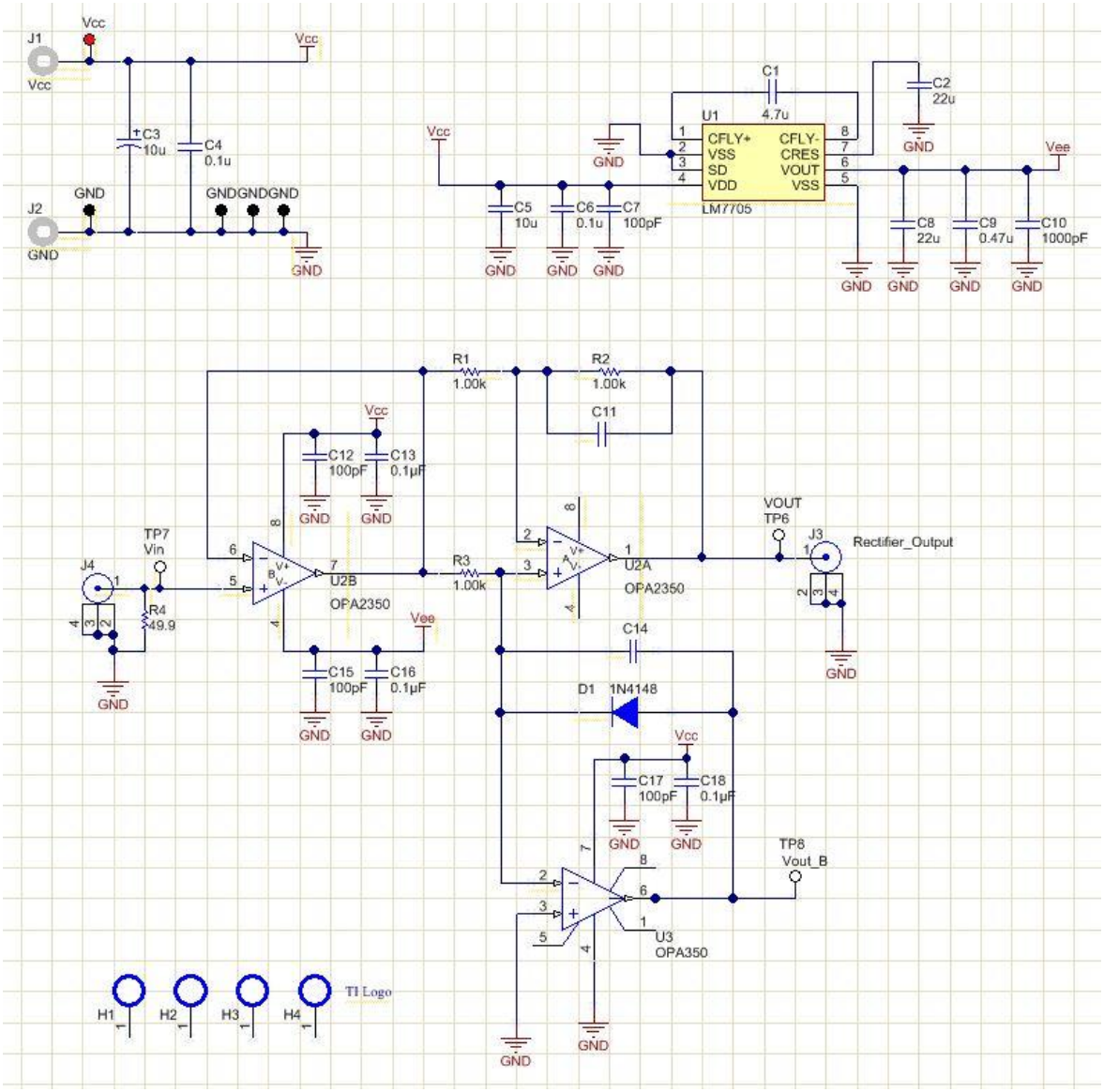


Figure A-1: Electrical Schematic

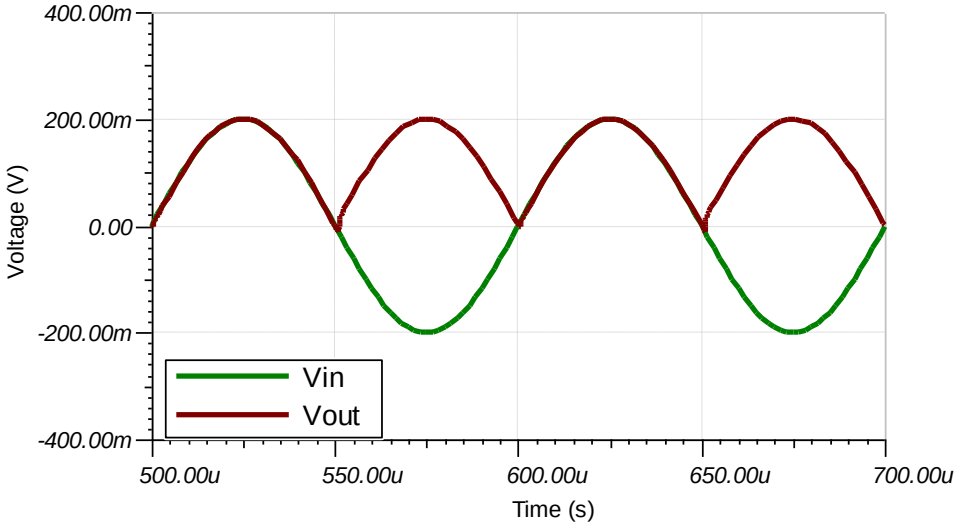
A.2 Bill of Materials

The bill of materials for this circuit can be seen in Figure 19.

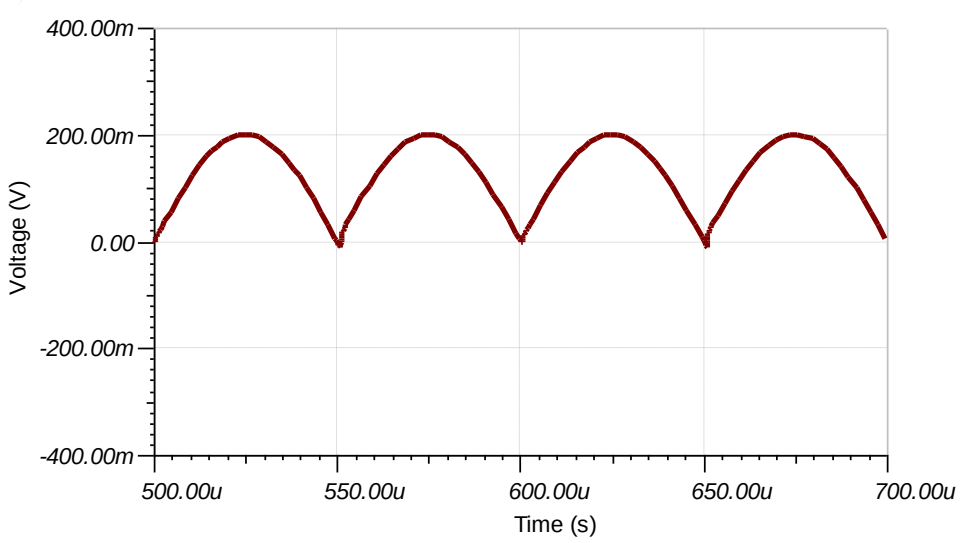
Item #	Quantity	Designator	Value	Description	Manufacturer	Manufacturer Part Number	Supplier Part Number
1	1	C1	4.7uF	CAP, CERM, 4.7uF, 25V, +/-10%, X7R, 1206	TDK	C3216X7R1E475K	445-1606-1-ND
2	2	C2, C8	22uF	CAP, CERM, 22uF, 16V, +/-20%, X7R, 1210	TDK	C3225X7R1C226M	445-3955-1-ND
3	1	C3	10uF	CAP, TANT, 10uF, 50V, +/-10%, 0.4 ohm, 7343-43 SMD	AVX	TPSE106K050R0400	478-3361-1-ND
4	2	C4, C6	0.1uF	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0805	MuRata	GRM21BR71H104KA01L	490-1666-1-ND
5	1	C5	10uF	CAP, CERM, 10uF, 25V, +/-10%, X7R, 1206	MuRata	GRM31CR71E106KA12L	81-GRM31CR71E106KA12
6	1	C7	100pF	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0805	MuRata	GRM2165C1H101JA01D	490-1615-1-ND
7	1	C9	0.47uF	CAP, CERM, 0.47uF, 16V, +/-10%, X7R, 0805	AVX	0805YC474KAT2A	478-1403-1-ND
8	1	C10	1000pF	CAP, CERM, 1000pF, 100V, +/-5%, C0G/NP0, 0805	AVX	08051A102JAT2A	478-1290-1-ND
9	2	C11, C14	DNI	DNI	DNI	DNI	DNI
10	3	C12, C15, C17	100pF	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0603	Kemet	C0603C101J5GACTU	399-1061-1-ND
11	3	C13, C16, C18	0.1uF	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0603	MuRata	GRM188R71E104KA01D	490-1524-1-ND
12	1	D1		Diode, Ultrafast, 100V, 0.15A, SOD-123	Diodes Inc.	1N4148W-7-F	1N4148W-FDICT-ND
13	1	J1		Standard Banana Jack, Uninsulated, 5.5mm	Keystone	575-4	575-4K-ND
14	1	J2		Standard Banana Jack, Uninsulated, 5.5mm	Keystone	575-4	575-4K-ND
15	2	J3, J4		Right Angle BNC Connector	TE Connectivity	1-1634612-0	571-1-1634612-0
16	3	R1, R2, R3	1.00k	RES, 1.00k ohm, 0.1%, 0.1W, 0603	Yageo America	RT0603BRD071KL	603-RT0603BRD071KL
17	1	R4	49.9	RES 49.9 OHM 0.20W 0.1% 0805	Vishay Thin Film	PAT0805E49R9BST1	PAT49.9BCT-ND
18	1	TP1		Test Point, TH, Miniature, Red	Keystone	5000	5000K-ND
19	4	TP2, TP3, TP4, TP5		Test Point, TH, Miniature, Black	Keystone	5001	5001K-ND
20	1	TP6		Test Point, TH, Miniature, White	Keystone	5002	5002K-ND
21	1	TP7		Test Point, TH, Miniature, White	Keystone	5002	5002K-ND
22	1	TP8		Test Point, TH, Miniature, White	Keystone	5002	5002K-ND
23	1	U1		IC REG SWITCHED CAP INV 8VSSOP	Texas Instruments	LM7705MME	LM7705MME/NOPBCT-ND
24	1	U2		IC OPAMP GP R-R 38MHZ DUAL 8SOIC	Texas Instruments	OPA2350UA	OPA2350UA-ND
25	1	U3		IC OPAMP GP R-R 38MHZ SGL 8SOIC	Texas Instruments	OPA350UA	OPA350UA-ND

Figure 19: Bill of Materials

A.3 Additional Simulated Data



A. Transient simulation with +/- 200 mV at 10 kHz sinusoid wave input



B. Simulated output with +/- 200 mV at 10 kHz sinusoid wave input

Figure 20: TINA-TITM simulated transient waveform at 10 kHz with +/- 200 mV sine-wave input

A.4 Additional Measured Data

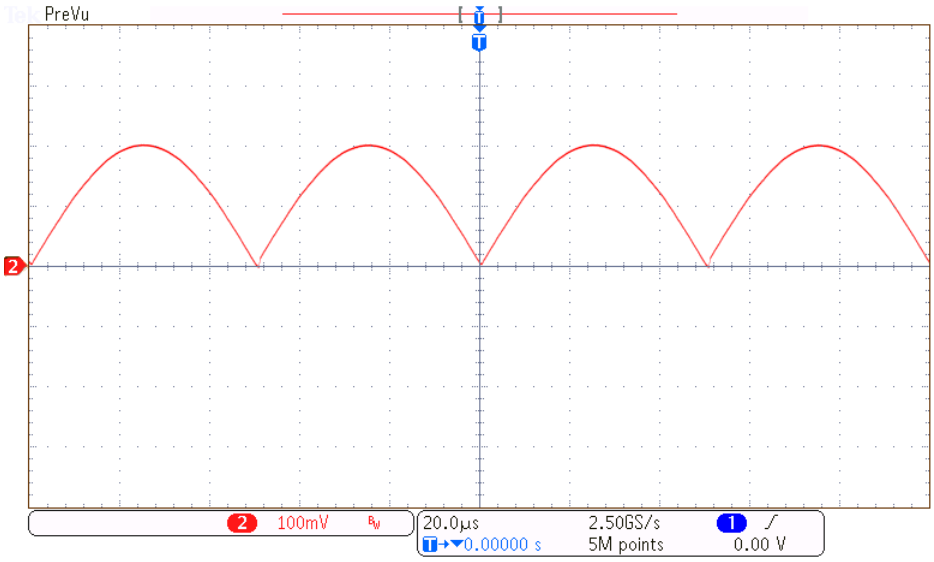


Figure 21: Measured output with 400 mVpp at 10 kHz sine-wave input

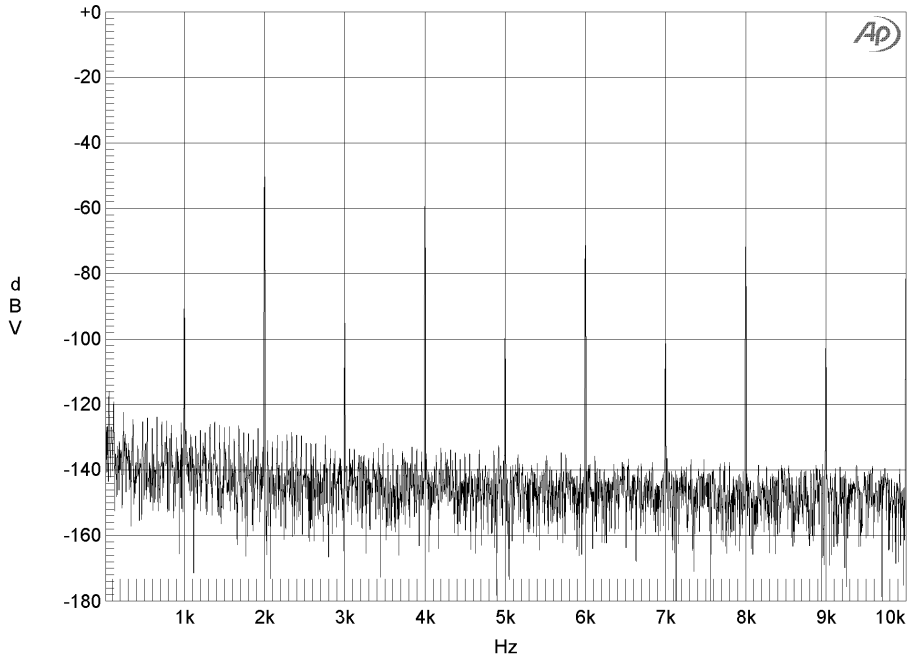


Figure 22: FFT of output at 1 kHz with 50 mVpp sine-wave input

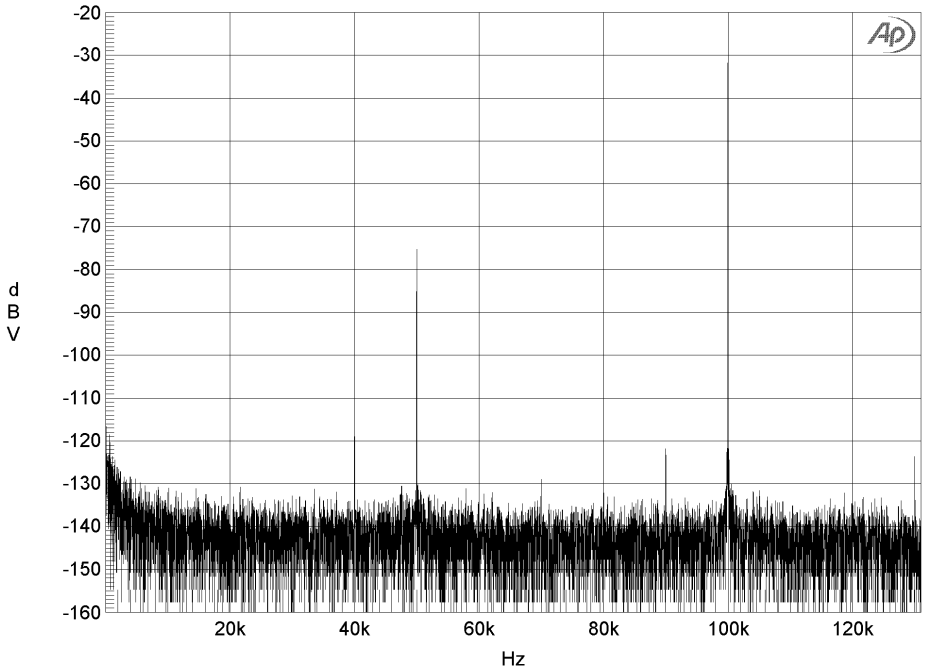


Figure 23: FFT of output at 50 kHz with 400 mVpp sine-wave input

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