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TI Designs High Speed
Driving the GSPS ADCs in Single-Channel or Dual-Channel Mode for High Bandwidth Applications

TI Designs High Speed

TI Designs High Speed are analog solutions created by TI's analog experts. Reference Designs offer the theory, part selection, simulation, complete PCB schematic & layout, bill of materials, and measured performance of useful circuits. Circuit modifications that help to meet alternate design goals are also discussed.

Design Resources

Design Zip File	Design Files for Board A, Board B, Board C, Board F, and Board G
ADC10D1000	Product Folder
ADC10D1500	Product Folder
ADC12D1000	Product Folder
ADC12D1600	Product Folder
ADC12D1800	Product Folder
ADC12D500RF	Product Folder
ADC12D800RF	Product Folder
ADC12D1000RF	Product Folder
ADC12D1600RF	Product Folder
ADC12D1800RF	Product Folder

Design Overview

This purpose of this reference design is to help a system designer understand the tradeoffs and optimize implementation for driving the various available DES and Non-DES Modes of the GSPS ADC with balun configurations. For the purpose of this reference design, *ADC* refers to the following devices: ADC12D1800RF, ADC12D1600RF, ADC12D1000RF, ADC12D800RF, ADC12D500RF, ADC12D1800, ADC12D1600, ADC12D1000, ADC10D1500, and ADC10D1000. The actual product evaluated is the ADC12D1600RF.

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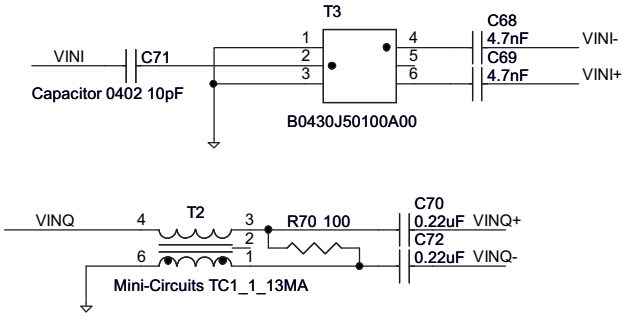

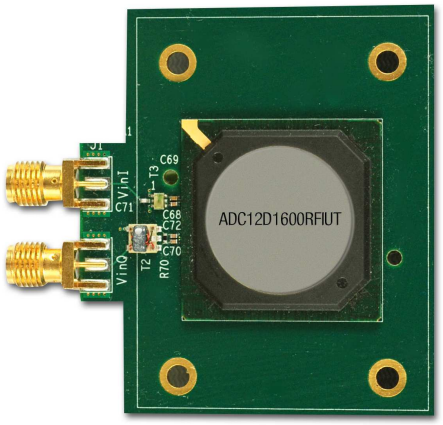

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Overview

The GSPS ADCs are dual-channel devices (as denoted by the ***D*** in the product name) and can also be interleaved in order to achieve 2-times the sample rate (see Figure 1). In the interleaved mode, the I-channel and Q-channel sample the same analog input signal. There are a number of options for driving the ADC in the interleaved mode; however, this flexibility also presents a design challenge. This reference design addresses what the recommended topology, layout, and balun type is to effectively drive each mode.

The scope of the study was limited to baluns in order to show general best practices of design and layout. However, these principles can be applied to an amplifier design as well.

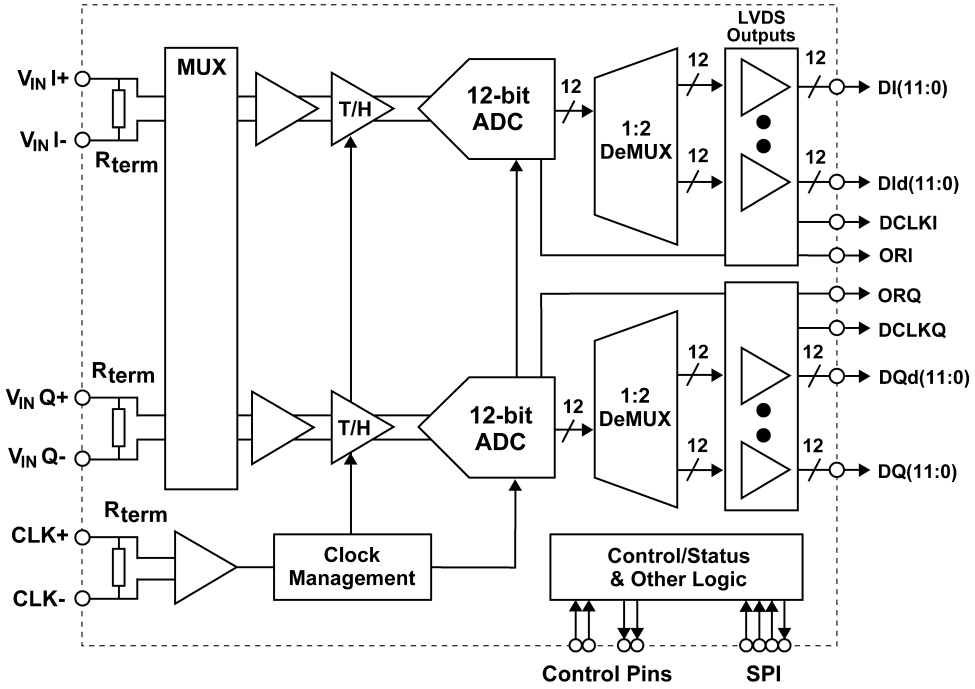

Figure 1. GSPS ADC Block Diagram

Dual-edge sampling mode (DES) is descriptive of how the interleaved mode is clocked. One channel samples on the rising edge of the clock while the other channel samples on the falling edge of the clock. Both channels sample the same analog input (see Figure 2).

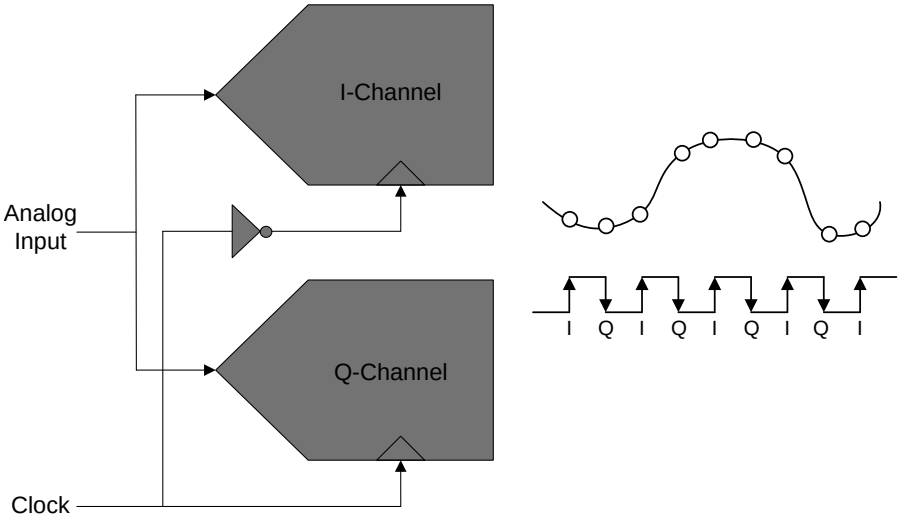

Figure 2. DES Mode sampling

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Table 1 lists the five possible input-driving modes as well as which input is driven for that mode and whether the mode is interleaved.

Table 1. DES and Non-DES Modes(1)

Mode	Input Driven	Interleaved
Non-DES	I and Q separately	No
DESI	I only	Yes
DESQ	Q only	Yes
DESIQ	I and Q together	Yes
DESCLKIQ	I and Q together	Yes

(1) Not every mode is available on every product, see Table 2. Specifically, the DESCLKIQ Mode is only available on the RF-sampling ADCs.

Table 2. Available Mode by Product

Product	Non-DES	DESI, DESQ	DESIQ	DESCLKIQ
ADC12D1800RF, ADC12D1600RF, ADC12D1000RF	√	√	√	√
ADC12D800RF, ADC12D500RF	√	√	√	√
ADC12D1800, ADC12D1600, ADC12D1000	√	√	√	
ADC10D1500, ADC10D1000	√	√	√	

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Depending on which mode is selected, an input mux configures the analog input signal, and distributes the signal to one or both cores for sampling. In Figure 3, Figure 4, Figure 5, Figure 6, and Figure 7, the dashed grey line shows what connections can be made in the mux. However, the red lines show which connections are actually made for that particular mode. The inputs are actually differential (such as I± and Q±) but are shown as single-ended for simplicity in the figures.

Figure 3 shows the Non-DES Mode. In this dual-channel mode, each I-input and Q-input is independently driven and sampled. The bandwidth is maximized because one input is driving one channel with the minimum routing.

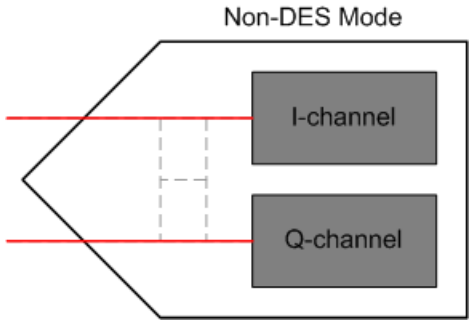

Figure 3. Non-DES Mode Input-Mux Configuration

Figure 4 and Figure 5 show the DESI and DESQ Modes, respectively. For DESI Mode, only the I-input is driven and the mux distributes the input signal to both cores for sampling. For DESQ Mode, the same is true, except that only the Q-input is driven. The bandwidth is reduced as compared to Non-DES Mode because one input is driving two channels with additional routing.

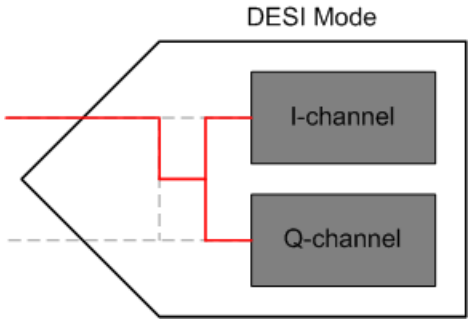

Figure 4. DESI Mode Input-Mux Configuration

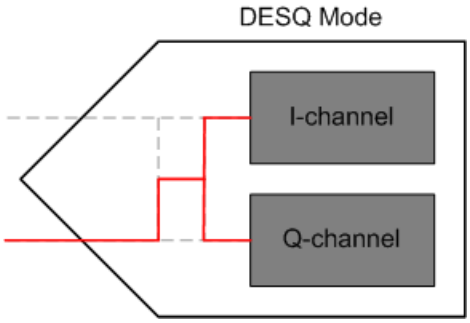

Figure 5. DESQ Mode Input-Mux Configuration

Figure 6 and Figure 7 show the DESIQ and DESCLKIQ Modes, respectively. For both of these modes, the I-channel and Q-channel must be driven externally. Internally, however, the configurations are different which affects the input bandwidth and spurious performance. For both DESIQ Mode and DESCLKIQ Mode, the bandwidth is increased as compared to DESI (DESQ) Mode because both inputs are driving the two channels with better optimized routing. For DESCLKIQ Mode, the bandwidth is better than DESIQ Mode, but the spurious performance is worse.

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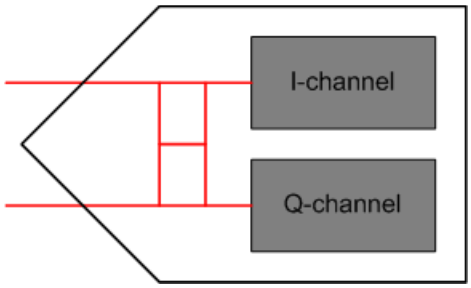

Figure 6. DESIQ Mode Input-Mux Configuration

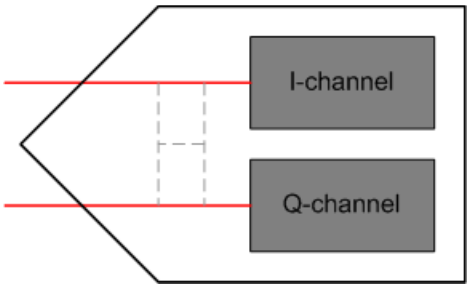

Figure 7. DESCLKIQ Mode Input-Mux Configuration

Solutions Evaluation Criteria

In order to effectively evaluate each solution, some criteria is required. These designs are evaluated based on dynamic performance, insertion loss, the ability to minimize the interleaving timing spur, and the ability to handle multi-mode applications.

Dynamic performance includes SNR, SFDR, THD, and ENOB from a CW full-scale input signal.

Insertion loss is the system insertion loss including loss from evaluation board traces, the balun configuration, and the ADC front-end (see Figure 8).

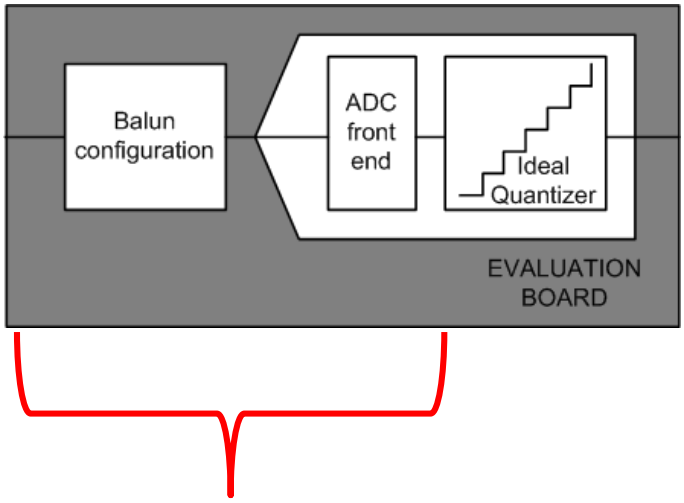

Figure 8. System Insertion Loss

Gain mismatch and timing skew result in an interleaving spur, located at Fs/2-Fin (see Figure 9). Offset mismatch results in a spur at Fs/2. The Fs/2-Fin spur is minimized by using the I- and Q-Channel FSR Adjust and DES Timing Adjust features on the GSPS ADC. This criteria evaluates whether the design allows for the magnitude of the Fs/2-Fin spur to be reduced such that the magnitude is not the SFDR-limiting spur.

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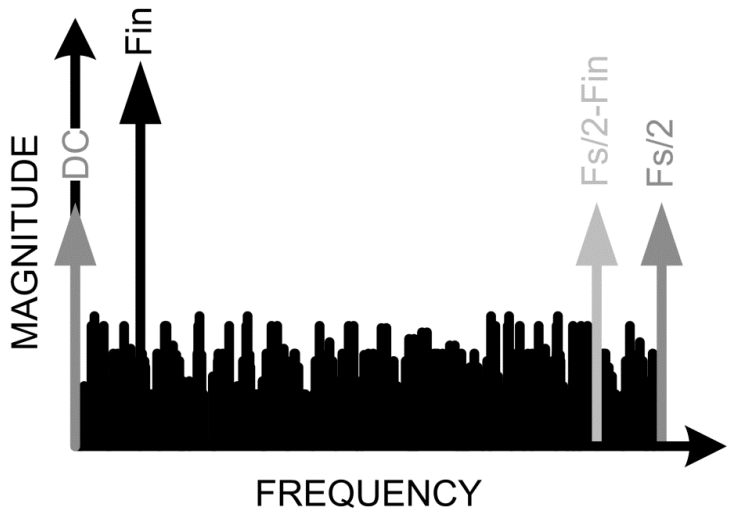

Figure 9. 2x Interleaving Mismatch Spur

Some applications require the flexibility to configure the ADC into multiple interleaved modes. The multi-mode application criteria tests whether the balun topology can accommodate that. For example, a digitizer card application may accommodate both interleaved and non-interleaved modes.

Designs Considerations

When planning for the various designs, ADC input topology, input impedance, and balun properties must be considered.

The ADC analog inputs, I± and Q± are mirrored in their placement in the 292-pin BGA package. Driving the I-channel and Q-channel with the same signal becomes challenging because neither the I+ and Q+ nor the I– and Q–, and I+ and Q+, the challenge is to make a symmetrical layout with minimal series impedance and inductance.

When driving one I-input or Q-input, such as in Non-DES, DESI, and DESQ Modes, the input impedance is nominally 100-Ω differential (see Figure 11). When driving both inputs, such as in DESIQ and DESCLKIQ Modes, the parallel combination is 50-Ω differential. Carefully considering which balun is appropriate for the design is important. For example, some designs require a 1:1 impedance ratio balun and others require a 1:2 balun. Ensuring that layout traces are the correct impedance is also important.

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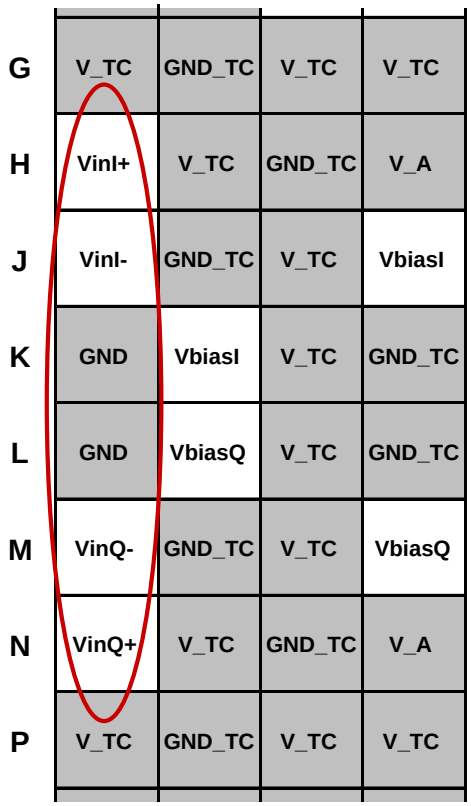

Figure 10. ADC Inputs Topology

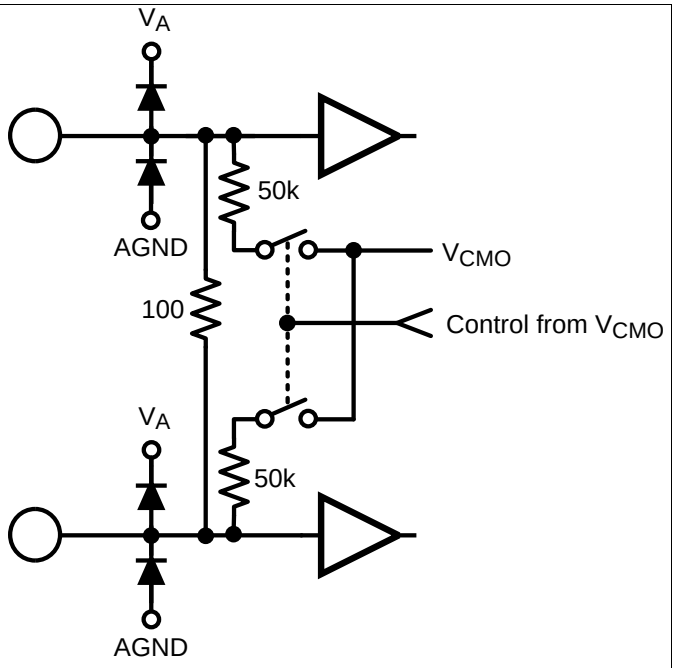

Figure 11. ADC Input Impedance

Table 3 lists the several different baluns that were selected for use in these designs. Baluns were selected for a convenient impedance ratio, wide frequency range to match the ADC input, and variety of construction.

Table 3. Baluns Evaluated

Manufacturer	Model	Frequency Range	Impedance Ratio	Description
Anaren	B0430J50100	400 MHz to 3000 MHz	1:2	Multi-layer: coupled strip-line with softboard dielectric
Anaren	B0322J5050	300 MHz to 2200 MHz	1:1	Multi-layer: coupled strip-line with softboard dielectric
Mini-Circuits	TC1-1-13MA+	4.5 MHz to 3000 MHz	1:1	Wire-wound with ferrite core

Designs Tested

Five designs were tested: Board A, Board B, Board C, Board F, and Board G. The following sections includes a schematic, layout clip, and brief description of each board.

NOTE: Board D and Board E are not included in the following sections. Board D was an attempt to recreate the internal short for DESIQ Mode, externally. The performance was very poor, so the design and results are not included because the design is not recommended to drive any mode.

These boards were developed from a board known as the EVAL Board, which was considered as Board E and therefore Board E was skipped over in the naming convention. This board has independent inputs from SMA connector to each I+, I–, Q+, and Q– input on the ADC.

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Board A — Multi-Layer Balun With Resistive Splitter to the I-Input and Q-Input

This board drives the DESIQ and DESCLKIQ Modes. A single multi-layer balun is used for the balun configuration. Resistors are used to route the differential signal to each input and to maintain impedance matching. A benefit of this design is that the signal can arrive at each input with a minimum of additional timing skew because resistive splitter is used. This design, however, must be routed in multiple layers, which adds extra series inductance and impedance. Another drawback of this design is that the resistors also increase the insertion loss.

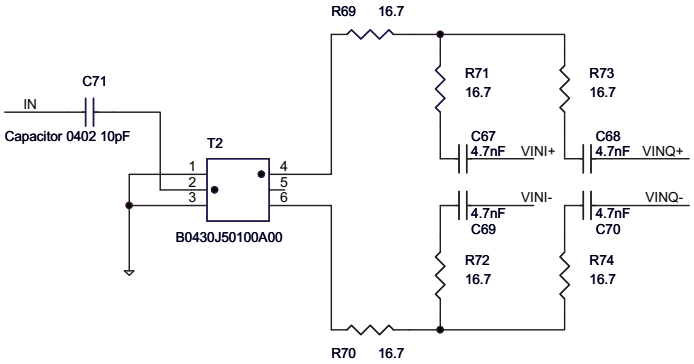

Figure 12. Board A Schematic

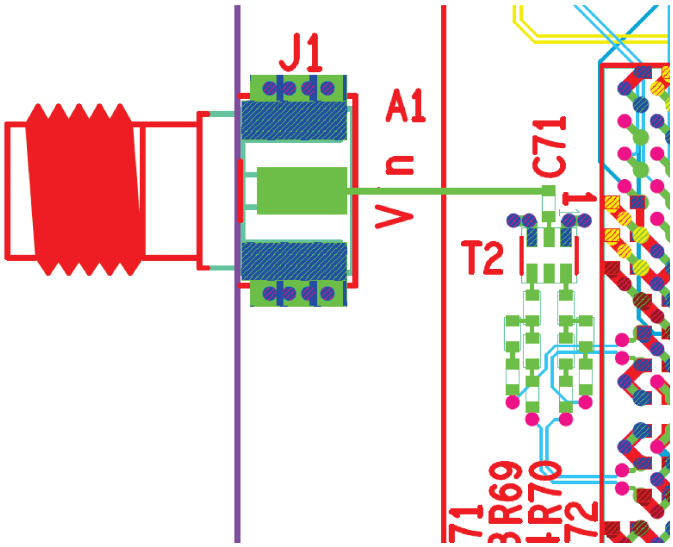

Figure 13. Board A Layout

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Board B — Multi-Layer Balun on the I-input and Wire-Wound Balun on the Q-input

This board drives the Non-DES, DESI, and DESQ Modes. Both a multi-layer and wire-wound balun is used in this design. All routing for this design is accomplished in one layer. To achieve the best dynamic performance results, TI recommends to place the baluns and AC-coupling caps as close as possible to the ADC input. The TC1_1_13MA balun is a 1:1 impedance ratio, so an additional parallel 100-Ω resistor is placed in the design to match to the 50-Ω impedance at the input of the balun.

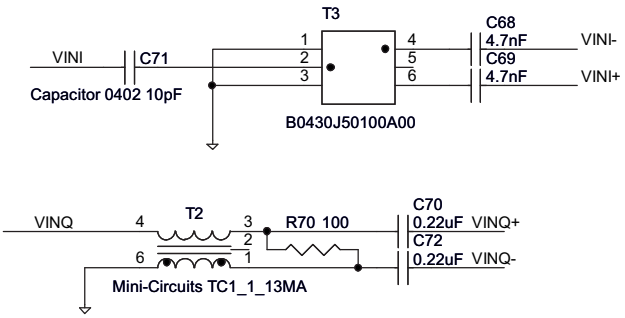

Figure 14. Board B Schematic

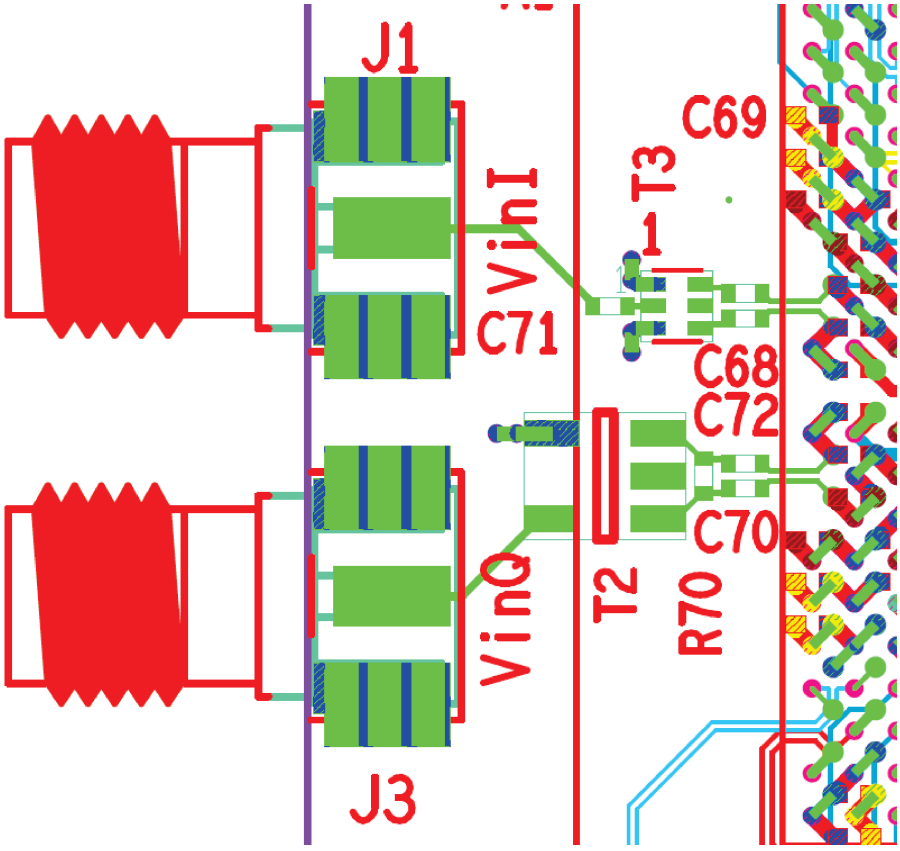

Figure 15. Board B Layout

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Board C — Multi-Layer Balun on the I-input and Wire-Wound Balun on the Q-Input

This board drives the DESIQ and DESCLKIQ Modes. The cascaded multi-layer balun topology allows for each input to be driven with the correct phase, while accomplishing the routing in one layer. However, this design can also incur additional insertion loss. This design also has the added benefit of allowing multiple modes to be driven with a small addition to the design. If a switch is added at the input of T2 and T3, the switched inputs drive the ADC in Non-DES Mode.

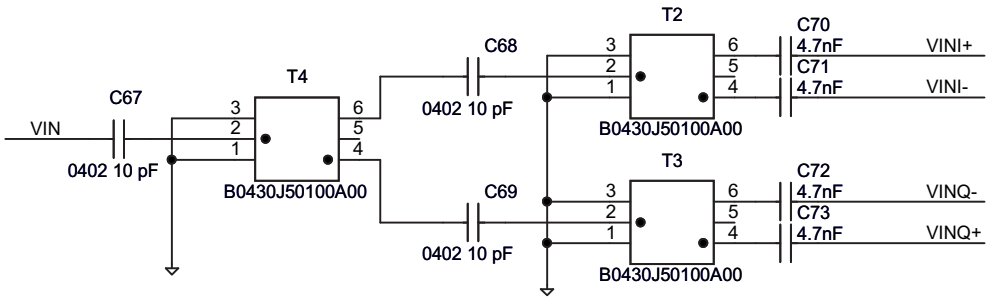

Figure 16. Board C Schematic

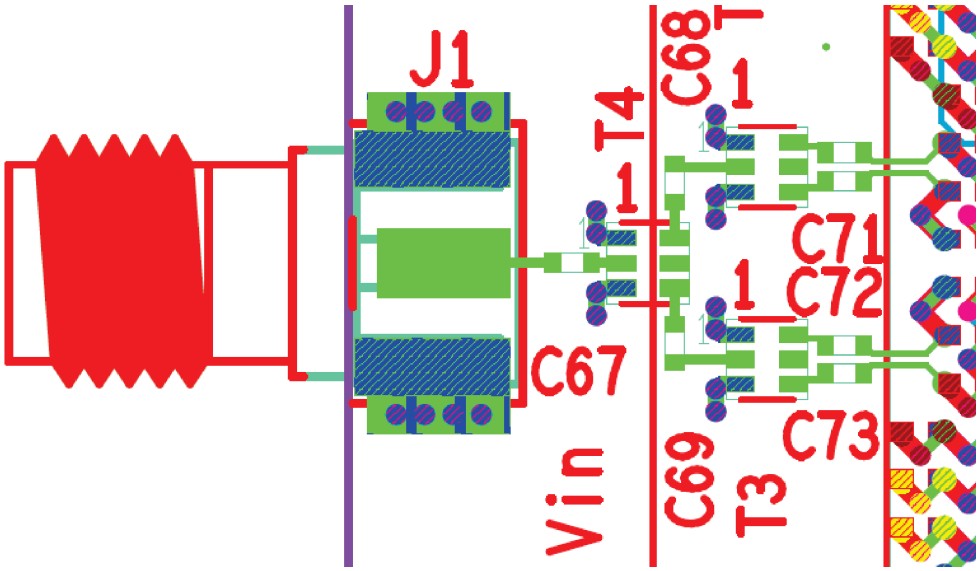

Figure 17. Board C Layout

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Board F — Wire-Wound Balun to the I-Input and Q-Input

This board is used to test the DESIQ and DESCLKIQ Modes. The single wire-wound balun requires routing in multiple layers. Note that the differing trace widths which accommodate for a 50-Ω impedance to the balun input and to the signal split at the output. After the split, the traces are 25-Ω (single-ended). This design is similar to using the TC1-DESIQ-SBB to drive GSPS ADC reference boards, except that in this design the balun is integrated onto the board. Placing the balun close to the ADC inputs is best because longer traces at the input accommodate standing waves which cause gain ripple and degrade the dynamic performance.

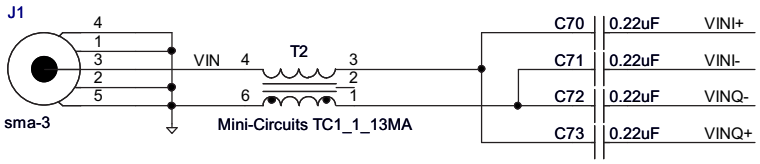

Figure 18. Board F Schematic

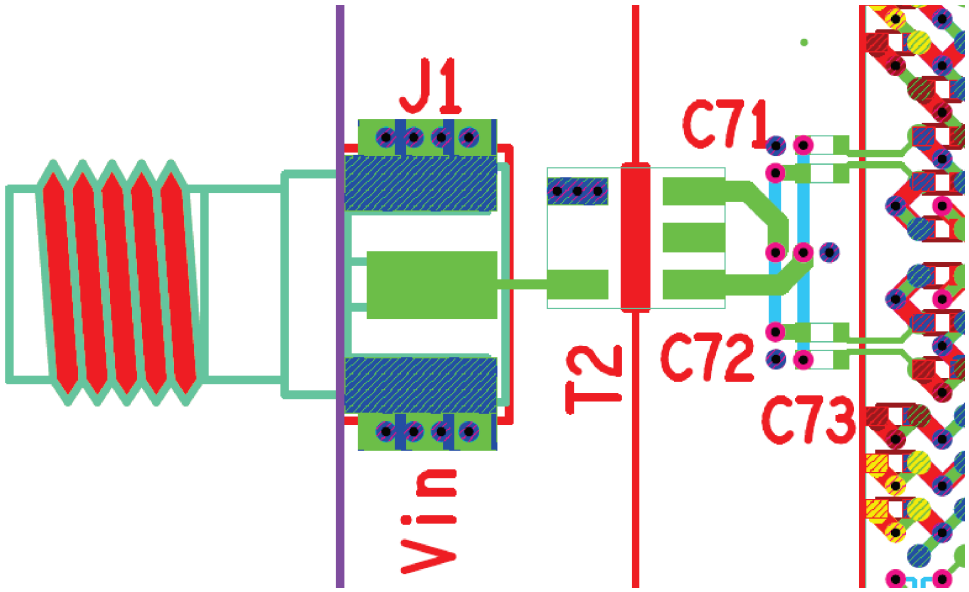

Figure 19. Board F Layout

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Board G — Wire-Wound Balun to the I-Input and Q-Input

This board drives the DESIQ and DESCLKIQ Modes. The single multi-layer balun requires routing in multiple layers. The board is very similar in design to Board F, except that Board G uses a multi-layer balun instead of a wire-wound balun.

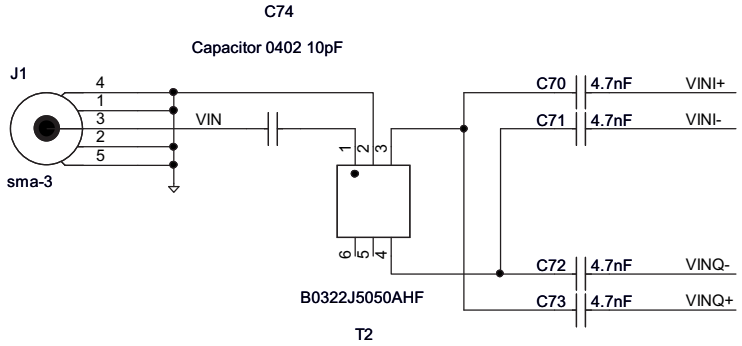

Figure 20. Board G Schematic

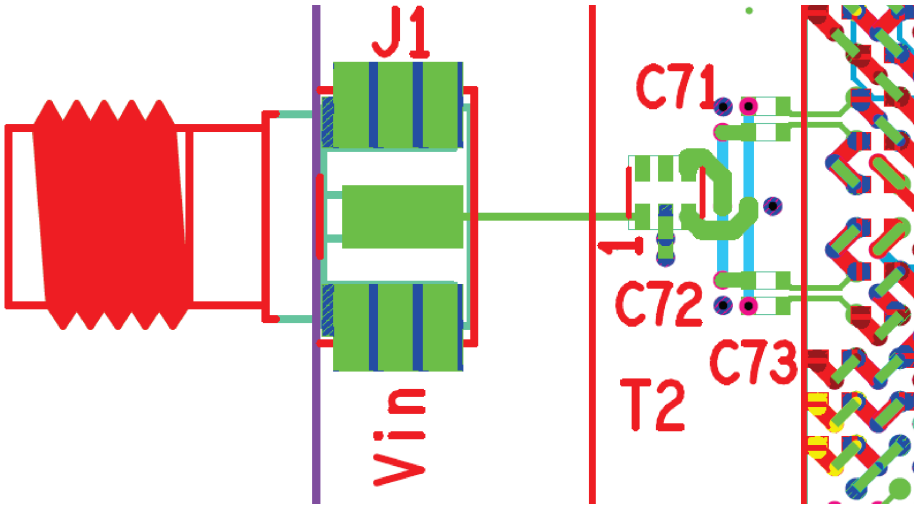

Figure 21. Board G Layout

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Non-DES Mode Results Summary

Results are shown for insertion loss and dynamic performance. Only Board B was designed to drive Non-DES Mode, but for this board, there is a multi-layer and wire-wound option.

For the Non-DES Mode insertion loss, shown in Figure 22, the insertion loss for the wire-wound design is +3 dB from the multi-layer design because the 100-Ω resistor consumed half the signal power. Both designs have relatively little gain ripple over frequency.

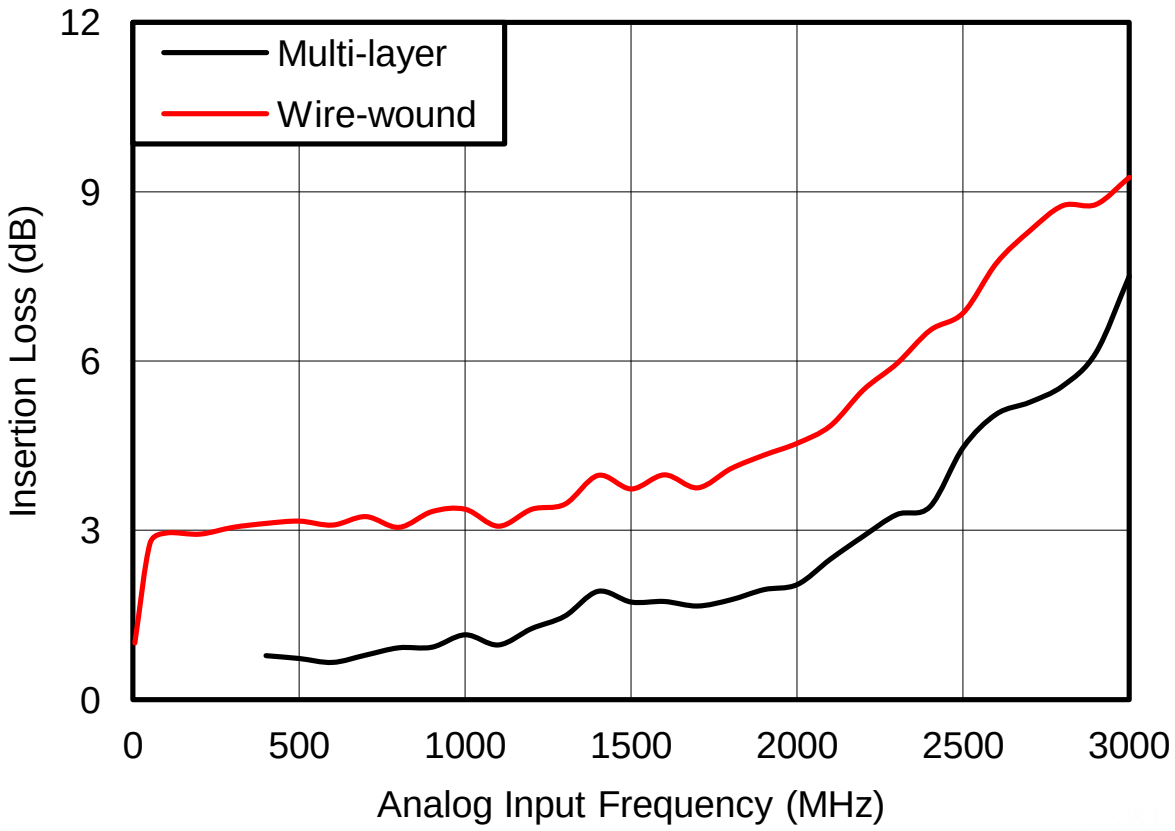

Figure 22. Non-DES Mode Insertion Loss (Board B)

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Non-DES Mode Dynamic Performance (Board B) shows the dynamic performance. Note that the better SNR performance of the multi-layer design translates to better overall effective number of bits (ENOB).

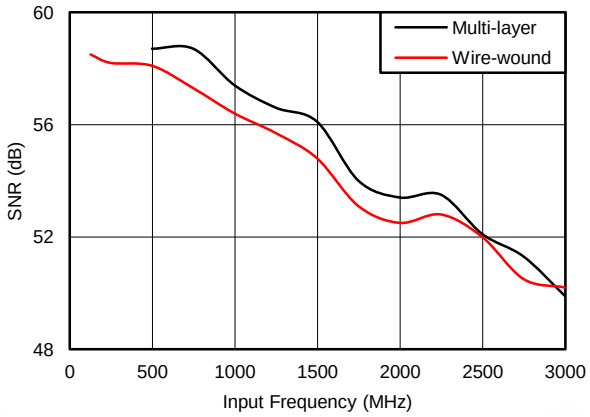

Figure 23. SNR vs Fin

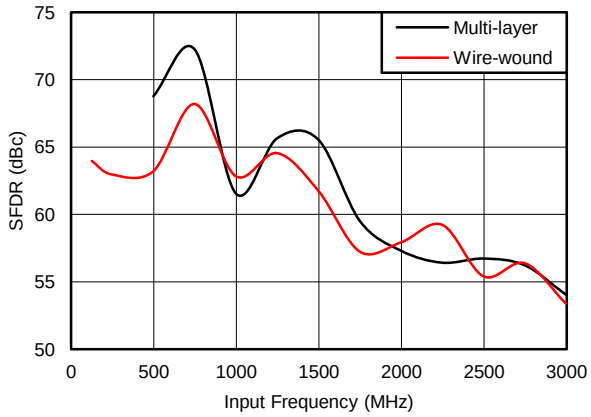

Figure 24. SFDR vs Fin

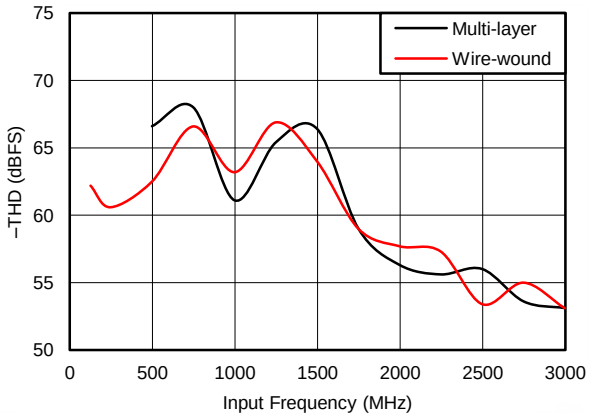

Figure 25. THD vs Fin

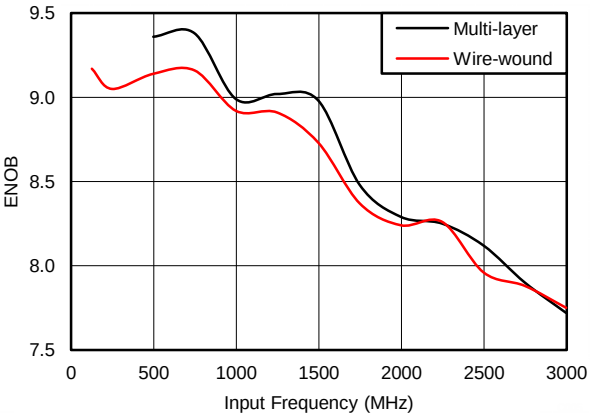

Figure 26. ENOB vs Fin

Non-DES Mode Dynamic Performance (Board B)

Table 4 lists the results for Non-DES Mode. The multi-layer balun is the better solution for driving the Non-DES Mode, except for applications which require a large input frequency range, especially at low frequencies.

Table 4. Non-DES Mode Summary

Criteria	Multi-Layer	Wire-Wound
Dynamic Performance	Excellent	Average
Insertion Loss	Excellent	Average
Frequency Range	Good	Excellent
Multi-mode Application	Average	Average

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DESI and DESQ Mode Results Summary

Results are shown for insertion loss and dynamic performance. As with the Non-DES Mode, only Board B was designed to drive DESI and DESQ Mode.

For the DESI and DESQ Mode insertion loss, shown in Figure 27, the insertion loss for the wire-wound design is approximately +3 dB greater than the multi-layer design because the 100-Ω resistor consumed half the signal power. Both designs have relatively little gain ripple over frequency, but the wire-wound design has a slightly smoother profile.

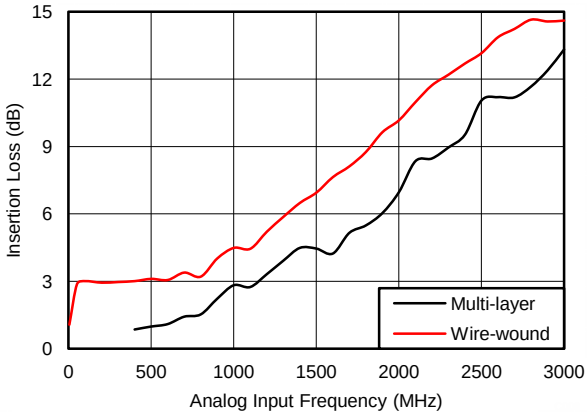

Figure 27. DESI and DESQ Mode Insertion Loss (Board B)

Figure 28 shows the adjusting of the DES timing spur. The DES Timing Adjust feature allows the user to delay or advance the sample instant of the I-channel relative to the Q-channel from the nominal setting. This feature becomes increasingly effective on input signals greater than 1 GHz. For this test, an input signal of 1.3 GHz at –1 dBFS was used and the full range of the Timing Adjust was exercised. Note that the multi-layer design achieves a nice null while the wire-wound design struggles to provide the same. Although the gain mismatch also affects the magnitude of the Fs/2-Fin interleaving spur, the gain mismatch of both designs is low — 0.14% for the multi-layer design and 0.33% for the wire-wound design. The percent mismatch was calculated by using the highest and lowest code at each I- and Q-converter.

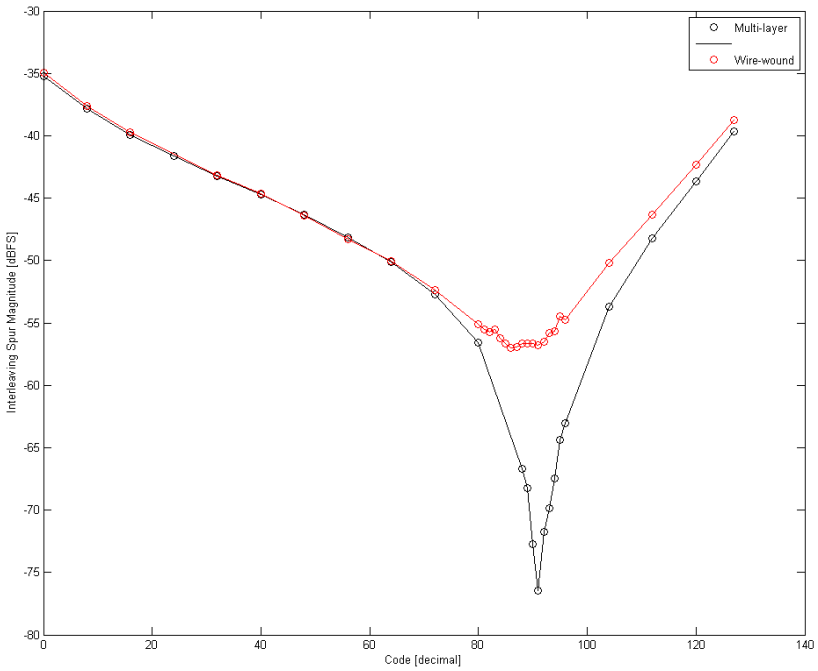

Figure 28. DESI and DESQ Mode Timing Adjust (Board B)

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The graphs in DESI and DESQ Mode Dynamic Performance (Board B) show the dynamic performance for the DESI and DESQ Modes. The SFDR for the multi-layer balun is better because the Fs/2-Fin interleaving spur can be adjusted below other spurs whereas the interleaving spur can not be adjusted for the wire-wound balun. This larger spur also contributed to the noise floor and degraded the SNR and ENOB for the wire-wound case. At high frequencies (greater than 2.5 GHz), the SNR for the multi-layer balun performed much better than the wire-wound balun design which is seen directly reflected in the ENOB.

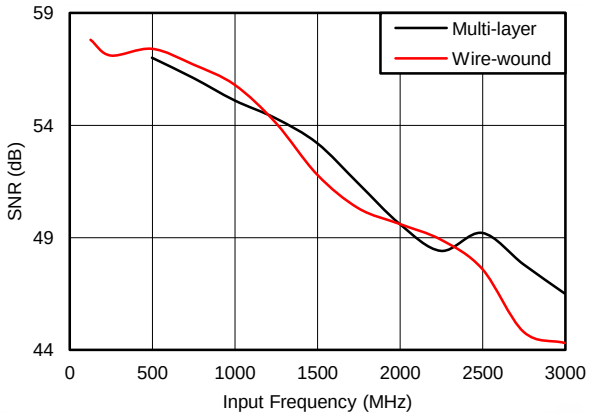

Figure 29. SNR vs Fin

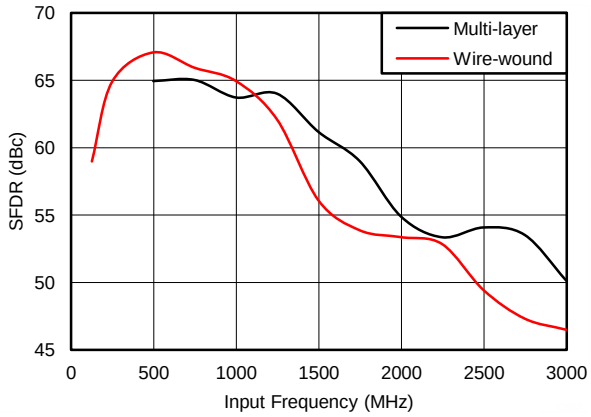

Figure 30. SFDR vs Fin

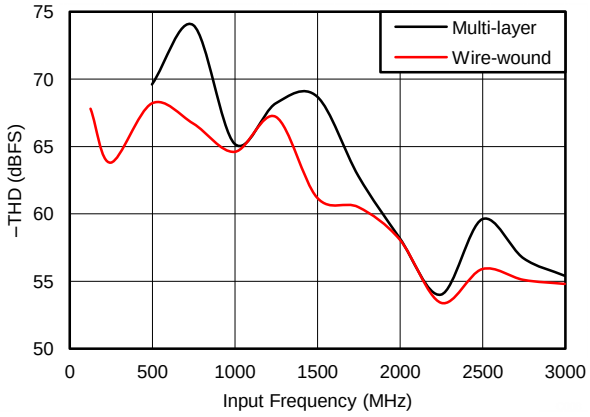

Figure 31. THD vs Fin

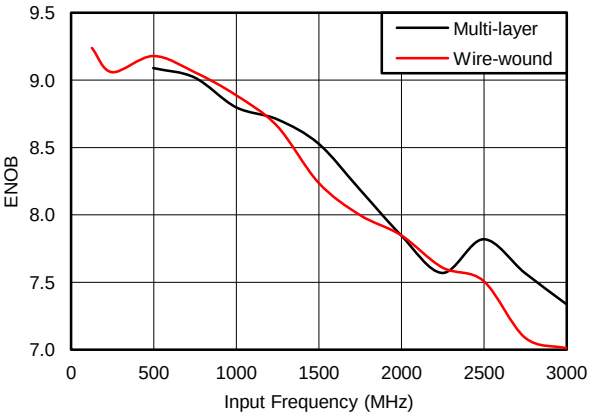

Figure 32. ENOB vs Fin

DESI and DESQ Mode Dynamic Performance (Board B)

Table 5 lists the results for the DESI and DESQ Modes. The multi-layer balun is a good all-round choice for multiple criteria. The wire-wound balun is excellent for frequency range, especially at low Fin, but is poor for adjusting the DES timing spur.

Table 5. DESI and DESQ Mode Summary

Criteria	Multi-Layer	Wire-Wound
Dynamic Performance	Excellent	Average
Insertion Loss	Excellent	Average
Frequency Range	Good	Excellent
Multi-Mode Application	Average	Average

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1 DESIQ and DESCLKIQ Mode Results Summary

The insertion loss for DESIQ Mode and DESCLKIQ Mode is shown side-by-side for easy comparison (see DESIQ and DESCLKIQ Mode Insertion Loss (Board A, Board C, Board F, and Board G)). Externally, both modes are driven by the same balun configuration, so the results can be tested for Board A, Board C, Board F, and Board G. Board A has a higher insertion loss than the other boards because of the power lost in the resistive split. The other three boards (Board C, Board F, and Board G) perform similarly between DESIQ Mode and DESCLKIQ Mode except that DESCLKIQ Mode maintains a slightly-lower insertion loss above 2 GHz. The DESCLKIQ Mode of the ADC has a higher 3-dB bandwidth than DESIQ Mode, but the advantage of the ADC (such as higher 3-dB full-power bandwidth) when observing system insertion loss is not as attractive.

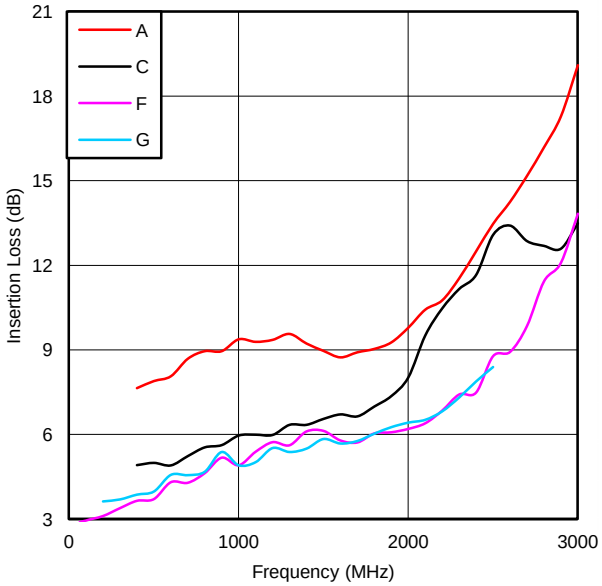

Figure 33. DESIQ

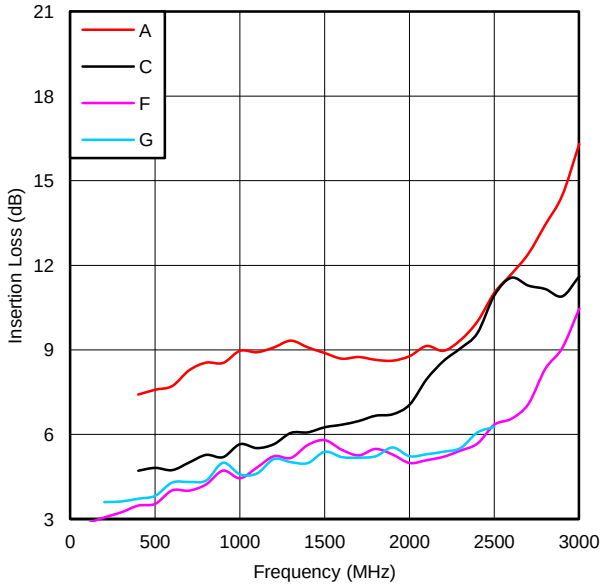

Figure 34. DESCLKIQ

DESIQ and DESCLKIQ Mode Insertion Loss (Board A, Board C, Board F, and Board G)

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Figure 35 shows the adjusting of the DES timing spur for DESIQ Mode. All of the boards (A, C, F, and G) allow for a relative null to be achieved regardless of balun construction (wire-wound or multi-layer), or balun topology (cascaded, single-balun, or resistive splitter). A relative null is achieved because the DESIQ Mode effectively shorts the I-input and Q-input internally to the chip which minimizes any gain mismatch or timing skew incurred by the individual inputs in the circuit that drives the inputs. This achievement is an important benefit of the DESIQ Mode. Note that the wire-wound balun design (Board F) shows an imperfect null.

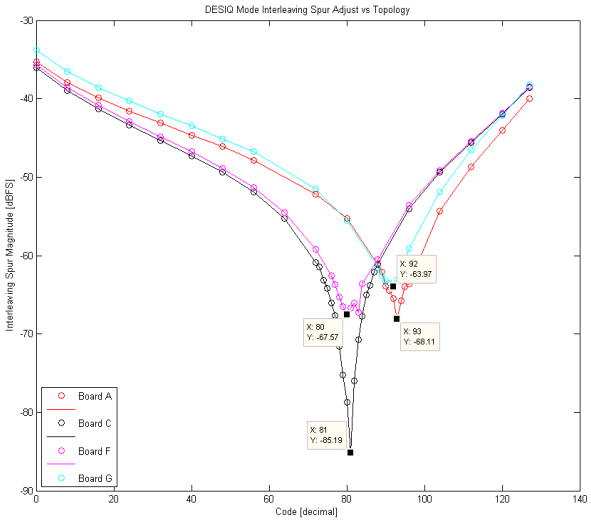

Figure 35. DESIQ Mode Timing Adjust (Board A, Board C, Board F, and Board G)

Figure 36 shows the adjusting of the DES timing spur for DESCLKIQ Mode. In this mode, the timing spur becomes much more difficult, or impossible in some cases, to adjust. The timing skew and gain mismatch at the inputs to the ADC, for Board C with the cascaded balun topology, prevent the DES timing spur from going below –35 dBFS. Board A is shown with the gain unadjusted (green trace). For Board A, the gain mismatch was 5.4%. After the gain is adjusted to 0.06%, the DES timing spur achieves a better controlled null (red trace). Board F and Board G show similar trends, but did not perform as well. For example, these designs did not achieve as low of a null as the DES timing spur. The DESCLKIQ Mode is generally not recommended to use in this configuration because of the difficulty in adjusting the DES timing spur which makes the DESCLKIQ Mode difficult to drive. Additionally, this adjustment takes the place for one frequency at one temperature and further variation occurs as these parameters are swept over the full operating range of the chip.

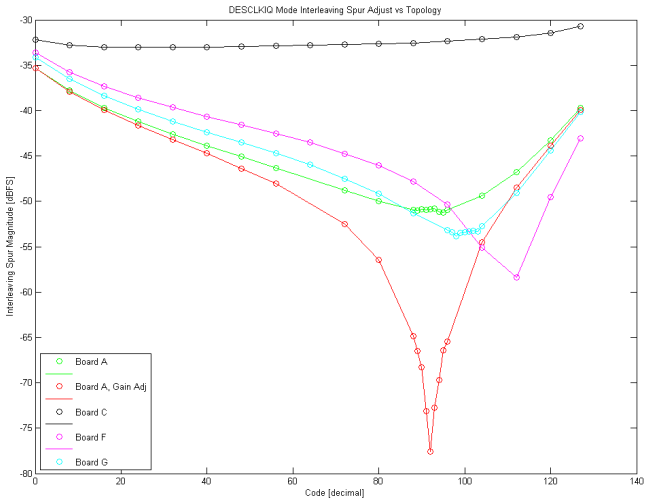

Figure 36. DESCLKIQ Mode Timing Adjust (Board A, Board C, Board F, and Board G)

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The graphs in DESIQ Mode Dynamic Performance (Board A, Board C, Board F, and Board G) show the dynamic performance for DESIQ Mode. All of the designs show similar performance.

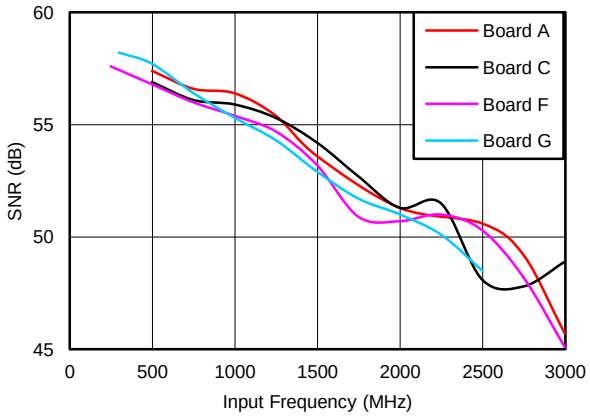

Figure 37. SNR vs Fin

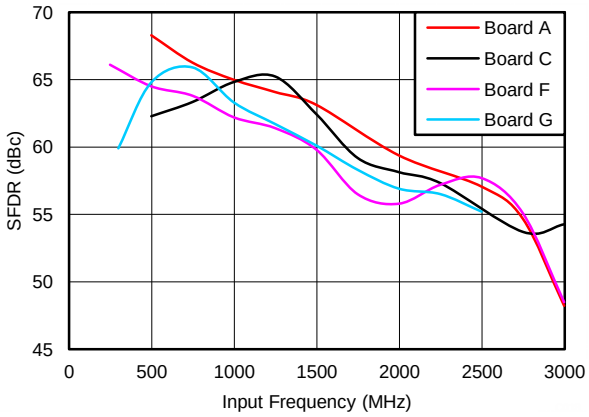

Figure 38. SFDR vs Fin

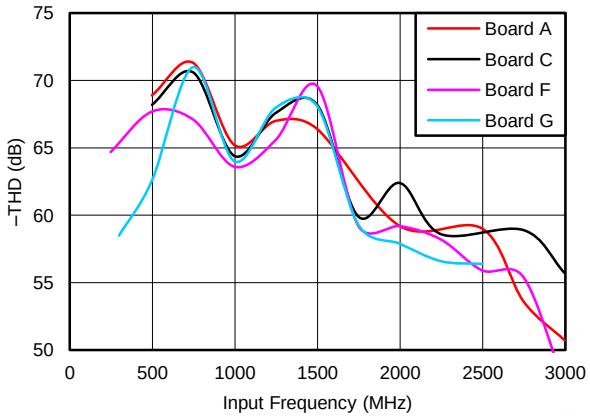

Figure 39. THD vs Fin

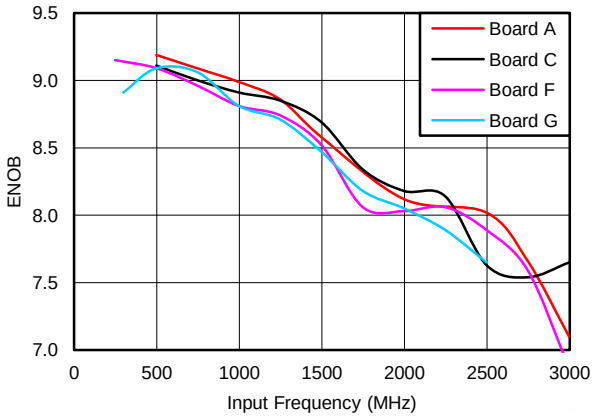

Figure 40. ENOB vs Fin

DESIQ Mode Dynamic Performance (Board A, Board C, Board F, and Board G)

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The graphs in DESCLKIQ Mode Dynamic Performance (Board A) show the dynamic performance is for DESCLKIQ Mode. Only the results for Board A are shown because adjusting the timing spur to the necessary level to get reasonable performance results for the other designs (Board C, Board F, and Board G) was not possible. Board A results are shown after the DES Timing Adjust and Gain Adjust features were used to optimize the DES timing spur. Note that the SFDR degrades as the input frequency decreases because the DES timing spur was optimized at a different frequency.

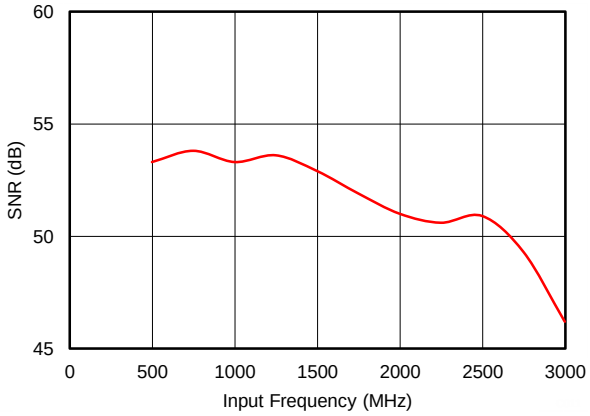

Figure 41. SNR vs Fin

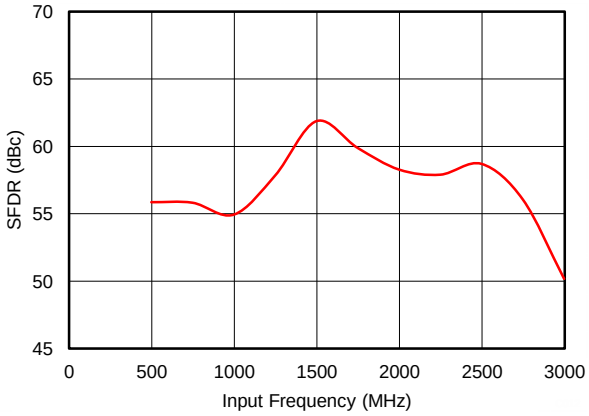

Figure 42. SFDR vs Fin

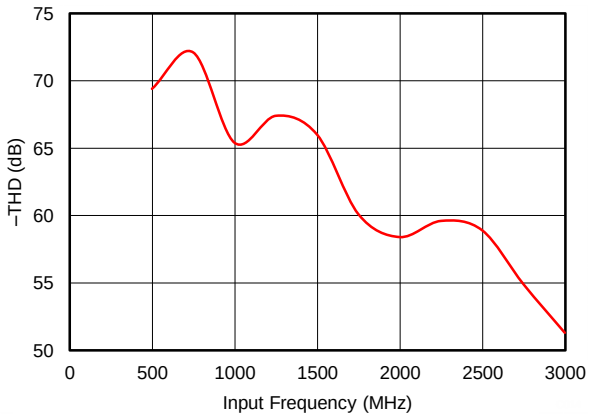

Figure 43. THD vs Fin

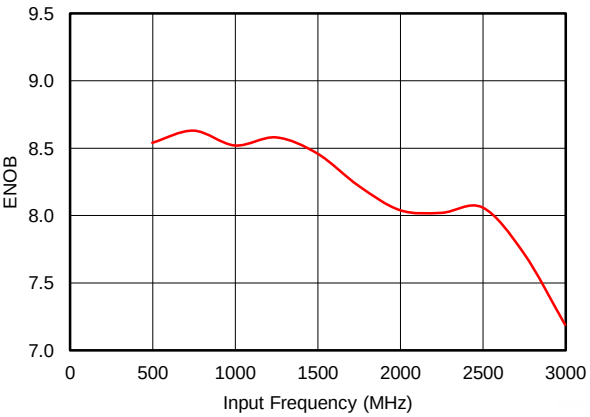

Figure 44. ENOB vs Fin

DESCLKIQ Mode Dynamic Performance (Board A)

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Table 6 and Table 7 list a summary of the DESIQ Mode and the DESCLKIQ Mode, respectively. In general, TI recommends to use the DESIQ Mode instead of the DESCLKIQ Mode because the timing spur is difficult to adjust in DESCLKIQ Mode. The insertion loss is slightly better in DESCLKIQ Mode, but the DESIQ Mode insertion loss is comparable.

Table 6. DESIQ Mode Summary

DESIQ Criteria	Board A	Board C	Board F	Board G
Dynamic Performance	Average	Good	Average	Good
Insertion Loss	Below Average	Average	Good	Excellent
Frequency Range	Average	Good	Average	Average
Multi-Mode Application	Average	Excellent	Average	Average

Table 7. DESCLKIQ Mode Summary

DESCLKIQ Criteria	Board A	Board C	Board F	Board G
Dynamic Performance	Below Average	Not Recommended	Average	Average
Insertion Loss	Below Average	Good	Excellent	Excellent
Interleaving Spur Adjust	Good	Poor	Average	Average
Multi-Mode Application	Average	Excellent	Average	Average

Calibrating to Optimize Performance

In any of the DES Modes, follow these steps to optimize the performance in a specific mode.

1. Configure the ADC into the desired operating mode including DES Mode, FSR, or AC-DC coupled mode, and allow the self-heating of the device to stabilize.
2. Use the calibration feature to calibrate the ADC. The calibration initiates through the CAL pin (Pin D6) or the CAL bit (Addr: 0**h**, Bit 15).
3. Use the DES Timing Adjust feature (Addr: 7**h**) to optimize the DES timing spur. Place a CW input tone near to full scale in the middle of the band of interest. For example, if the band of interest is 1 GHz or 2 GHz use a CW tone of Fin equal to 1.5 GHz at –1 dBFS.
4. Optimize the gain mismatch using the FSR Adjust feature (Addr: 2**h**, B**h**). Use the same CW tone as for the DES timing spur adjust. The minimum and maximum code from each I– and Q– converter shows the difference in gain for each channel. Reduce or increase the FSR for one channel until the FSR matches the other.

NOTE: The timing adjust and gain adjust can be performed independently of one another (for example, step 3 and step 4 can be reversed).

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When to Use DESCLKIQ Mode

DESCLKIQ Mode was originally designed to accommodate applications with multiple interleaved GSPS ADCs for maximum input bandwidth. Figure 45 shows an example application using DESCKLIQ mode with system Fs = 7.2 Gsps. The DES clocking provides 180° clocking internally to each chip, and external clock generation provides the required 0° and 90° clocks. A track-and-hold on the front-end increases the analog input bandwidth.

Using DESIQ Mode reduces the analog input bandwidth, but DESCLKIQ Mode maintains separate analog inputs to each I-input and Q-input, which results in the maximum possible bandwidth, the same as for Non-DES Mode. The interleaving spurs can be addressed by the FSR Adjust, DES Timing Adjust, and post-processing digital correction.

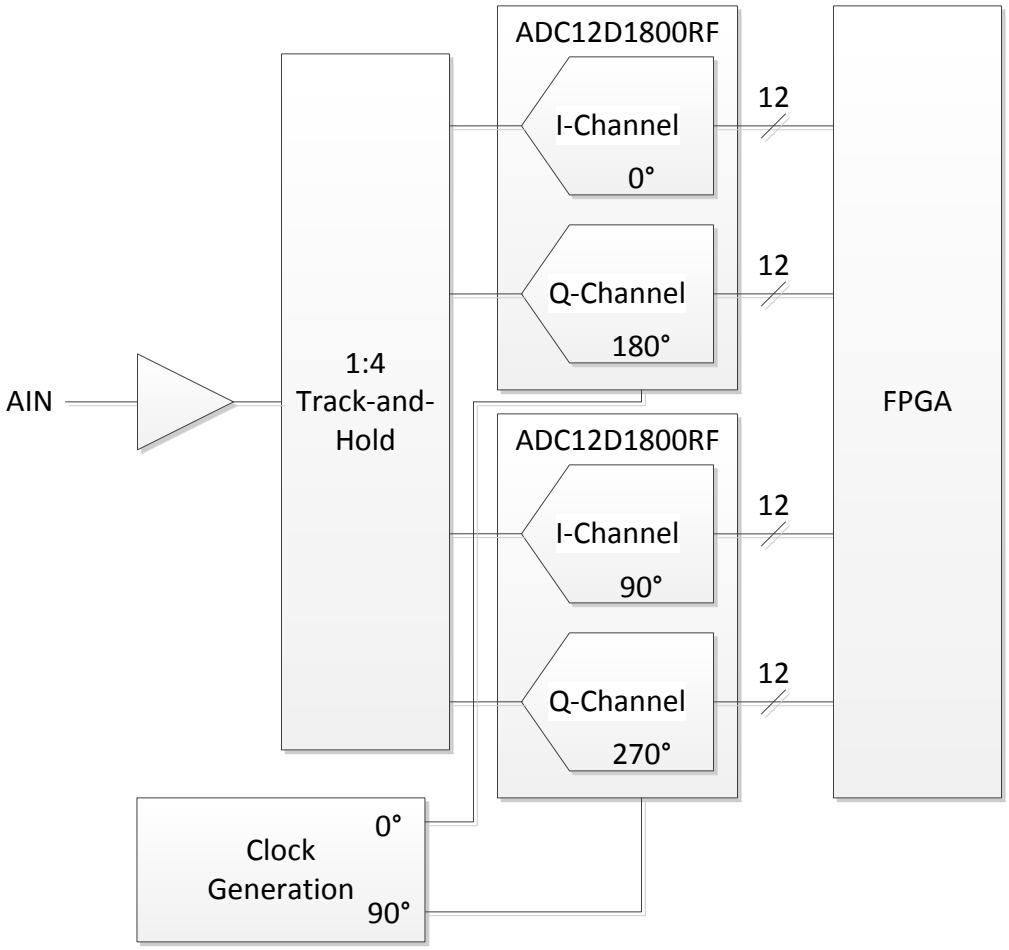

Figure 45. Using DESCLKIQ Mode to Interleave ADCs With Maximum Bandwidth

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Revision History A

Changes from Original (November 2013) to A Revision	Page
• Changed the values for Table 7 *DESCLKIQ Mode Summary*	21

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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