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TI Designs

12-Bit, 4/8 Channel, Integrated Analog Input module for Programmable Logic Controllers (PLC)

TEXAS INSTRUMENTS

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Design Resources

TIDA-00118	Output Module Design Files
TIDA-00123	IO Controller Design Files
ADS8638	Product Folder
REF3330	Product Folder
OPA4140	Product Folder
LM5069	Product Folder
LM5017	Product Folder
TPS7A3001	Product Folder
TPS71501	Product Folder
TPS71533	Product Folder
ISO7141	Product Folder

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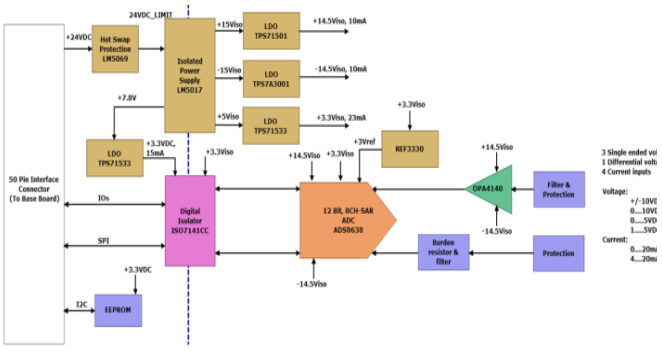
Block Diagram

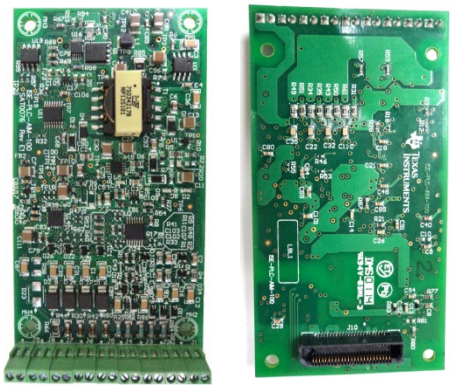


Design Features

- Designed to comply with IEC61000-4 standards for ESD, EFT and Surge
- Up to 8 channels user programmable inputs and configurable over-range capability of 20%
- Four Voltage Inputs: (3 Single ended & 1 Differential with impedance > 1M)
  - o ±10V, ±5V, ±2.5V, 0-10V,0- 5V
    Up to ±12V with External Reference
- Four Current Inputs: (With input impedance of 250Ω) 0-20 mA, 4-20 mA
- 12-Bit SAR ADC with Digitally isolated SPI interface
- Accuracy over entire input range
  Voltage : < ±0.2% full scale at 25 °C
  Current :< ±0.35% full scale at 25 °C
- On-board isolated Flybuck power supply with inrush current protection
- Slim form factor 96 x 50.8x10mm (L x W x H)
- Pluggable to IO Controller for easy evaluation (TIDA-00123)
- LabView based GUI for functional testing and characterization

Featured Applications

- PLC: Current and voltage input module
- Remote PLCs and DCS
- Data Acquisition Systems
- Test and Measurement



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1 System Description

Standard industrial Analog Input (AI) modules are generally dedicated voltage or current inputs. This reference design using the ADS8638 measures standard industrial voltage and current inputs. Eight channels have been provided on the module.

The Analog Input Module reference design is intended as an evaluation module for users to develop end-equipment like PLC, Data acquisition, Test and Measurement systems etc. This design is an isolated Analog Input Module with Digital isolators for SPI interface and Flybuck transformer for power supply isolation. On-board EEPROM has been provided to store calibration data and module configuration. Screw type terminals for individual input channels have been provided for easy wiring. LEDs are provided for Power Supply indication.

The reference design provides a complete guide for the design of an Analog Input Module that can be configured for voltage or current inputs, for different ranges in a slim form factor. This module has been design to be pluggable to the IO Controller (TIDA-00123) for quick testing & evaluation. This module has been designed to comply with EMC standards for industrial environment. The design files include schematics, BOM, layer plots. Altium files, Gerber Files and an easy-to use Graphical User Interface (GUI).
The Analog Input Module has been tested for the following:

- Isolated SPI interface
- Voltage and Current inputs for functionality and accuracy
- Surge, EFT and ESD: Pre-compliance as per IEC61000-4 standards

2 Design Specification

12-Bit resolution SAR ADC configured as:

- Single ended voltage,
- Differential voltage
- Single ended Current

Inputs with software programmable ranges

Voltage	Current
• ±10V, • ±5V, • ±2.5V, • 0- 10V, • 0- 5V	• 0-20 mA • 4-20 mA

*Can be configured to measure Over-voltage up to 20%

Input impedance

Voltage > 1M Ω	Current < 300 Ω

Overall accuracy

Voltage Input: ±0.2% full scale at 25 °C	Current Input: ±0.35% full scale at 25 °C

Isolation

Power supply: 1500VAC	Signal: 2500

EMC

Test	Levels
IEC61000-4-2: Electro Static Discharge	±8k Air Discharge, ±4kV Contact Discharge
IEC61000-4-4 : Electrical Fast Transients	±2kV, 5kHz ±2kV,100kHz
IEC61000-4-5 : Surge	±1kV Common Mode

3 Block Diagram

The Analog Input Module has the following blocks:

1. Analog-to-Digital Convertor (ADC)
2. Power supply
3. Isolation
4. Interface

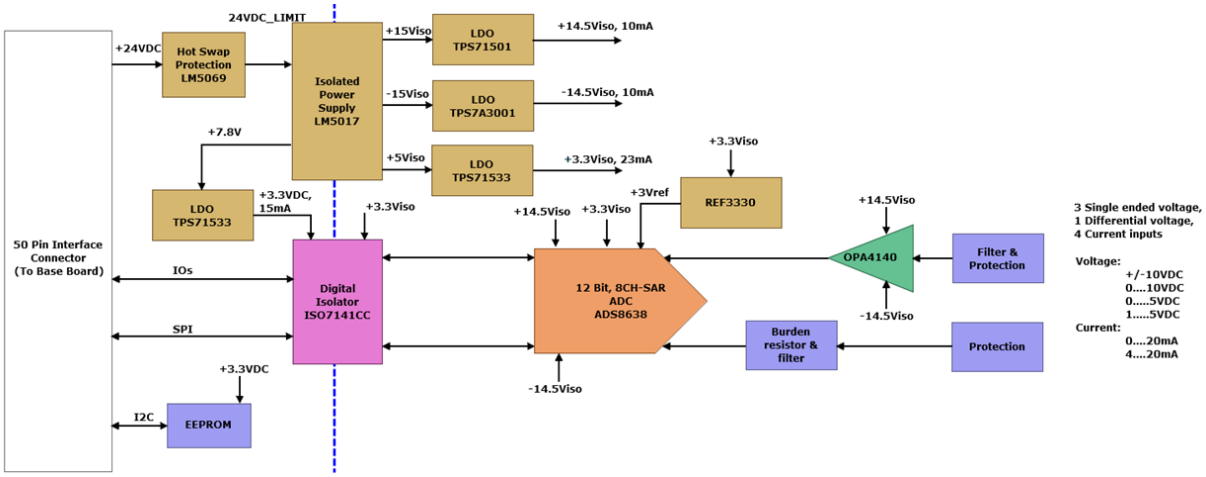


Figure 1 Block Level Design

Analog-to-Digital Converter (ADC):

This Module utilizes TI's 12-Bit resolution ADS8638. This ADC has 8 multiplexed input channels with software programmable input ranges for individual channels. Maximum sampling rate is upto 1MSPS/ (Number of selected channels).Digital output of ADC is read over SPI interface. The module has an EEPROM that store all the calibration data and configuration.

Power Supply:

The required voltage rails for non-isolated and isolated sections are generated on-board using Flybuck converter topology. The voltage rails are derived from 24VDC from the IO Controller. The ADC and Op Amp needs +/-14.5V power supply. The ADC additionally needs 3.3V for digital interface and 3V reference. The power supply section uses LDO to reduce ripple.

Isolation:

Most AI modules require isolation from the backplane and other modules. This is typically accomplished by isolating the digital signals between the host processor/controller and the ADC in the AI Module. There are many topologies available to achieve the isolation but galvanic (capacitive) isolation has many advantages over other topologies and has been selected for this design. The Power supply isolation is achieved by the use of Flybuck configured transformer.

Interface:

The Analog Input Module has one 50 Pin connector for interface with IO Controller. This SPI signals, I2C signals and control signals from the IO controller card is connected to the AI module through this connector. Eight 2-pin connectors have been provided for connecting analog inputs and one 2-Pin connector for connecting system earth has been provided.

4 Circuit design and Component Selection

4.1 ADC

ADS8638 was chosen for this design for its wide bipolar and unipolar input range. ADS8638 is capable of measuring inputs up to ±10V at 1MSPS with no missing code and INL< ±1LSB. ADS8638 uses a capacitor-based switching method to create an adjustable input voltage range option. The device also features two preset alarms with hysteresis per channel. During normal operation, ADS8638 dissipates < 22.5 mW at 5V AVDD and ±15V supplies.

ADS8638 features software-selectable bipolar and unipolar ranges, has an internal reference (with an internal temperature sensor) with option to use an external reference. ADS8638 offers multiple software-programmable ranges ±10V, ±5V, ±2.5V, 0- 5V, and 0-10V with a 2.5V reference. Any of these ranges can be assigned to any analog input (for instance, ±10V can be assigned to AIN1 ± 2.5V to AIN2, 0- 10V can be assigned to AIN3, and so on). The Block Diagram is shown in figure2.

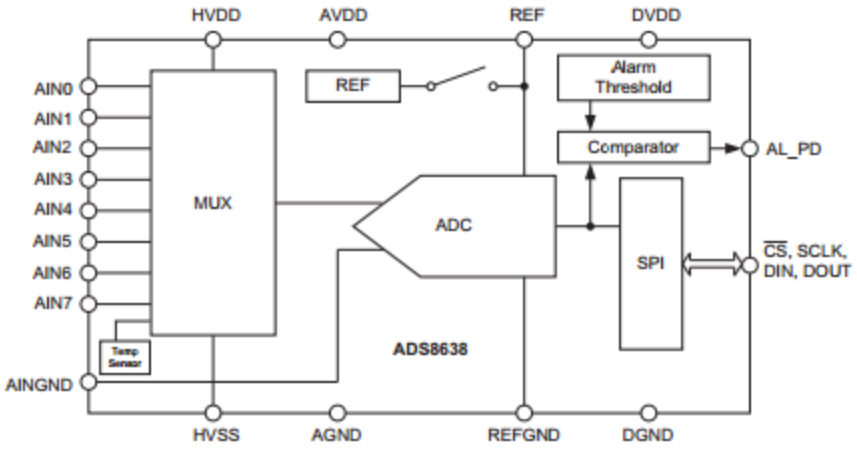


Figure 2 ADC Block Diagram

Bipolar Range Ideal Output Codes:

Bipolar Range Ideal Output Codes

INPUT SIGNAL (AINx – AINGND)			IDEAL OUTPUT CODE
±10V RANGE (V)	±5V RANGE (V)	±2.5V RANGE (V)	
≥ 10 × (2^{11}– 1)/2^{11}(2)	≥ 5 × (2^{11}– 1)/2^{11}	≥ 2.5 × (2^{11}– 1)/2^{11}	FFFh
10/2^{11}	5/2^{11}	2.5/2^{11}	801h
0	0	0	800h
–10 /2^{11}	–5/2^{11}	–2.5/2^{11}	7FFh
≤ –10 × (2^{11}– 1)/2^{11}	≤ –5 × (2^{11}– 1)/2^{11}	≤ –2.5 × (2^{11}– 1)/2^{11}	000h

Unipolar Range Ideal Output Codes:

Unipolar Range Ideal Output Codes

INPUT SIGNAL (AINx – AINGND)		IDEAL OUTPUT CODE
0V TO 10V RANGE (V)	0V TO 5V RANGE (V)	
≥ 10 × (2^{12}– 1)/2^{12}	≥ 5 × (2^{12}– 1)/2^{12}	FFFh
10/2^{12}	5/2^{12}	001h
< 10/2^{12}	< 5/2^{12}	000h

4.1.1 ADC reference

The ADS8638 can be configured for internal or external reference. The external reference used is REF3330AIDCK, which allows increasing input range by 20%. An external reference can be connected to ADC using zero ohm resistors.

4.1.2 Voltage Input

The Analog Input Module has been configured for three single ended voltage inputs and one differential voltage input. The front end of the ADC input includes an OPA4140. The Op Amp is configured as unity gain amplifier and has RC low-pass filters. This filter at the input stage filters external noise. To achieve the best performance from the ADC, Op Amp input signal chain, Op Amp with high PSRR has been selected. The high input impedance of Op Amp reduces loading effect when external transducers are connected and also meets input impedance requirement of >1MΩ.

4.1.3 Current Input

The current input has an impedance of 250 Ω. The Current inputs are single ended and has the required protection and filtering at the front end.

4.1.4 ADC input filter

The RC filter is placed at the inputs to filter noise, minimize aliasing (i.e. frequency harmonics folding back into the pass band) and to serve as a "flywheel" or charge reservoir for the internal sample and hold circuitry of the ADC. The RC forms low pass filter with a cutoff frequency of $1/2\pi RC$. The voltage droop due to sampling capacitor of the ADC would be less than 5% of actual value if $C_{FLT} \geq 20 * C_{SH}$. Since C_{SH} is 8pF, C_{FLT} is set to 180pF for voltage channel and 0.1µF for current channel.

4.1.5 Filter and Protection for Surge, EFT and ESD

The input stage is designed to meet ESD, EFT and Surge requirements for industrial environment. Transient Voltage Suppressors (TVS diodes) are used to clamp the surge voltage.

Voltage Inputs:

Surge voltage	Surge generator resistor (Ω)	CDN resistance (Ω)	Series resistor (Ω)	R total (Ω)	Clamping voltage of the diode (V)	Delta (V)	Current (A)	Wattage (W)	Package
1200	2	40	100	142	29.5	1170.5	8.24	243.16	SOD-323

Selected Device	Condition	Wattage (W)
CD SOD323 - T 12 SC	Wattage at 25˚C	400
	Wattage de rated at 50˚C	320

CD SOD323 - T 12 SC has a clamp voltage of 29.5V at 14A. The IO signals need to meet 1kV surge level. To limit the maximum voltage seen by the Op Amp input stage, we need to limit the current to <14A for a voltage drop of 29.5V at the Op Amp inputs. For a 1kV surge and 10A max current through the TVS diodes, we will need a series resistance of 100Ω and of Pulse withstanding type.

Current Inputs:

Surge voltage	Surge generator resistor (Ω)	CDN resistance (Ω)	Series resistor (Ω)	R total (Ω)	Clamping voltage of the diode (V)	Delta (V)	Current (A)	Wattage (W)	Package
1200	2	40	33	75	29.2	1170.5	15.61	460.40	SMB (DO-214A

Selected Device	Condition	Wattage (W)
SMBJ18CA	Wattage at 25˚C	600
	Wattage derated at 50˚C	480

SMBJ18CA has a clamp voltage of 29.2V at 20.6A. The IO signals need to meet 1kV surge levels. To limit the maximum voltage seen by the Op Amp input stage, we need to limit the current to <20.6A for a voltage drop of 29.2V at the Op Amp inputs. For a 1kV surge and 15A max current through the TVS diodes, we will need a series resistance of 33Ω and of Pulse withstanding type.
The ESD protection diodes also protect against overvoltage inputs. Layout guidelines have to be followed to ensure compliance to EMC standards. The protection devices are selected to dissipate the required energy.

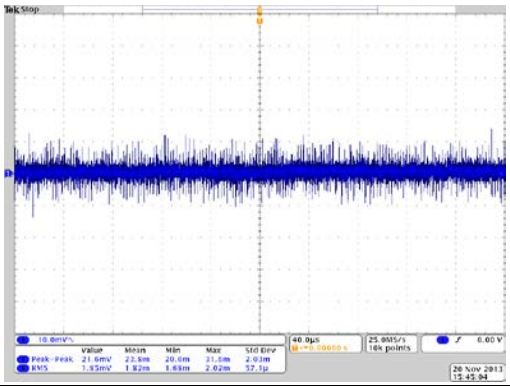
4.2 Power Supply

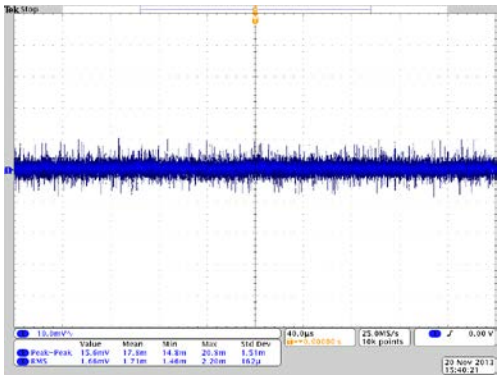
The Analog Input Module uses 24V DC from the IO Controller.

The LM5069 hot swap controller provides intelligent control of the power supply connections during insertion and removal of module from the powered IO Controller. The LM5069 provides in-rush current limiting during turn-on and monitoring of the load current for faults during normal operation. Additional functions include Under-Voltage Lock-Out (UVLO) and Over-Voltage Lock-Out (OVLO) to ensure voltage is supplied to the load only when the system input voltage is within a range. The inrush current of the module is limited to 2.75A.

The ADC and Op Amps are supplied with +/- 14.5V, which is derived from Flybuck DC-DC converter (LM5017) followed by a low noise LDOs. A 0.47µF capacitor is placed near the LM5017 to provide a bypass path for the high frequency component of the switching current. This reduces the switching noise. The Flybuck DC-DC converter is designed to give +/-15V and 5V with a ripple of <50mV peak. A soft-start feature is implemented to the LM5017 to limit the inrush current.

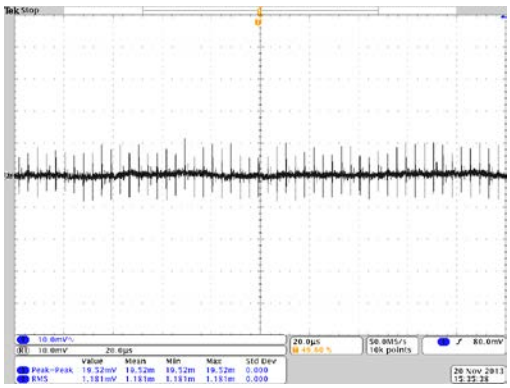
The DC-DC converter output is given to LDO TPS71501DCKR and TPS7A3001, which has a PSRR of 55dB from 10kHz to 1MHz frequency range, refer AN-2292.





Ripple on 3.3VDC power supply

Ripple on +14.5VDC



Ripple on -14.5VDC

4.3 Isolation

4.3.1 Power Isolation

The LM5017 based Flybuck Isolated Power Supply provides Galvanic Isolation to the IO controller. This Isolation is required to keep the IO controller protected from any unexpected overvoltage on the Analog input field connections. The level of isolation depends on the Coupled Inductor's specification. This design utilizes a coupled Inductor of 1500VAC, Isolation.

4.3.2 Digital Isolation

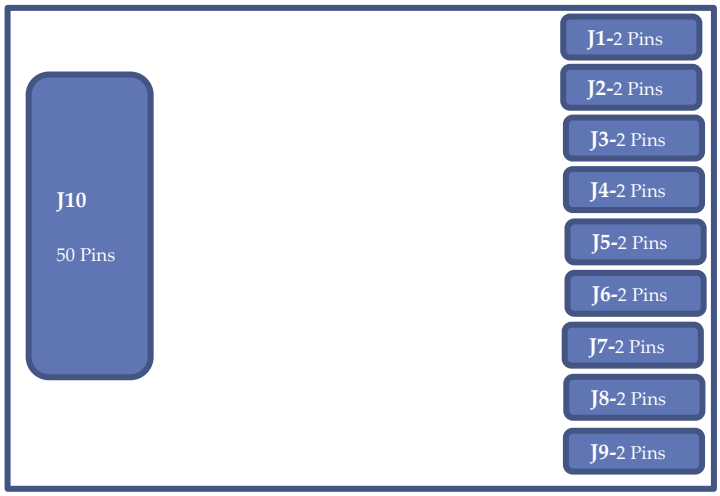
The IO Controller SPI is connected to the ADC SPI interface by the High Speed Digital Isolator ISO7141CC. 2.5kVrms Galvanic Isolation between IO Controller and Analog Input Module is maintained to protect IO Controller.

The SPI Signals isolated are: SCLK, MISO, MOSI, and /CS. Series termination resistors are provided to maintain Signal Integrity. In order to maintain isolation from the host controller, these signals are isolated through a digital isolator. The SPI Signals isolated are: SCLK, MISO, MOSI, CSO (Latch), CLR, SDRDY. The IO Controller is connected to the ADC by the High Speed Digital Isolator ISO7141CC and ISO7221. With this digital isolator the Host Processor on IO Controller maintains 2.5kVrms of galvanic isolation. Ten ohms termination resistance is placed near to the Isolators to maintain Signal Integrity.

4.4 Interface

The Analog Input Board has the following connector:

1. J1 to J8 : 2 Pin Screw Terminal type 2.54mm Pitch connectors for interfacing external inputs
2. J9 : 2 Pin Screw Terminal type 2.54mm Pitch connectors for connecting protective Earth
3. J10 : 50 Pin connector for connecting SPI , I2C and Power Supply from the IO Controller



4.5 Analog Input Module SPI communication timing

SPI Communication

The Master and Slave transmit the data on the bus on one clock phase and read the data on the next/opposite clock phase. SPI communication works fine without bit shift as long as the total round trip propagation delay is less than half of the clock period. Using Digital Isolators on the SPI bus for isolation can reduce the operating speed due to its propagation delay. The max speed at which Analog. Input Module can operate with isolators is derived below:

SPI Communication with Isolation

ADC clock to D_{out} output delay	33nsec (Max)
Isolator propagation Delay	45nsec (Max)
MCU setup time	17.15nsec (Min)
Total Delay	95.15nsec

Max SPI clock speed up to which SPI works with isolator: 5.25MHz
To increase the speed, CPLD solution has been implemented on the IO Controller board.

5 Software Description

The ADS8638 internal registers are mapped in two pages: page 0 and page 1. Page 0 is selected by default after power-up and reset.

Page 0 registers are used to select the channel sequencing mode, program the configuration registers, and to read the alarm flags. Page 1 resisters are used to program the alarm thresholds for each channel and for the temperature sensor.
A brief overview is as described here. For details refer the datasheet of ADS8638.

Page 0 Register Map for the ADS8638

REGISTER	REGISTER ADDRESS BITS[15:9]	DEFAULT VALUE(1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Channel Sequencing Control Registers										
Manual	04h	00h	0	Channel Select[2:0]			Range Select[2:0]			Sel Temp Sensor
Auto	05h	00h	Reset-Seq	0	0	0	Range Select[2:0]			Sel Temp Sensor
Holding the DIN line low continuously (equivalent to writing '0' to all 16 bits) during device operation as per Figure 85 continues device operation in the last selected mode (auto or manual).										
Configuration Registers										
Reset-Device	01h	00h	0	0	0	0	0	0	0	Reset-Dev
Aux-Config	06h	08h	0	0	0	0	AL_PD Control	Int V_{REF} Enable	Temp Sensor Enable	0
Auto-Md Ch-Sel	0Ch	00h	Sel Ch0	Sel Ch1	Sel Ch2	Sel Ch3	Sel Ch4	Sel Ch5	Sel Ch6	Sel Ch7
Ch0-1 Range	10h	11h	0	Range Select Ch0[2:0]			0	Range Select Ch1[2:0]		
Ch2-3 Range	11h	11h	0	Range Select Ch2[2:0]			0	Range Select Ch3[2:0]		
Ch4-5 Range	12h	11h	0	Range Select Ch4[2:0]			0	Range Select Ch5[2:0]		
Ch6-7 Range	13h	11h	0	Range Select Ch6[2:0]			0	Range Select Ch7[2:0]		
Alarm Flag Registerss (Read-Only)										
Temp-Flag	20h	00h	Tripped Alarm Flag Temperature Low	Tripped Alarm Flag Temperature High	Active Alarm Flag Temperature Low	Active Alarm Flag Temperature High	0	0	0	0
Ch0-3 Tripped-Flag	21h	00h	Tripped Alarm Flag Ch0 Low	Tripped Alarm Flag Ch0 High	Tripped Alarm Flag Ch1 Low	Tripped Alarm Flag Ch1 High	Tripped Alarm Flag Ch2 Low	Tripped Alarm Flag Ch2 High	Tripped Alarm Flag Ch3 Low	Tripped Alarm Flag Ch3 High
Ch0-3 Active-Flag	22h	00h	Active Alarm Flag Ch0 Low	Active Alarm Flag Ch0 High	Active Alarm Flag Ch1 Low	Active Alarm Flag Ch1 High	Active Alarm Flag Ch2 Low	Active Alarm Flag Ch2 High	Active Alarm Flag Ch3 Low	Active Alarm Flag Ch3 High
Ch4-7 Tripped-Flag	23h	00h	Tripped Alarm Flag Ch4 Low	Tripped Alarm Flag Ch4 High	Tripped Alarm Flag Ch5 Low	Tripped Alarm Flag Ch5 High	Tripped Alarm Flag Ch6 Low	Tripped Alarm Flag Ch6 High	Tripped Alarm Flag Ch7 Low	Tripped Alarm Flag Ch7 High
Ch4-7 Active-Flag	24h	00h	Active Alarm Flag Ch4 Low	Active Alarm Flag Ch4 High	Active Alarm Flag Ch5 Low	Active Alarm Flag Ch5 High	Active Alarm Flag Ch6 Low	Active Alarm Flag Ch6 High	Active Alarm Flag Ch7 Low	Active Alarm Flag Ch7 High
Page Selection Register										
Page	7Fh	00h	0	0	0	0	0	0	0	Page Addr

(1) All registers are reset to the default values at power-on or at device reset using the register settings method.

Page 1 Register Map for the ADS8638

REGISTER	REGISTER ADDRESS BITS[15:9]	DEFAULT VALUE(1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Alarm Threshold Registers										
TLA MSB	00h	00h	TLA Hysteresis[3:0]				TLA[11:8]			
TLA LSB	01h	00h	TLA[7:0]							
THA MSB	02h	00h	THA Hysteresis[3:0]				THA[11:8]			
THA LSB	03h	00h	THA[7:0]							
Ch0LA MSB	04h	00h	Ch0-LA Hysteresis[3:0]				Ch0-LA[11:8]			
Ch0LA LSB	05h	00h	Ch0-LA[7:0]							
Ch0HA MSB	06h	00h	Ch0-HA Hysteresis[3:0]				Ch0-HA[11:8]			
Ch0HA LSB	07h	00h	Ch0-HA[7:0]							
Ch1LA MSB	08h	00h	Ch1-LA Hysteresis[3:0]				Ch1-LA[11:8]			
Ch1LA LSB	09h	00h	Ch1-LA[7:0]							
Ch1 HA MSB	0Ah	00h	Ch1-HA Hysteresis[3:0]				Ch1-HA[11:8]			
Ch1 HA LSB	0Bh	00h	Ch1-HA[7:0]							
Ch2 LA MSB	0Ch	00h	Ch2-LA Hysteresis[3:0]				Ch2-LA[11:8]			
Ch2 LA LSB	0Dh	00h	Ch2-LA[7:0]							
Ch2 HA MSB	0Eh	00h	Ch2-HA Hysteresis[3:0]				Ch2-HA[11:8]			
Ch2 HA LSB	0Fh	00h	Ch2-HA[7:0]							
Ch3 LA MSB	10h	00h	Ch3-LA Hysteresis[3:0]				Ch3-LA[11:8]			
Ch3 LA LSB	11h	00h	Ch3-LA[7:0]							
Ch3 HA MSB	12h	00h	Ch3-HA Hysteresis[3:0]				Ch3-HA[11:8]			
Ch3 HA LSB	13h	00h	Ch3-HA[7:0]							
Ch4 LA MSB	14h	00h	Ch4-LA Hysteresis[3:0]				Ch4-LA[11:8]			
Ch4 LA LSB	15h	00h	Ch4-LA[7:0]							
Ch4 HA MSB	16h	00h	Ch4-HA Hysteresis[3:0]				Ch4-HA[11:8]			
Ch4 HA LSB	17h	00h	Ch4-HA[7:0]							
Ch5 LA MSB	18h	00h	Ch5-LA Hysteresis[3:0]				Ch5-LA[11:8]			
Ch5 LA LSB	19h	00h	Ch5-LA[7:0]							
Ch5 HA MSB	1Ah	00h	Ch5-HA Hysteresis[3:0]				Ch5-HA[11:8]			
Ch5 HA LSB	1Bh	00h	Ch5-HA[7:0]							
Ch6 LA MSB	1Ch	00h	Ch6-LA Hysteresis[3:0]				Ch6-LA[11:8]			
Ch6 LA LSB	1Dh	00h	Ch6-LA[7:0]							
Ch6 HA MSB	1Eh	00h	Ch6-HA Hysteresis[3:0]				Ch6-HA[11:8]			
Ch6 HA LSB	1Fh	00h	Ch6-HA[7:0]							
Ch7 LA MSB	20h	00h	Ch7-LA Hysteresis[3:0]				Ch7-LA[11:8]			
Ch7 LA LSB	21h	00h	Ch7-LA[7:0]							
Ch7 HA MSB	22h	00h	Ch7-HA Hysteresis[3:0]				Ch7-HA[11:8]			
Ch7 HA LSB	23h	00h	Ch7-HA[7:0]							
Page Selection Register										
Page	7Fh	00h	0	0	0	0	0	0	0	Page Addr

(1) All registers are reset to the default values at power-on or at device reset using the register settings method.

- Channel Sequencing Control Registers: There are two modes for channel sequencing: auto and manual mode
    - Auto-scan mode: the device automatically scans the preselected channels in sequential order with a new channel selected for every conversion
    - Manual mode, the channel is manually selected for the next conversion

  In both modes, the preselected signal range is considered for each channel independently
- Configuration Registers: The configuration registers allow device configuration (signal range selection for individual channels, selection of channels for auto sequence, enabling/disabling of the internal reference and temperature sensor, and configuration of the AL_PD pin as either an alarm output or a power-down input). All registers can be reset to the default values using the configuration register
- Alarm Flag Registers: The alarm conditions related to individual channels are stored in these registers. The flags can be read when an alarm interrupt is received on the AL_PD pin. There are two types of flag for every alarm: active and tripped. The active flag is set to '1' under the alarm condition (when data cross the alarm limit) and remains so as long as the alarm condition persists. The tripped flag turns on the alarm condition similar to the active flag, but it remains set until it is read. This feature relieves the device from having to track alarms
- Page Selection Register: The registers are arranged on two pages: page 0 and page 1. The page register selects the register page
- Alarm Threshold Setting Registers: The ADS8638 feature high and low alarms individually for the temperature sensor and each of the eight channels. Each alarm threshold is 12-bit wide

with a 4-bit hysteresis. This 16-bit setting is accomplished through two 8-bit registers associated with every high/low alarm

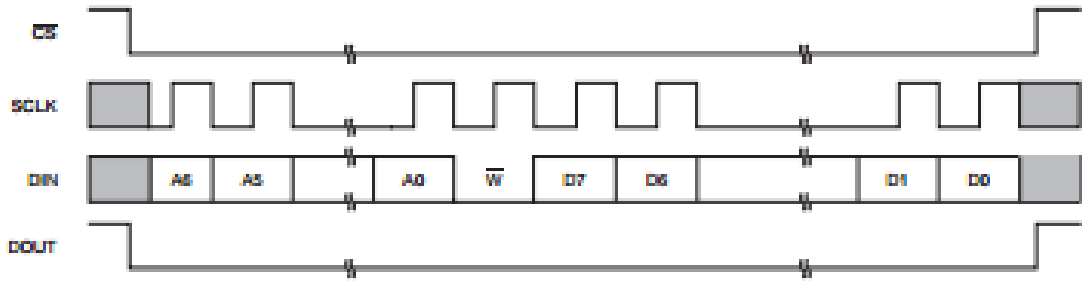
A typical programming sequence for the ADS868 is:

1. When module is powered up, by default ADC starts in manual mode channel 0, ±10V input range
2. Program the Configuration Registers (Page 0, Register 06h)
3. Program the Range Select Register (Page 0, Register 10h to 13h)
4. Program mode of operation:
   - Manual Mode: Page 0, Register 04h
   - Auto Mode: Page 0, Register 05h

Write Cycle Command Word:

	REGISTER ADDRESS							RD/WR	DATA							
PIN	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DIN	ADDR 6	ADDR 5	ADDR 4	ADDR 3	ADDR 2	ADDR 1	ADDR 0	R/$\overline{W}$	DIN7	DIN6	DIN5	DIN4	DIN3	DIN2	DIN1	DIN0

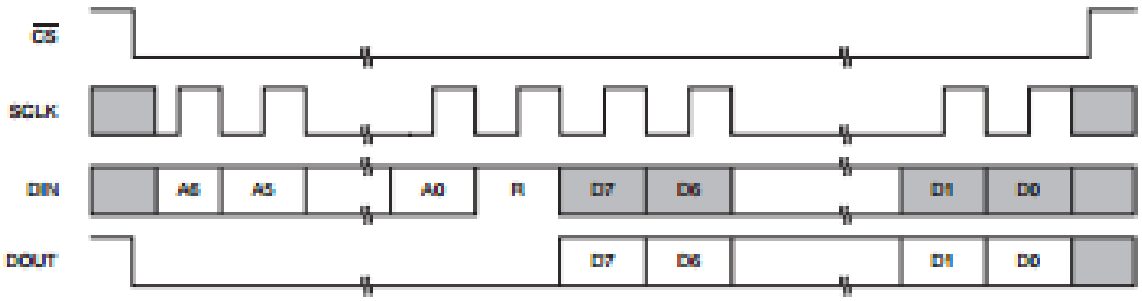
Write cycle:



Read Cycle Command Word:

	REGISTER ADDRESS							RD/WR	DATA							
PIN	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DIN	ADDR 6	ADDR 5	ADDR 4	ADDR 3	ADDR 2	ADDR 1	ADDR 0	R/$\overline{W}$	X	X	X	X	X	X	X	X
DOUT	X	X	X	X	X	X	X	X	DOUT 7	DOUT 6	DOUT 5	DOUT 4	DOUT 3	DOUT 2	DOUT 1	DOUT 0

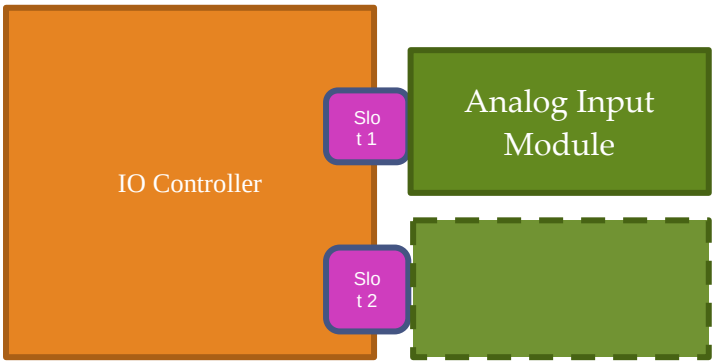
Read Cycle:

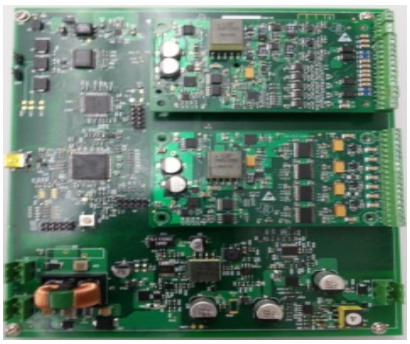


6 Test Setup

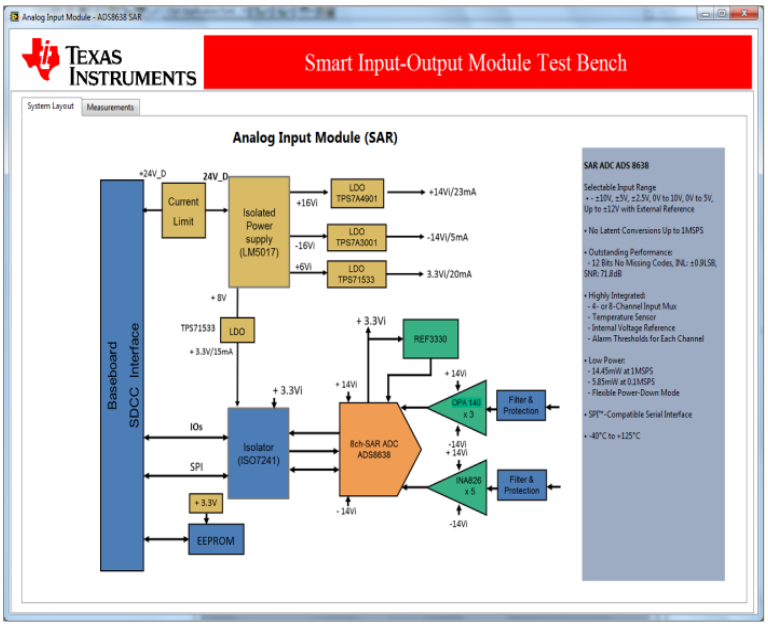
6.1 Hardware Test setup

Functional Test setup
The IO Controller has the required connectors and the MCU to interface with the Analog Input Module. 24V power input to the Analog Input Module is supplied by the IO Controller.

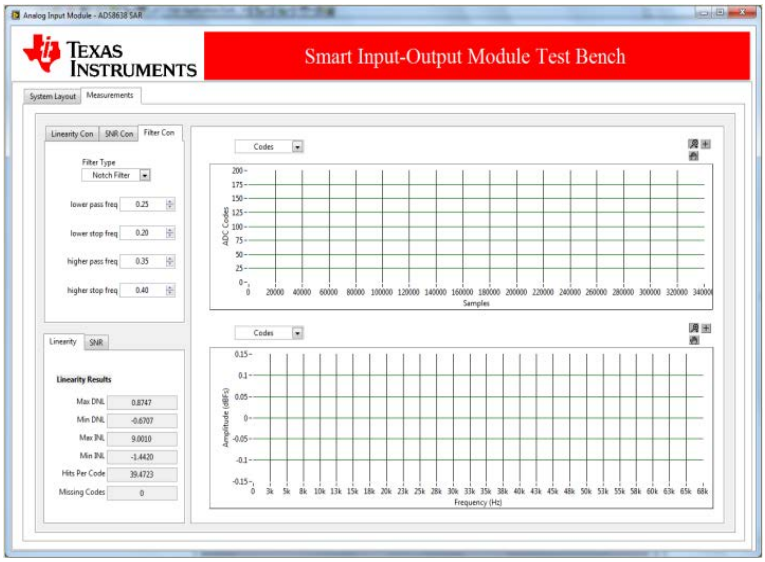




The IO Controller communicates with the Analog Input Module through an isolated SPI interface. A graphical user interface is provides to communicate with the IO Controller.



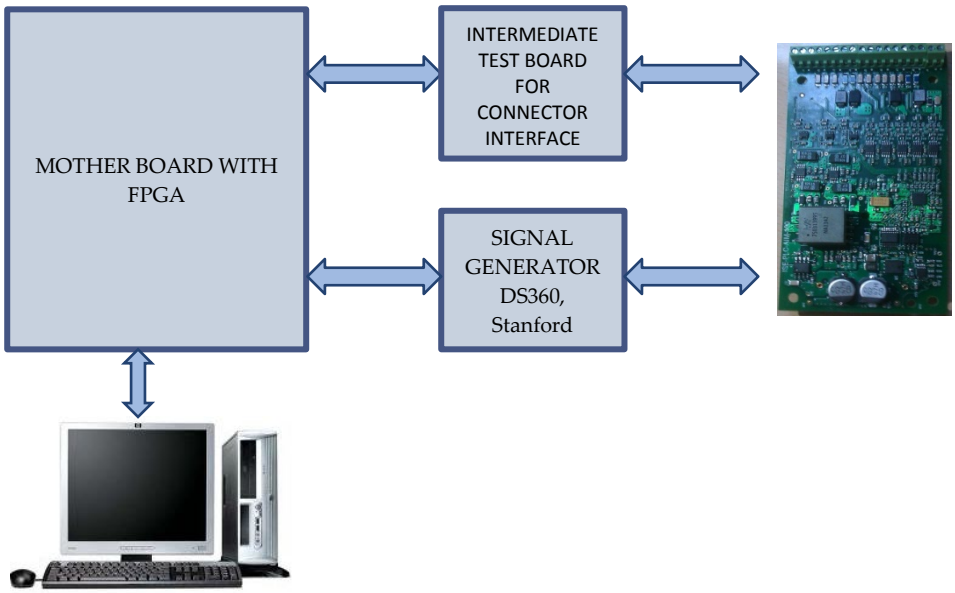
GUI to demonstrate the signal chain information



GUI to demonstrate the results

6.2

Characterization



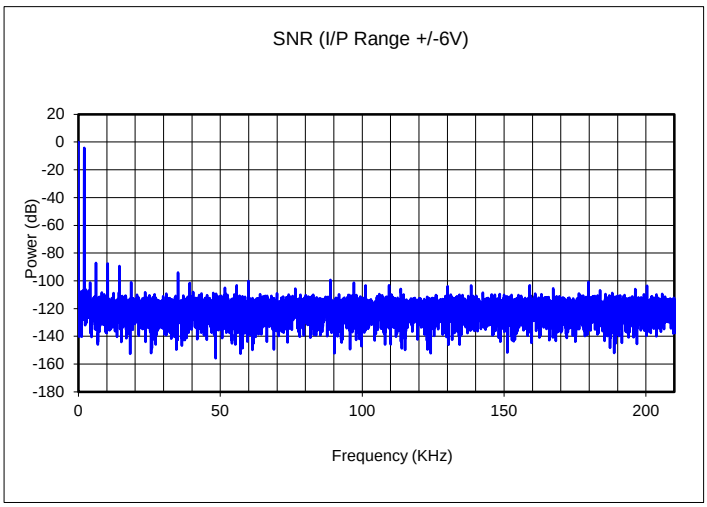
The design verification setup uses FPGA and GUI based Test Setup. The GUI on the PC connects to the FPGA based data capture card through USB communication. The FPGA based data capture card then controls the Analog Input Card via SPI interface. The setup has a precision signal generator (DS360, Stanford Research Systems), which feeds the analog input signal to the Analog Input Module. The Digital Output generated is measured by the data capture card. The GUI does the computation of results.

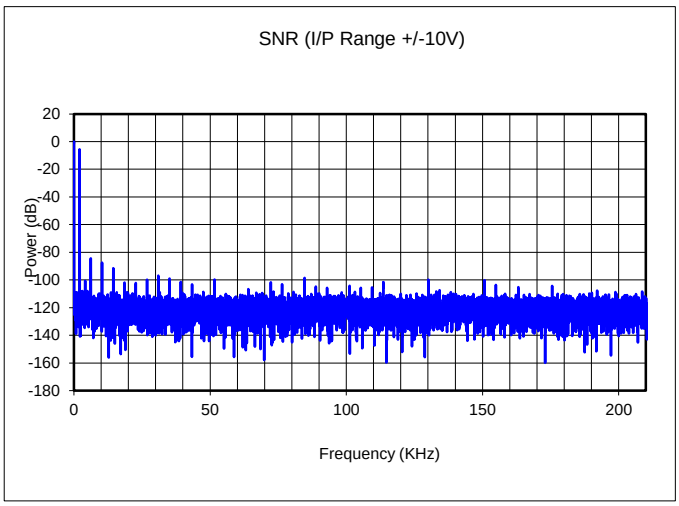
The GUI is LabView based software. It can set the below functionalities:

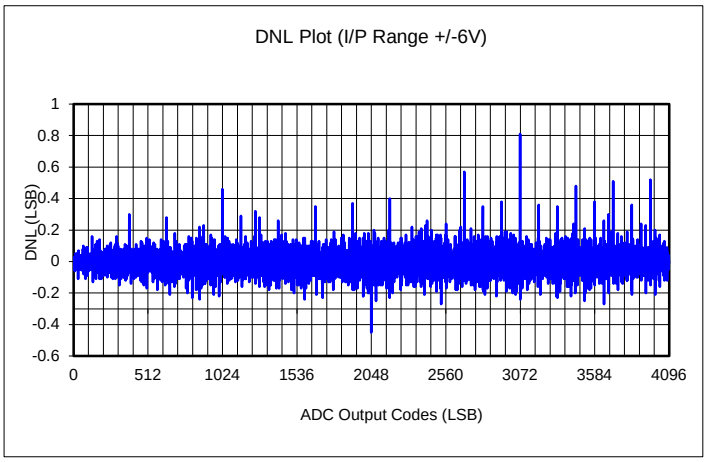
1. Configures all the registers in the ADS8638
2. The GUI controls data capture card to generate the required serial communication patterns
3. Reads the digitized data from the module
4. Post processing of the data
5. Result Options: SNR, ENOB, DNL, INL and CMRR

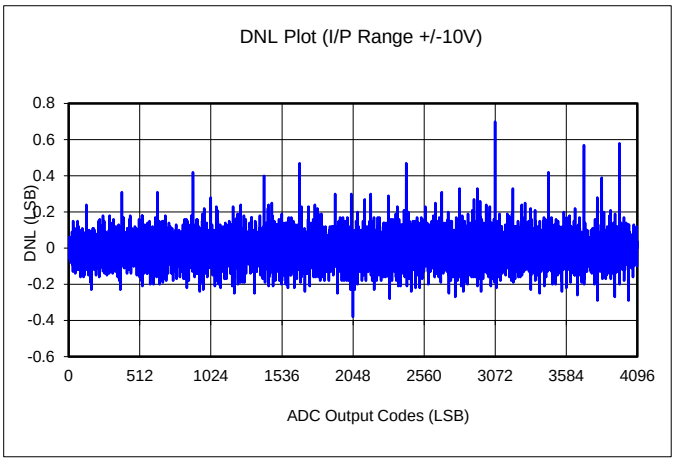
7 Test Results

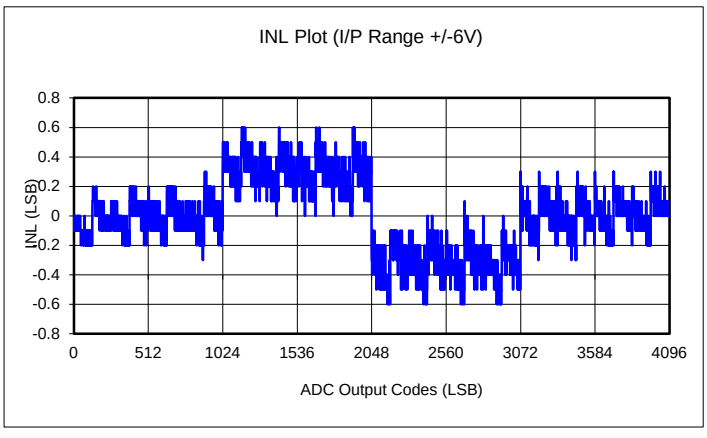
7.1 Typical performance characteristics

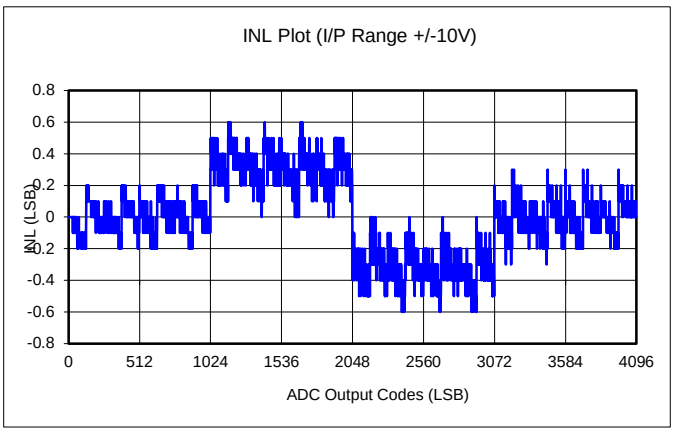


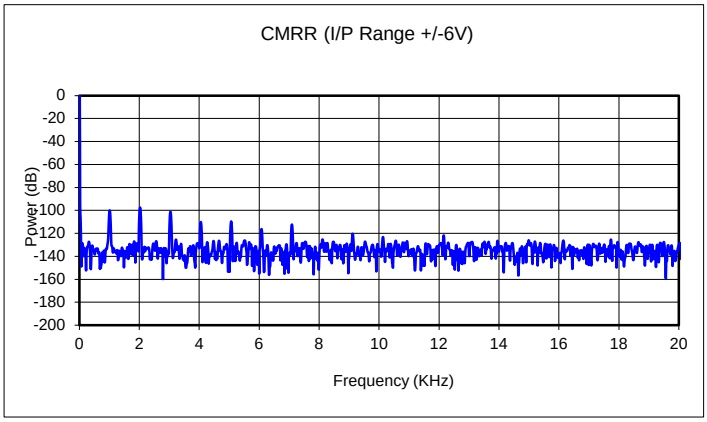


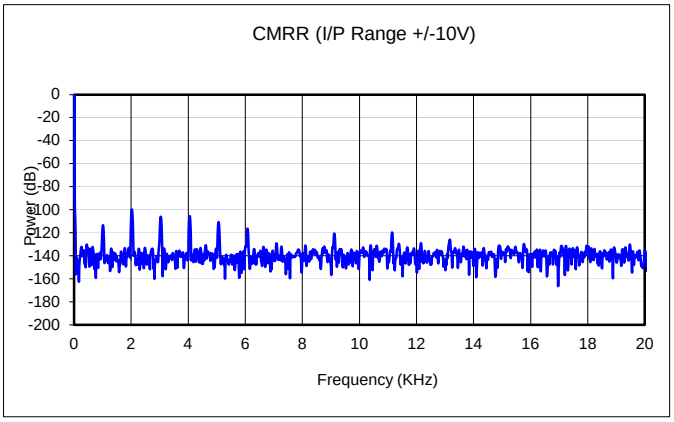












7.2 Results Summary

Sr. No.	Parameter	6V Range	10V Range	Expected Result	Note
1	Signal to Noise ratio	72.19dB	71.13dB	71.8dB	Measured For 10V Range , used ADC internal reference
2	Total Harmonic Distortion	78.80dB	76.00dB	81 dB	
3	SINAD	71.33dB	69.92dB	71.3dB	
4	SFDR	82.83dB	78.71dB	83 dB	
5	ENOB	11.56	11.32	11.59	
6	Max DNL	0.8137	0.6995	1.6	
7	Min DNL	-0.4491	-0.3753	-1	
8	Max INL	0.636	0.7106	1.5	
9	Min INL	-0.6254	-0.7312	-1.5	
10	CMRR	100 dB	110 dB	95 to 115 dB	Measured at At 1KHz
11	CMRR	104 dB	110 dB	95 to 115 dB	Measured at At 50Hz

Table 1 Measurement Results Summary

7.3 Pre compliance Testing

The Analog Input Module has been designed to meet standard EMC requirements for Industrial PLC application.

The following EMC tests have been performed

Tests	Standards
Electro Static Discharge	IEC61000-4-2
Electrical Fast Transients	IEC61000-4-4
Surge	IEC61000-4-5

Criteria and performance as per IEC61131-2

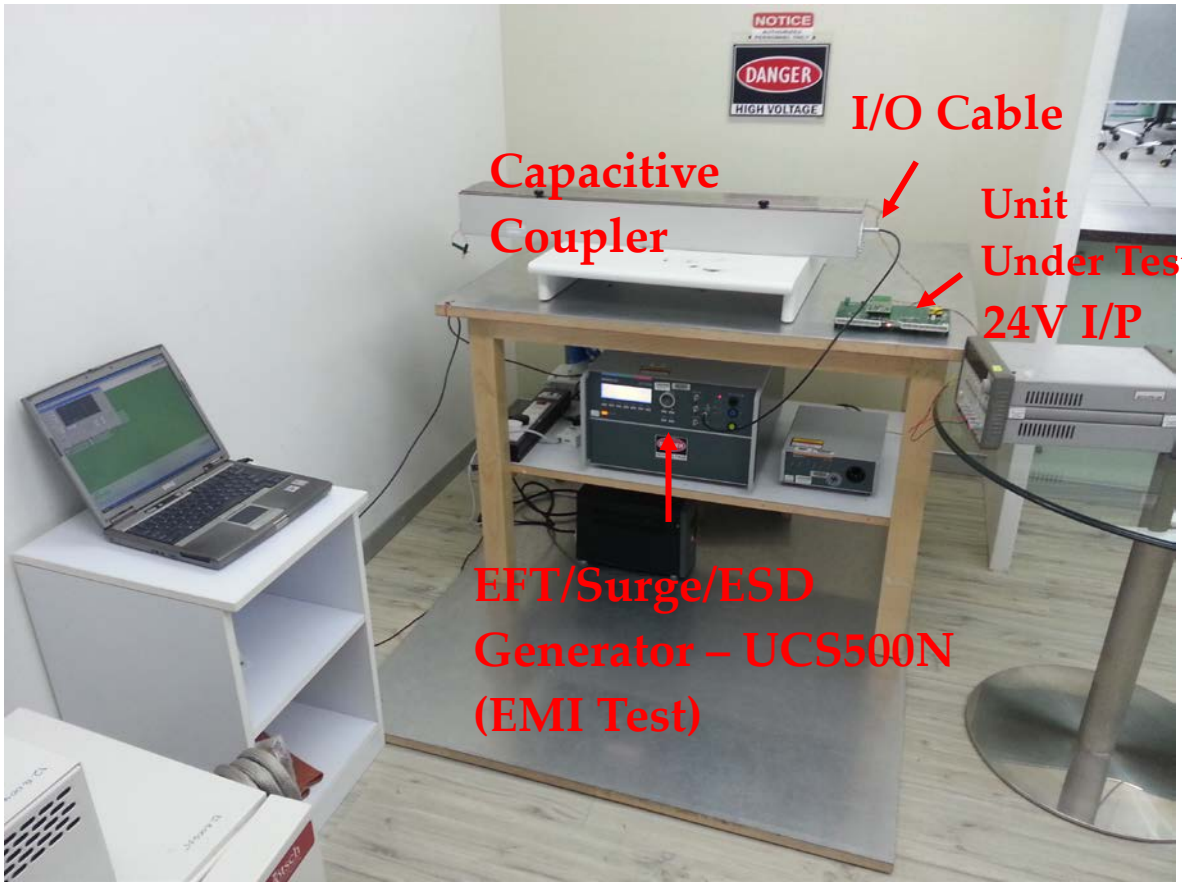
Criteria	Performance (Pass) Criteria
A	The Analog Output Module shall continue to operate as intended. No loss of function or performance even during the test.
B	Temporary degradation of performance is accepted. After the test Analog Output Module shall continue to operate as intended without manual intervention.
C	During the test loss of functions accepted, but no destruction of hardware or software. After the test Analog Output Module shall continue to operate as intended automatically, after manual restart or power off/power on.

The targeted accuracy for criteria A is

- Voltage Terminal: ±0.2% full scale at 25 °C
- Current Terminal: ±0.35% full scale at 25 °C

The next sections explain the test setup, procedures and observations.

7.3.1 Test Set-Up



7.3.2 Electro Static Discharge (ESD): IEC61000 -4-2

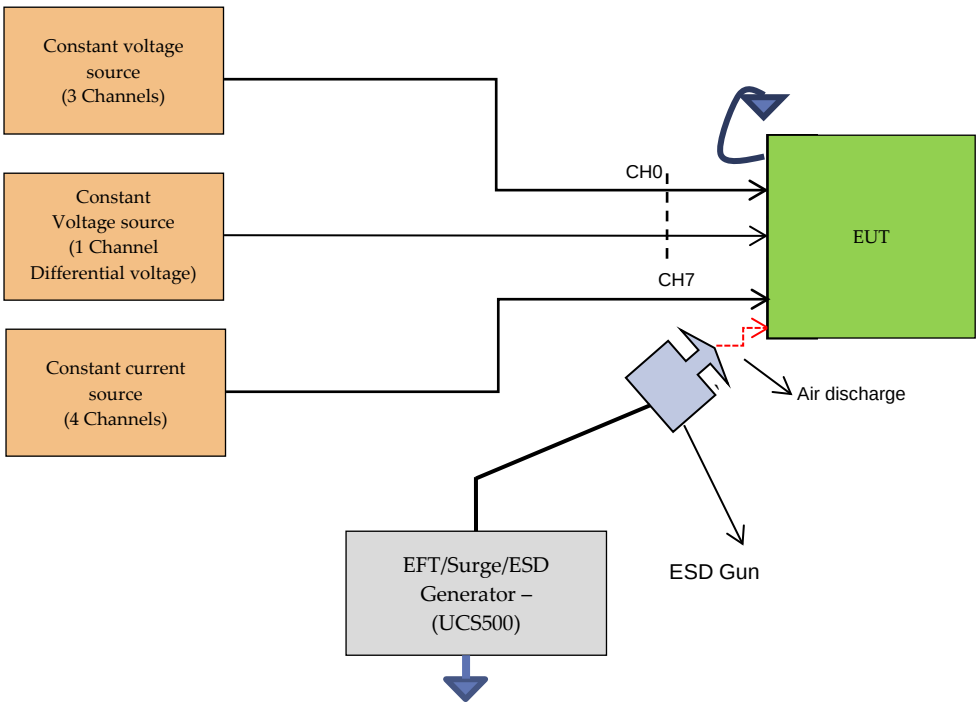
Test Level & Expected Performance

The ESD level at I/O connectors and the performance criteria expected are as follows:

Generic Test Standard	Test Level	Performance
ESDIEC 61000-4-2	4 kV contact discharges – Level 2 8 kV air discharges – Level 3	Criteria B (After the test Analog Input Module continued to operate as intended)

Setup Description

The ESD is injected to the EUT in two ways: **Contact discharge or Air discharge.**



The EUT is placed on a horizontal coupling plane (HCP) of 160 x 80cm dimensions on top of a wooden table 80cm high and located above ground reference plane. The EUT and its attached cables were isolated from the HCP by a thin insulating support of 0.5mm thickness. Electrostatic discharges were applied using an ESD gun directly (via contact or air discharges) or indirectly (via horizontal coupling plane). EUT operation was monitored after the test. The EUT is tested in active mode using unshielded 3m cables on IO ports.

- Connect the EUT as shown in the Test Setup. The shield Pin is connected to Local Earth same as the Test Generator
- Power on the EUT
  - The test s/w is configured to check the Analog Input for level with in a tolerance limit of 0.2%
  - If the input level exceed the tolerance limit, the LED on the IO Controller toggles
- Set the voltage level to 3VDC and current level to 8mA
- The ESD test is performed as per below test levels mentioned in below table
- After the test is performed, to check the degradation conduct a performance test

- Repeat the test by changing the input voltage level to 6VDC and current level to 16mA

Results

Test No	Test Mode	Observation
1	Air +2kV	PASS
2	Air– 2kV	PASS
3	Air +4kV	PASS
4	Air -4kV	PASS
5	Air +6kV	PASS
6	Air -6kV	PASS
7	Air +8kV	PASS
8	Air +8kV	PASS
9	Contact +1kV	PASS
10	Contact -1kV	PASS
11	Contact +2kV	PASS
12	Contact -2kV	PASS
13	Contact +4kV	PASS
14	Contact -4kV	PASS
15	HCP +2kV	PASS
16	HCP – 2kV	PASS
17	HCP +4kV	PASS
18	HCP -4kV	PASS
19	VCP +2kV	PASS
20	VCP – 2kV	PASS
21	VCP +4kV	PASS
22	HCP -4kV	PASS

7.3.3 Electric Fast Transients test: EFT – IEC61000 – 4-4

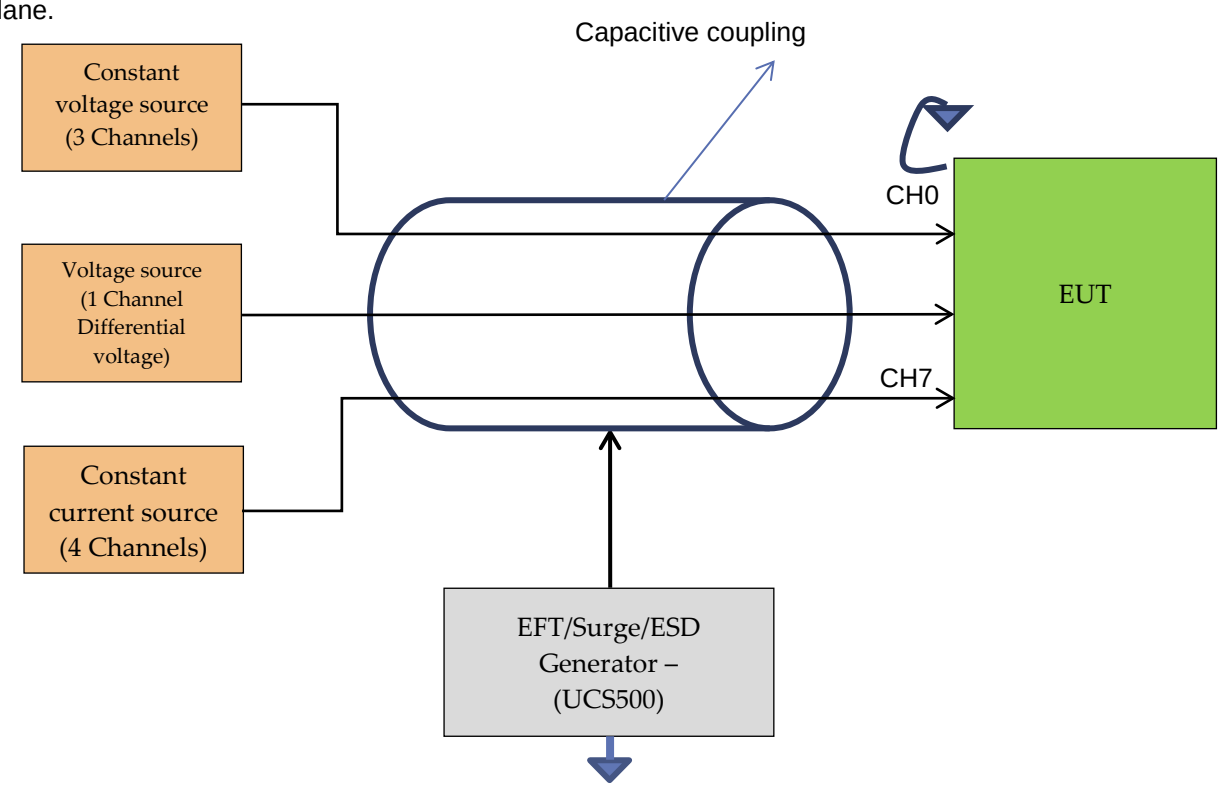
Test Level & Expected Performance

The EFT burst at I/O connectors and the performance criteria expected are as follows:

Generic Test Standard	Test Level	Performance
EFT/B IEC 61000-4-4	±2 KV at 5 KHz, 100KHz on signal ports	Criteria A

Description

Setup:
The burst signal is injected on all cables together using a Capacitive Coupling Clamp.
EUT is connected to auxiliary sources by unshielded cables. The lengths of the cables are set to 3m and cables are placed 10cm above the reference plane. The test is carried out with the EUT placed 10cm above the reference plane on insulating material, and with the EUT placed on the reference plane.



Monitoring:

- Connect the EUT as shown in the Test Setup. The shield Pin is connected to Local Earth same as the Test Generator.
- Power on the EUT
  - The test s/w is configured to check the Analog Input for level with in a tolerance limit of 0.2%
  - If the input level exceed the tolerance limit, the LED on the IO Controller toggles
- Set the voltage level to 3VDC and current level to 8mA
- The EFT test is performed as per below test levels mentioned in below table
- After the test is performed, to check the degradation conduct a performance test
- Repeat the test by changing the input voltage level to 6VDC and current level to 16mA

Results

Result summary to be updated with observations.

Test No	Test Mode	Observation
1	+ 0.5 kV , 5kHz	PASS
2	- 0.5 kV , 5kHz	PASS
3	+ 1 kV , 5kHz	PASS
4	- 1 kV , 5kHz	PASS
5	+ 1.5 kV , 5kHz	PASS
6	- 1.5 kV , 5kHz	PASS
7	+ 2 kV , 5kHz	PASS
8	- 2 kV , 5kHz	PASS
9	+ 0.5 kV , 100kHz	PASS
10	- 0.5 kV , 100kHz	PASS
11	+ 1 kV , 100kHz	PASS
12	- 1 kV , 100kHz	PASS
13	+ 1.5 kV , 100kHz	PASS
14	- 1.5 kV , 100kHz	PASS
15	+ 2 kV , 100kHz	PASS
16	- 2 kV , 100kHz	PASS

7.3.4 SURGE- IEC61000 -4-5

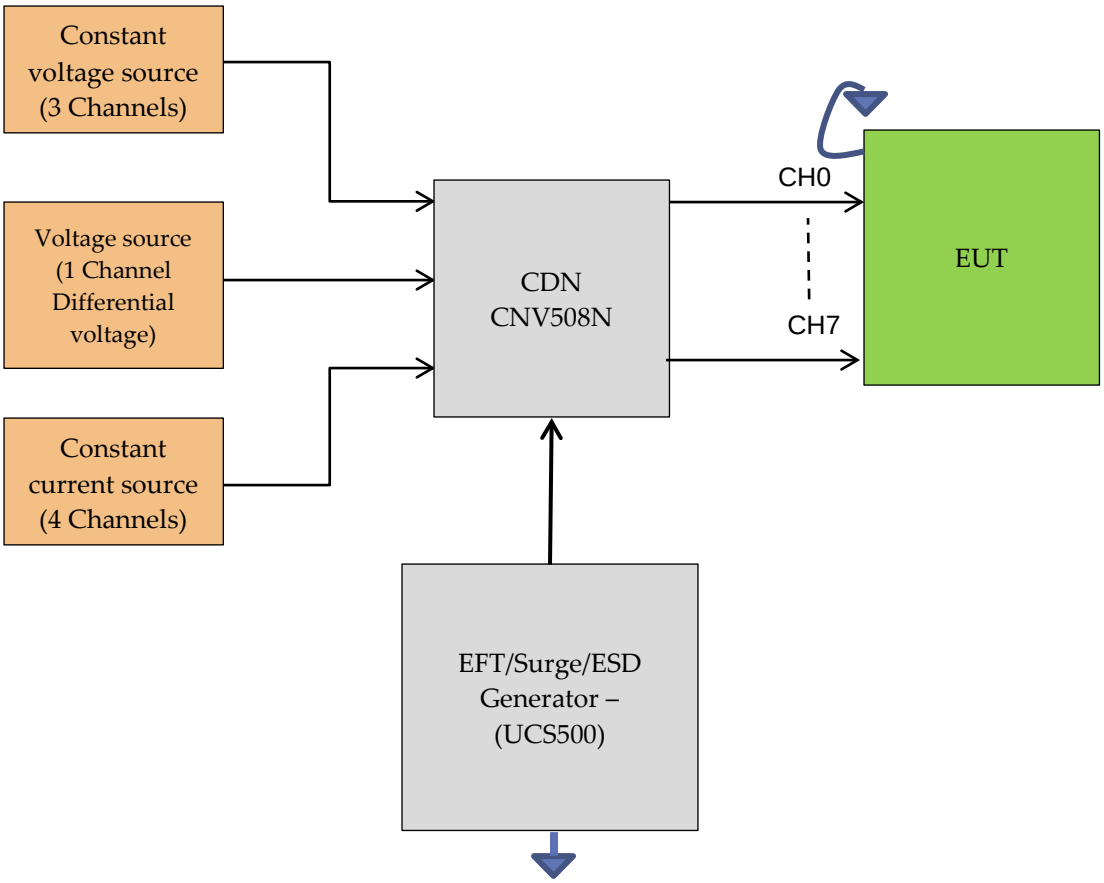
Test Level & Expected Performance

The Common-Mode Surge at I/O connectors and the performance criteria expected are as follows:

Generic Test Standard	Test Level	Performance
Surge IEC 61000-4-5	±1kV CM on signal ports	Criteria B (After the test Analog Input Module continued to operate as intended without manual intervention)

Description

Setup:
The EUT and analog input cable were placed on non-conductive support 10cm above a reference ground plane. Surge was injected into analog input cable (I/O cable) for testing via Coupling Decoupling Network. The EUT operation was monitored before and after the test.



EUT operation monitored after the test. All the eight channels were monitored after the test by the MCU (on IO Controller) and compared with a Set Value (equivalent of the external constant voltage or current source). The Error should be within accuracy as mentioned in Section 6.3.1.
Method of monitoring:

- Connect the EUT as shown in the Test Setup. The shield Pin is connected to Local Earth same as the Test Generator.
- Power on the EUT
  - The test s/w is configured to check the Analog Input for level with in a tolerance limit of 0.2%
  - If the input level exceed the tolerance limit, the LED on the IO Controller toggles
- Set the voltage level to 3VDC and current level to 8mA
- The Surge test is performed as per below test levels mentioned in below table
- After the test is performed, to check the degradation conduct a performance test
- Conduct the test by changing the input voltage level to 6VDC and current level to 16mA

Results

Test No	Test Mode	Observation
1	+ 0.5 kV	PASS
2	- 0.5 kV	PASS
3	+ 1 kV	PASS
4	- 1 kV	PASS

8 References

1. Texas Instruments Application Report, Noise Analysis in Operational Amplifier Circuits, SLVA043A, 1999
2. Op Amp Noise Theory and Applications Literature Number SLOA082 Design files

8.1.1 Terminology

Signal-to-Noise Ratio (SNR)
SNR is a measure that compares the level of a desired signal to the level of background noise. It is defined as the ratio of signal power to the noise power. The Signal-to-Noise Ratio (SNR) specification provides information regarding the noise energy excluding the fundamental and harmonic energy present in the frequency spectrum for a particular input frequency. The SNR calculation usually integrates noise till Nyquist frequency.

$$SNR = P_{SIGNAL} / P_{NOISE}$$

SNR = 10 log10 (Signal Power 2 / (Sum of all harmonic amplitudes without F_{IN} and without DC) * 2)

Total Harmonic Distortion (THD)
The Total Harmonic Distortion (THD) specification provides information regarding the harmonic energy present in the frequency spectrum for a particular input frequency. The frequency spectrum is typically shown till the Nyquist frequency and the THD calculation usually takes into account all the harmonics energy till Nyquist. Harmonics beyond Nyquist fall back into the frequency spectrum as noise or spurious tone. These are taken care of in the SNR and SINAD specifications.

THD = Summation of harmonic energy / Fundamental input energy

Signal-to-Noise and Distortion (SINAD)
The Signal-to-Noise and Distortion (SINAD) specification provides information regarding the noise and harmonic energy present in the frequency spectrum.

SINAD = Fundamental input energy / Summation of noise + distortion energy

Spurious Free Dynamic Range (SFDR)

The Spurious Free Dynamic Range (SFDR) specification provides information regarding the difference between maximum amplitude tone in frequency spectrum and the fundamental input tone.

SFDR = Fundamental input energy – Max (all frequency bins except fundamental)

Differential Non Linearity (DNL) and Integral Non Linearity (INL)

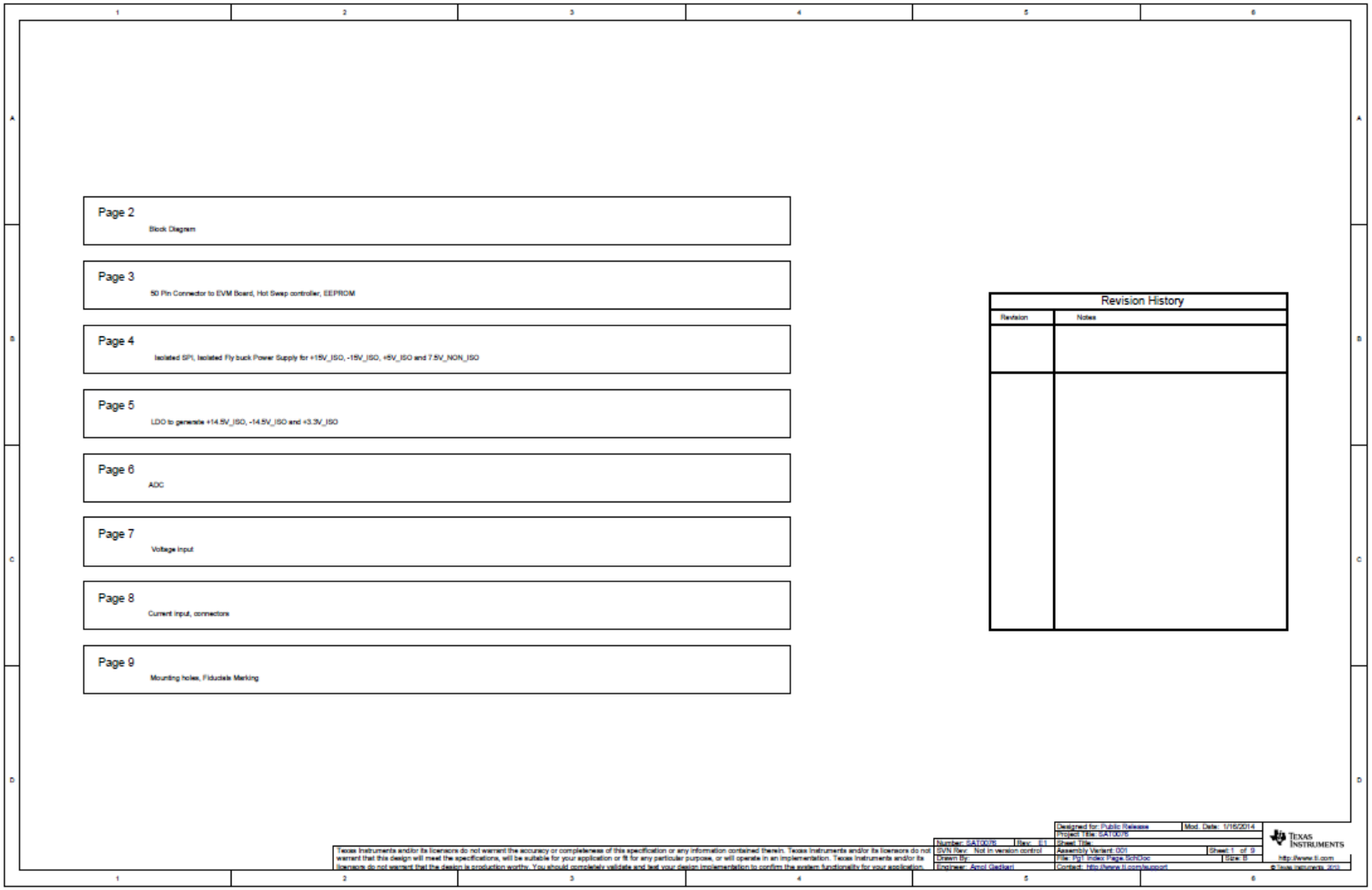
DNL is the deviation between two analog values corresponding to adjacent input digital values. Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. Any deviation from the ideal step width (LSB) is the Differential Non-Linearity.
DNL errors accumulate to produce a total Integral Non-Linearity (INL).
DNL and INL values are usually specified using one of the following units: LSB or %FSV

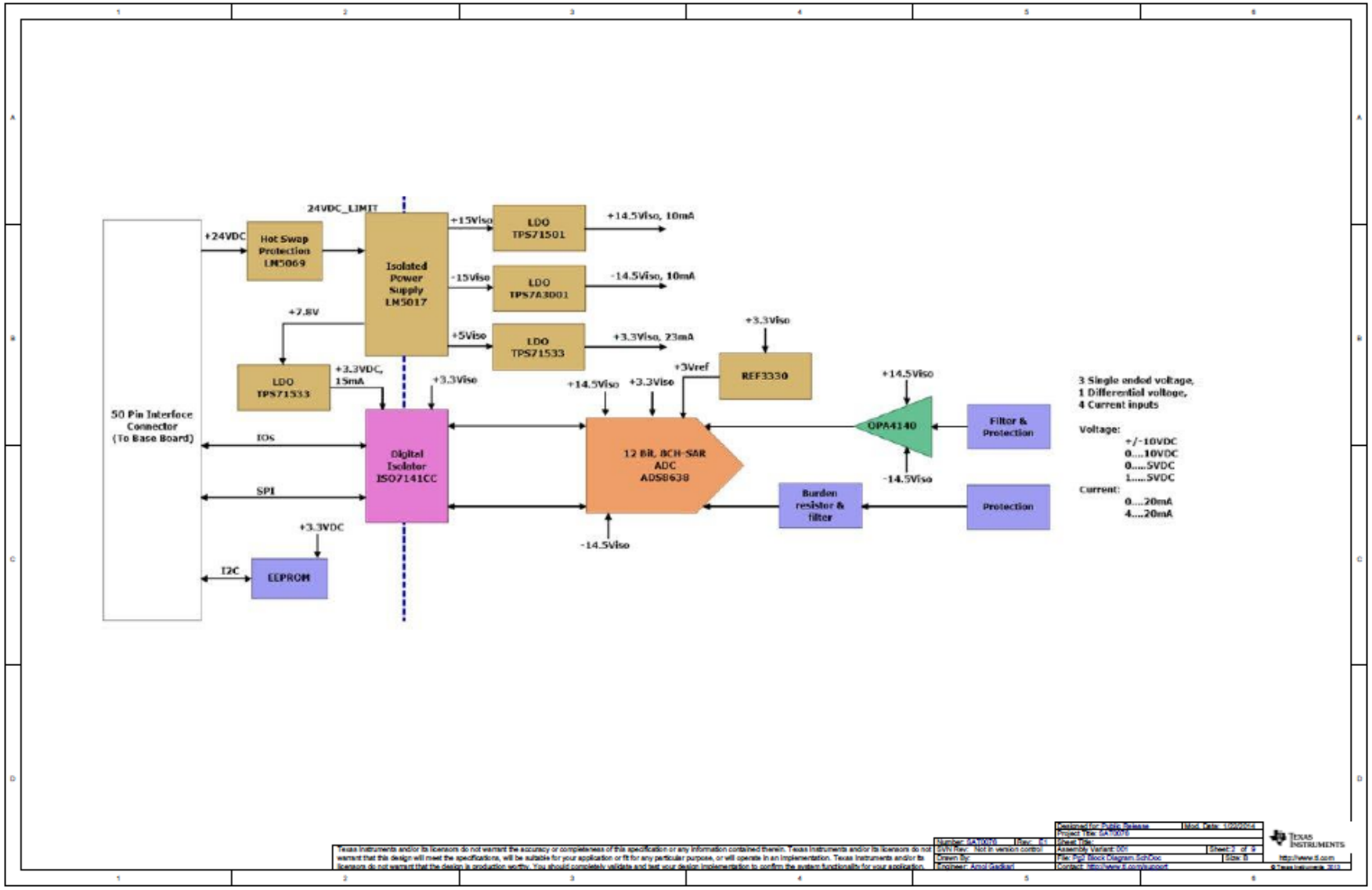
Common-Mode Rejection Ratio (CMRR)

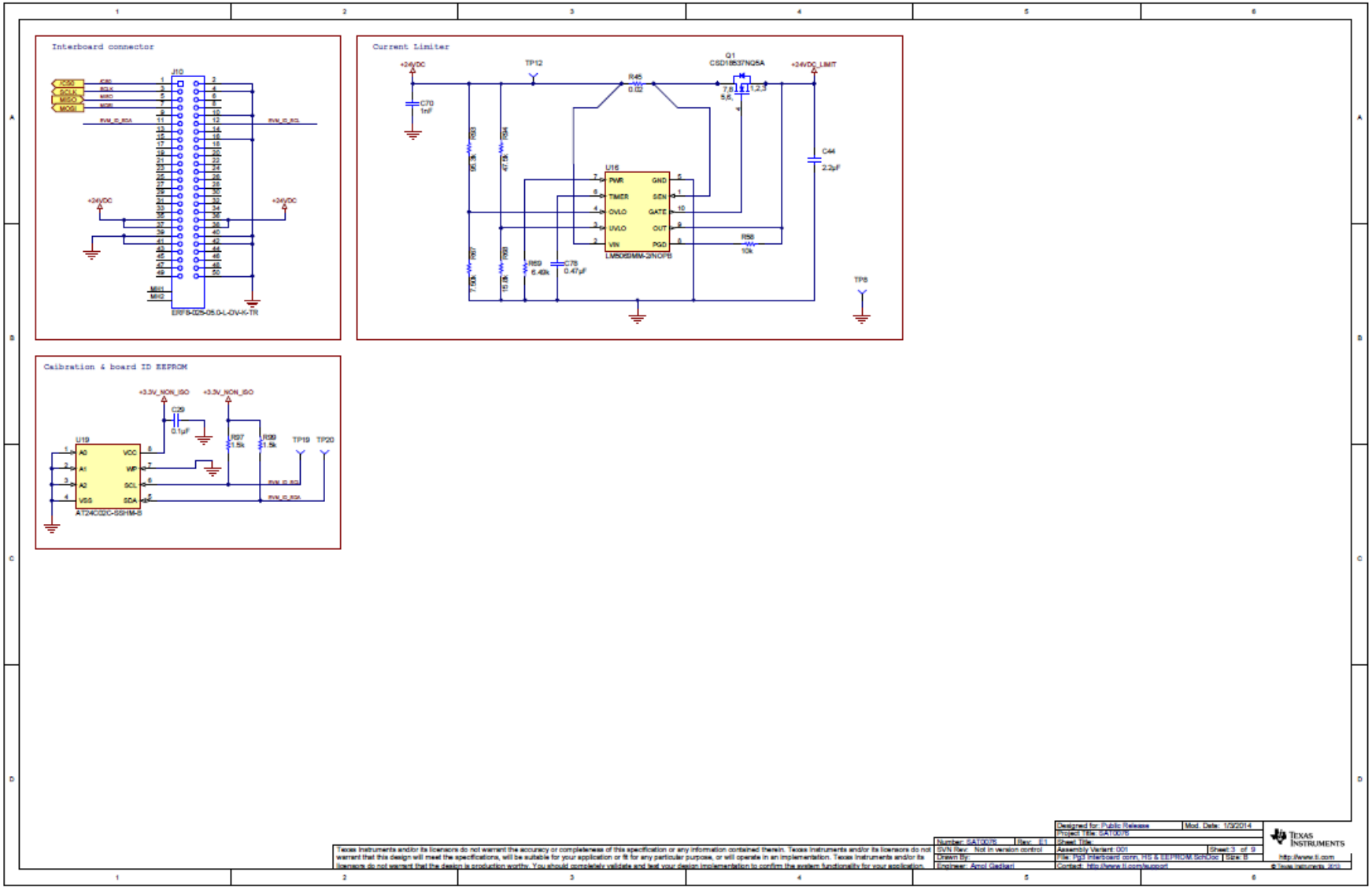
The common-mode rejection ratio (CMRR) is the tendency of the devices to reject common noise from the input signal.

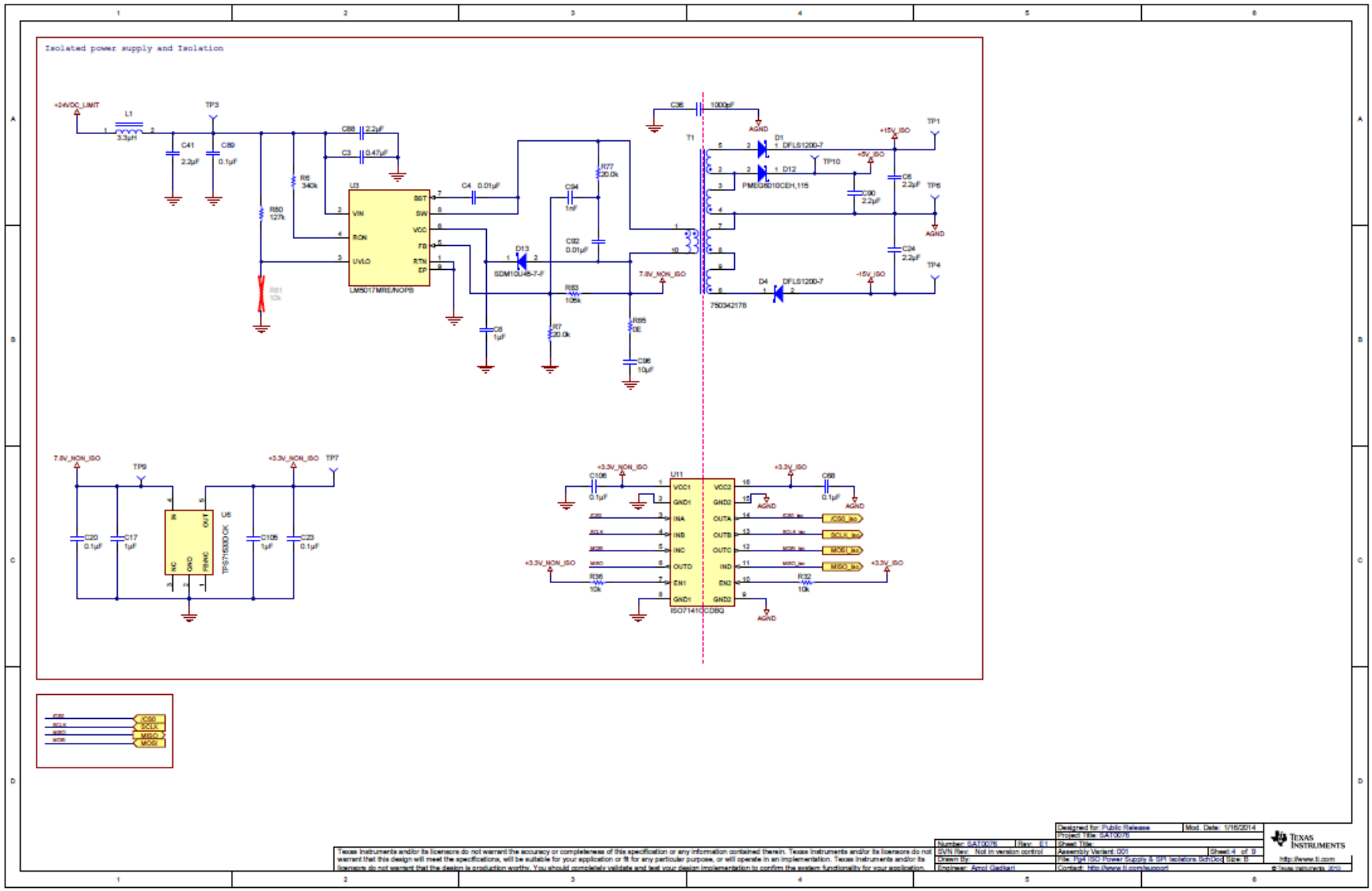
CMRR = Output Signal power (dB) – 20 log (Voltage Range/Input power)

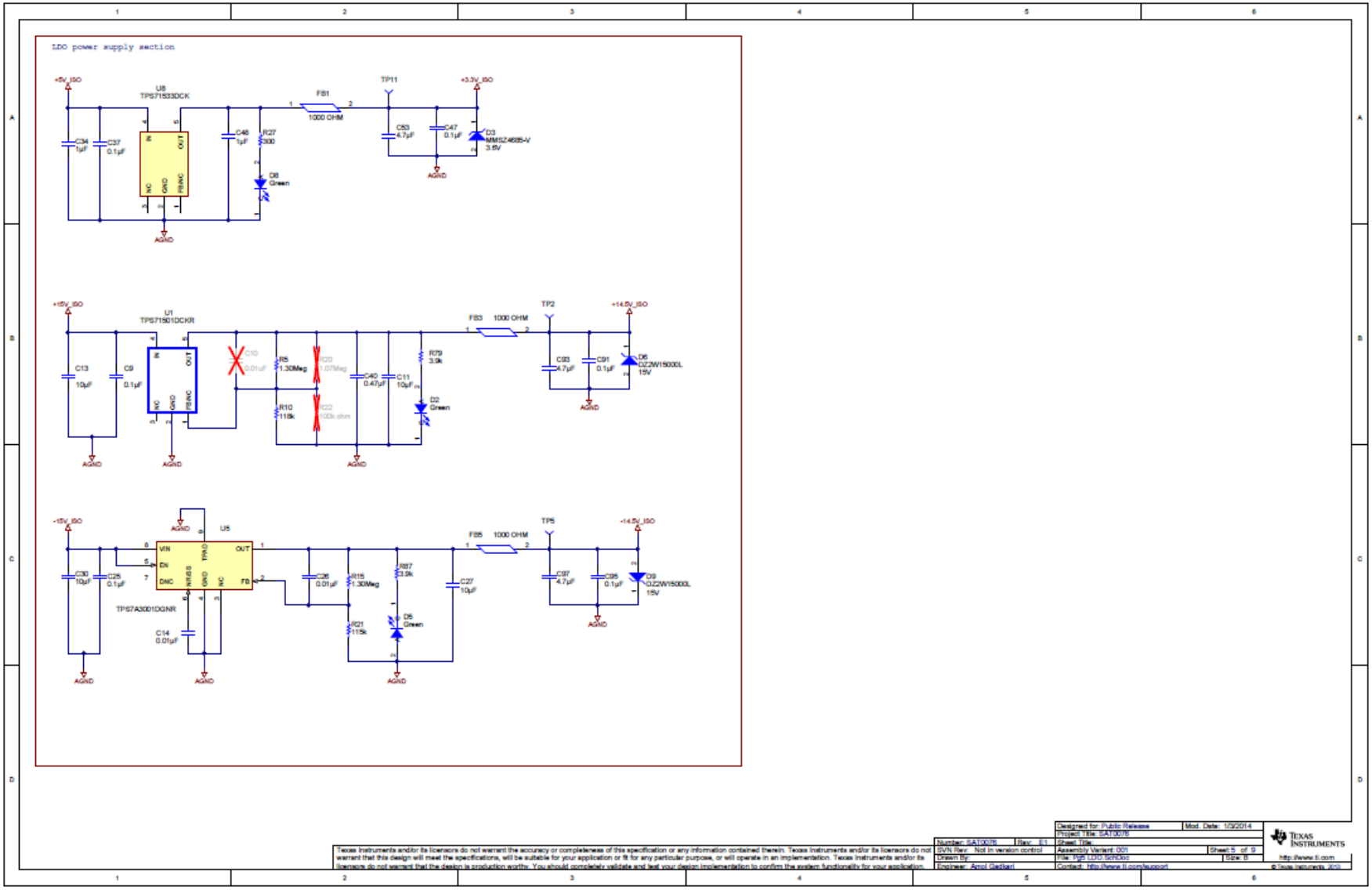
8.2 Schematics

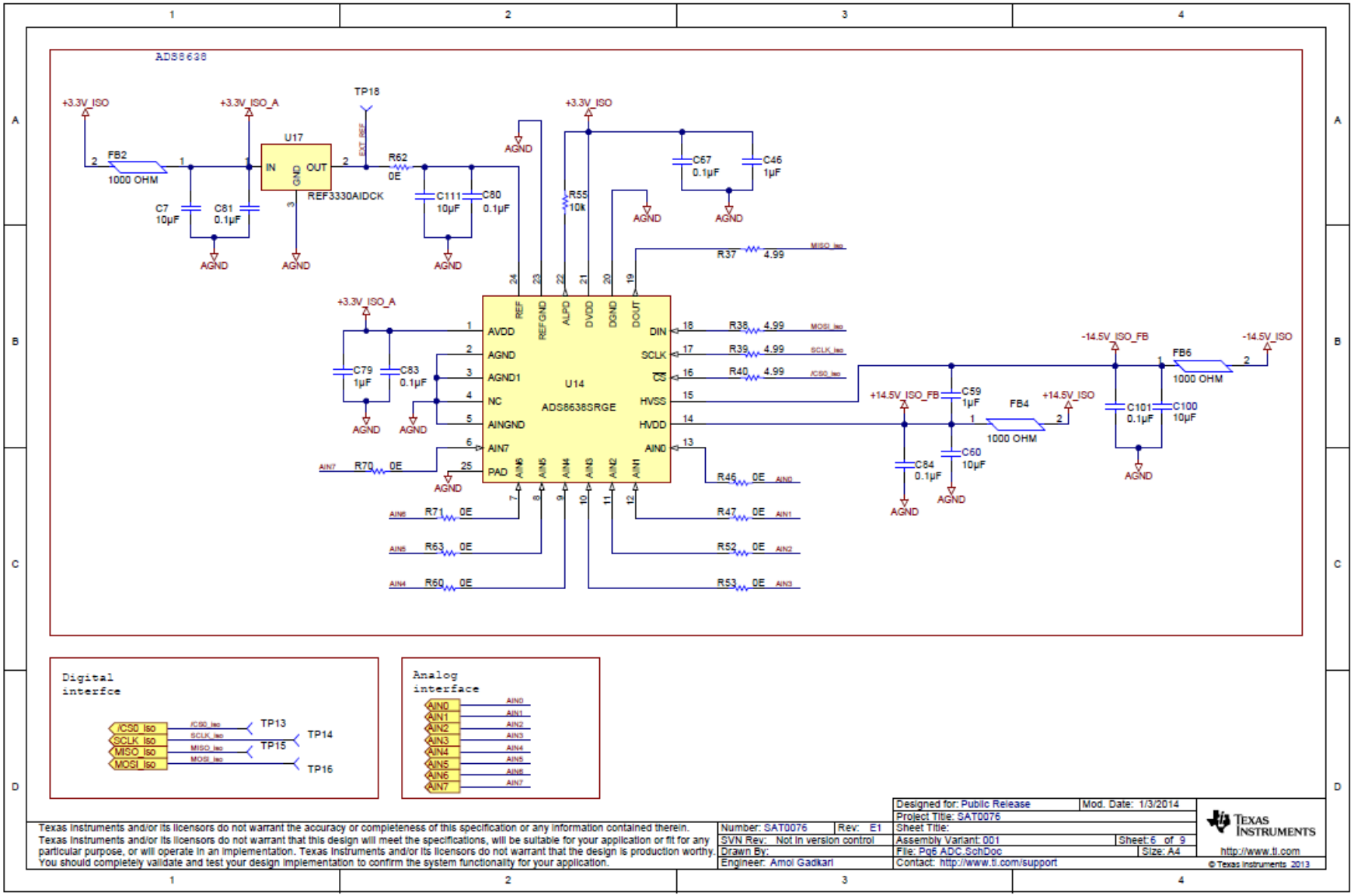


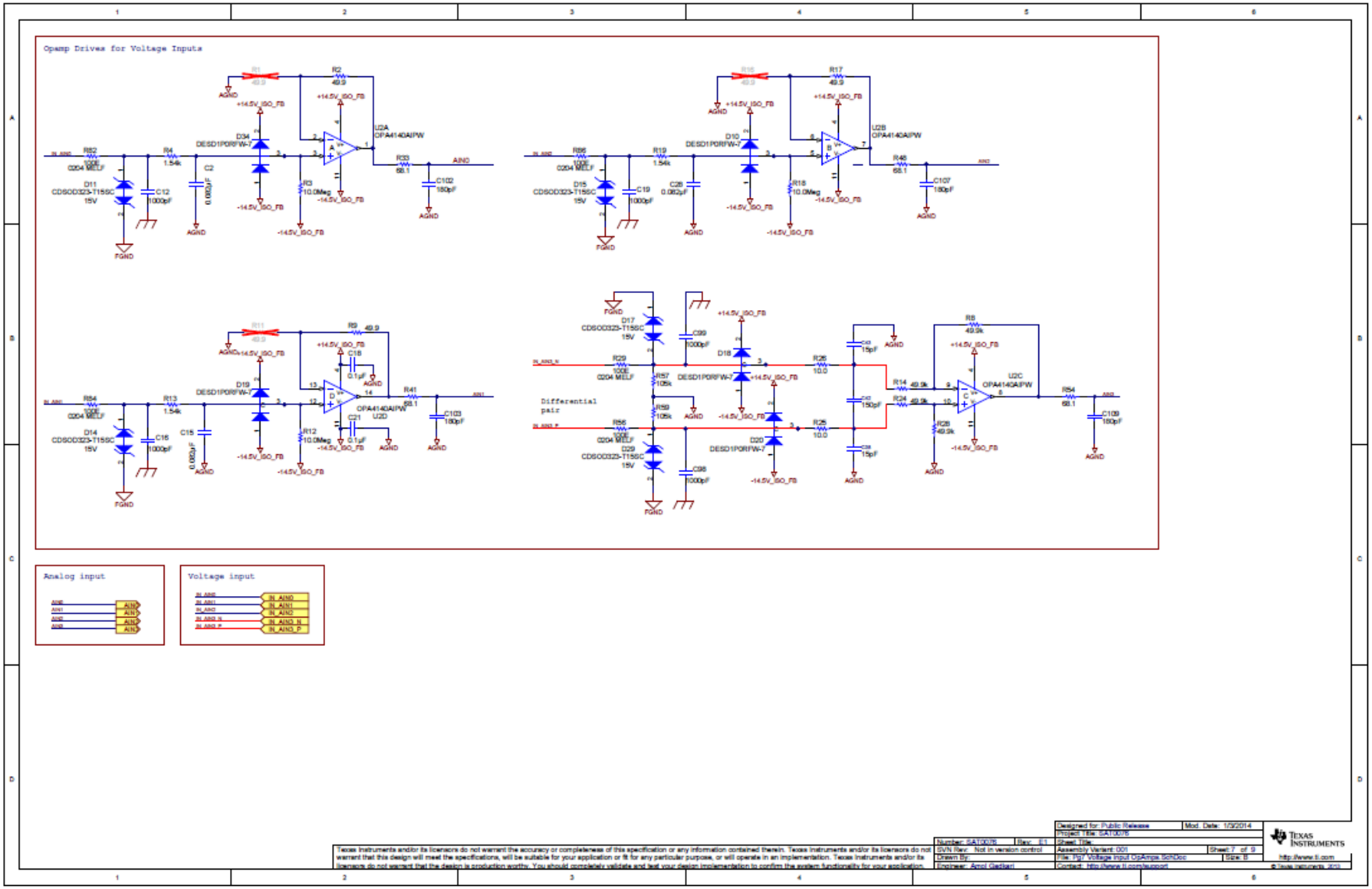


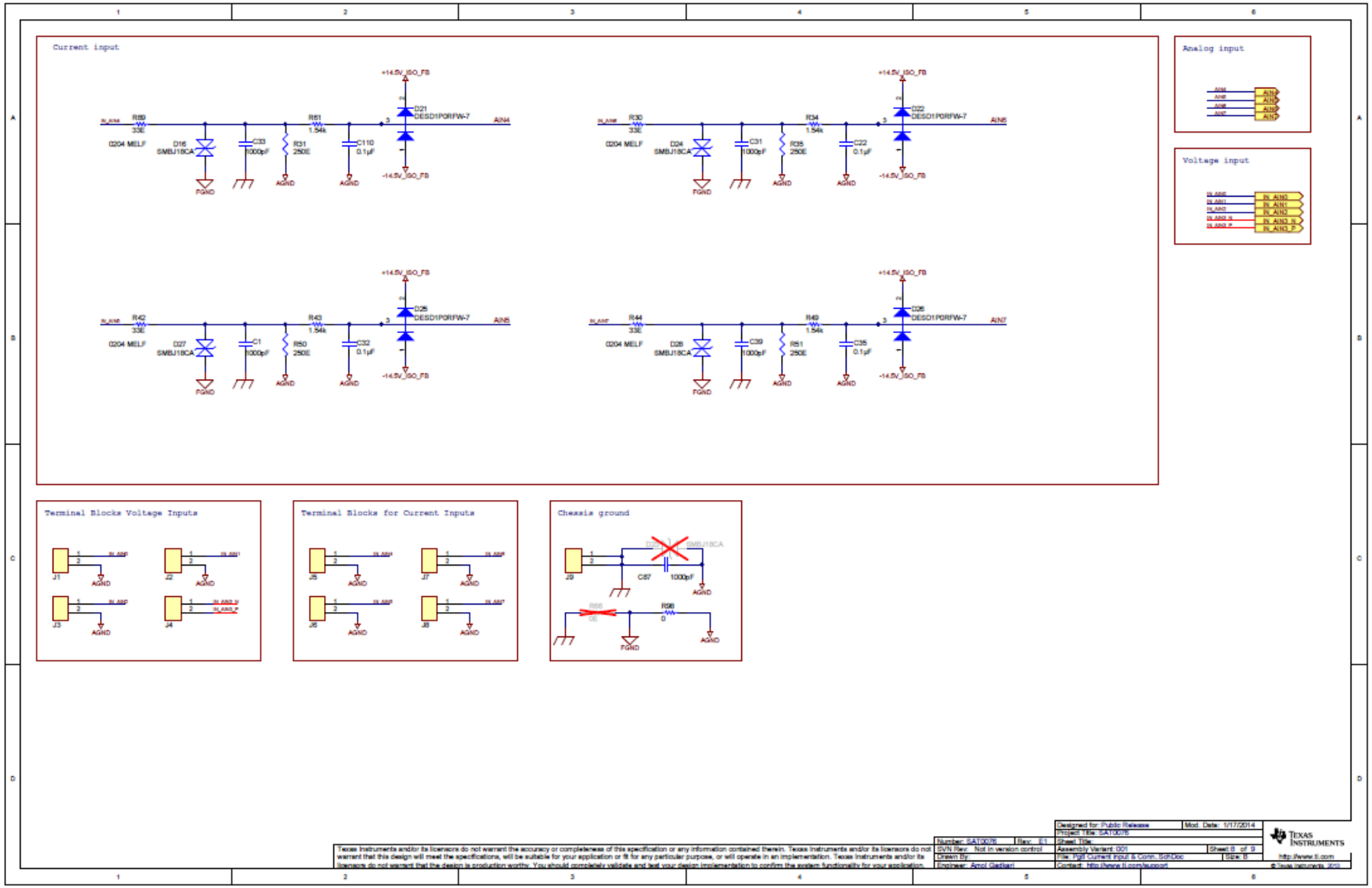


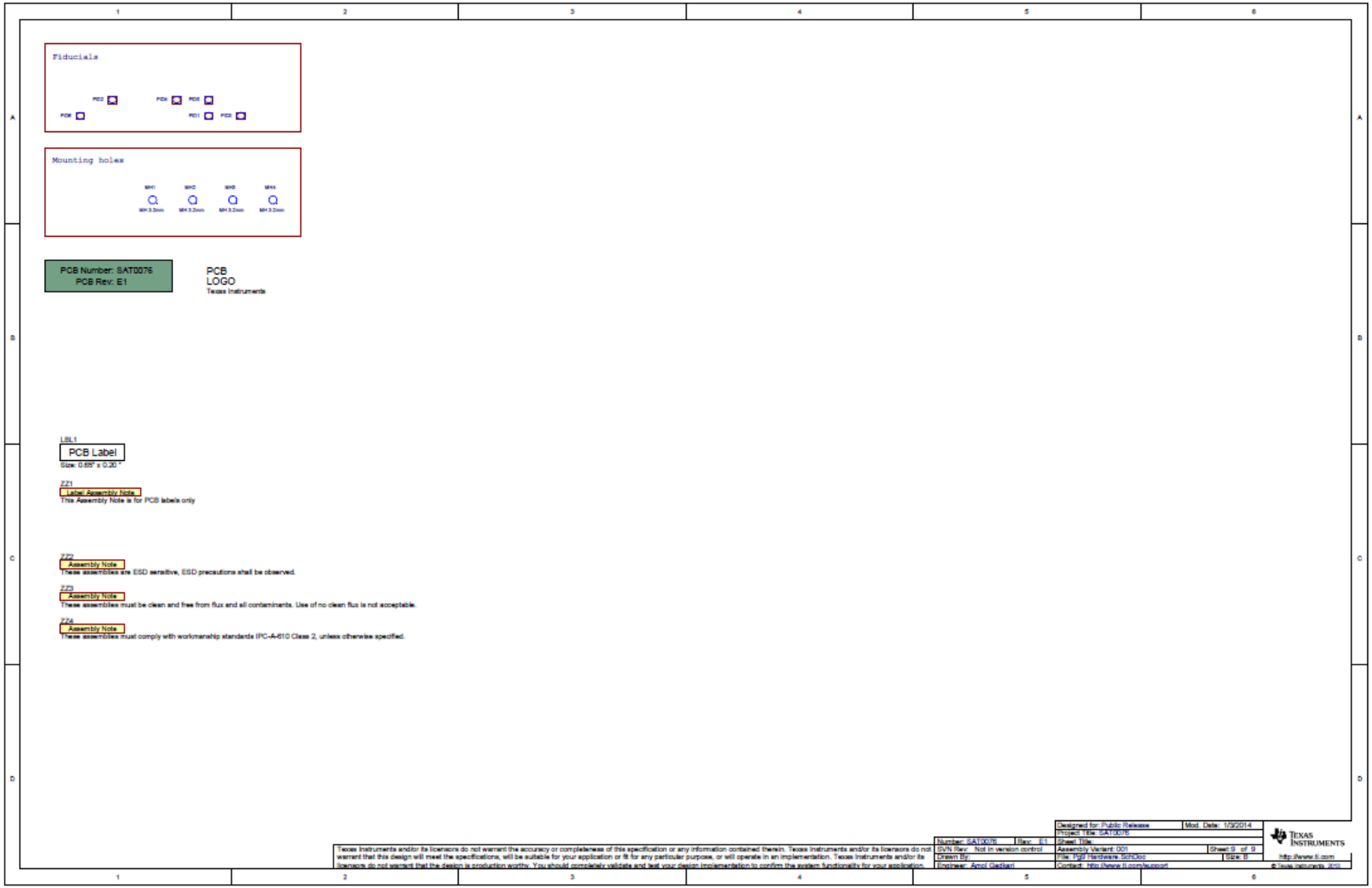












8.3 Bill of Materials

Fitted	Description	Designator	Manufacturer	PartNumber	Quantity	RoHS	PackageReference
Fitted	Printed Circuit Board	!PCB	Any	SAT0076	1	O	
Fitted	CAP, CERM, 1000pF, 2KV 10% X7R 1206	C1, C12, C16, C19, C31, C33, C36, C39, C87, C98, C99	Johanson Dielectrics Inc	202R18W102KV4E	11	Y	1206
Fitted	CAP, CERM, 0.082uF, 50V, +/-10%, X7R, 0805	C2, C15, C28	AVX	08055C823KAT2A	3	Y	0805
Fitted	CAP, CERM, 0.47uF, 100V, +/-10%, X7R, 1206	C3	MuRata	GRM31MR72A474KA35L	1	Y	1206
Fitted	CAP, CERM, 0.01uF, 100V, +/-5%, X7R, 0603	C4, C14, C26, C92	AVX	06031C103JAT2A	4	Y	0603
Fitted	CAP, CERM, 2.2uF, 25V, +/-10%, X7R, 0805	C6, C24, C90	MuRata	GRM21BR71E225KA73L	3	Y	0805
Fitted	CAP, CERM, 10uF, 35V, +/-20%, X7R, 1210	C7, C11, C13, C27, C30, C60, C96, C100, C111	Taiyo Yuden	GMK325AB7106MM-T	9	Y	1210
Fitted	CAP, CERM, 1uF, 50V, +/-10%, X5R, 0603	C8, C17, C34, C46, C48, C59, C79, C105	MuRata	GRM188R61H105KAALD	8	Y	0603
Fitted	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603	C9, C18, C20, C21, C23, C25, C29, C37, C47, C67, C68, C80, C81, C83, C84, C89, C91, C95, C101, C106	Kemet	C0603C104K5RACTU	20	Y	0603
Fitted	CAP, CERM, 0.1uF, 50V, +/-5%, X7R, 0805	C22, C32, C35, C110	AVX	08055C104JAT2A	4	Y	0805
Fitted	CAP, CERM, 15pF, 50V, +/-5%, C0G/NP0, 0402	C38, C43	MuRata	GRM1555C1H150JA01D	2	Y	0402
Fitted	CAP, CERM, 0.47uF, 50V, 10%, X5R, 0603	C40, C78	Taiyo Yuden	UMK107ABJ474KA-T	2	Y	0603
Fitted	CAP, CERM, 2.2uF, 100V, +/-10%, X7R, 1210	C41, C44, C88	MuRata	GRM32ER72A225KA35L	3	Y	1210

Fitted	CAP, CERM, 150pF, 50V, +/-5%, C0G/NP0, 0603	C42	AVX	06035A151JAT2A	1	Y	0603
Fitted	CAP, CERM, 4.7uF, 50V, +/-10%, X5R, 0805	C53, C93, C97	TDK	C2012X5R1H475K125AB	3	Y	0805
Fitted	CAP, CERM, 1000pF, 100V, +/-20%, X7R, 0603	C70, C94	AVX	06031C102MAT2A	2	Y	0603
Fitted	CAP, CERM, 180pF, 50V, +/-5%, C0G/NP0, 0603	C102, C103, C107, C109	AVX	06035A181JAT2A	4	Y	0603
Fitted	Diode, Schottky, 200V, 1A, PowerDI123	D1, D4	Diodes Inc.	DFLS1200-7	2	Y	PowerDI123
Fitted	LED SmartLED Green 570NM	D2, D5, D8	OSRAM	LG L29K-G2J1-24-Z	3		0603
Fitted	Diode, Zener, 3.6V, 500mW, SOD-123	D3	Vishay-Semiconductor	MMSZ4685-V	1	Y	SOD-123
Fitted	Diode, Zener, 15V, 1W, SOD-123	D6, D9	Panasonic	DZ2W15000L	2	Y	SOD-123
Fitted	Diode, P-N, 70V, 0.2A, SOT-323	D10, D18, D19, D20, D21, D22, D25, D26, D34	Diodes Inc	DESD1P0RFW-7	9	Y	SOT-323
Fitted	Diode, TVS, ARRAY, 15V, SOD323	D11, D14, D15, D17, D29	Bourns Inc.	CDSOD323-T15SC	5	Y	SOD-323
Fitted	Diode, Schottky, 60V, 1A, SOD-123F	D12	NXP Semiconductor	PMEG6010CEH,115	1	Y	SOD-123F
Fitted	Diode, Schottky, 45V, 0.1A, SOD-523	D13	Diodes Inc.	SDM10U45-7-F	1	Y	SOD-523
Fitted	TVS 18 VOLT 600 WATT BI-DIR SMB	D16, D24, D27, D28	Littelfuse Inc	SMBJ18CA	4		SMB
Fitted	FERRITE CHIP 1000 OHM 300MA 0603	FB1, FB2, FB3, FB4, FB5, FB6	TDK Corporation	MMZ1608B102C	6	Y	0603
Fitted	[NoValue], [NoValue], [NoValue], [NoValue], [NoValue], [NoValue], Mountin hole, NPTH Drill 3.2mm, Mountin hole, NPTH Drill 3.2mm, Mountin hole, NPTH Drill 3.2mm, Mountin hole, NPTH Drill 3.2mm	FID1, FID2, FID3, FID4, FID5, FID6, MH1, MH2, MH3, MH4			10		
Fitted	Terminal Block, 4x1, 2.54mm, TH	J1, J2, J3, J4, J5, J6, J7, J8, J9	On Shore Technology Inc	OSTVN02A150	9	Y	TERM_BLK, 2pos, 2.54mm
Fitted	Receptacle, 0.8mm, 25x2, SMT	J10	Samtec	ERF8-025-05.0-L-DV-K-TR	1	Y	25x2 Socket Strip
Fitted	Inductor, Chip, ±10%	L1	Panasonic	ELJ-EA3R3MF	1		1210
Fitted	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	LBL1	Brady	THT-14-423-10	1	Y	PCB Label 0.650"H x 0.200"W

Fitted	MOSFET, N-CH, 60V, 50A, SON 5x6mm	Q1	Texas Instruments	CSD18537NQ5A	1	Y	SON 5x6mm
Fitted	RES, 49.9 ohm, 1%, 0.063W, 0402	R2, R9, R17	Vishay-Dale	CRCW040249R9FKED	3	Y	0402
Fitted	RES, 10.0Meg ohm, 1%, 0.063W, 0402	R3, R12, R18	Vishay-Dale	CRCW040210M0FKED	3	Y	0402
Fitted	RES, 1.54k ohm, 1%, 0.125W, 0805	R4, R13, R19, R34, R43, R49, R61	Vishay-Dale	CRCW08051K54FKEA	7	Y	0805
Fitted	RES, 1.30Meg ohm, 1%, 0.125W, 0805	R5, R15	Vishay-Dale	CRCW08051M30FKEA	2	Y	0805
Fitted	RES, 340k ohm, 1%, 0.1W, 0603	R6	Vishay-Dale	CRCW0603340KFKEA	1	Y	0603
Fitted	RES, 20.0k ohm, 1%, 0.1W, 0603	R7, R77	Yageo America	RC0603FR-0720KL	2	Y	0603
Fitted	RES, 49.9k ohm, 0.1%, 0.1W, 0603	R8, R14, R24, R28	Yageo America	RT0603BRD0749K9L	4	Y	0603
Fitted	RES, 118k ohm, 0.1%, 0.1W, 0603	R10	Yageo America	RT0603BRD07118KL	1	Y	0603
Fitted	RES, 115k ohm, 0.1%, 0.1W, 0603	R21	Yageo America	RT0603BRD07115KL	1	Y	0603
Fitted	RES, 10.0 ohm, 1%, 0.1W, 0603	R25, R26	Vishay-Dale	CRCW060310R0FKEA	2	Y	0603
Fitted	RES, 300 ohm, 5%, 0.1W, 0603	R27	Vishay-Dale	CRCW0603300RJNEA	1	Y	0603
Fitted	RES, 100 ohm,1/4W, 1%, 0204 MELF	R29, R56, R82, R84, R86	TT Electronics/Welwyn	WRM0204C-100RFI	5	Y	0204 MELF
Fitted	RES, 33 ohm, 0.4W, 1%, 0204 MELF	R30, R42, R44, R89	Vishay Beyschlag	MMA02040C3309FB300	4	Y	0204 MELF
Fitted	250 OHM 5PPM .02% 0805	R31, R35, R50, R51	Vishay Thin Film	PLTT0805Z2500QGT5	4	Y	0805
Fitted	RES, 10k ohm, 5%, 0.063W, 0402	R32, R36, R55	Vishay-Dale	CRCW040210K0JNED	3	Y	0402
Fitted	RES, 68.1 ohm, 0.1%, 0.1W, 0603	R33, R41, R48, R54	Yageo America	RT0603BRD0768R1L	4	Y	0603
Fitted	RES, 4.99 ohm, 1%, 0.063W, 0402	R37, R38, R39, R40	Vishay-Dale	CRCW04024R99FKED	4	Y	0402
Fitted	RES, 0.02 ohm, 1%, 1W, 1206	R45	Susumu Co Ltd	PRL1632-R020-F-T1	1	Y	1206
Fitted	RES, 0 ohm, 5%, 0.063W, 0402	R46, R47, R52, R53, R60, R63, R70, R71	Vishay-Dale	CRCW04020000Z0ED	8	Y	0402
Fitted	RES, 105k ohm, 0.1%, 0.1W, 0603	R57, R59	Susumu Co Ltd	RG1608P-1053-B-T5	2	Y	0603
Fitted	RES, 10k ohm, 5%, 0.1W, 0603	R58	Vishay-Dale	CRCW060310K0JNEA	1	Y	0603
Fitted	RES, 0 ohm, 5%, 0.1W, 0603	R62	Panasonic	ERJ-3GEY0R00V	1	Y	0603
Fitted	RES, 7.50k ohm, 1%, 0.1W, 0603	R67	Vishay-Dale	CRCW06037K50FKEA	1	Y	0603

Fitted	RES, 15.8k ohm, 1%, 0.1W, 0603	R68	Vishay-Dale	CRCW060315K8FKEA	1	Y	0603
Fitted	RES, 6.49k ohm, 1%, 0.1W, 0603	R69	Vishay-Dale	CRCW06036K49FKEA	1	Y	0603
Fitted	RES, 3.9k ohm, 5%, 0.1W, 0603	R79, R87	Vishay-Dale	CRCW06033K90JNEA	2	Y	0603
Fitted	RES, 127k ohm, 1%, 0.1W, 0603	R80	Vishay-Dale	CRCW0603127KFKEA	1	Y	0603
Fitted	RES, 105k ohm, 1%, 0.1W, 0603	R83	Vishay-Dale	CRCW0603105KFKEA	1	Y	0603
Fitted	RES, 0 ohm, 5%, 0.25W, 1210	R85	Rohm	MCR25JZHJ000	1	Y	1210
Fitted	RES, 95.3k ohm, 1%, 0.1W, 0603	R93	Vishay-Dale	CRCW060395K3FKEA	1	Y	0603
Fitted	RES, 47.5k ohm, 1%, 0.1W, 0603	R94	Vishay-Dale	CRCW060347K5FKEA	1	Y	0603
Fitted	RES, 1.5k ohm, 5%, 0.063W, 0402	R97, R99	Vishay-Dale	CRCW04021K50JNED	2	Y	0402
Fitted	RES, 0 ohm, 5%, 0.25W, 1206	R98	Vishay-Dale	CRCW12060000Z0EA	1	Y	1206
Fitted	Transformer, 50uH, SMT	T1	Wurth Elektronik eiSos	750342178	1	Y	17.75x12.7x13.46mm
Fitted	Test Point 40mil pad 20mil drill	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP18, TP19, TP20	STD	STD	19		
Fitted	IC, Regulator, LDO, Micropower, 3.2µA @ 50mA. Vin 2.5, 3.3V and Adjustable. 24 Max. Vin	U1	TI	TPS71501DCKR	1		SOP-5 (DCK)
Fitted	,High-Precision, Low-Noise, Rail-to-Rail Output,11MHz JFET Op Amp PW0014A	U2	Texas Instruments	OPA4140AIPW	1	Y	TSSOP (PW) 14
Fitted	100V, 600mA Constant On-Time Synchronous Buck Regulator, DDA0008B	U3	Texas Instruments	LM5017MRE/NOPB	1	Y	DDA0008B
Fitted	-36V, -200mA, Ultralow-Noise, Negative Linear Regulator	U5	Texas Instruments	TPS7A3001DGNR	1	Y	MSOP-PowerPAD (DGN) | 8
Fitted	50 mA, 24 V, 3.2-mA Supply Current Low-Dropout Linear Regulator, DCK0005A	U6, U8	Texas Instruments	TPS71533DCK	2	Y	DCK0005A
Fitted	4242-VPK Small-Footprint and Low-Power Quad Channels Digital Isolators, DBQ0016A	U11	Texas Instruments	ISO7141CCDBQ	1	Y	DBQ0016A

Fitted	12-bit, 8-Channel, Bipolar SAR with software selectable input ranges	U14	TI	ADS8638SRGE	1		RGE24P
Fitted	Positive High Voltage Hot Swap / Inrush Current Controller with Power Limiting, 10-pin MSOP, Pb-Free	U16	National Semiconductor	LM5069MM-2/NOPB	1	Y	MUB10A
Fitted	30ppm/C Drift, 3.9uA, Voltage Reference	U17	TI	REF3330AIDCK	1		SC70-3
Fitted	IC, EEPROM, 2KBIT, 1MHZ, SOIC-8	U19	Atmel	AT24C02C-SSHM-B	1	Y	SOIC-8
Not Fitted	CAP, CERM, 0.01uF, 100V, +/-5%, X7R, 0603	C10	AVX	06031C103JAT2A	0	Y	0603
Not Fitted	TVS 18 VOLT 600 WATT BI-DIR SMB	D23	Littelfuse Inc	SMBJ18CA	0		SMB
Not Fitted	RES, 49.9 ohm, 1%, 0.063W, 0402	R1, R11, R16	Vishay-Dale	CRCW040249R9FKED	0	Y	0402
Not Fitted	RES, 1.07Meg ohm, 0.1%, 0.125W, 0805	R20	Yageo America	RT0805BRD071M07L	0	Y	0805
Not Fitted	RES, 100k ohm, 0.1%, 0.1W, 0603	R22	Yageo America	RT0603BRD07100KL	0	Y	0603
Not Fitted	RES, 0 ohm, 5%, 0.25W, 1206	R66	Panasonic	ERJ-8GEY0R00V	0	Y	1206
Not Fitted	RES, 10k ohm, 5%, 0.1W, 0603	R81	Vishay-Dale	CRCW060310K0JNEA	0	Y	0603

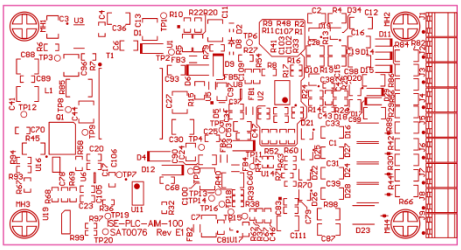
8.4 PCB Layout

The Analog Input Module is implemented in 4 layers PCB. For optimal performance of this design follow standard PCB layout guidelines, including proper decoupling close to all integrated circuits and adequate power and ground connections with large copper pours. Additional considerations must be made for providing robust EMC/EMI immunity. All protection elements should be placed as close to the output connectors as possible to provide a controlled return path for transient currents that does not cross sensitive components. To allow optimum current flow wide, low impedance, low-inductance traces should be used along the output signal path and protection elements. When possible copper pours are used in place of traces. Stitching the pours provides an effective return path around the PCB and helps reduce the impact of radiated emissions Layout Recommendations
In order to achieve a high performance, the below Layout Guidelines are recommended

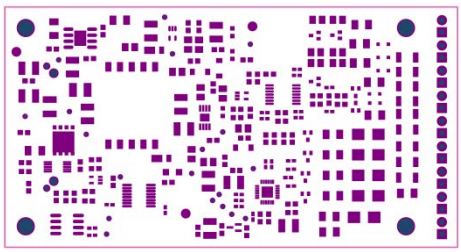
1. A common ground plane for both analog and digital is recommended
2. All signals must be routed, assuming there is a split ground plane for analog and digital. Furthermore, it is better to split the ground initially during layout. Route all analog and digital traces so that the traces see the respective ground all along the second layer. Then, short both grounds to form a common ground plane.
3. The ADC ground pins are returned to the ground plane through multiple vias (PTH)
4. Ensure that protection elements such as TVS diodes, capacitors are placed as close to connectors as possible to ensure that return current from high-energy transients does not cause damage to sensitive devices. Further use large and wide traces to ensure a low-impedance path for high-energy transients.
5. Place the decoupling capacitors close to supply pin of IC.
6. It is recommended to use multiple vias for power and ground for decoupling caps.
7. Current sense resistor must be routed as Kelvin Sense connection.
8. SPI lines: For signal integrity the termination resistances should be placed near to the source.
9. Each AVDD/AVSS should have decoupling capacitors placed close to the respective pins.
10. The reference capacitor should be placed close to the voltage reference input pin.

8.4.1 Layout Prints

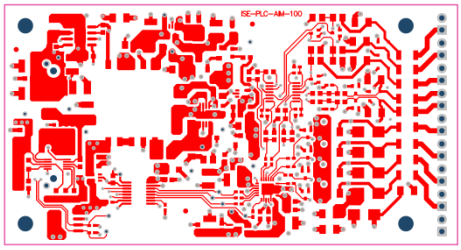
TOP SILKSCREEN



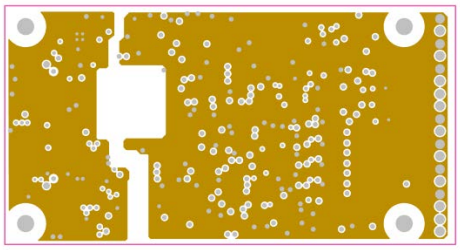
TOP SOLDER MASK



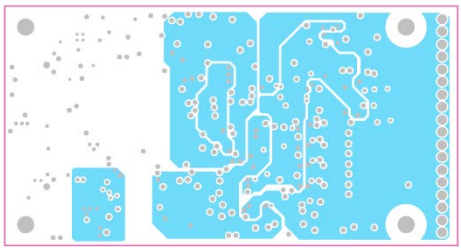
TOP LAYER



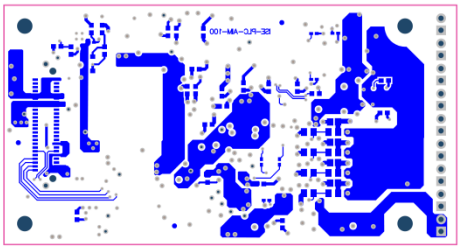
GROUND PLANE LAYER 2



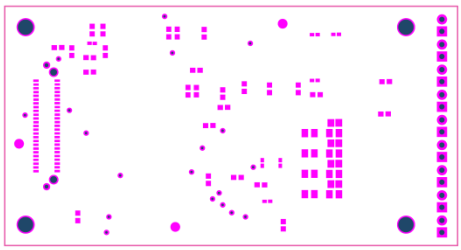
PWR PLANE LAYER3



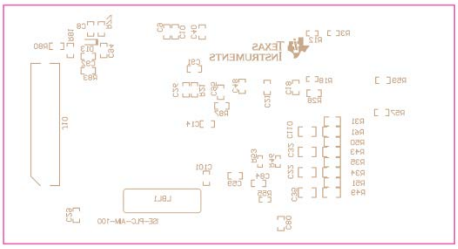
BOTTOM LAYER



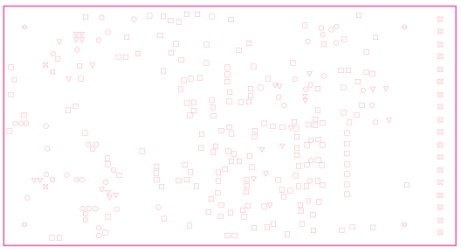
BOTTOM SOLDER MASK



BOTTOM SILKSCREEN



DRILL DRAWING



Symbol	Hit Count	Tool Size	Plated	Hole Type
○	27	12mil (0.305mm)	PTH	Round
○	49	16mil (0.406mm)	PTH	Round
□	176	20mil (0.508mm)	PTH	Round
⌗	2	33mil (0.838mm)	PTH	Round
⌗	18	44mil (1.118mm)	PTH	Round
○	2	57.087mil (1.45mm)	NPTH	Round
○	1	128mil (3.251mm)	NPTH	Round
	278 Total			

Drill Table

MECHANICAL DIMENSIONS

8.5 Altium Project

To download the Altium project files for each board, see the design files at www.ti.com/tool/TIDA-00119

8.6 Gerber files

To download the Gerber files for each board, see the design files at www.ti.com/tool/TIDA-00119

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