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Isolated, Ultra-Low Power Design for 4- to 20-mA Loop-Powered Transmitters

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TI Designs provide the foundation that you need including methodology, testing and design files to quickly evaluate and customize the system. TI Designs help *you* accelerate your time to market.

Design Resources

TIDA-00167	Tool Folder Containing Design Files
TPS7A1601	Product Folder
TPS27082L	Product Folder
TPS60402	Product Folder
TPS71733	Product Folder
TPS71533	Product Folder

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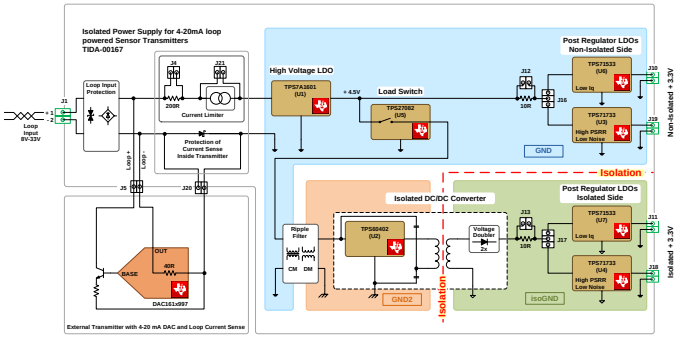
Design Features

- Isolated Design for Ultra-Low Power Applications
- Highly Efficient Isolated DC/DC Converter, ≥70% at 5-mW to 8-mW Output Power
- 8-V to 33-V Input
- Pre- and Post-Regulator LDOs for Low Noise
- Reverse Input and Overvoltage Protection
- Designed to meet EN 61000-4-5: ±1 kV
- Ripple Filter to Address Conducted EMI (EN 55011) and Decoupling from Loop Current
- Flexible Configurable Board Enables Easy Evaluation and Modification

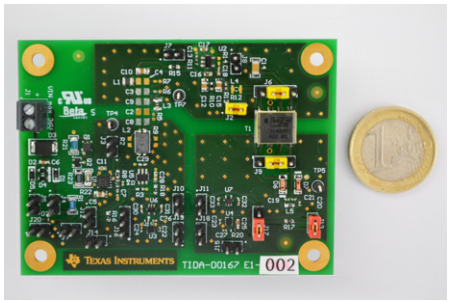
Featured Applications

- Loop Powered 4- to 20-mA Transmitters
- Factory Automation and Process Control
- Sensors and Field Transmitters
- Building Automation
- Portable Instrumentation

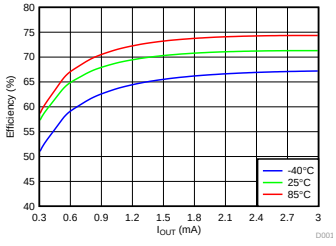
Block Diagram



Board Picture



Isolated DC/DC Converter Performance Graph



1 Introduction

The objective of this design is to provide a turn-key solution able to power the electronics of isolated loop powered 4- to 20-mA transmitters or other low-power applications with a limited input-current budget. The board offers multiple configuration options, enabling designers to use it as a starting point for their own designs and for further design modifications and optimizations.

Special care has been taken to address the need to achieve a high efficiency for the ultra-low power isolated DC/DC converter part and for offering different protection features, which can be used in a flexible way.

This design philosophy is supported by multiple headers and jumpers on the board, enabling the flexible activation or de-activation of dedicated circuit parts, according to specific application needs. For the same reason of enabling the designer to make his own modifications, the design uses a single-side populated, dual-layer board and avoids the use of ultra-small components.

Therefore, this design is not optimized for board size. TIDA-00189 is an example containing almost the complete TIDA-00167 design plus an analog front end (AFE), microcontroller (MCU), buffer, data transformer, and a DAC to control the 4- to 20-mA loop current on a board with a much smaller size, as shown in Figure 1.

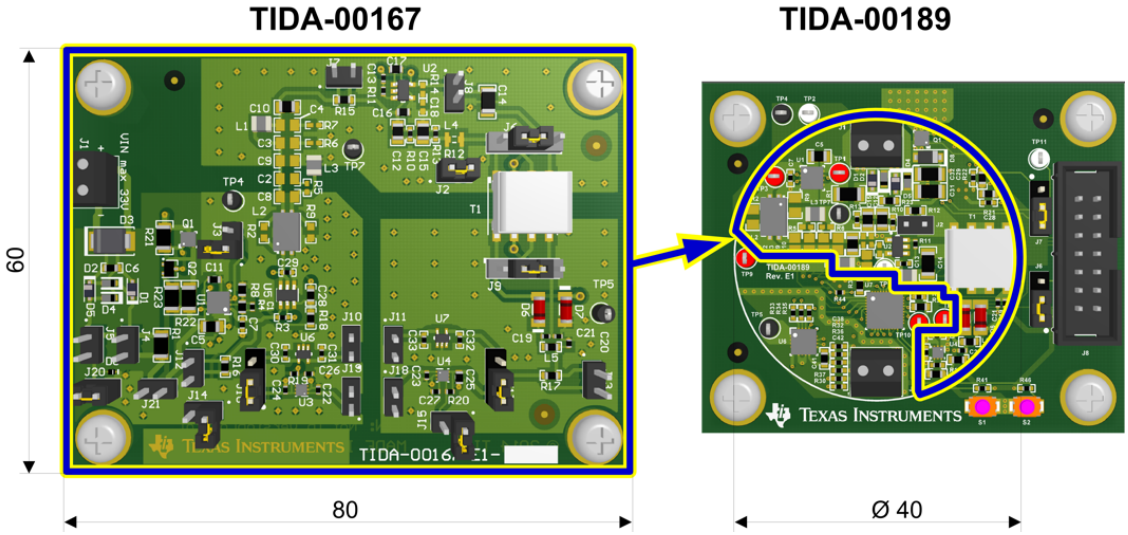


Figure 1. TIDA-00189 Showcases a High-Density Version of TIDA-00167

2 Key System Specifications

The circuitry was designed with the specifications and features listed in Table 1.

Table 1. Key System Specifications

PARAMETERS	SPECIFICATIONS AND FEATURES
LOOP INPUT	
Nominal input-voltage range	8-V to 33-V DC (1)
Continuous reverse input voltage	Up to –33-V DC
Compliance voltage	8 V
Surge-voltage capability (EN 61000-4-5)	±1 kV, differential mode
Input-leakage current (adds an error to the loop current (2))	<3.3 µA
Input current (provided all IOUTs are within their limits)	<3.3 mA (3)
NONISOLATED LDO OUTPUT	
Output voltage	3.3 V
Output current (all LDOs TPS71533, isolated IOUT = 1.88 mA)	0.39 mA (4)
Output current (all LDOs TPS71733, isolated IOUT = 1.69 mA)	0.39 mA (4)
ISOLATED DC/DC CONVERTER	
Type of converter	Optocoupler-less Half bridge on primary Voltage doubler on secondary
Input voltage of DC/DC	4.5 V
Output voltage of DC/DC	4.2 V
Efficiency ($VIN_{DC/DC}$ = 4.5 V; T = 25°C; $IOUT_{DC/DC}$ = 1.9 mA)	70.50%
Transformer insulation Dielectric	Functional 1500-V AC 1 min 1875-V AC 1 sec
ISOLATED LDO OUTPUT	
Output voltage	3.3 V
Output current (all LDOs TPS71733, nonisolated IOUT = 390 µA)	1.69 mA (4)
Output current (all LDOs, TPS71533, nonisolated IOUT = 390 µA)	1.88 mA (4)
PROTECTION	
Reverse input voltage	Continuous
Surge protection	EN 61000-4-5
Internal input-clamp voltage (DM ±1 kV, 42 Ω; EN 61000-4-5)	<60 V
Input-current limit	<50 mA; optional
Protection of current sense inside 4- to 20-mA transmitters	Optional
ENVIRONMENT	
Temperature range	–40°C to 85°C
PCB	
Form factor (L × W)	80 × 60 mm
Number of layers	Two layers, single side populated

(1) Can be extended to lower and higher values.

(2) In a 4- to 20- mA application, the leakage current is not seen by the DAC controlling the loop current. Instead, the leakage current adds to the current seen by the loop receiver and causes an error.

(3) Provided all IOUTs are within their limits.

(4) The output current given is based on a 3.3-mA maximum input-current budget of complete circuitry and on a given output current of the other 3.3-V rail. The current needs to be adopted and re-balanced in case of another current budget or different loading of the other 3.3-V rail.

3 System Description

The power management of transmitters is often a central part of the complete design and also one of the major design challenges. An overview, showing how this design, TIDA-00167, fits into a complete 2-wire, loop-powered 4- to 20-mA sensor transmitter is shown in the simplified system block diagram, Figure 2. The understanding of the total system is very helpful for a better understanding of the specific power design requirements and challenges.

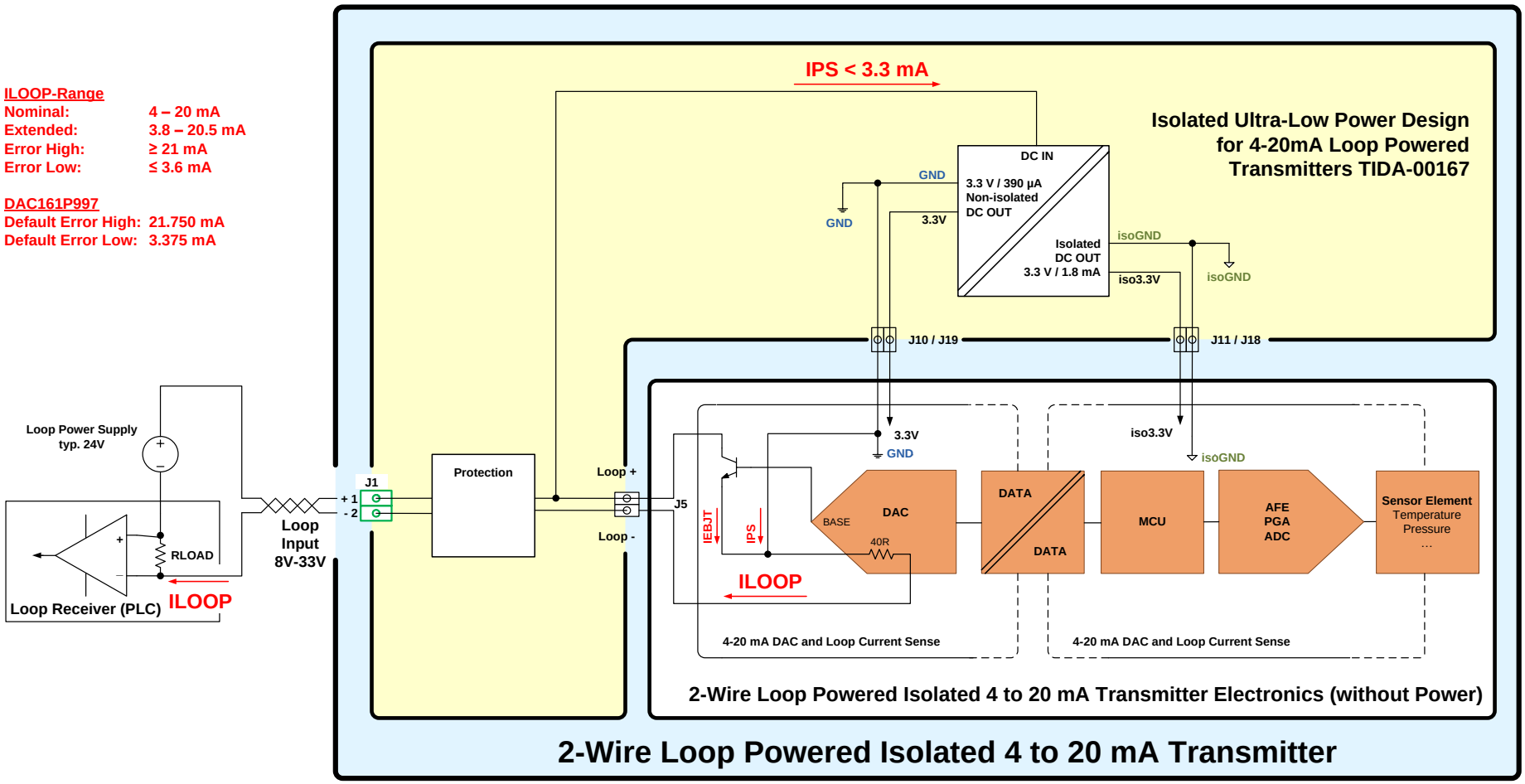


Figure 2. TIDA-00167 — Simplified System Block Diagram

The complete system is powered by the loop power supply, typically at a 24-V level. This power source forms together with the loop receiver (often a programmable logic controller [PLC]) and with the 2-wire loop powered transmitter, the so-called loop. A 2-wire cable is sufficient for the electrical connection. Those two wires are used for powering the transmitter as well as for transmitting the signal by controlling the loop current ILOOP, which equals the total current consumption of the transmitter.

On the loop receiver side of the system, the loop current causes a voltage drop across the load resistance RLOAD inside the receiver. This voltage drop is usually amplified and then converted into a digital signal for further processing inside the receiver. Typical receivers are, for example, PLCs.

Typical load resistance levels range from some tens of Ω to some hundreds of Ω. At an exemplarily assumed RLOAD of 500 Ω, the voltage drop across this resistor will change from 2 V to 10 V for loop currents of 4 to 20 mA.

NOTE: This voltage drop reduces the voltage at the loop-input terminals J1. The higher the loop current, the less voltage is available to power the transmitter.

The minimum voltage level needed at the loop-input terminals J1 to ensure operation of the transmitter within its performance specification is the so-called *compliance voltage*.

On the transmitter side of the system, the physical quantities are detected by the transmitter's sensor element. The output signal of the sensor element is typically conditioned by an AFE, amplified by a programmable gain amplifier (PGA), and converted into a digital value by an analog-to-digital converter (ADC). This digital value is then processed by a MCU and the resulting digital output data generated by the MCU is converted by a digital-to-analog converter (DAC) into the accurately controlled loop current ILOOP. The normal range of the loop current is a span of 4 to 20 mA, where 4 mA usually represents the lowest (often zero), or the most negative, value of the sensed physical quantities, and 20 mA stands for the most positive value (100% full scale value).

Additional values or value ranges for ILOOP are, for example, specified in the NAMUR recommendation Namur 43 [1], extending the working range from 3.8 mA to 20.5 mA to support activities like adjustment, calibration, and the detection of range overflow. Furthermore, loop currents below 3.6 mA or above 21 mA are recommended to be used for failure detection. More details can be found in TIDA-00165 and TIDA-00189.

For example, TI's DAC161P997 device uses 3.375 mA as a default *low- error* current level and 21.75 mA as default *high-error* current. The maximum value for the controllable loop current for this device is 24 mA.

The principle of controlling the loop current is based on the fact that the DAC is sensing the ILOOP by the internal 40-Ω sense resistor of the DAC. The DAC then controls the bias current into an external bipolar junction transistor (BJT) to obtain the exact loop current desired. By this process, the DAC can control the base current and the emitter current of the BJT (IEBJT). However, according to Equation 1, a second component influences the ILOOP, which cannot be controlled by the DAC. The second component is the total current of the power supply IPS, which is determined by the total power consumption of the electronics of the transmitter, which cannot be influenced by the BJT or the DAC.

$$ILOOP = IEBJT + IPS \quad (1)$$

where

- ILOOP is the loop current.
- IEBJT is the emitter current of the BJT.
- IPS is the total current of the power supply powering the complete electronics of the transmitter.

The isolated ultra-low power design is usually an internal block inside a transmitter. However, the isolated ultra-low power design is provided for the purpose of this TIDA-00167 design as a separate board. The board provides main protection features and a nonisolated, as well as isolated, 3.3-V output. The isolated power output is required for powering the isolated side inside the transmitter. Isolation inside transmitter is a measure to avoid ground loops between the transmitter and the receiver.

3.1 Design Challenges

If a DAC161P997 device is used in a transmitter design, and if the DAC161P997 device is utilizing its 3.375 mA *low- error* level, then the IPS must be less than 3.375 mA. Therefore, the input current for this power design was targeted to be less than 3.3 mA in order to have some additional margin. With this small input current budget, the power design must be able to provide a nonisolated 3.3-V rail with an output current of at least 390 µA, as well as an isolated 3.3-V rail with at least 1.69 mA. A complete list of all challenges applicable to the design is given in the following list.

- Be able to provide the desired outputs (nonisolated 3.3 V and 390 µA plus isolated 3.3 V and 1.69 mA), with an input-current budget of 3.3 mA.
- Optimizing the efficiency of the isolated DC/DC conversion, since the current needed on the isolated side is approximately four times larger than the current on the nonisolated side.
- Operating the isolated DC/DC converter with a fixed switching frequency to minimize noise.
- Protecting the loop input against differential surge pulses and against continuous reverse voltage.
- Limiting the inrush current during hot-plug events and during the application of differential surge pulses on the input.
- Avoid protection circuitry from negatively impacting total system performance.
- Additional application specific requirements which can only be addressed by the user, but require a power design with maximum flexibility to verify, reconfigure, and optimize the circuit.

3.2 Converting the Design Challenges to Dedicated Circuit Blocks

Taking into account all the challenges listed in Section 3.1, a board represented by the block diagram in Figure 3 consists of the following components and features.

3.2.1 Loop-Input Protection

Protects the design against differential input surge pulses (according to EN 61000-4-5, up to ±1 kV, 42 Ω), as well as against reverse input voltage (reverse connection of the nominal input voltage by miswiring). Surge pulses are clamped by an onboard transient-voltage suppressor (TVS) diode to a safe voltage level below 60 V. Reverse input voltage can be applied continuously. The complete circuitry works even under
reverse input voltage condition, but the accuracy and other performance parameters will be degraded.

3.2.2 Current Limiter and Circuitry to Protect the Current Sense Circuitry Inside a Loop-Powered Transmitter

Each sudden increase of the loop-input voltage will cause a sudden pulse current through the input capacitor of the complete power circuitry. Sudden increases of the input voltage at the loop-input terminals happen, for example, during initial power-up or during positive differential-mode surge pulses. Because the loop current is sensed and controlled by the respective 4- to 20-mA DAC in a connected transmitter circuit, this pulse current will flow through the sensitive current shunt inside this DAC.

There is a maximum current rating for the current through this current shunt. The maximum rating requires limiting the current below 50 mA when using a DAC161x997. The design offers two different methods for this purpose: a simple 200-Ω resistor and a dedicated active current source.

Each method can separately be enabled or disabled (in case the function will not be needed in specific applications). Additionally, another clamping diode can be activated in parallel to the integrated current shunt of the DAC, which offers an additional level of protection against overvoltage across the shunt.

3.2.3 High Input Voltage LDO to Provide a Nonisolated Intermediate Voltage (4.5 V)

The output voltage of the protection circuits powers the first LDO, which can withstand input voltages up to 60 V. The first LDO provides an intermediate voltage rail of 4.5 V, which powers the nonisolated post-regulator LDOs, as well as to power the isolated DC/DC converter (through a load switch and ripple filter).

The LDO offers a power-good (PG) pin, as well as a pin targeted to set the power-good delay. This additional feature can serve as a control signal for the power sequencing inside a system. The PG signal can directly control the high PSRR LDO on the nonisolated side, the load switch, and therefore, can also control the isolated DC/DC converter.

3.2.4 Load Switch

A dedicated load switch is used to switch the isolated DC/DC converter ON and OFF. In contrast to the use of a standard field effect transistor (FET), the load switch can be directly controlled by the PG signal of the high voltage LDO. Therefore, no additional level shifter or inverting stage will be needed. A capacitor and a resistor provide a straightforward method of programming the rise time of the output voltage of the load switch.

3.2.5 Isolated DC/DC Converter

The optocoupler-less converter transfers its regulated 4.5-V input voltage into a secondary voltage, which is mainly determined by the transformer's turns ratio and forward voltage of the secondary diodes. In addition, the secondary voltage is determined by the load-current-dependent voltage losses across the DC resistance of the transformer windings and the switches inside the integrated DC/DC converter. The selection of the best fitting DC/DC converter and isolated converter topology ensures an optimized efficiency for this type of ultra-low power application. The output voltage of the converter is at 25ºC and an output current of 1.5 to 2.0 mA in the range of 4.10 to 4.25 V.

3.2.6 Ripple Filter

Although the isolated DC/DC converter operates with low-input ripple currents due to the selected half bridge topology, an additional ripple filter has been placed on the board, which allows a fourth-order, differential-mode (DM) filter, plus a common-mode (CM) filter. In the current design version, a second-order DM filter plus the single-stage CM filter was sufficient to meet the conducted noise requirements of the EN 55011 specification.

3.2.7 Post Regulation to Provide Stable and Noise-Free, Nonisolated 3.3 V

One out of two different LDOs can be selected to provide the required 3.3-V output. The LDOs differ significantly in their parameters such as PSRR and quiescent current (Iq). The placement of those two LDOs enable the user to find the optimized solution fitting his specific needs by selecting the respective LDO. High PSRR ensures lowest noise on the 3.3-V rails. Therefore, best system accuracy is obtained, while the use of the low Iq LDO increases the output current of the rails at the same given total 3.3-mA input current budget.

3.2.8 Post Regulation to Provide Stable and Noise-Free, Isolated 3.3 V

As on the nonisolated side, there are also two LDOs provided on the isolated side. One of these LDOs can be selected. Although designed with the requirements of a 4- to 20-mA loop-powered transmitter in mind, the complete power-supply design or its circuit blocks are equally usable in other projects with similar needs and requirements.

4 Block Diagram

The circuit blocks described in Section 3.2 can be found in Figure 3.

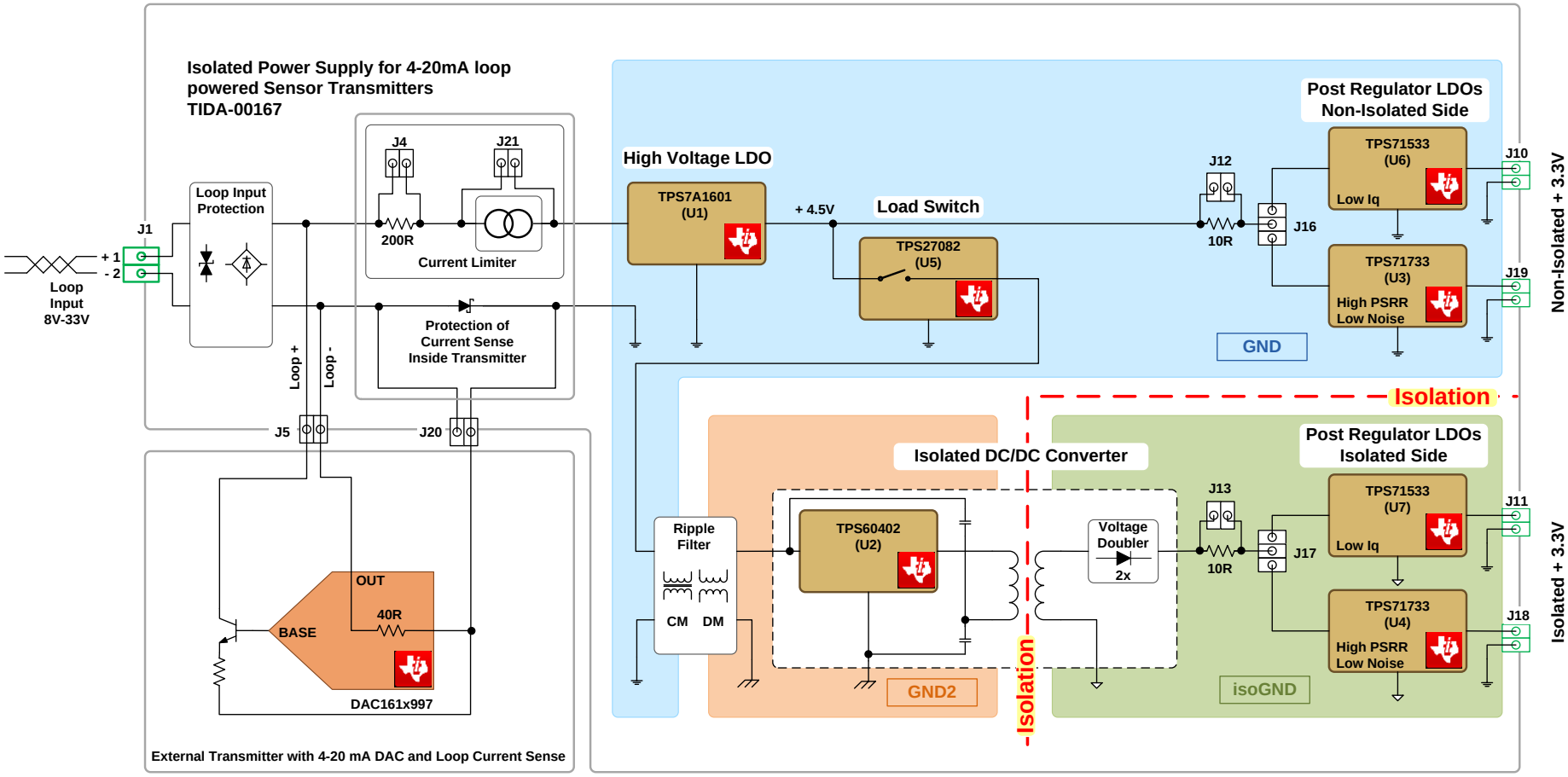


Figure 3. TIDA-00167 Block Diagram

The circuit blocks can be identified easily in the PCB assembly view as well, shown in Figure 4.

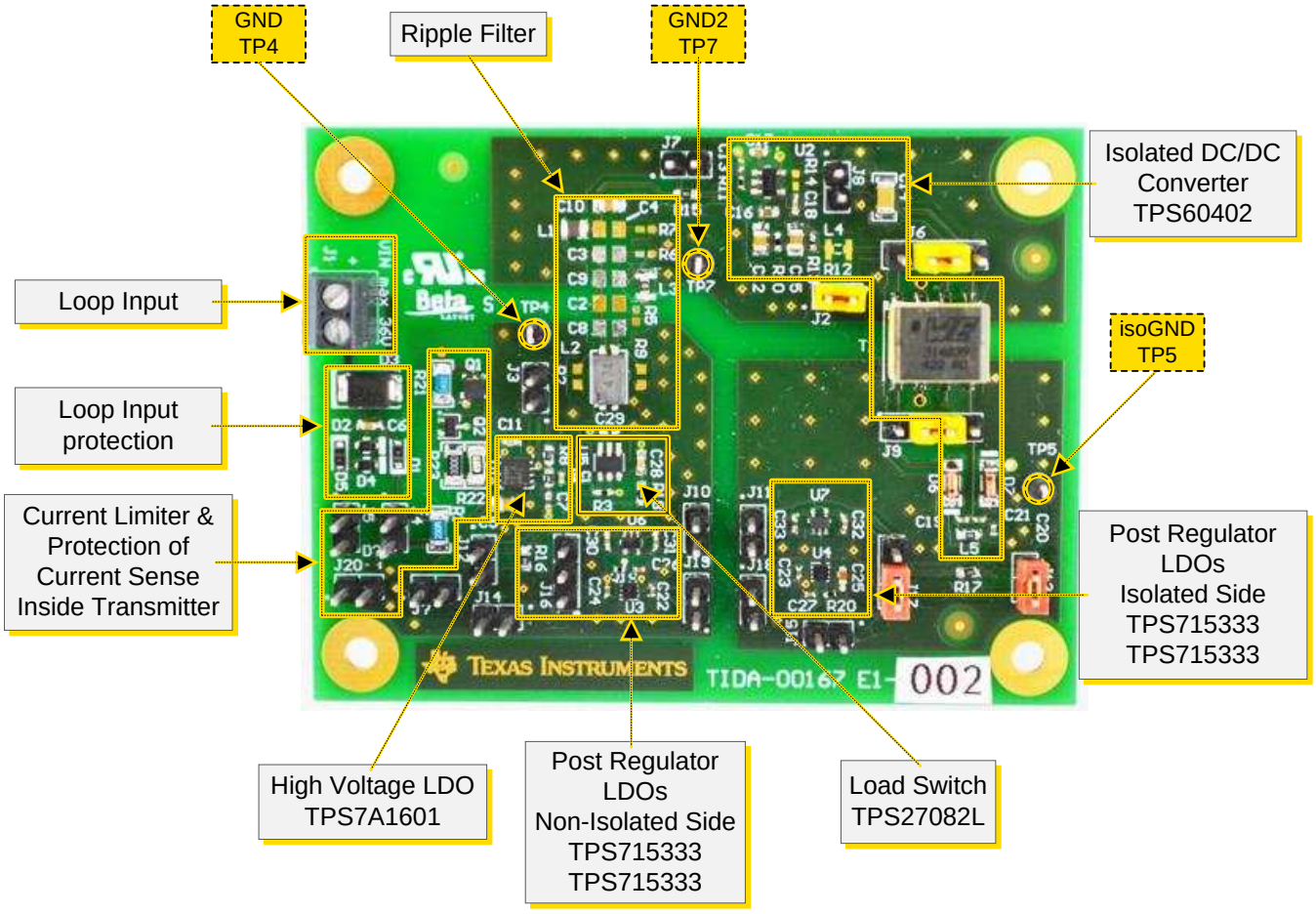


Figure 4. TIDA-00167 PCB Assembly View

5 Circuit Design and Component Selection

5.1 Loop-Input Protection

Before going into protection circuit details, one important statement in Section 3.1 should be stressed again:

Avoid protection circuitry from negatively impacting total system performance.

The term *system performance* is especially related to the accuracy of the loop-current control. The basis for this accuracy is actually an accurate sensing of the loop current. Leakage currents IR, which will not pass the 40-Ω current sense resistor inside the DAC, are critical for this accuracy.

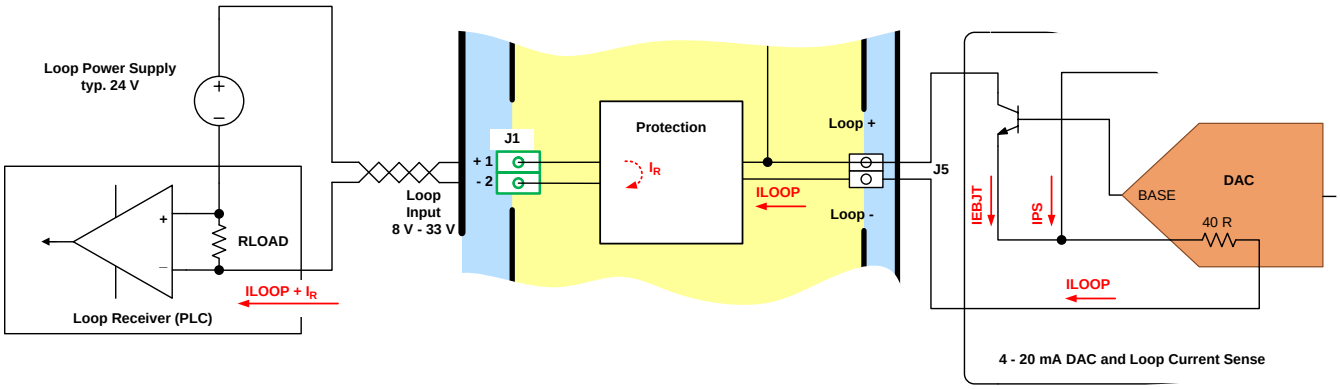


Figure 5. Negative Impact of Leakage Current inside the Protection Block

The leakage current IR inside the protection block is not seen by the DAC at all, but adds to the loop current seen by the loop receiver, which causes an error, as shown in Figure 5. Therefore, the design philosophy is to select the components contributing to this IR in a way that the value of the IR can be neglected, when compared to the 4- to 20-mA span of the loop current. A total leakage current less than 3 µA is desirable to keep the error referred to the 16-mA span less than 0.02%.

5.1.1 Input-Overvoltage Protection

The input overvoltage protection of this power design protects all blocks and components of the transmitter which can be considered to have a more-or-less direct connection to the loop. As can be seen in Figure 2 and Figure 3, the current limiter and the high voltage LDO of the power design can be considered to have such a direct connection to the loop. Moreover, the BJT controlled by the 4- to 20-mA DAC inside the transmitter electronics is exposed to the voltage on the loop-input terminals J1.

To reduce the input-voltage stress of these blocks, the voltage applied to the input terminals of the power design needs to be limited. The nominal maximum input voltage expected is provided either by dedicated modules of the PLC or by a separate (DIN-Rail) power supply. The output voltage of such separate power supplies can be often adjusted by users (approximately up to 20% to 25%), resulting in a maximum nominal voltage of approximately 30 V. Possible overvoltage events are mainly transients and overvoltage pulses caused by the following:

- Supply voltage overshoot during power-up of the power supply.
- Coupling and cross-talk between the loop cable and adjacent cables with large voltage or current transients on these adjacent cables.
- Surge, burst, or ESD pulses leading to differential mode voltages. Such pulses are used, for example, in EMC compliance testing during the approval procedure of the complete transmitter.

Out of these transients, the 8/20-µs surge pulse coupled through a total resistance of 42 Ω and through a coupling capacitor of 0.5 µF differentially into the loop input, according to the EN 61000-4-5, is the most critical pulse. This power design was created with the need to handle this critical surge pulse in mind.

A bidirectional TVS diode (D3) and a ceramic capacitor (C6) are used to clamp any overvoltage transient on the loop-input terminal J1 to a safe voltage level, independent of the transient voltage's polarity. J5 of the power design is the output of the loop-input protection and the interface to the loop-related block of the transmitter electronics. Therefore, J5 already provides a safe voltage level to the BJT controlled by the 4- to 20-mA DAC inside the transmitter electronics.

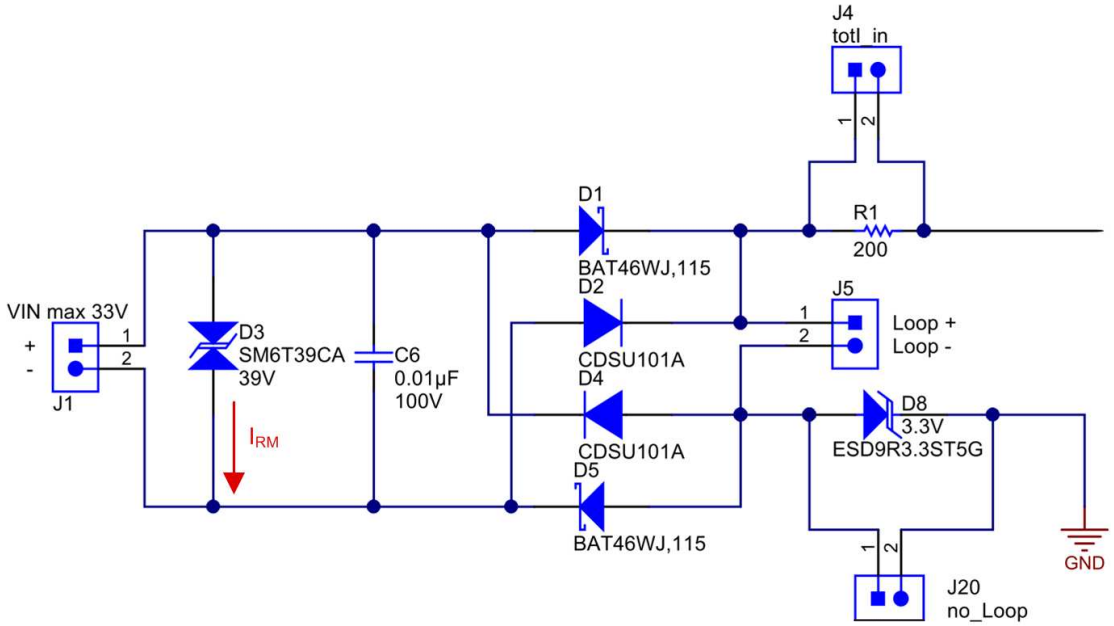


Figure 6. Input Overvoltage Protection

5.1.1.1 TVS Selection — D3

In order to choose the TVS appropriately for this design, the following requirements must be satisfied:

1. The TVS stand-off voltage V_{RM}, the voltage where the TVS does not conduct, must be higher than the maximum nominal loop-input voltage to prevent the TVS from conducting during normal operation. For most projects and applications, the condition *not conduct* can be considered to be fulfilled if the leakage current I_{RM} of the TVS at the given V_{RM} is less than 100 µA. However, for this design, a leakage current much less than 3 µA was targeted as outlined in Section 5.1. Because the leakage currents usually grow with increased temperature, the I_{RM} specification o the TVS should be given not only at the maximum nominal loop-input voltage, but also at the maximum operating temperature (85°C) of the design.
2. The TVS peak current and peak pulse power specifications must be higher than the surge current and pulse power under the design-specific conditions. Most of the TVS diode manufacturers specify the device with respect to a 10/1000 µs double-exponential test pulse. However, the pulse used for surge test according to EN 61000-4-5 is an 8/20-µs pulse. Ideally, TVS manufacturers provide the specification for this shorter pulse also. If not, the *Peak-Pulse Power Versus Pulse Time Graph*, which shows how the peak-pulse power of the TVS is affected by shorter or longer pulse duration needs to be used. For shorter pulse widths, the TVS can withstand a higher-peak pulse power.
3. When the TVS conducts and becomes low-impedance to clamp the voltage at a safe level, the TVS clamping voltage V_{CL} at the specific peak pulse current I_{PP} and at the maximum operating temperature of the design must be lower than the maximum recommended operating voltage of the circuits connected to that voltage (High Voltage LDO – U1, BJT controlled by the 4- to 20-mA DAC, diodes in the reverse-polarity protection, input capacitor C6).

More details regarding the selection process of the TVS can be found in TI Design, *Small Form Factor, 2-Wire, 4- to 20-mA Current-Loop, RTD Temperature Transmitter*, TIDA-00165.

The selected TVS is an SM6T39CA (see Section 9.2), fulfilling these three requirements:

1. I_{RM} (max): 1 µA at V_{RM} = 33.3 V and at 85°C — this is much less than the required 3 µA
   I_{RM} (max): 0.2 µA at V_{RM} = 33.3 V and at 25°C
2. The data sheet specifications for the 8/20 µs pulse are as follows:
   I_{PP} (max): 57 A
   P_{PP} (max): 4 kW
   Both parameters are much higher than the application specific values:
   I_{PP}: is approximately 22.6 A
   P_{PP}: is approximately 1.2 kW
3. $V_{CL\ (MAX\ at\ 100°C)}$ is approximately 55 V
   The devices connected to that voltage should be able to operate at up to 60 V.

5.1.1.2 Selection of Input Capacitor C6

To be able to bypass the higher frequency transient voltages caused by burst or ESD, a 10-nF ceramic X7R capacitor was selected. With the 100-V DC voltage rating of the capacitor, the device matches the clamping voltage of the TVS with plenty of margin.

5.1.1.3 Layout Recommendation

To be effective, the TVS (D3) and the input capacitor (C6) — both are highlighted by a blue edge in Figure 7 — should be directly placed between the loop-input connector (J1) and the reverse-protection diodes (D1, D2, D4, D5).

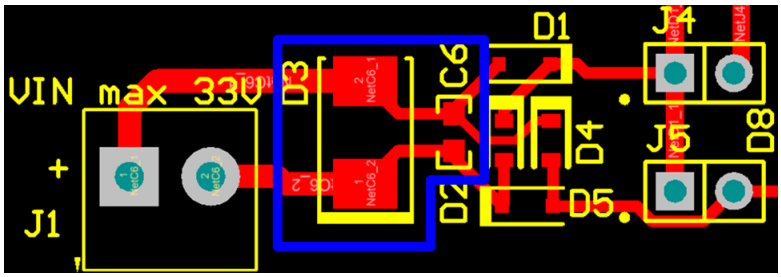


Figure 7. Input Overvoltage Protection — Layout Details

5.1.2 Reverse Input Voltage Protection

The reverse input voltage protection enables a transmitter to withstand operation at reverse input voltage conditions on the loop input (J1). Examples of such conditions are as follows:

- Interchange of the two wires at the loop-input terminals due to miswiring. Interchange can last even continuously.
- Negative differential-mode surge pulses (may happen due to lightning events or during testing by applying the negative 1-kV surge pulse, according to EN 61000-4-5).

The positive and negative input terminals are protected separately by protection diodes. Schottky diodes are preferred, due to their low-forward voltage VF. Their huge high-temperature reverse currents IR (hundreds of µA at >85°C) do not matter if the diodes are forward biased.

One-way rectifiers — half-wave rectifiers — can provide sufficient protection. An example would be a circuit consisting of the diodes D1 and D5 (as shown in Figure 8), but not having D2 and D4. The disadvantage of half-wave rectifiers is that the rectifier diodes need to withstand the sum of the rectifiers' output voltage (usually stored in the bypass capacitor on the input of the following block or blocks), plus the absolute value of an applied negative voltage. Using this design as an example, the sum of 33 V plus 60 V equals almost 100 V.

In the case of using separate diodes for the positive and negative loop-input terminals, this voltage can divide equally. In real cases, this equal splitting cannot be guaranteed because of the wide spread of reverse currents between the two diodes, especially when Schottky diodes are used at high temperatures. Another disadvantage of the half-wave rectifier configuration is the missing current, which would normally keep the blocks following the protection circuit alive during any negative input-voltage events.

Therefore, a better solution is a full-wave rectifier configuration, which provides a perfect voltage clamp across the rectifier diodes to the absolute value of the input voltage. The full-wave rectifier configuration also ensures a continuous current delivery to the following blocks, even during reverse input-voltage events. Nevertheless, if the rectifier bridge is built using Schottky diodes only, their hundreds of µA of reverse current IR is adding to the 1-µA IR of the TVS (D3). Therefore, the total error on the loop current measured by the loop receiver is no longer acceptable.

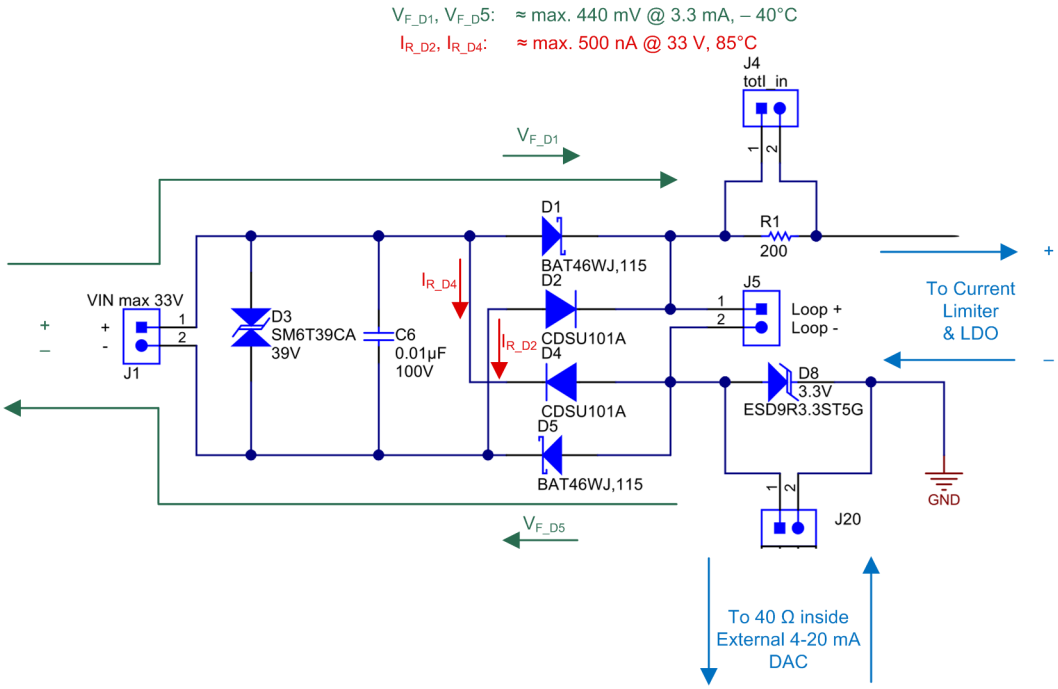


Figure 8. Input Reverse Protection — Loop Input with Correct Polarity

By using the mix of Schottky diodes and silicon diodes shown in Figure 8, the advantages of both diode types can be preserved. The two forward-biased Schottky diodes D1 and D5 cause a total worst-case forward-voltage drop of only 880 mV at 3.3 mA, –40°C. The two silicon diodes D2 and D4 prevent D1 and D5 from being stressed with more than 60 V during miswiring events or negative-differential surge pulses.

D2 and D4 are reverse-biased, but add together only 1 µA of additional IR at 85°C on the 1-µA IR of the TVS. The resulting 2-µA IR is within the design limit of 3 µA.

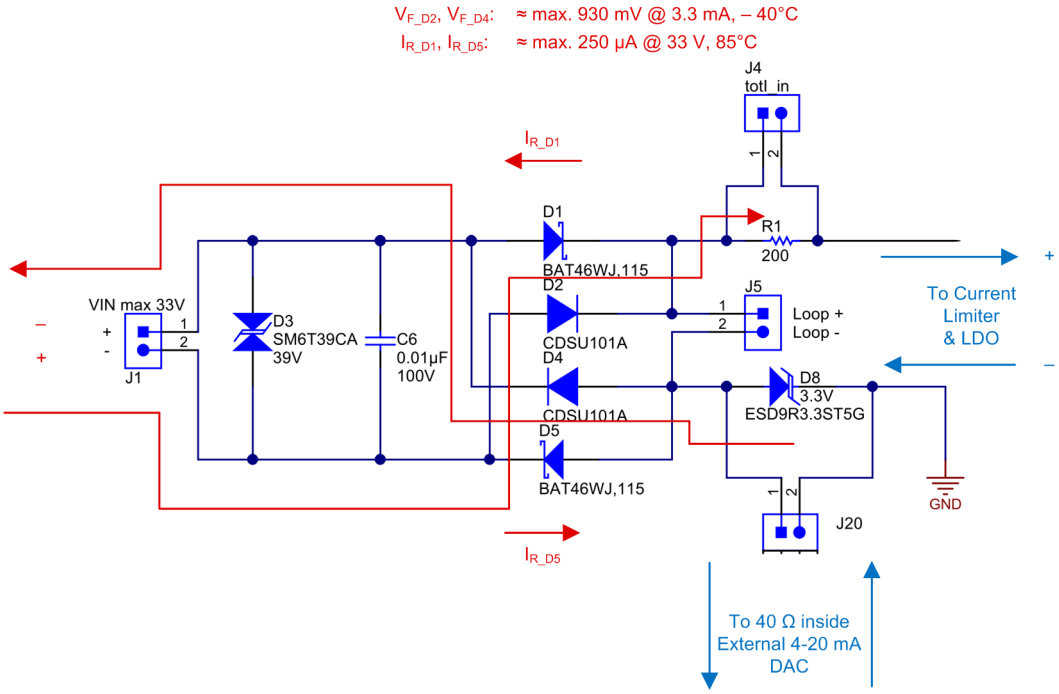


Figure 9. Input Reverse Protection — Loop Input with Reverse Polarity

Even when the loop-input voltage is applied in reverse direction, as shown in Figure 9, the output of the protection circuitry provides a voltage with the correct polarity to the following blocks. In this situation, the silicon diodes D2 and D4 are now forward-biased. However, the total forward-voltage drop of those two diodes is now in the worst-case situation, almost 1.9 V, which is more than twice the total drop caused by the Schottky diodes (almost 900 mV in total). The two Schottky diodes D1 and D5 are reverse-biased and contribute in total an additional 500 µA reverse current to the total leakage current of the protection circuitry, which has a maximum value of 3 µA.

Therefore, a transmitter powered by this design continues to work even with reverse loop-input voltage polarity. However, the transmitter will no longer be able to match the accuracy specification of the transmitter. Nevertheless, there is the clear advantage that the transmitter electronics will not lose power during negative transient events. Therefore, the transmitter is immediately back in operation with full, normal performance after the transient without any time delay due to an otherwise required restart the internal electronics of the transmitter.

5.1.2.1 Schottky Diode Selection – D1, D5

Key parameters for the selection of the Schottky diode are as follows:

- Lowest possible forward voltage V_F at the given forward current of 3.3 mA (maximum input current of this design). The V_F of the diodes increases the minimum needed input voltage on the loop input (compliance voltage). Because V_F is rising with decreasing temperature, the V_F at –40°C is of special interest.
- Reverse current does not matter. When the loop-input voltage has its correct polarity, D1 and D5 are forward biased.
- Sufficient reverse voltage: >60 V (V_{CL} of TVS)
- Sufficient forward current: The continuous current is given by the maximum 3.3-mA specification for the total input current of the design. In addition, there should be margin to cover inrush and other peak currents. Due to the current limiting resistor R1, any current will be limited to less than 300 mA (based on V_{CL} <60 V)
- Small package size: this is clearly desirable, but also in conflict with the requirement for lowest possible V_F

Based on the key parameters for the selection of the Schottky diode, a BAT46WJ has been selected with the specifications shown in Table 2.

Table 2. BAT46WJ Specifications

Maximum forward voltage	470 mV at 10 mA, –40°C V_F in the characteristics table inside the BAT46WJ data sheet: Approximately 440 mV at 3.3 mA, –40°C approximated
Maximum reverse voltage	100 V
Maximum forward current	250 mA; 2.5 A non-repetitive peak (at 25°C)
Package	SOD323F (SC-90); max 2.7 × 1.35 mm^2

5.1.2.2 Silicon Diode Selection — D2, D4

Key parameters for the selection of the two silicon diodes are as follows:

- Lowest possible reverse current I_R at the given 33-V maximum nominal input voltage of the design. The I_R of these two diodes needs to be added to the I_R of the TVS (D3), worsening the total accuracy for the transmitter. Because I_R is rising with increasing temperature, the value of I_R at the maximum operating temperature of the design (85°C or higher) is of special interest.
- Forward voltage does not matter. D2 and D4 are forward-biased during reversed-loop-input voltage condition only. Operation of the transmitter at this condition leads to performance and accuracy degradation as, explained in Section 3.2, *Loop -Input Protection*.
- Sufficient reverse voltage: >60 V (V_{CL} of TVS).
- Sufficient forward current: although it is not expected that the silicon diodes will operate in forward condition under normal operation, the silicon diodes must be able to withstand a continuous 3.3-mA current.
  The same requirements for the pulse current capability apply as for the Schottky diodes.
- Small package size: this is a clearly desirable parameter.

Based on the key parameters for the selection of the silicon diodes, CDSU101A has been selected with the specifications shown in Table 3.

Table 3. CDSU101A Specifications

Maximum reverse current	50 nA at 75 V, 25°C, ≈ 500 nA at 33 V, 85°C approximated using the 25°C specification above and the reverse characteristics graph in the CDSU101A data sheet.
Maximum reverse voltage	80 V
Maximum forward current	100 mA; 1-A surge peak (at 25°C)
Package	SOD-523F (0603); max 1.8 × 1.0 mm^2

5.2 Current Limiter and Circuitry to Protect the Current-Sense Circuitry Inside a Loop-Powered Transmitter

As shown in Figure 10, there is a dedicated circuit block responsible to reduce any inrush or surge current. The main concern here is to protect the 40-Ω current sense resistor inside the external DAC (belonging to the transmitter electronics). Inrush and surge currents are caused by sudden increase in the voltage applied to the loop-input terminals. The inrush or surge current is at the end the charging current, charging C5, as shown in Figure 10 from the voltage it had before to the same voltage level as the input terminals already have. This charge can happen during the following events:

- Initial power-up, especially when there is no dedicated low current limit in the 24-V loop power supply: sudden voltage step of a maximum 33 V (max input voltage).
- 1-kV differential surge; clamped by TVS D3 to approximately 60 V: resulting step is 52 V, assuming a condition when the voltage on the loop-input terminals before the 1-kV surge had been at the minimum V_{IN} of 8 V.

The different measures provided by the current limiter circuit are as follows:

- Ability to measure the current on the board: connect a voltmeter to header J4. The measured voltage drop across R1 represents the current with a scale of 200 mV/mA.
- The 200-Ω resistor (R1) serves as a passive type of current limiter.
- The 200-Ω resistor (R1) can be disabled (shorted) by populating a jumper to header J4.
- Active current limiter consisting of R21 to R23, Q1 and Q2: provides an easy way to limit the current to a value programmable by R22.
- The active current limiter can be disabled (shorted) by populating a jumper to header J21.
- 3.3-V TVS voltage clamp on header J20: J20 is the connection to an external DAC. Under normal conditions, the loop current flows through the DAC's current sense resistor, unless the voltage drop across the current sense resistor exceeds the clamping voltage of the 3.3-V TVS diode D8. The maximum expected loop current in case of using a DAC161x997 is 24 mA, resulting in 960 mV across the DAC's internal 40-Ω current sense resistor. It is important that the reverse current of this diode under normal operating condition is minimized. Otherwise, the accuracy of the complete system would be degraded. The data sheet of the ESD9R3.3ST5G specifies a maximum 1-nA reverse current for reverse voltages up to 3.3 V.
- Connection to an external DAC and the on-board 3.3-V TVS D8 can be disabled (shorted) by populating a jumper to header J20.

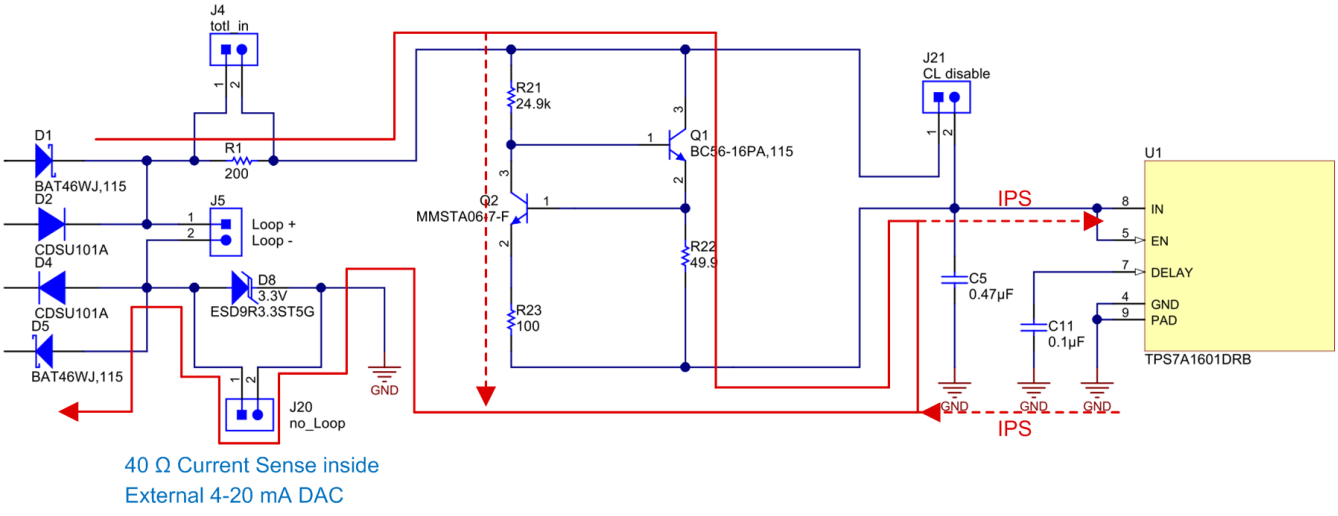


Figure 10. Current Limiter and Sense Resistor Protection

5.2.1 Active Current Limiter — Circuit Implementation

While the 200-Ω resistor R1 can be considered as a basic type of current limiter, additional active circuitry with the following features has been implemented:

- Greatly reduced dependency of the output current (IOUT) on the voltage difference (VIN – VOUT) between the input and the output of the active current limiter.
- Floating circuitry, no connection to GND.
- Simple circuit, just two NPN BJTs plus three resistors.

The performance of the circuit can be best described by the IOUT versus VIN–VOUT characteristic, as shown in Figure 12.

5.2.1.1 Basic Operation

The main path for the current flow is controlled by Q1 in Figure 11. The relation between the main currents is given by Equation 2.

$$IOUT = IIN + I\_R23 + I\_R22 \quad (2)$$

- Q2 and R23 can be almost neglected for voltage differences between VIN and VOUT less than 2.5 V. In that range of differences less than 2.5 V, the output current is provided completely by Q1 through R22. R21, R22, and the DC current gain of Q1 determines the value of IOUT.
  R21 is biasing Q1 with the base current IB_Q1. For a VIN-VOUT of 2.5 V, the IOUT is in the range of 9 mA.
- For voltage differences larger than 2.5 V, Q2 activates and finally tries to keep the voltage across R22 at the sum of its base-emitter voltage VBE and the voltage drop across R23.
  For a VIN-VOUT from 3 V to 40 V, the IOUT rises from 10 mA to slightly more than 15 mA.
- R23 stabilizes the circuitry against temperature changes.

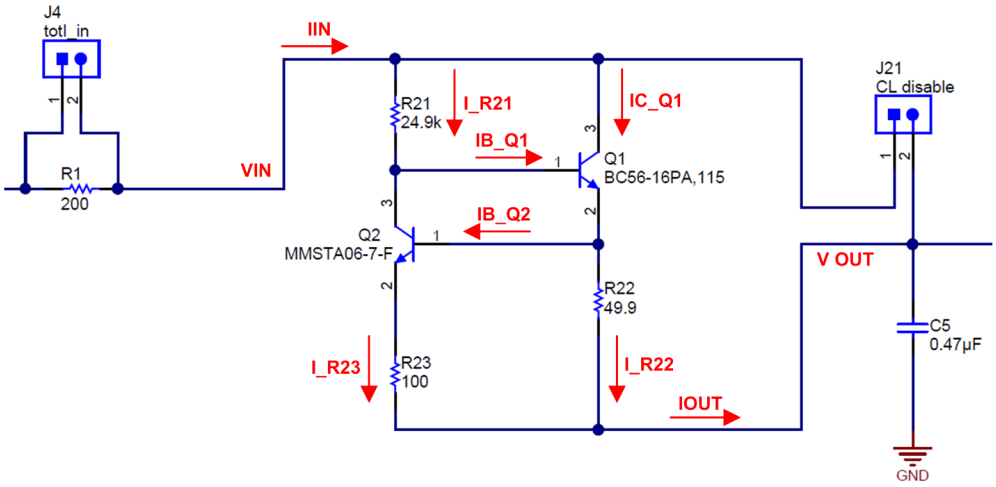


Figure 11. Active Current Limiter — Schematic and Operation

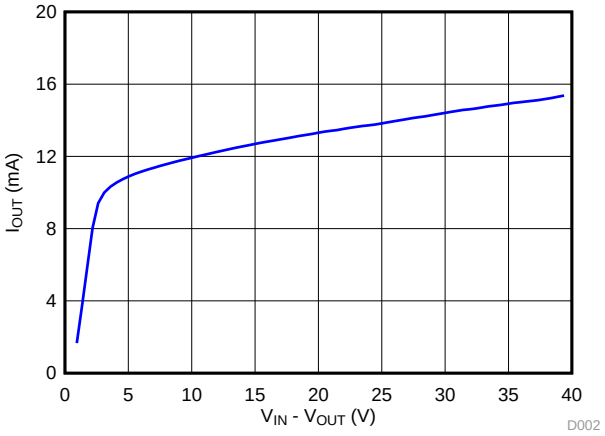


Figure 12. Active Current Limiter Characteristic: IOUT versus VIN-VOUT

5.3 High-Input Voltage LDO

Depending on the jumper setting, the high input voltage LDO is powered through different paths in the circuit. An overview of the different options is provided in Table 4.

Table 4. Jumper Settings(1) for Different Power Options of the High-Voltage LDO U1

J4	J21	J20 (2)	HIGH INPUT VOLTAGE LDO POWERED OFF... OR THROUGH...
☑	☑	☑	Output of reverse polarity protection
	☑	☑	Current limiting resistor R1
☑		☑	Active current limiter
		☑	Current limiting resistor R1 + active current limiter
☑	☑	DAC	Loop DAC
	☑	DAC	Current limiting resistor R1 + loop DAC
☑		DAC	Active current limiter + loop DAC
		DAC	Current limiting resistor R1 + active current limiter + DAC

(1) ☑ Jumper on respective header populated
(2) DAC — 4 to 20 mA DAC with current sense resistor connected to J20

5.3.1 High-Voltage LDO Selection

For this specific design, the selection of the first LDO is based on the following key concerns:

- Output option: Although fixed output-voltage LDOs are in general beneficial, the specific LDO for providing the nonisolated intermediate voltage needs to have an adjustable output voltage. An adjustable output voltage helps to optimize the total efficiency and keeps the transmitter electronics total supply current budget (3.3 mA).
- Maximum input voltage – Vin (Max): The LDO needs to withstand the voltage applied to the loop terminals of the transmitter. The voltage applied to the loop terminals can range up to 33 V under normal operation, but can rise to higher voltage levels under a condition of a differential surge voltage applied to the loop. Therefore, the maximum input voltage of the LDO needs to exceed the maximum clamping voltage of the TVS used for overvoltage protection. Under the condition of a 1-kV differential surge coupled through a 42 Ω / 0.5 µF coupling resistor and capacitor, the maximum clamping voltage of the TVS will be almost 60 V.
- Quiescent current — Iq: This parameter is important, because the complete transmitter electronic has a strict, input-current budget of less than 3.3 mA. The lower the current consumption of the LDO, the better. This budget is also applicable to cases where the input voltage of the LDO falls down near to the desired output voltage. Some LDOs (especially LDOs using BJTs as an internal series pass element) will show much higher Iq under such conditions. Therefore, these LDOs are not usable in such applications.
- Dropout voltage — Vdo: The dropout voltage characterizes the minimum voltage difference between the input and the output of the LDO. This parameter is mostly specified at the rated output current of the LDO. The dropout voltage of LDOs using FETs as an internal series pass element will scale proportionally to the output current. Please note that an LDO operated in dropout condition will be more a switch than a regulator. Therefore, the LDO input voltage needs to be some hundreds of mV larger than the desired output voltage to obtain the expected LDO performance.
- Output capacitor: It is highly desirable that LDO ensures stability even when ceramic capacitors are connected to the output. The majority of LDOs available today are designed to give stable operation even when ceramic capacitors are connected to the output.
- Package: Because the transmitter designs are usually limited in available board space, small components are needed. The small components requirement is valid for this power design.
- Operating temperature range: The transmitter design is targeted to operate from –40°C to 85°C. Therefore, the LDO operating temperature range needs to include the minimum operating temperature and needs to exceed the maximum operating temperature of the application for a thermally-reliable design.

	TPS7A4001	TPS7A4101	TPS7A1601	TPS7A6601-Q1
Output Options	Adjustable Output	Adjustable Output	Adjustable Output	Adjustable Output
Iout (Max) (A)	0.05	0.05	0.1	0.15
Vin (Max) (V)	100	50	60	40
Vin (Min) (V)	7	7	3	5.5
Accuracy (%)	2.5	2.5	2	2
Iq (Typ) (mA)	0.02	0.02	0.005	0.012
Vdo (Typ) (mV)	290	290	60	180
Output Capacitor Type	Ceramic	Ceramic	Ceramic	Ceramic
Additional Features	Enable Over Current Protection Thermal Shutdown	Enable Over Current Protection Thermal Shutdown	PG Enable Over Current Protection Thermal Shutdown	Enable Over Current Protection PG Soft Start Thermal Shutdown
Package Group	MSOP-PowerPAD	MSOP-PowerPAD	SON MSOP-PowerPAD	MSOP-PowerPAD
Estimated Package Size (WxL) (mm^2)	3 x 5: 15 mm^2	3 x 5: 15 mm^2	3 x 3: 9 mm^2 3 x 5: 15 mm^2	3 x 5: 15 mm^2
Operating Temperature Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125

Figure 13. Selection Table for High-Voltage LDO

As shown in Figure 13, the TPS7A1601 was selected. The TPS7A1601 outperforms all the other LDOs by its low Iq (5-µA typical), its 3-V to 60-V input-voltage range, its low dropout voltage (60 mV typical at 20 mA) and by the fact that it is available in a space-saving 3 × 3 mm^2 SON-8 package. The block diagram as shown in Figure 14 illustrates the comprehensive set of additional features the TPS7A1601 device includes.

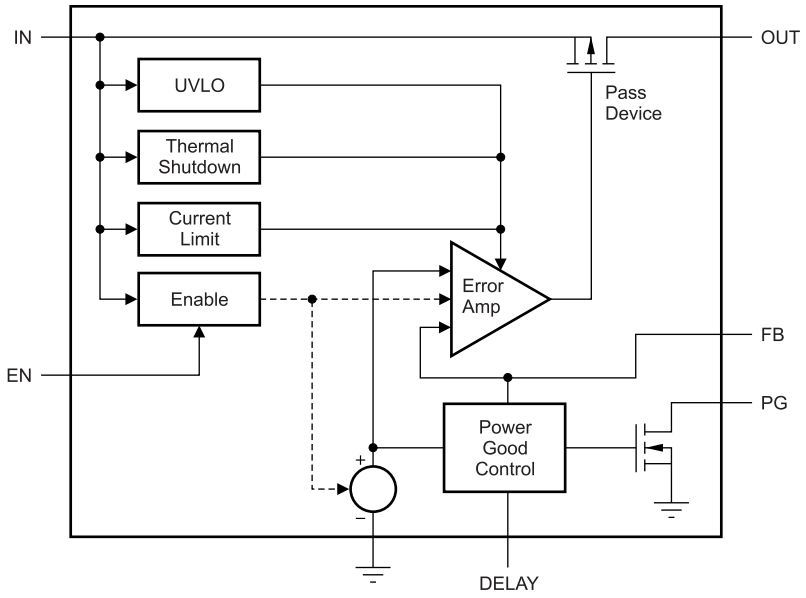


Figure 14. TPS7A1601 Block Diagram

Besides the thermal protection and the overcurrent protection, dedicated ENABLE (EN) and PG pins are provided. A DELAY pin enables system designers to program a specific power-good delay by a single capacitor (C_{DELAY}, as shown in Figure 15), which can be used to implement dedicated system-sequencing solutions if needed. The power-good delay time (t_{DELAY}) is defined as the time period beginning when V_{OUT} exceeds the PG trip threshold voltage (V_{IT}) to when the PG output is high.

The output voltage can easily be adjusted by a resistor divider (R1 and R2 in Figure 15). The TPS7A1601 is stable with a minimum input capacitance C_{IN} of 0.1 µF and output capacitance C_{OUT} of 2.2 µF.

Although a feed-forward capacitor (C_{FF}) from OUT to FB is not needed to achieve stability, use a 0.01-µF, feed-forward capacitor to maximize AC performance.

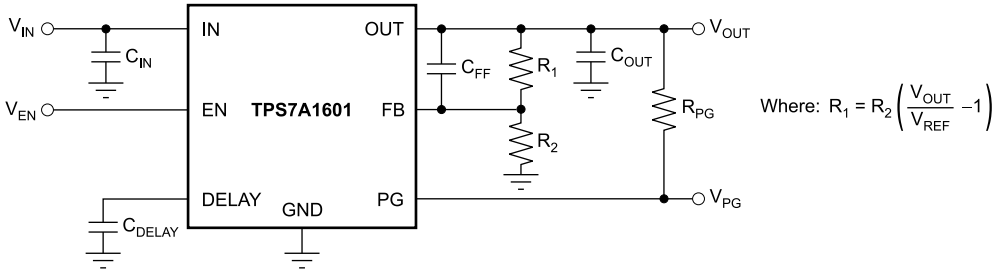


Figure 15. TPS7A1601 — Programming of Output Voltage and PG Delay Time

The 60-V maximum input voltage of the TPS7A1601 (absolute maximum rating is 62 V) provides a good cost-to-performance and size trade-off between the input overvoltage protection diode (TVS) needed and the input voltage capability of the LDO. The use of a FET as an internal pass device supports the ultra-low 5 µA of quiescent current and a dropout voltage scaling which is almost linear with the output current of the LDO, as shown in Figure 16.

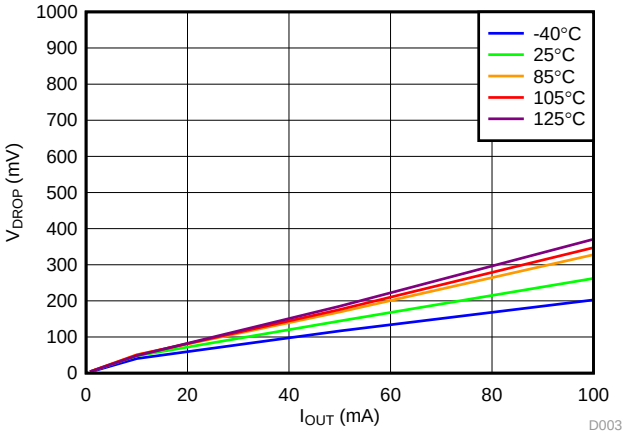


Figure 16. TPS7A1601 - Dropout Voltage versus Output Current

5.3.2 High-Voltage LDO — Circuit Implementation

The specific implementation of the TPS7A1601 (U1) is shown in Figure 17. As already explained, the output voltage of the LDO is adjustable. The target is a level of 4.5 V, which was found to offer the best efficiency of the isolated DC/DC converter used in this design. R4 and R8 are used for setting the voltage. R8 was pre-set to 255 kΩ. R4 can be calculated using Equation 3.

$$R4 = R8\left(\frac{VOUT}{VREF} - 1\right) = 255\,k\left(\frac{4.5\ V}{1.193\ V} - 1\right) = 706.8\,k \tag{3}$$

A standard value of 698 kΩ has been selected for R4. R4 and R8 need to be resistors with 1% or better tolerance. The resulting output voltage based on the selected resistors is derived according to Equation 4 as 4.459 V.

$$VOUT = \left(\frac{R4}{R8} + 1\right) \times VREF = \left(\frac{698\,k}{255\,k} + 1\right) \times 1.193\ V = 4.459\ V \tag{4}$$

The device is bypassed on the input by C5, a 470-nF, X7R capacitor with 100-V rating to cover high-voltage transients up to the 60-V level. The 470 nF is already more than the minimum recommended bypass capacitor (100 nF). It is intentionally chosen that way to cancel out the increase of input impedance caused by R1 or the active current limiter. Higher capacitance values would increase the charging time during initial power-up or at differential surge pulses. The inrush or surge-current limitation is provided by R1 or the active current limiter as described in Section 5.2.

The output bypass capacitor C7 is a 2.2-µF, X5R capacitor, which is in-line with the minimum-required capacitance. The voltage rating of the capacitor (16 V0 is not usually required for a 4.5-V output voltage. However, the 16 V voltage rating reduces the degradation of the capacitance value at the 4.5-V DC bias level. The TPS7A1601 data sheet's recommendation to use an even larger capacitance value (10 µF) to optimize AC performance was not followed, because the device is just a pre-regulator. The total accuracy and AC performance will be provided by the post-regulator LDOs.

In this design, the ENABLE feature (and respective input-pin 5) is not used. The EN pin is instead directly connected to the LDO's input-voltage pin 8. Therefore, the LDO is always on and starts automatically once the input voltage of the LDO exceeds the internal undervoltage lockout (UVLO) threshold of 2.7 V.

With this design, the power-good function of the LDO can be demonstrated and used in a flexible way — see the PG signals in Figure 17, highlighted by red circles. The PG uses an open-drain structure internally in the device. This internal FET is ON (and the PG-signal LOW), as long as the output voltage of the LDO does not exceed 90% of its programmed value. In this design, the PG pin 3 can be easily connected to the EN pin of the load switch (U5) by populating a jumper on the header J3. The same procedure can be followed by using a jumper on the header J14 to enable the low-noise, post-regulator LDO on the nonisolated side (U3) by the PG signal of the high voltage LDO U1. The needed pull-up resistors for the open-drain PG output are already on the board (R3 and R19).

An external pull-up resistor is needed, if the user intends to use the PG function for other purposes.

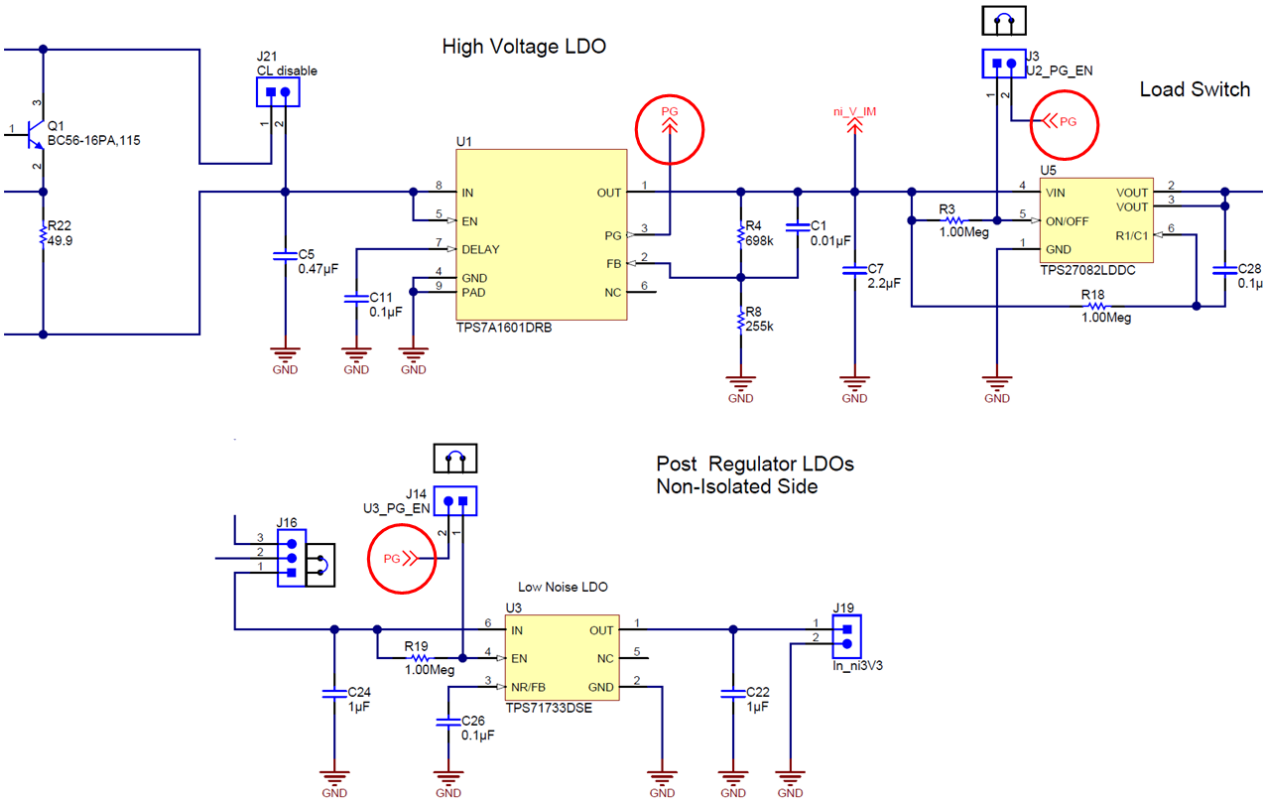


Figure 17. High-Voltage LDO — Circuit Implementation

The circuit offers the ability to program a desired power-good delay time with the capacitor C11. The power-good delay time (tDELAY) is defined as the time period from when the VOUT of the LDO exceeds the PG trip threshold voltage to when the PG output goes to open-drain (HIGH). With an arbitrary chosen C11 value of 100 nF, the delay time can be calculated using Equation 5 to be approximately 120 ms.

$$tDELAY = \frac{C11 \times VREF}{IDELAY} = \frac{100\,nF \times 1.193}{1\,\mu A} \approx 120\,ms \quad (5)$$

5.4 Load Switch

Following the philosophy to have flexibility designed into the complete power solution, a number of subfunctions have been implemented from the beginning. One of those subfunctions is the possible sequencing of the different voltage rails from a system perspective with the ability to enable and disable dedicated circuit blocks.

A particular possible use of the sequencing could be to enable the isolated DC/DC during power-up only after the PG of the high-voltage LDO indicates that the output voltage of the LDO is at its nominal level and the PG delay time has been elapsed. While the low-noise LDOs (U3 and U4) have dedicated EN pins, an ENABLE function is missing for the isolated DC/DC converter.

As a solution to address power sequencing for the DC/DC converter, a load switch is used to interrupt the path from the output of the high-voltage LDO (U1) to the subsequent ripple filter and isolated DC/DC converter.

5.4.1 Load Switch Solution Selection

A device used for offering ENABLE and DISABLE capability for the ripple filter and isolated DC/DC converter should fulfill the following requirements:

- >6-V rating
- Direct drive by power good of high-voltage LDO: active HIGH enable
- Low effort, almost no external components needed
- Low-voltage drop across the device when enabled
- Reasonable small package and solution size
- Programmable timing or slew rate

The table shown in Figure 18 compares the most commonly used solutions for load switching.

	N-Channel FET	P-Channel FET	Dedicated Load Switch
> 6 V rating	✓	✓	✓
Direct drive by PG, active HIGH enable	No, Level Shifter needed	No, Inverting needed	✓
Low effort	No, additionally charge pump needed to ensure VGS > VS	No	✓
Robust Logi Level Interface	No	No	✓ (with Hysteresis)
Used Type of Switch	N-Channel FET	P-Channel FET	P-Channel FET
Low voltage drop	✓	✓	✓
Reasonable small package	✓	✓	✓
Small solution	✓	✓	✓
Programmable timing or slew rate	✓	✓	✓

Figure 18. Selection Table for Load-Switch Solution

As a result of the comparison shown in Figure 18, a dedicated load-switch solution is chosen, using the TPS27082L as the specific device. This switch can support input voltages up to 8 V. The TPS27082L device has a logic HIGH-ENABLE input (labeled ON/OFF), so that it can be directly interfaced with the power good of the high-voltage LDO (U1). Furthermore, the TPS27082L does not need a charge pump to generate a more positive voltage than its input voltage (as an N-FET solution would need). The TPS27082L does not need an inverting stage to feature a HIGH-ENABLE characteristic (as a P-FET solution would need).

The typical ON-resistance of approximately 32 mΩ causes at the specific current level (approximately 2.4 mA) on that specific voltage rail a negligible voltage drop of only 77 µV. The TPS27082L device comes in a SOT-23 package, and the device has all the level shifting that otherwise would be needed, already integrated, as shown in Figure 19.

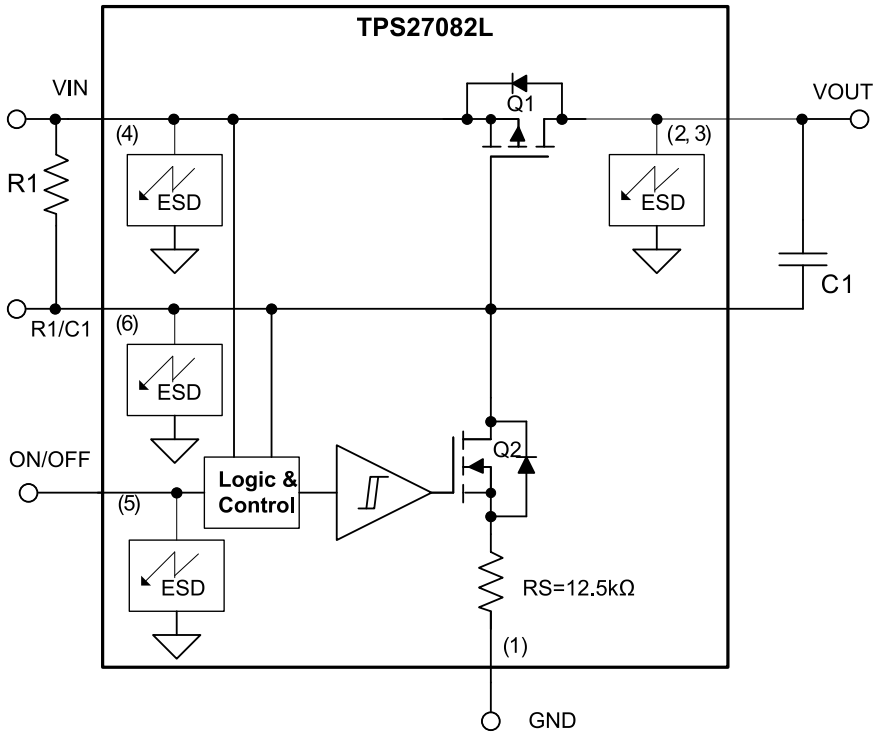


Figure 19. TPS27082L — Typical Application Diagram

During the ON-state of the switch, R1 in Figure 19 and the internal RS form a resistive-voltage divider allowing to program the Gate-Source voltage (VGS) of the internal PMOS (P-channel FET). This feature can be used to increase the ON-resistance of the PMOS, according to Table 5 (if needed), but also to influence the hysteresis between the turn-ON and turn-OFF thresholds of the ON/OFF pin, as shown in Figure 20.

Table 5. TPS27082L - RON as Function of VGS

PARAMETER		TEST CONDITIONS	$T_A = T_J = 25°C$			FULL TEMP RANGE		UNIT
			MIN	TYP	MAX	MIN	MAX	
$R_{Q1(ON)}$	Q1 Channel ON resistance	VGS_{Q1} = –4.5 V, ID = 3.0 A		32	52		64	mΩ
		$VGS1_{Q1}$ = –3.0 V, ID = 2 .5 A		44	66		84	
		$VGS1_{Q1}$ = –2.5 V, ID = 2.5 A		50	76		92	
		VGS_{Q1} = –1.8 V, ID = 2.0 A		82	113		147	
		VGS_Q1 = –1.5 V, ID = 1.0 A		97	150		173	
		VGS_{Q1} = –1.2 V, ID = 0.50 A		155	250		260	

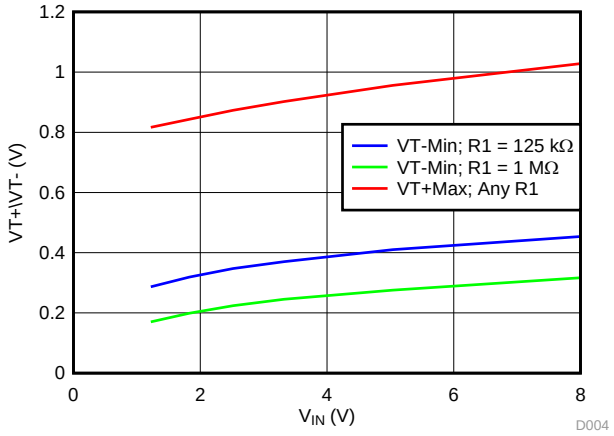


Figure 20. TPS27082L — ON/OFF Positive- and Negative-Going Threshold Voltage

An additional capacitor (C1 in Figure 19) can be used to configure the Turn-ON (and Turn-OFF) slew rate of the voltage on the output of the load switch to enable further reduction of inrush current of the connected load.

5.4.2 Load Switch — Circuit Implementation

The specific implementation of the TPS27082L (U5) is shown in Figure 21.

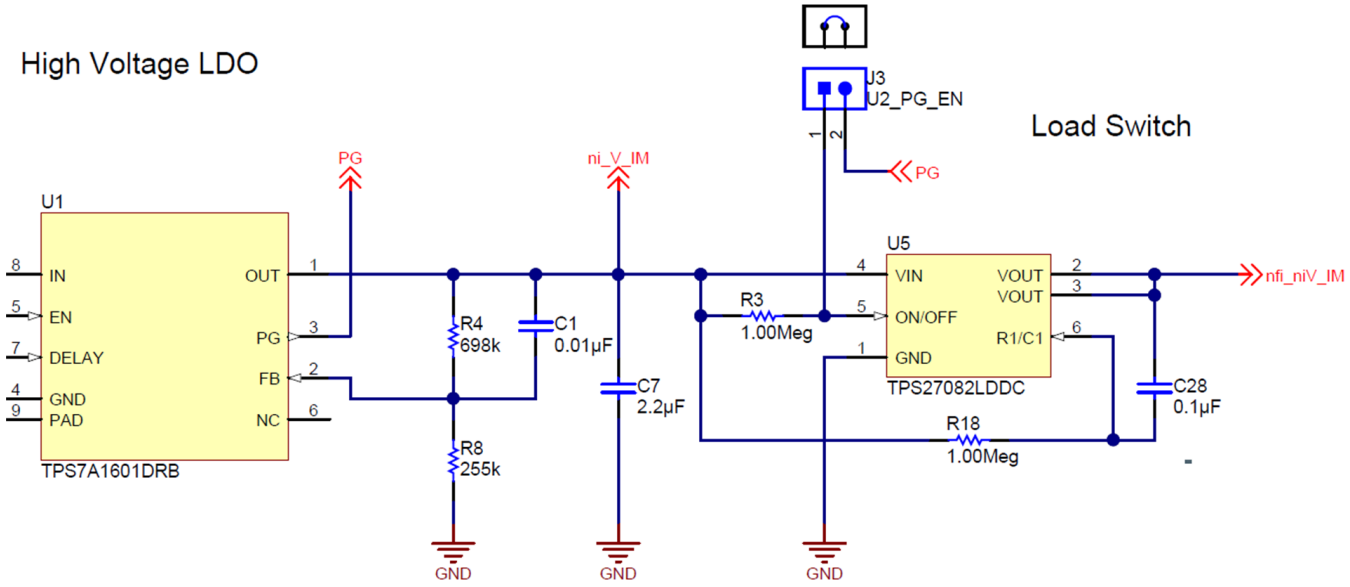


Figure 21. Load Switch — Circuit Implementation

The load switch is taking the output voltage of the high voltage LDO as input. The load switch connects the output voltage through the internal PMOS inside the load switch to the ripple filter and through the ripple filter to the input of the isolated DC/DC converter.

R3 is used to provide a logic HIGH to the ON/OFF pin of the device, as long as there is no dedicated ON/OFF control intended. The resistor also functions as a high impedance pull-up resistor for any onboard or external control signal. Table 6 lists the options for controlling the ON/OFF behavior of U5, based on the jumper setting or the use of external control signals on header J3.

Table 6. Jumper Settings for the ON/OFF Control of Load Switch U5

J3	LOAD SWITCH U5
	Always ON (continuously ENABLED)
☑ (1)	Controlled by power good of high-voltage LDO (U1) – ENABLED after the power good of the high-voltage LDO indicates that the output voltage of the LDO is at its nominal level and the power-good delay time has been elapsed.
External control signal connected to pin 1, referenced to GND (TP4)	Controlled by external signal. Voltage level applied to pin 1 of J3 needs to match the required logic levels as given in the TPS27082L data sheet.

(1) ☑ Jumper on respective header populated

As already expressed in Table 5, the effective internal gate-source voltage (VGS) influences the RON of the internal PMOS and can be calculated according to Equation 6 using the values (4.5 V as the input voltage VIN of the load switch) and components (R18) of the specific implementation in the circuitry.

$$VGS = -VIN\frac{R18}{RS + R18} = -4.5\ V\frac{1M}{12.5\,k + 1M} = -4.44\ V \quad (6)$$

With the high resistance value chosen for R18, almost the full VIN is applied as VGS to the internal P-channel FET of the load switch, so the load switch will be fully enhanced according to Table 5 once switched ON.

C28 is used to reduce the turn-on slew rate, resulting in a rise time t_{rise}, which can be calculated as shown in the empirically derived Equation 7, which is taken from the TPS27082L data sheet.

$$t_{rise} = \frac{50000 \times C28}{VIN^{2/3}}s = \frac{50000 \times 100n}{4.5^{2/3}}s = \frac{5m}{2.726}s \approx 1.8ms \quad (7)$$

where

- t_{rise} is the rise time of the load switch to charge its output capacitor from 10% to 90%
- VIN is the input voltage of the load switch (pin 4)
- s is second — base unit of time.

5.4.3 Load Switch – Avoiding the Pitfalls

Although controlling the ON/OFF pin of the load switch directly by the PG of the high-voltage LDO looks like a perfect sequencing solution, there is a possible pitfall when one or all of the following conditions are met:

- The system is powered by a current-limited (low current) loop power supply
- The jumper of header J4 is not populated (current-limiting resistor R1 is active)
- The jumper of header J21 is not populated (active-current limiter is active)

NOTE: Most important: even if both jumpers are populated, and even if the loop power supply does not limit the current, the load resistor inside the loop receiver (see Figure 2) will cause similar effects as the current-limiting resistor or the active-current limiter.

The behavior of the load switch has been tested at different loop-input voltage levels and with different jumper settings on the board. A power supply (current limit set to 300 mA) was directly connected to J1 with the correct polarity.

As outlined in the following paragraphs of this section, Section 5.4.3, the most critical operation happens at minimum loop-input voltage (8 V) and with both current-limiting features (current limiting resistor R1 and active current limiter) activated (jumpers J4 and J21 not populated on the respective headers).

The first test was successful with 33-V loop-input voltage, J3 populated to use the PG of U1 to control the load switch, and J21 populated to short the active current limiter (see Figure 22). The first test did not confirm the critical operation concerns, although J4 was not populated, so the current-limiting by R1 was active.

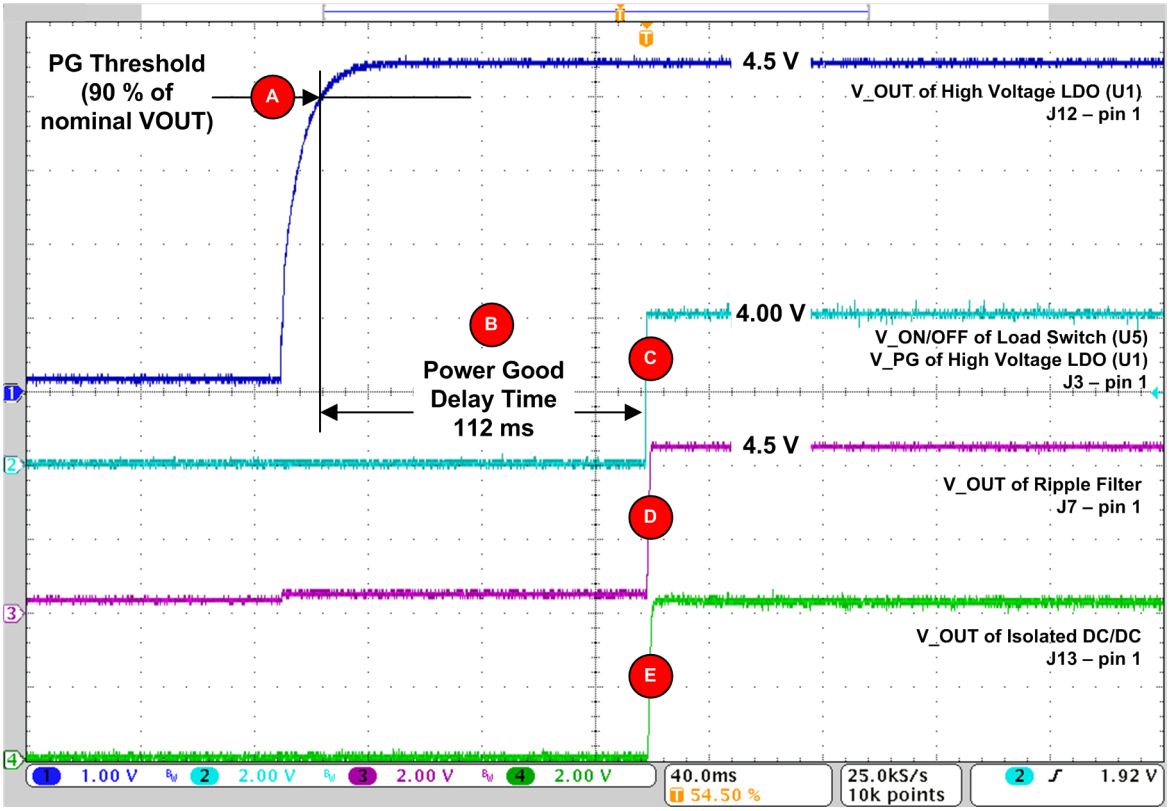


Figure 22. Load Switch Controlled by Power Good, 33-V Loop Input, R1 Active

After applying the loop-input voltage, the output voltage of the LDO rises up to the programmed level of 4.5 V. The LDO output voltage crosses the internal PG threshold level at approximately 90% of the nominal VOUT (A) of the LDO. At this time, the PG is still LOW. Once the power-good delay time (B) has elapsed, power good goes open drain, representing a logic HIGH (C). Based on the voltage divider, which is generated by the 10-MΩ, oscilloscope-probe impedance and the onboard 1-MΩ pull-up resistor (R3), the measured voltage by the oscilloscope is not 4.5 V but only approximately 4 V.

The load switch (U5) is switched ON by the PG signal connected to the ON/OFF pin of the load switch. The 4.5 V is connected by the load switch to the ripple filter, so the ripple filter's output rises to the same 4.5 V (D), powering the isolated DC/DC converter. The DC/DC converter starts immediately and generates the isolated voltage (E). Despite the current limiting effect of R1, there is no voltage dip noticeable on the output of the high voltage LDO (A) due to the large loop-input voltage of 33 V. There is no voltage dip, provided there is enough headroom for the LDO and enough stored energy in the input bypass capacitor (C5) of that LDO.

However, repeating the same test and only lowering the loop-input voltage to 8-V confirmed the concerns completely, as shown in Figure 23.

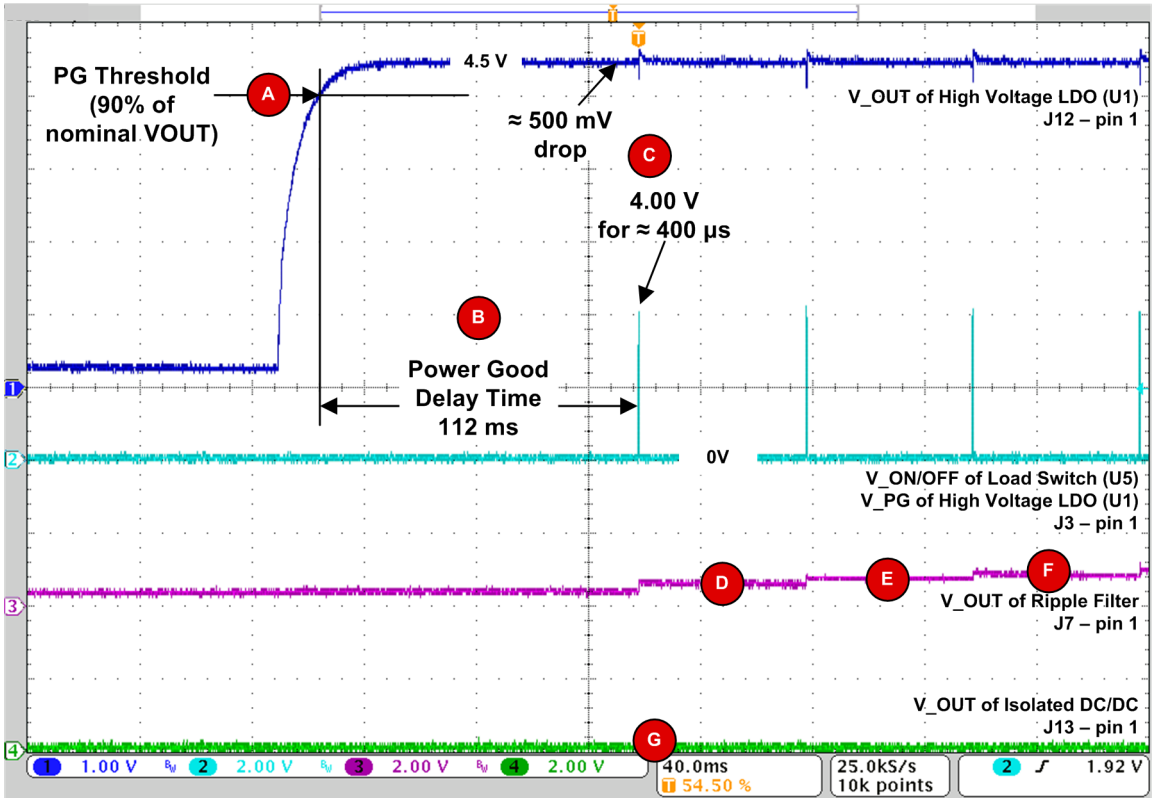


Figure 23. Load Switch Controlled by Power Good, 8-V Loop Input, R1 Active

The circuit initially starts with the lower loop-input voltage the same way as described for 33-V loop-input condition (A) and (B), as shown in Figure 22. However, at the moment the power good rises, the drastically reduced headroom voltage (approximately 2.6 V based on approximately 7.1 V_{IN} and 4.5 V_{OUT} of the LDO) and the minimized energy stored in C5 begin to cause what eventually switches OFF the load switch. As in the case before (Figure 22), the load switch turns ON controlled by the power good. The attempt to charge all the capacitors after the load switch (C29, C10, C16, C12, and C15) and to start the isolated DC/DC converter will cause a voltage dip (approximately 500 mV) on the output (C) of the high-voltage LDO, crossing the negative-going PG threshold. As a result, the PG goes LOW after 400 µs, switching OFF the load switch.

This sequence (ending in switching OFF the load switch) might be repeated for an infinite time if the output of the ripple filter cannot establish a high-enough voltage level to finally reduce the charging current of the capacitor to a safe value and to stabilize the output voltage of the LDO above the power-good threshold. This sequence arises with only 200 Ω as a current-limiting resistor (R1) in the path of the current flow. In real applications, the load resistor in the loop receiver may be much higher in resistance. In addition, the active current limiter may be enabled (J21 populated). All these effects together worsen the outcome and impact even the operation at a 33-V loop input.

NOTE: Therefore, the direct control of the load switch by the PG of the high voltage LDO cannot be recommended at all.

In case of a required start-up sequencing of the isolated power rail, the ON/OFF pin of the load switch should be controlled by an externally generated signal, as shown in Figure 24. This external signal can be generated, for example, by an external open-drain output connected to pin 1 of J3. Using an external open-drain output connected to pin 1 of J3, the output voltage of the high-voltage LDO rises to its nominal 4.5-V value and stays there (A). Usually, the isolated DC/DC converter is OFF at the beginning. Therefore, the external control signal needs to provide a logic LOW (B) to the ON/OFF pin of the load switch, which is achieved by switching the external open-drain structure ON.

To start the isolated DC/DC converter, the external open-drain structure needs to go into high impedance; thus, causing a sudden rise (C) of the control voltage on the ON/OFF pin of the load switch. The load switch turns ON and charges the capacitors of the ripple filter. The bypass capacitor (C16) and the two capacitors (C12 and C15) of the DC/DC converter form the right leg of the half-bridge and will be charged as well. The converter begins to start-up (D).

The resulting inrush current causes a sudden decline of the input voltage of the high-voltage LDO, due to the active current limiter and activated R1. If the input voltage of the LDO falls below its nominal output voltage, even the output voltage of the LDO will decline (E). Because the ON/OFF signal uses the VOUT of the LDO for its pullup resistor R3, the ON/OFF control signal will show the same decline as well. As long as this negative-going voltage (F) still exceeds the negative-going ON/OFF threshold (Figure 20) of U5, the load switch continues to stay ON and ensures a smooth and continuous rise of all the signals shown of the output voltage of the ripple filter, as well as of the isolated output voltage of the DC/DC converter.

One way to eliminate the voltage drop (F) on the control signal completely may be to decouple the voltage (R3) with a decoupling diode and an additional bypass capacitor.

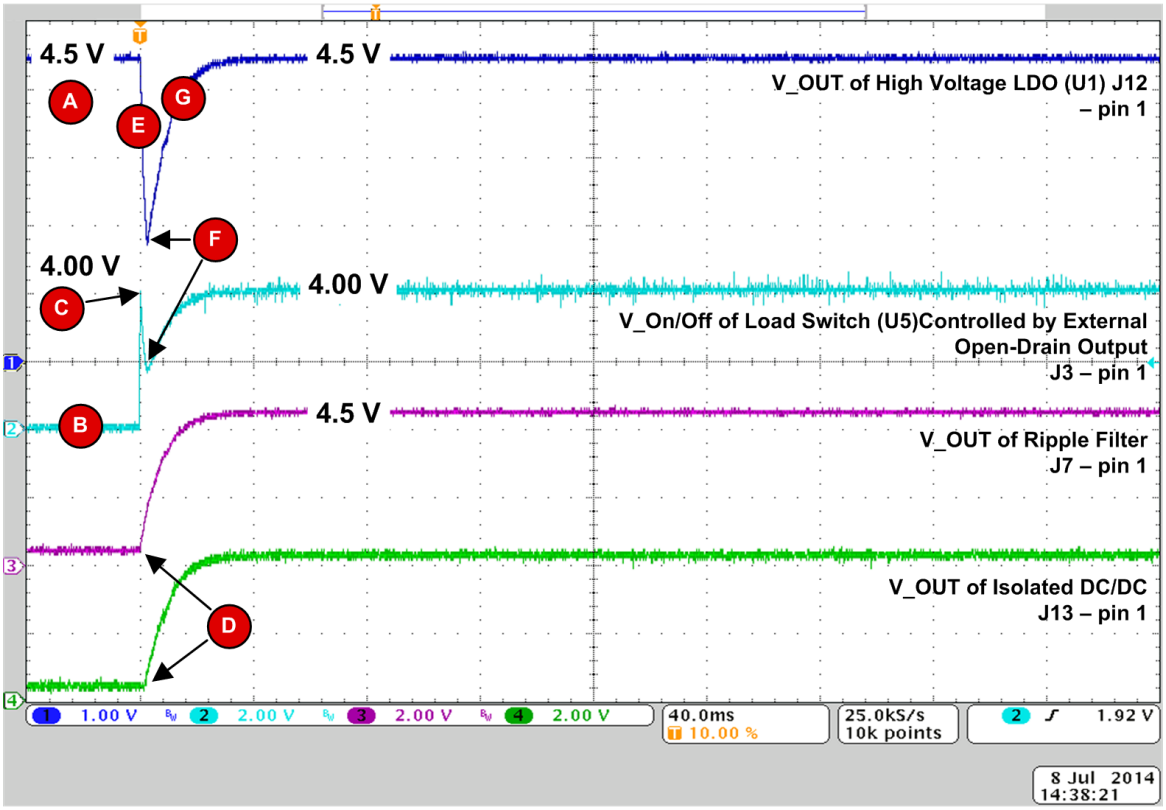


Figure 24. Load Switch Controlled by External ENABLE Signal, 8-V Loop Input, Active Current Limiter Used and R1 Active

If sequencing is not needed, the load switch can be kept always on simply by not populating J3 and also not connecting any control signal to the respective ON/OFF pin. The resulting start-up behavior of the circuit is shown in Figure 25. From the moment when the output voltage of the LDO starts to rise, all other signals start their smooth and continuous rise until the output voltage and the other signals reach their final value.

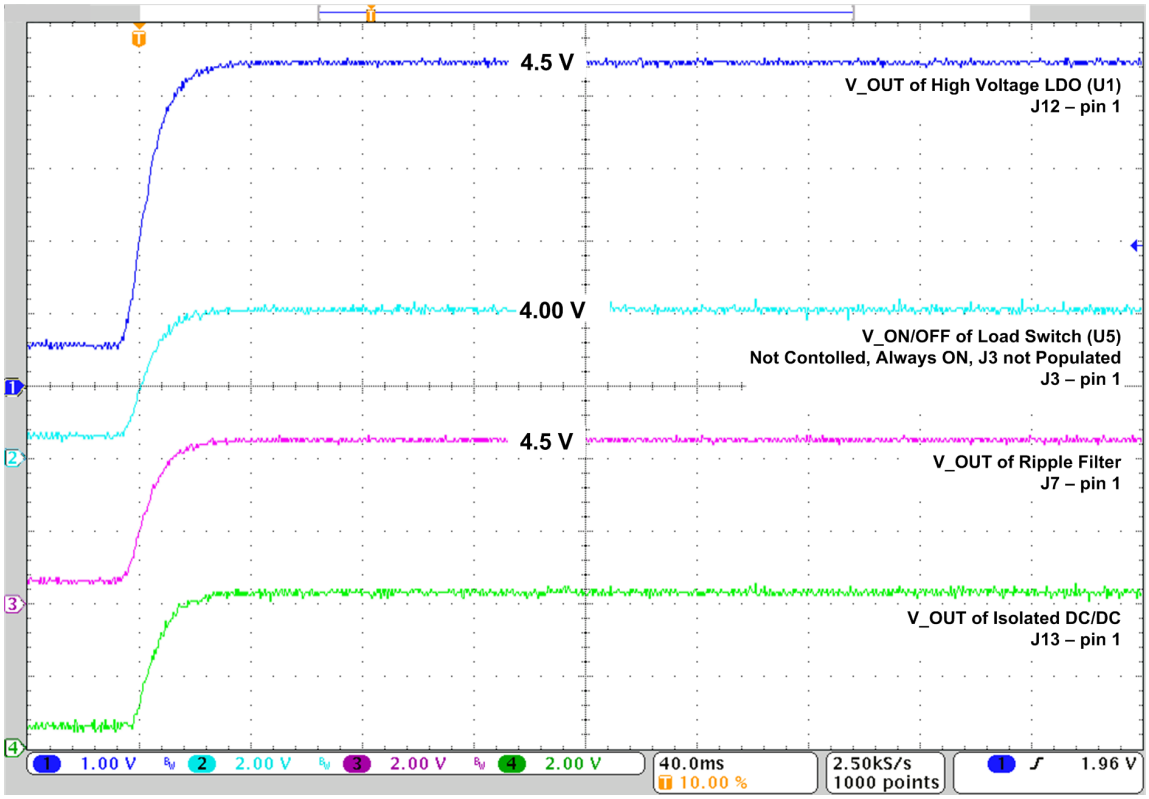


Figure 25. Load Switch Not Controlled but Always ON, 8-V Loop Input, Active-Current Limiter Used, R1 Active

5.5 Ripple Filter

The ripple filter is designed to act as a countermeasure against input-ripple currents generated by the isolated DC/DC converter. Without any filter, this ripple current would be directly superimposed on the loop current (assuming no suppression by the load switch and the high-voltage LDO). The ripple current would also be seen by the input of the post-regulator LDOs on the nonisolated side, as shown in Figure 2.

Both ripple current effects can negatively impact system accuracy and performance, as well as cause conducted EMI on the loop power input (J1), exceeding the respective limits in EN 55011. The specific intention of this design is to offer suppression for the differential-mode and common-mode noise caused by the isolated DC/DC converter.

5.5.1 Ripple Filter Component Selection

The final-use case of the complete design is in small transmitters with limited space. Therefore, the inductive components have been selected to provide a reasonable filtering effect and low DC resistance, while offering the smallest possible component and solution size. The small operating current seen by the filter definitely helps. However, the low-switching frequency of the DC/DC converter may be a challenge.

Special selection was mainly done for the inductors, while the filter capacitors are identical with other X5R or X7R ceramic capacitors commonly used.

The following filter inductors are selected.

- For use in the differential mode filter:
  CB2518T470K: 47-µH chip inductor, 1.235-Ω max DC resistance, 2.5 × 1.8 mm^2, more details in the CB2518T470K specification sheet.
- For use in the common mode filter:
  DR221-474AE: 470 µH surface mount data line choke, max RDC 2 × 0.35 Ω, 6 × 3.3 mm^2. The specific choke is selected because it belongs to the ones with the largest inductance and with the highest impedance in the frequency range from 1 to 20 MHz, see the Impedance versus Frequency graph in the DR221-474AE data sheet.

5.5.2 Ripple Filter —Circuit Implementation

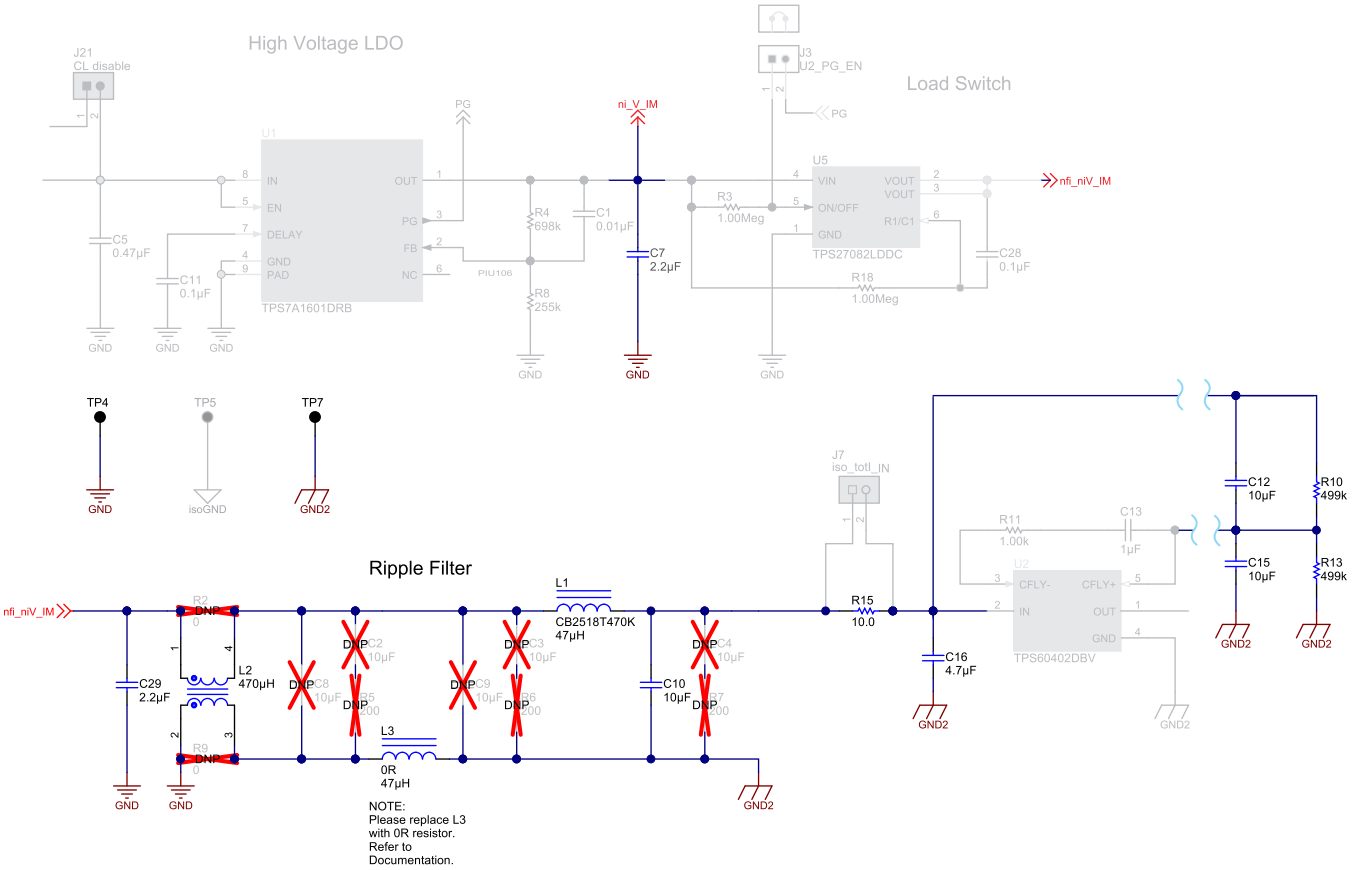


Figure 26. Ripple Filter — Circuit Implementation

The ripple filter has been designed by providing a number of placeholder components in the schematic Figure 26, as well as in the PCB layout, enabling the user to build his own filter structure. In the fully populated version, the filter consists of:

- Common mode inductor L2: filtering out the common mode (CM) noise, mainly targeted to suppress frequencies above approximately 500 kHz
- Two filter inductors L1 and L3 to form in total a 4th order differential mode filter: filtering the differential mode (DM) noise, mainly frequencies below about 500 kHz
- The filter capacitors C8 to C10 to complete the filters
- RC-damping networks C2 to R5, C3 to R6, and C4 to R7 for attenuation of the filter resonances. Details about this configuration, especially about the special arrangement of the two DM-inductors to form a fourth order filter, can be found in SLUP298.

NOTE: The ground on the input of the ripple filter is different from the ground on the output of the filter, due to filter inductors in the ground path (ground-related part of L2, L3).

Beside this filter structure, other components, such as the isolated DC/DC converter's input bypass capacitor (C16) and the input current sense resistor (R15), together with C10, have a noise reduction effect as well. The output capacitors of the high-voltage LDO (C7 and C29) also have a noise-reduction effect.

Pre-compliance EMI testing showed a clear reduction of common-mode noise at frequencies larger than 1 MHz measured with the fully-populated ripple filter versus an alternative test without the filter at all, as shown in Figure 27.

The DC/DC converter was loaded by a 1.65-kΩ load resistance connected on the isolated 3.3-V LDO (J18), resulting in 2-mA output current. One terminal of the load was earthed to represent the worst case.

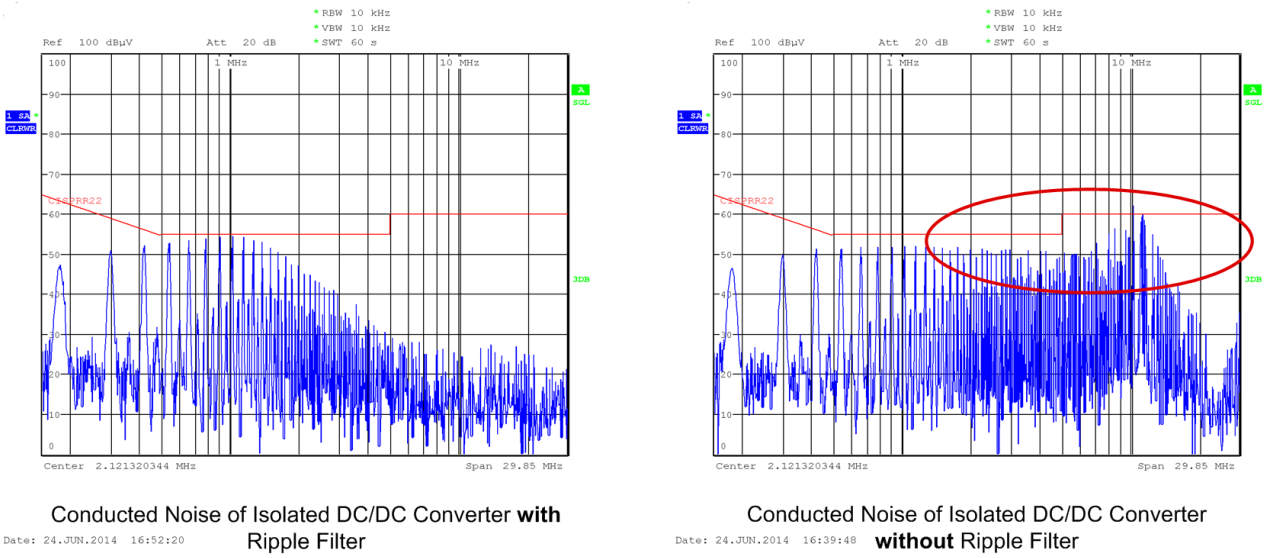


Figure 27. Conducted Noise of Isolated DC/DC Converter with and without Ripple Filter

In an additional series of tests conducted with the complete board, the ripple filter was scaled down step-by-step. The result from these tests show that there is no advantage of the fully-populated filter versus a scaled-down version. No noticeable difference has been discovered between the test cases with different populated filters.

As a result, the final schematic and BOM show the fully populated filter and list all the components. The components that are not needed are clearly marked with *DNP* (Do Not Populate) in the schematic and show a quantity of zero in the BOM. In the scaled down version, L3 is replaced with a simple 0-Ω resistor — see Figure 26 and the complete schematic, Figure 71.

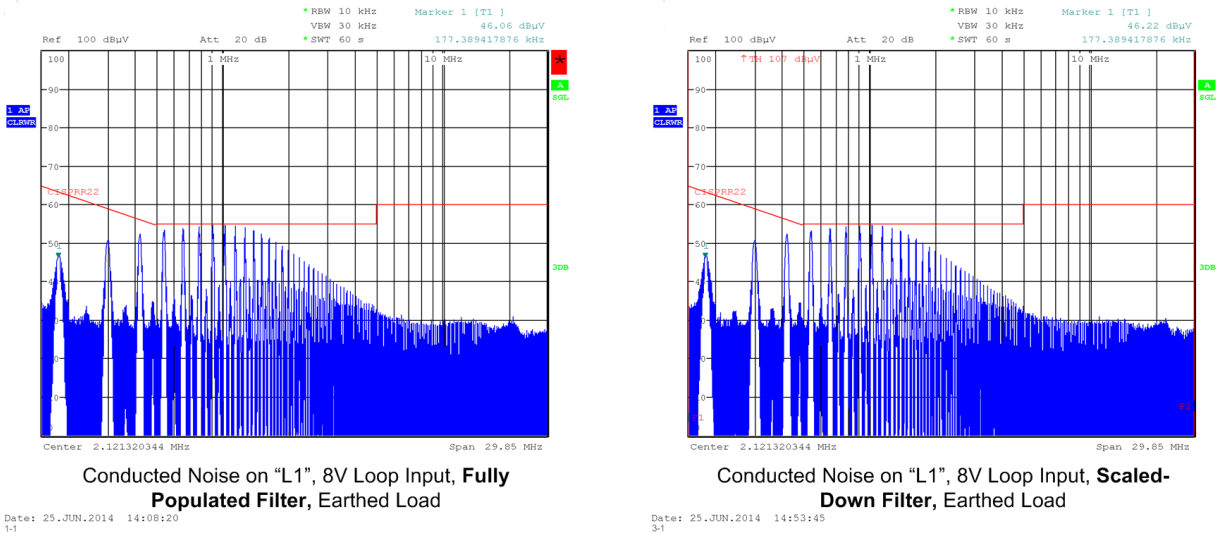


Figure 28. Conducted Noise with 8-V Loop Voltage, Full Filter versus Scaled-Down Filter

Furthermore, tests showed that the loop-input voltage on J1 does not influence the test results. The fact that the loop-input voltage on J1 does not influence the test results is a consequence of always powering the DC/DC converter off the same supply voltage — the 4.5 V-output of the high-voltage LDO — independent of the loop-input voltage. Details about those measurements can be found in Section 8.1.2.

5.6 Low-Noise, High-PSRR LDOs and Low-Iq LDOs Used as Post Regulators to Provide Isolated and Nonisolated 3.3-V Rails

The design uses LDOs as post regulators to provide stable and noise-free 3.3 V to the analog and digital parts on the isolated and nonisolated side of the transmitter design.

5.6.1 Post-Regulator LDO Selection

Key concerns for the post-regulator LDO selection (as compared in Figure 29) are as follows.

- Ideally the same LDO should be used for the post regulators on both sides of the design, which reduces the number of different devices needed.
- Output voltage option: because the needed output voltage is specified as 3.3 V, fixed output voltage LDOs are beneficial for saving the otherwise-needed, output-voltage resistor divider and reducing the solution size.
- Maximum input voltage – Vin (Max): the output voltage of the TPS7A1601, used to provide the nonisolated intermediate voltage, is 4.5 V. This voltage range determines the minimum value for the required Vin (Max) of the LDO on the nonisolated side. Because the output voltage provided by the isolated DC/DC converter is not regulated by a voltage control loop, there is an expectation that this nonregulated isolated voltage which serves as input voltage for the post-regulator LDOs on the secondary side can rise to voltage levels in the range of 5 to 6 V. Rising to voltage levels in the range of 5 to 6 V is especially likely to happen under operation at high ambient temperatures (85°C) and under no-load conditions on the secondary side. Therefore, the maximum input voltage of the post-regulator LDO needs to exceed 6 V.
- Quiescent current – Iq / package: A low Iq is important for the post-regulator LDOs for the same reason as a low Iq is important for the high voltage LDO (providing the nonisolated intermediate voltage). The reason is the strictly-limited, input-current budget of a complete transmitter electronics, which is less than 3.3 mA. Equally, the requirement for using small package size devices is applicable for the post-regulator LDOs as it is a requirement for the high-voltage LDO to finally enable the smallest size solution.
- Dropout voltage – Vdo / Power Supply Rejection Ratio (PSRR): both parameters are very important for the specific application case. On the secondary side, the post-regulator LDO will not only be used to provide a stable 3.3 V, but also to provide the voltage noise-free. The post-regulator LDO acts as a type of active filter, filtering out the switching frequencies' output ripple voltage of the DC/DC converter. By doing this, the post-regulator LDO also reduces the needed capacitance C19 - C21 on the output.

  On the primary side, the LDO will generate a stable 3.3 V to power the DAC (inside a connected transmitter circuit), which is controlling the loop current. This rail needs to be noise-free also to get the full performance and accuracy from the DAC.

  A potential noise source on the nonisolated, primary side is the isolated DC/DC converter. The isolated DC/DC converter feeds its input ripple current back to the intermediate voltage rail generated by the high voltage LDO (TPS7A1601). The resulting ripple voltage on this intermediate voltage rail needs to be filtered out by the post-regulator LDO on the primary side.

  The ability of an LDO to act as a filter is best characterized by the PSSR of the LDO. The higher the PSRR of a LDO at the specific switching frequency, the better the LDO can act as a filter. The PSRR specification in the data sheet is always related to a needed difference voltage, often named *headroom voltage* (VIN-VOUT). The lower this headroom voltage is (at which the LDO is able to perform with a specific PSRR), the better. This voltage difference is related to the dropout voltage, because a low Vdo specification of a LDO is a prerequisite for the LDO to perform with a high PSRR, with even a low VIN-VOUT headroom.
- Iq versus PSRR: there is a major conflict when trying to find low-Iq LDOs that have outstanding PSRR at the same time. PSRR characterizes the dynamic behavior of the LDO, and is therefore related to the bandwidth of the internal error amplifier of the LDO. Therefore, this design offers two different LDOs on both sides, one with low Iq and one with high PSRR. The user can select and test easily which of the LDOs fits the specific requirements best in a specific application. LDO selection is simplified by dedicated headers and jumpers.

	LP5900	TPS71733	TPS71533	TPS7A4901
Output Options (V)	Fixed Output 1.5 … 4.5	Fixed Output 3.3	Fixed Output 3.3	Adjustable Output
Iout (Max) (A)	0.15	0.15	0.05	0.15
Vin (Max) (V)	5.5	6.5	24	36
Vin (Min) (V)	2.5	2.5	2.5	3
Iq (Typ) (µA)	25	45	3.2	60
Vdo (Typ) (mV)	80	170	415	260
PSRR @ 100KHz (dB)	40	67	60	54
Output Capacitor Type	Ceramic	Ceramic	Ceramic	Ceramic
Package	DSBGA 1.08 x 1.05: 1.2 mm^2 WSON 2.2 x 2.5: 5.5 mm^2	SC70 2.1 x 2: 4.2 mm^2 SON 2 x 2: 4 mm^2 WSON 1.5 x 1.5: 2.25 mm^2	SC70 2.1 x 2: 4.2 mm^2	MSOP-PowerPAD 3 x 5: 15 mm^2
Additional Features	Over Current Protection Thermal Shutdown Enable	Over Current Protection Thermal Shutdown Enable	Over Current Protection	Over Current Protection Thermal Shutdown Enable Soft Start
Operating Temperature Range (C)	-40 to 125	-40 to 125 -40 to 85	-40 to 125	-40 to 125

Figure 29. Selection Table for Low-Noise High-PSRR and Low-Iq LDOs

As a result of the tabular comparison as shown in Figure 29, the TPS71733 was selected as the high-PSRR LDO. The main criteria for selection was the 6.5-V maximum input-voltage capability of the TPS71733 with an absolute maximum rating of 7 V, availability in a space saving 1.5 × 1.5 mm^2 WSON-6 package, and outstanding 67-dB PSRR at 100 kHz. This specification holds even true for very small VIN – VOUT difference voltages of 0.25 V as highlighted in Figure 30, which is valid over the full operating temperature range T_J = –40°C to 125°C.

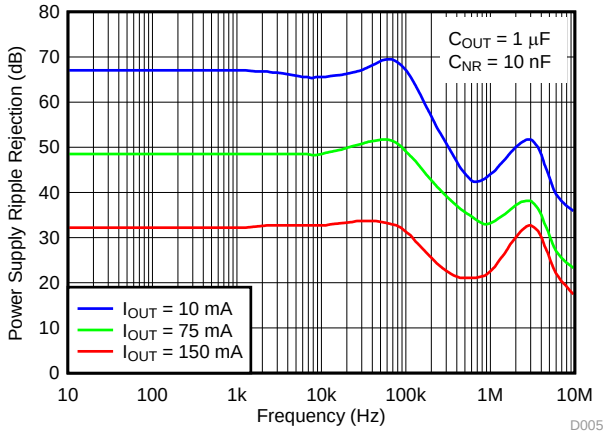


Figure 30. TPS71733 — PSRR versus Frequency at VIN – VOUT = 0.25 V

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1.0-µF low-equivalent series resistance (ESR) capacitor across the input supply near the regulator. This capacitor will counteract reactive input sources and improve transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1-µF input capacitor may be necessary to ensure stability. The TPS71733 is designed to be stable with standard ceramic capacitors of values 1.0 µF or larger used as output capacitors. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be <1.0 Ω.

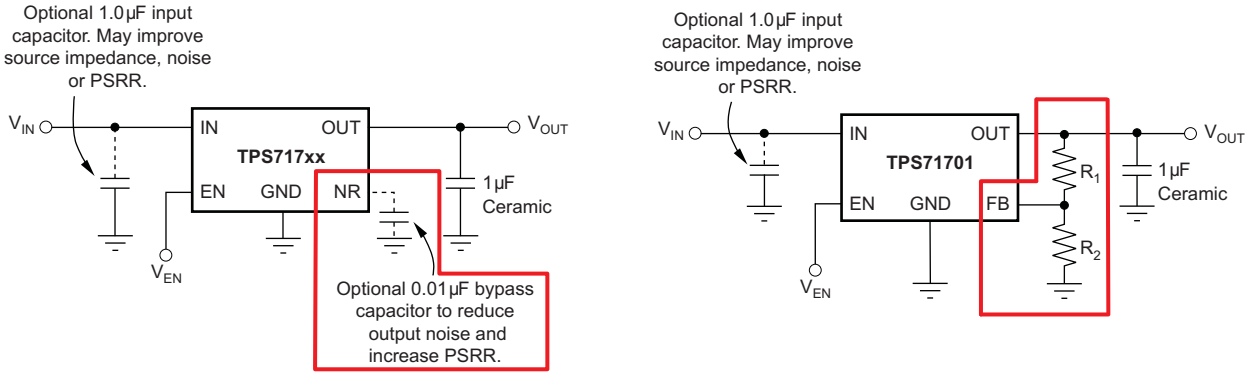


Figure 31. TPS717xx — Typical Application Circuit: Fixed Output Voltage Version vs. Adjustable Output-Voltage Version

The TPS71733 provides a fixed 3.3-V output and offers a noise-reduction (NR) pin. The TPS71733 contrasts with the adjustable version of the TPS717xx family, which does not have this NR pin. The adjustable version of the TPS717xx family provides a feedback (FB) pin to connect the output voltage resistor divider for setting the desired output voltage — as outlined in Figure 31.

The NR pin allows the connection of an optional external noise-reduction capacitor to bypass noise generated by the internal bandgap reference and to improve PSRR while an internal quick-start circuit fast-charges this capacitor, as shown in Figure 32.

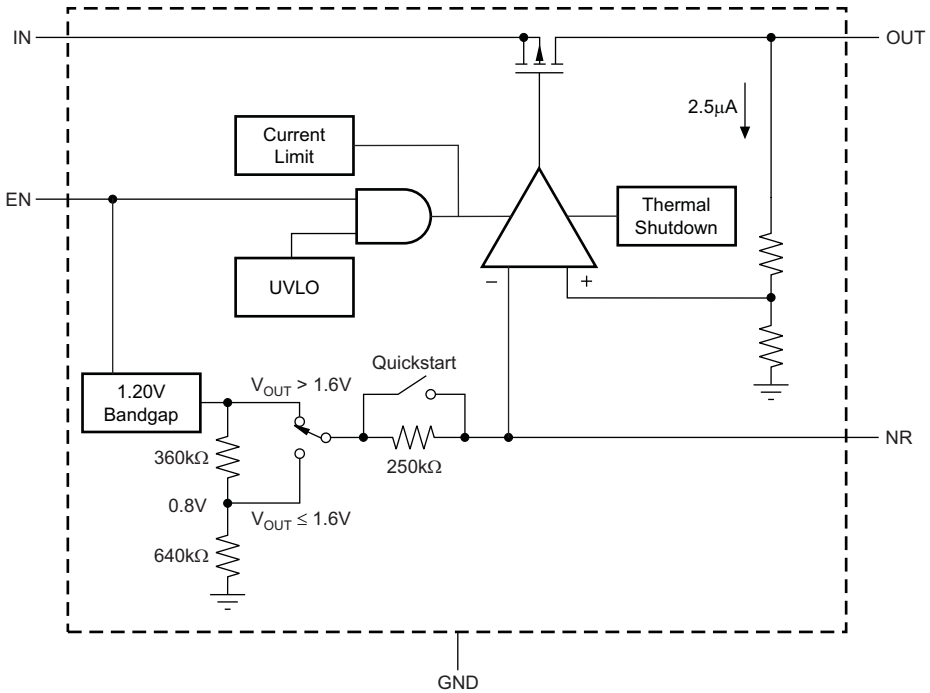


Figure 32. TPS71733 — Functional Block Diagram

An increase of the noise-reduction capacitor influences the output-noise density more than the output capacitor, as shown in Figure 33.

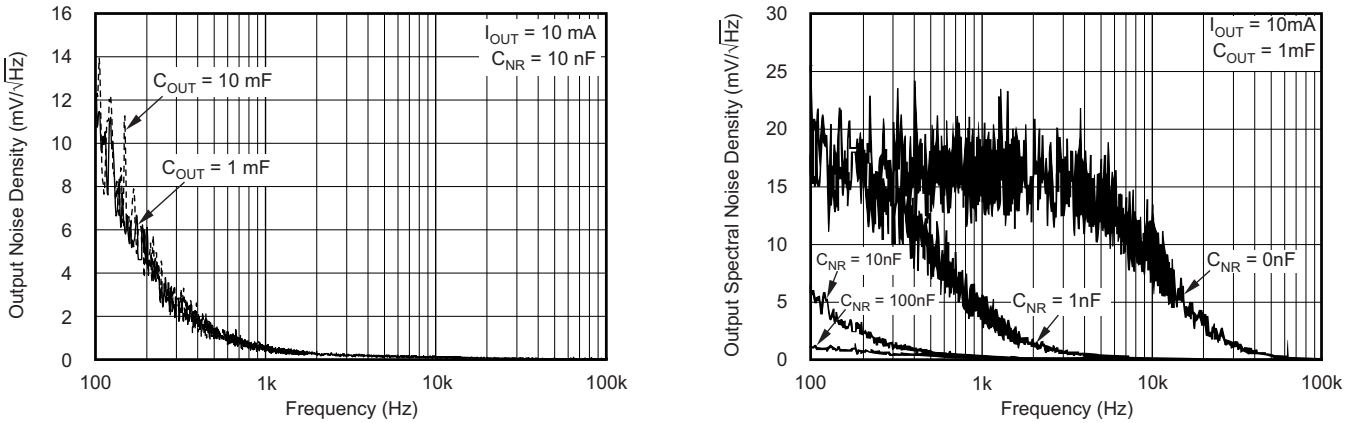


Figure 33. TPS71733 — Effect of Noise Reduction and Output Capacitor on Output-Noise Density

The device uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 3% overall load, line, process, and temperature variations over the full-operating temperature range. The TPS71733DSE, which is the device in the smallest package (1.5 × 1.5 mm WSON), is fully specified for an operating temperature range from T_J = –40°C to 125°C.

In contrast to the TPS71733, the TPS71533, as shown in Figure 34, has been selected as the best choice when the lowest Iq is the number one priority.

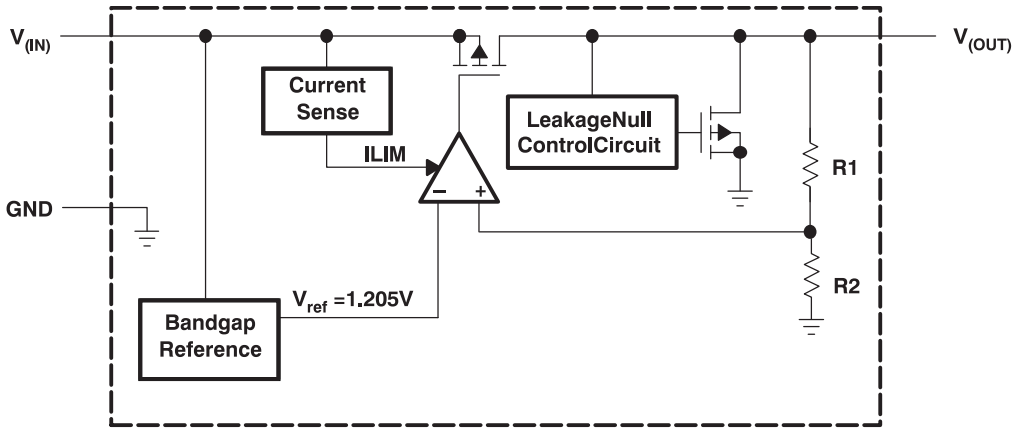


Figure 34. TPS71533 — Functional Block Diagram

The use of the TPS71533 extends the maximum output current on the isolated side from 1.69 mA (when both sides use TPS71733) to 1.88 mA (when both sides use TPS71533). The increase to 1.88 mA is because the Iq of the TPS71733 has a typical 3.2 µA and a maximum of 5.8 µA over input voltage, load current, and operating temperature range. The influence of temperature and load current on the value of absolute Iq-current increase for the TPS71533 is more-or-less negligible compared to the TPS71733.

The TPS71533 offers a maximum recommended input voltage of 24 V and is specified for the same temperature range as the TPS71733. However, the TPS71533 comes in a larger package — 4.2 mm^2 versus 2.25 mm^2 for the TPS71733.

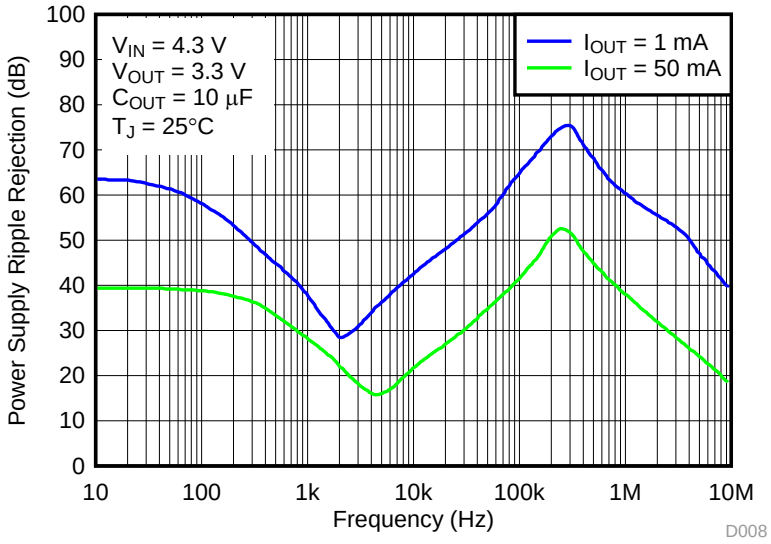


Figure 35. TPS71533 — PSRR versus Frequency at VIN – VOUT = 1 V

The PSRR specification of the TPS71533, as shown in Figure 35 is 60 dB, which is almost as good as the 67 dB of the TPS71733. However, the specifications in the data sheets for TPS71733 and TPS71533 show that the PSRR spec of the TPS71533 is given for a headroom voltage of 1 V, while the PSRR spec for the TPS71733 is for headroom voltage of 250 mV, as shown in Figure 30.

The minimum input and output capacitor requirements for the TPS71533 are similar to the requirements of the TPS71733. For the input bypass capacitor, the recommended capacitance is at least 47 nF. The output must be bypassed with at least 470 nF. An X5R or X7R type of multi-layer ceramic capacitor is recommended for both devices. The capacitors should be placed as close as possible to the LDO.

5.6.2 Post-Regulator LDOs —Circuit Implementation

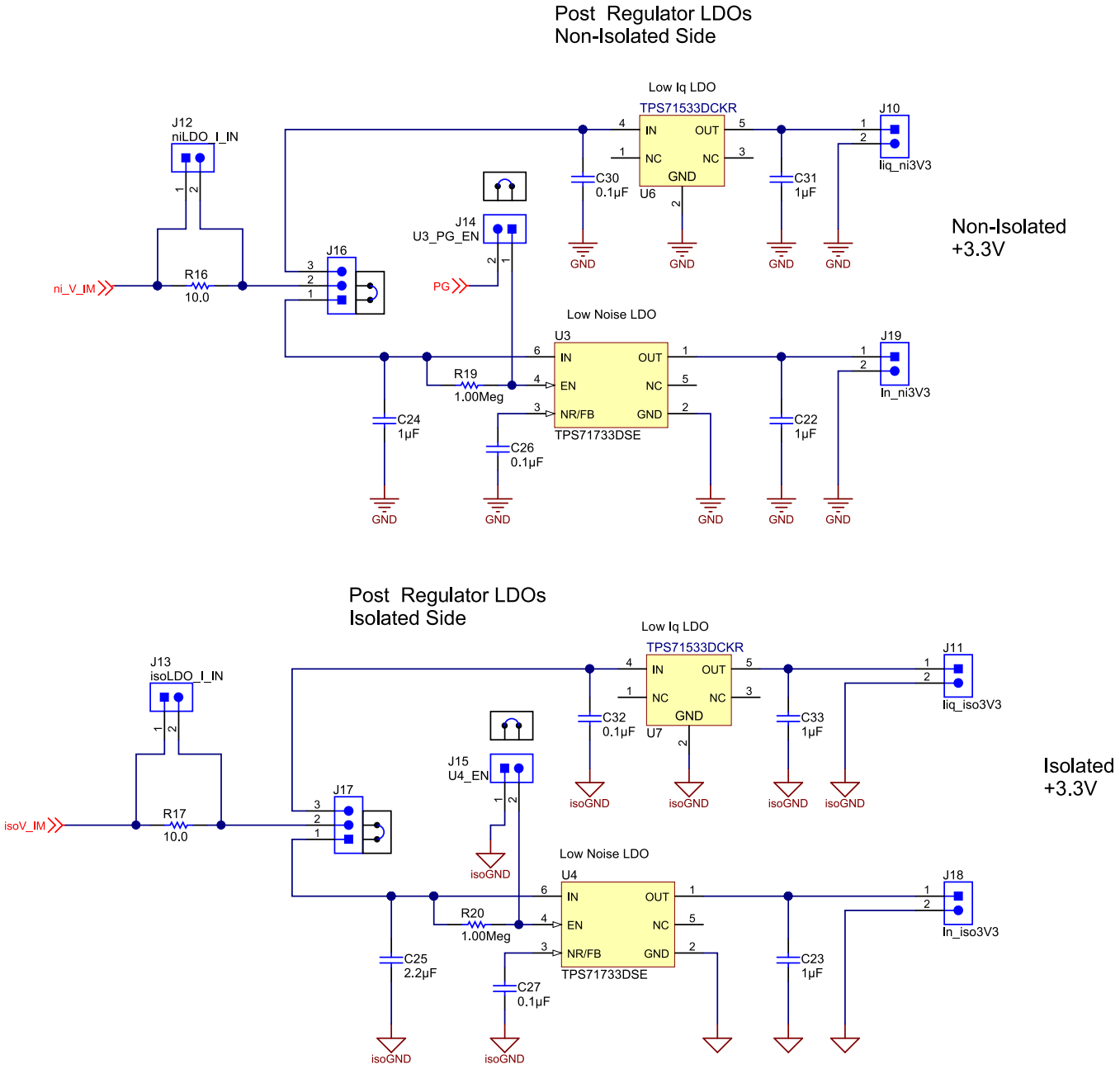


Figure 36. Post-Regulator LDOs — Circuit Implementation

The implementation for the post-regulator LDOs on the nonisolated and on the isolated side is almost identical. The LDOs on both sides provide a regulated 3.3-V rail. For each side, the user can select by jumper setting (J16, J17) independently to use either the low-Iq LDO (U6, U7) or the low-noise, high-PSRR LDO (U3, U4). J14 and J15 provide different options for controlling the EN pin (pin 4) of the low-noise, high-PSRR LDOs on each side.

While it is possible to control U3 (nonisolated side) directly by the power-good signal of the high voltage LDO (U1), this option is not available on the isolated side. The reason that the option is unavailable is that the control signal for the LDO (U4) on the isolated side needs to be referenced to a different ground (isoGND), but not to the nonisolated ground (GND), as for U3.

To provide the user an easy way to measure the current consumption of each rail in a noninvasive manner, current-sense resistors (R16 and R17) have been implemented in front of J16 and J17. Current measurements can be done by a voltmeter connected to the respective header J12 or J13, where 10 mV represents 1 mA of current.

The different jumper settings are listed in Figure 37.

All LDOs have been bypassed on the input and output with at least the minimum recommended capacitance values. Because the TPS71733 has been especially selected for best low-noise and highest-PSRR performance, the TPS71733 data sheet recommendation was followed to use a larger input capacitor to improve noise and ripple rejection further.

For the same reason to improve noise and ripple rejection, U3 and U4 have been also equipped with 100-nF, noise-reduction capacitors (C26 and C27). Figure 33 shows a major contribution of these capacitors for lowest output noise density. To ease the control of the ENABLE-pin of the TPS71733, the pins have been pulled-up by 1-MΩ resistors to the input voltage of the respective LDO.

Non-Isolated Side			
LDO Selection			
J16	Jumper on pins	1-2	Low Noise, High PSRR LDO **U3**
		2-3	Low Iq LDO **U6**
U3 Low Noise, High PSRR LDO ENABLE			
J14	☑		**U3 controlled by POWER GOOD of** High Voltage LDO **U1**; enabled when logic HIGH
			U3 always ON, can be controlled by externally provided open-drain signal **referenced to GND**
Isolated Side			
LDO Selection			
J17	Jumper on pins	1-2	Low Noise, High PSRR LDO **U4**
		2-3	Low Iq LDO **U7**
U4 Low Noise, High PSRR LDO ENABLE			
J15	☑		**U4 always OFF**
			U4 always ON, can be controlled by externally provided open-drain signal **referenced to isoGND**

(1) ☑ Jumper on respective header populated

Figure 37. Jumper Settings for LDO Selection and LDO ENABLE Options

5.6.2.1 Layout Recommendation

The data sheet TPS71533 and TPS71733 guidelines of placing the input and output bypass capacitors close to the respective pins of the devices have been followed (see Figure 38).

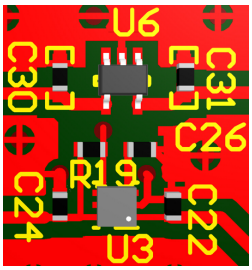


Figure 38. Post-Regulator LDOs — Component Placement

5.7 Isolated DC/DC Converter

The isolated DC/DC converter circuit block uses the nonisolated intermediate 4.5 V-rail generated by the high voltage LDO and filtered by the ripple filter to generate an isolated intermediate voltage, which is finally post-regulated by the respective 3.3-V LDO(s) on the isolated side.

There are two reasons why the efficiency gains in significance:

1. The main output current of the complete design is expected to be drawn on the isolated 3.3-V rail (1.69 mA / 1.88 mA on the isolated 3.3 V versus 0.39 mA on the non-isolated 3.3 V (see the nonisolated and isolated LDO output sections of Table 1).
2. In respect of the very limited total input current budget for the complete design (3.3 mA as given in the loop input section of Table 1 and Section 3.1).

5.7.1 Dedicated Design Challenges in this Application

Although there are countless converter ICs, transformers, MOSFETs, diodes, and different power topologies available, their usage is very limited for the specific case of this design.

All the different power solutions can cover output-power ranges from some hundreds of mW up to some kW in theory. However, the extreme low-power level of this design requires a new and more focused approach. The specific challenges for this design have already been expressed in Section 3.1.

Challenges for the isolated power converter are as follows.

- The converter requires high efficiency.
- Extreme low-output current (approximately 2 mA) and power level (approximately 2 mA × 4 V = 8 mW) of the DC/DC converter.
- 80 µW of losses represent approximately a 1% efficiency loss.
  - An assumed quiescent current of the DC/DC converter of 100 µA, drawn from the 4.5V intermediate voltage, results in 450 µW of losses, representing approximately 5.5% less of efficiency.
  - Reverse current of Schottky diodes on the secondary side can easily go up to 100 or more µA at 85°C, which accounts for another 5 to 6% loss at this voltage level.
- The frequency-dependent switching losses dominate, rising up proportionally with switching frequency.
- Related to the output current of the DC/DC converter, approximately 2 mA, the conduction losses (I^2R) are (even at 10-Ω resistance) almost negligible (2 mA × 2 mA × 10 Ω = 40 µW). However, these losses rise with the square of the RMS-current.
- The transformer size should be minimized to fit even in a real transmitter application.
- The transformer saturation current and the V-µs limits must be kept.
- The magnetizing current of the transformer has the same order of magnitude as the load current. Therefore, the magnetizing current of the transformer should be considered more carefully than in higher power designs.
- Constant switching frequency over all load conditions to minimize negative impact on the accuracy and noise performance of the transmitter.

Taking all these challenges into account, the final solution is a compromise between size and efficiency. Therefore, simply assuming that ultra-small output power automatically enables ultra-small transformers does not work.

5.7.2 Isolated DC/DC Converter — Selection of Control Approach

Making a decision on the control approach is the first decision to make. The control approach decision influences not only the design of the isolated DC/DC converter, but also the complete system design. The regulated control approach, as shown in Figure 39, appears at first as the more attractive solution.

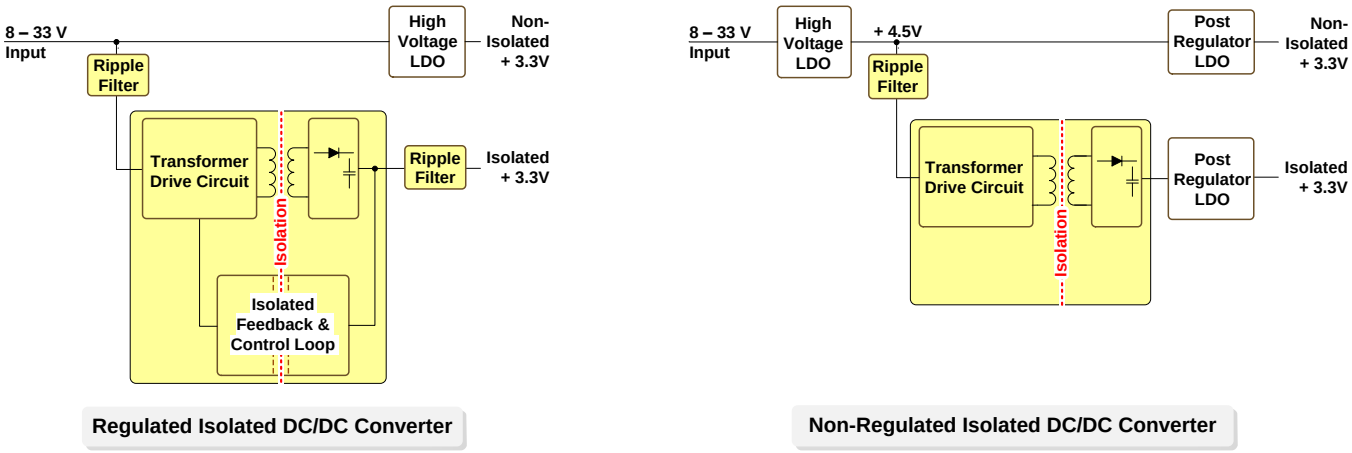


Figure 39. Isolated DC/DC Converter: Regulated versus Nonregulated Control Approach

However, an in-depth comparison, as shown in Figure 40, shows more advantages for the nonregulated approach.

Nonregulated isolated DC/DC conversion in this design means that a DC input voltage is simply converted into an isolated DC output voltage without any control loop. The simplest conversion approach is to use a fixed and optimized duty cycle to drive a transformer. The resulting output voltage is then mainly a function of the DC input voltage, the transformer winding ratios, and the load- and temperature-dependent voltage losses in the switches (MOSFETs), rectifiers, and copper resistance of the windings. Especially for the low-current ranges applicable for this design, the load-dependent losses can be neglected.

A detailed listing of the two approaches is provided in Figure 40 and in the text following.

	Isolated DC/DC Converter	
	Regulated	Non-Regulated
Needed Input Voltage Operating Range VIN (V)	8 to 33	4.3 to 4.46 (typ) to 4.62
Maximum Peak Input Voltage During Surge (V)	60	4.62
Number of High Voltage LDO (60V) Needed?	1	1
Output Voltage (V) @ IOUT = 2 mA; 25℃	3.3 ±3 %	4.18 ±4.5 %
Output Voltage (V) @ IOUT = 10 µA to 2 mA; -40 to 85 °C	3.3 ± 5 … 10 %	4.38 to 5.34 (10 µA) 3.77 to 4.58 (2 mA)
Isolated Feedback & Control Loop Needed?	YES	—
Variable Control Parameter	Switching Frequency, Duty Cycle or Peak Current	—
Approximated Input Current	POUT / (η x VIN)	Constant
Incremental Input Impedance	Negative	Positive
Control Loop - Design for Stability Needed?	YES	—
Expected Input Current Ripple	High, Magintude Depends on VIN & IOUT	Lower, Magnitude Depends on IOUT only
EMI Signature (Conducted EMI)	Depends on VIN & IOUT	Depends on IOUT only
Input Ripple Filter Needed?	YES	YES, Scaled Down
Influence of Input Ripple Filter on Control Loop Stability?	YES	—
Output Ripple Filter Needed?	YES	—
Number of Post Regulator LDOs Needed	0	2

Figure 40. Isolated DC/DC — Selection of Control Approach

The clear benefits of the nonregulated approach start with the fixed and low value input voltage, which is a constant 4.5 V under all operating conditions, even under surge pulses applied to the loop power input (J1) of the complete design.

A regulated DC/DC converter, in contrast, would need to withstand voltages up to approximately 60 V. 60 V is the maximum to-be-expected clamping voltage of the TVS diode D3 (plus some additional safety margin, as explained in Section 5.1.1.1). Even under normal operation, the input voltage of the regulated DC/DC has a very wide range and (most importantly) varies with the loop current due to the current-dependent voltage drop across the load resistance RLOAD in the loop receiver, as outlined in Section 3.

To keep the output voltage regulated at 3.3 V, the regulated DC/DC converter needs to change the duty cycle, switching frequency, or peak current to accommodate large changes in input voltage. Those changes negatively impact the efficiency. Additionally, those changes result in large changes of the input current, the ripple content of the input current, and the resulting conducted EMI signature. As with any regulated DC/DC converter (even nonisolated ones), the input characteristic of the circuit appears as a negative-incremental impedance.

The negative impedance can be explained by the simple assumption, that the input power of a DC/DC converter equals the output power of the converter (neglecting efficiency for the sake of simplicity). Therefore, it is also part of the assumption that the input current of a regulated DC/DC converter needs to be inversely proportional to the input voltage for the same (constant) amount of output power and input power.

This negative impedance may counteract with the proper function of the 4- to 20-mA loop DAC which controls the current flowing in the loop. An increased loop current by the DAC leads to a larger voltage drop across the RLOAD. The larger voltage drop results in less voltage on the loop-input terminals (J1) and less input voltage of the hypothetically-used, regulated-isolated DC/DC converter. Due to the reduced input voltage, the regulated DC/DC converter needs to increase its input current to maintain the same amount of output power. The increased input current also increases the loop current, requiring the loop DAC to react on the loop-current increase as well.

Another concern caused by the negative-input impedance of the regulated DC/DC converter is the interaction with the input ripple filter of the converter. This interaction is another potential source of instability.

Additional effort is also needed to establish the output voltage feedback loop needed for a regulated DC/DC converter in an isolated way.

The output voltage of a nonregulated, isolated DC/DC converter in contrast varies with the input voltage of the converter, temperature changes, and load changes. These variations can be easily compensated by using low-input voltage LDOs to generate a precisely regulated, nonisolated (as well as an isolated) fixed 3.3-V rail. These LDOs are available as very low-noise and high-PSRR versions, making a ripple filter on the output redundant.

The advantages of the nonregulated approach can be found in the simplicity of its implementation. No control loop is required. Therefore, there is no need for an additional isolation barrier to close the feedback loop. The nonregulated converter works always with a fixed duty cycle and switching frequency, which addresses an optimal operating point and ensures a stable EMI signature independent of the transmitter's input voltage.

In conjunction with the constant input voltage of the converter (typically 4.46 V), the resulting magnetizing current in the transformer will stay the same, independently of the widely changing 8 to 33 V at the systems loop-input terminals.

Under an assumption of a constant output power need, the input power of the converter can also be assumed to be constant for the constant input voltage applied to the converter. In case of small changes of the DC/DC converter's input-voltage, the incremental change of input current goes into the same direction, resulting in a positive incremental input impedance for the nonregulated, isolated approach.

As a result of the control approach comparison, the nonregulated, isolated DC/DC was chosen as the preferred control approach. The nonregulated, isolated DC/DC requires using one high input voltage LDO as pre-regulator to provide an intermediate, nonisolated 4.5-V rail and two post-regulator LDOs to generate the regulated 3.3 V on the nonisolated side and on the isolated side.

The post-regulator LDO on the nonisolated side uses the 4.5-V intermediate rail as input, while the LDO on the isolated side is powered by the nonregulated output voltage of the DC/DC converter, which may vary from 3.77- to 5.34-V over load, line, and temperature.

5.7.3 Isolated DC/DC Converter — Selection of Power Topology

Besides the control approach decision, the best fitting topology needs to be selected for the isolated power stage of the DC/DC converter. The selection process considered not only the features of the different topologies, but also the available DC/DC converter ICs for the respective topology to be selected.

Since the best efficiency can be expected for the so called *double-ended* topologies, as shown in Figure 41, driving the core of the transformer actively in two opposite directions, all the single-ended topologies have been excluded from the beginning. Likewise, the advanced double-ended topologies such as the full bridge were not considered due to the increased complexity level and the need to drive even four switches, leading to higher switching losses.

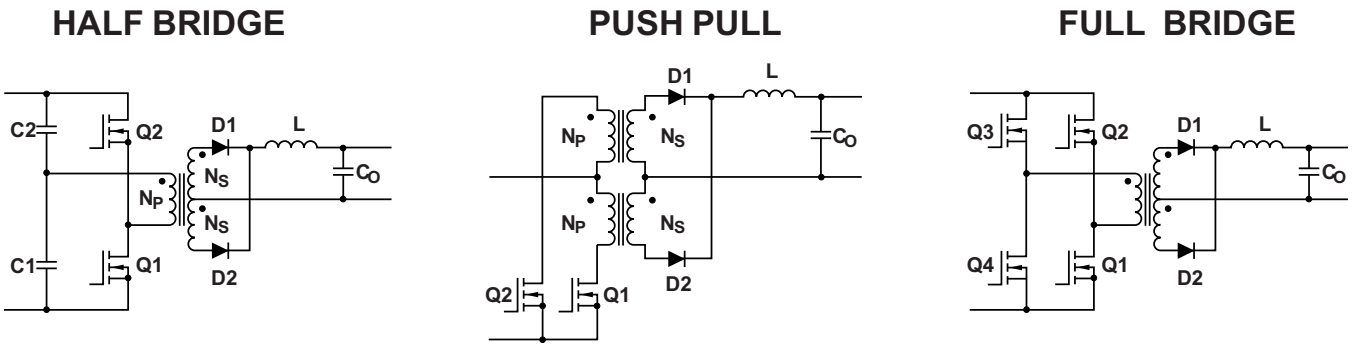


Figure 41. Basic Double-Ended Topologies

Therefore, only the push-pull and the half bridge have been preselected (for a more detailed investigation and comparison, see Figure 45).

Push-pull and half bridge topologies are topologies derived from the forward converter. Topologies derived from the forward converter involve energy transfer from the primary to the secondary side, which takes place during the ON-time of the switch without any energy storage used for the energy transfer. These topologies derived from the forward converter contrast to the operation of a flyback, which builds up magnetic energy during the ON-time of the primary side switch, stores the energy in the air gap of the core, and releases the energy to the secondary during the OFF-time.

Because the special version of the push-pull and half-bridge converter operating the primary side switches with 50% duty cycle have a continuous total input current flow, the energy transfer will be continuous as well and the continuous flow will be applicable to the secondary side current. Therefore, the storage inductors used on the secondary side (labeled *L* in Figure 41) are not needed for converters running with a 50% duty cycle for each of the primary side switches. Running with a 50% duty cycle is commonly used in low-power, isolated, nonregulated DC/DC converters like the ones based on the SN6501, which is optimized for an output power efficiency in the range of tens of milliwatts up to 1 W, as shown in Figure 42.

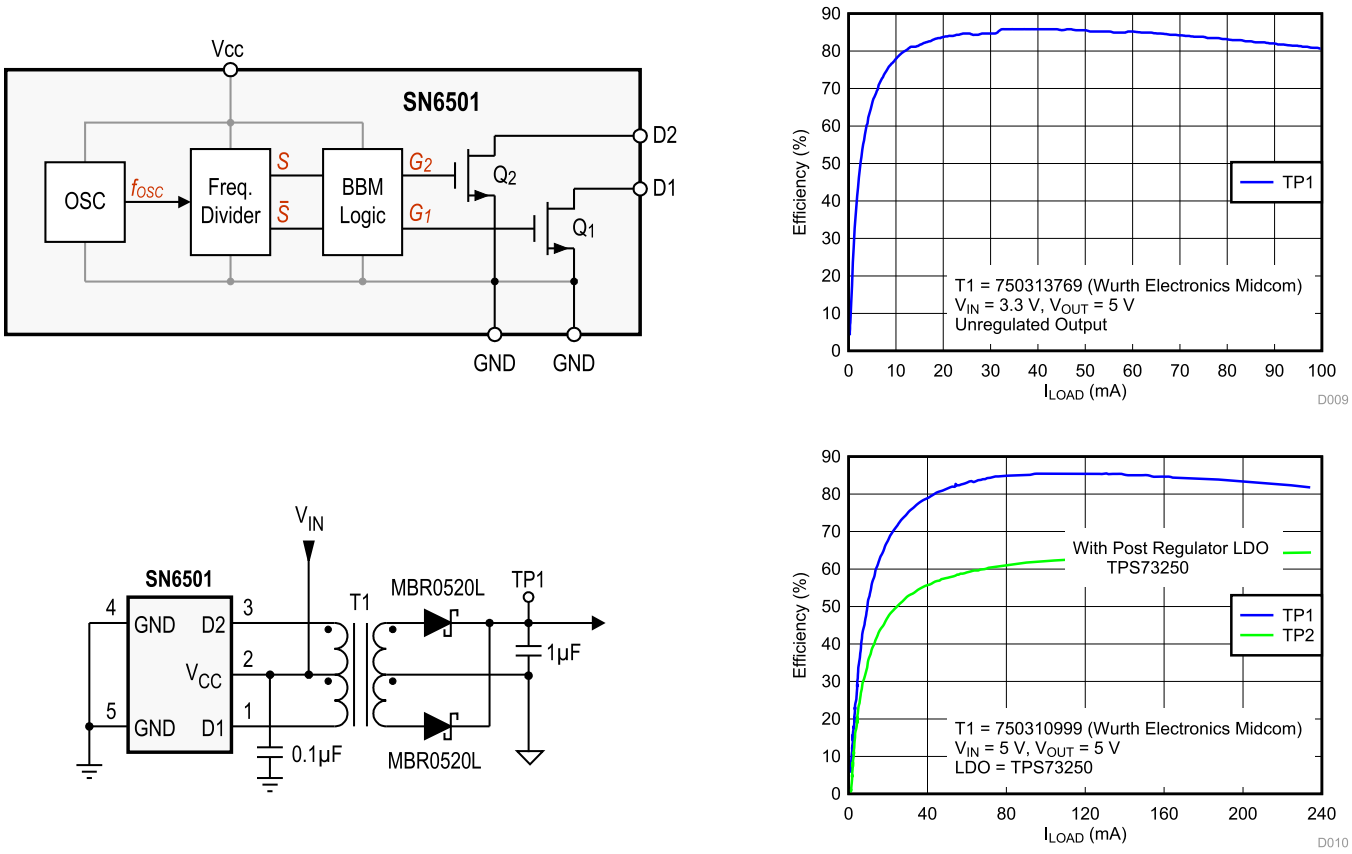


Figure 42. SN6501 — Block Diagram, Schematic, and Efficiency

Although the omission of a storage inductor on the secondary side simplifies the design in general, the greater design challenge is the power transformer itself.

While the symbol in schematics looks as simple as the ideal transformer, as shown in Figure 43, a simplified model of a real transformer shows additional components coming basically *for free* with each real transformer.

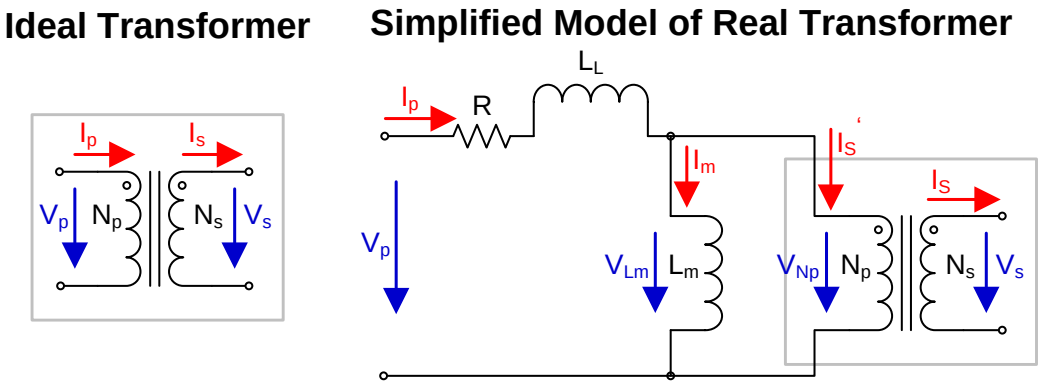


Figure 43. Ideal Transformer versus Simplified Model of Real Transformer

The basic equations describing an ideal transformer are simple, well known, and understood. In the simplest case, an ideal transformer consists only of one primary and one secondary winding. Each winding has a respective number of turns and is linked by a magnetic core together. As a result, the turns ratio (n) can be calculated.

$$n = \frac{N_p}{N_s}$$

where

- n is the primary-to-secondary turns ratio
- N_p is the number of primary turns
- N_s is the number of secondary turns (8)

The turns ratio does not only define the relation between the number of turns of the two windings, but also defines the relation of the related voltages and currents.

$$n = \frac{N_p}{N_s} = \frac{V_p}{V_s} = \frac{I_s}{I_p}$$

where

- V_p is the voltage across the primary winding
- V_s is the voltage across the secondary winding
- I_p is the current through the primary winding
- I_s is the current through the secondary winding (9)

This can be rearranged to get the most important relations.

$$\frac{V_p}{V_s} = \frac{N_p}{N_s} = n \quad (10)$$

The ratio of the voltages on both sides equals the ratio of the number of turns of the respective windings.

$$\frac{I_p}{I_s} = \frac{N_s}{N_p} = \frac{1}{n} \quad (11)$$

The ratio of the currents on both sides equals the reverse ratio of the number of turns of the respective windings.

The normal use case of a transformer assumes that a voltage V_p is applied to the primary side and appears multiplied by 1/n on the secondary side as the voltage V_s.

$$V_s = \frac{V_p}{n} \quad (12)$$

The current I_s drawn by a load on the secondary side appears multiplied by 1/n on the primary side as the current I_S' , which is called the *reflected current from the secondary*.

$$I_s' = \frac{I_s}{n} \quad (13)$$

Therefore, the current through the primary winding of a real transformer is the sum of the reflected current from the secondary side and the current of the magnetizing inductance of the primary-side winding.

$$I_p = I_s' + I_m \quad (14)$$

It should be noted that Equation 8 for the calculation of the turns ratio n as used in this document is only one possible way to define the turns ratio. In some literature, the turns ratio is defined exactly the other way around as secondary-to-primary turns ratio.

NOTE: Equation 9 through Equation 13 are valid for the AC signals and an ideal transformer only. This validity corresponds with the common knowledge that a transformer will not work with a DC at all. The questions regarding the borderline between AC and DC forces a more detailed look to (at the least) a simplified model of a real transformer.

The ideal transformer can thoroughly explain the ratio between voltages, currents, and number of turns on the primary and secondary side. However, the ideal transformer is missing the explanation of the inductive behavior which needs to be expected from practical experience, whenever a number of turns are wound, especially on a magnetic core.

An explanation of the inductive behavior comes with the simplified model of the real transformer, which takes the described ideal transformer and adds the magnetizing inductance L_m.

Since the design of a real transformer aims at keeping the other added components like the parasitic leakage inductance L_L orders of magnitude lower (compared to L_m), the effect of L_L can be neglected for the purpose of this discussion and for the sake of simplicity. The effect of the winding resistance R shown in series to L_L on the primary side can also be neglected for the purpose of this discussion.

The simplified model of the real transformer shows the magnetizing inductance L_m connected in parallel to the primary winding of the ideal transformer block. In this configuration, L_m represents the inductive properties of the primary winding wound on a magnetic core of specific dimensions and with specific magnetic properties. L_m can be calculated according to Equation 15 or Equation 17 and can be measured on the primary winding of the real transformer if the secondary winding is disconnected.

$$L_m = \frac{\mu \times A_C \times N_p^2}{l_C} \tag{15}$$

with

$$\mu = \mu_0 \times \mu_r \tag{16}$$

Core manufacturers often combine all the magnetics and mechanical size-related properties into a single term called A_L value or *inductance factor* to simplify the calculation to Equation 17.

$$L_m = A_L \times N_p^2 \tag{17}$$

A_L needs to be

$$A_L = \frac{\mu \times A_C}{l_C} \tag{18}$$

Due to Equation 15 and Equation 18 where

- L_m = magnetizing inductance
- μ = core permeability
- μ_0 = permeability of free space = $4\pi \times 10^{-7}$ H/m
- μ_r = relative permeability of core material
- A_C = core cross section
- l_C = core magnetic path length
- A_L = inductance factor or A_L–value (19)

The core links the primary and secondary winding together, and the magnetizing inductance models the magnetization of the core *as a real, physical inductor*. Unfortunately, the magnetizing inductance shows undesirable characteristics of inductors — saturation and hysteresis — as well (Fundamentals of Power Electronics). Both characteristics are represented by the hysteresis curve of the magnetizing inductance. The hysteresis causes hysteretic losses, while the saturation places a limit for the maximum current flow through the inductor or for the applied product of volt-seconds (V-s) to that inductor, respectively.

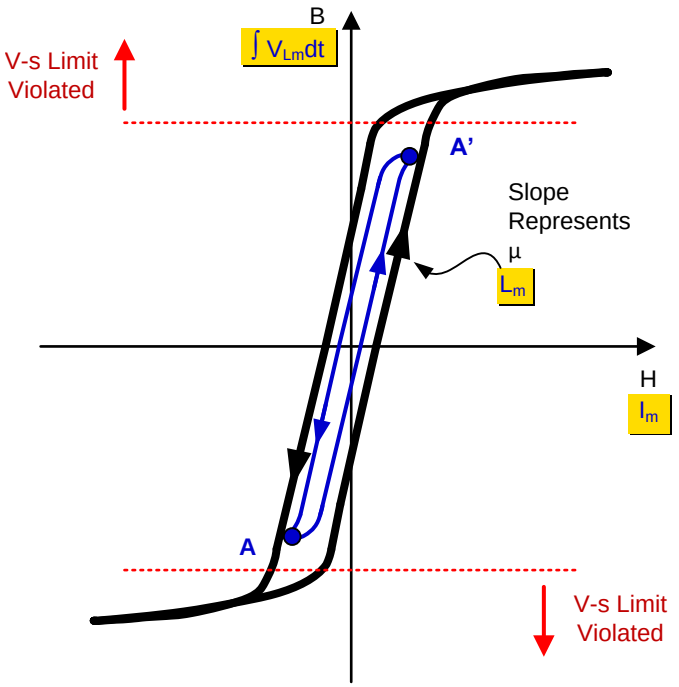


Figure 44. Hysteresis Curve of Ferrite and of Specific Inductor

The black hysteresis curve in Figure 44 is also known as the B-H curve and is used to characterize the core material itself. The slope of the curve represents the permeability, μ in this case. Applying the "Transformation of Axes" as described in the Section 1 of Magnetics Design Handbook, the vertical axis can also be used for the V-s applied to a specific inductor when the horizontal axis is used for the current flowing through this specific inductor. This specific inductor is in this case the magnetizing inductance L_m of the transformer and is then represented by the slope of the hysteresis curve as well. The horizontal axis is then specifically showing the magnetizing current I_m.

The blue curve is representing the so-called *minor loop* that is the practical range of excursion used in real applications.

If the applied V-s product (or the flux-density B) violates a certain limit (the red dotted lines), then the slope changes from a linear to a nonlinear behavior. Any further increase in the applied V-s will cause a drastic increase of the magnetizing current. The inductive characteristic diminishes, leaving finally, only the copper resistance of the winding. A drastic increase of the magnetizing current also causes shorting of the primary side of the ideal transformer block used in the simplified model of the real transformer. Any voltage applied to the magnetizing inductance can cause such an effect, no matter how small. The question is just how long the voltage is applied. This information explains why transformers can work for AC signals only, but not for DC signals.

Even AC signals can cause this effect if the AC signals violate the V-s limit of the specific inductor. Such a violation can happen, if the magnitude of the voltage is too large or the time the voltage is applied is too long (for example, when operated at low frequency). The violation can also happen if the AC signal has a DC voltage superimposed. To avoid this situation, the V-s applied to an inductor (or to the flux in the core) needs to be balanced. Therefore, any positive V-s excursion in one direction needs to be cancelled out by exactly the same excursion in the opposite direction. Otherwise, the so-called *flux walking* can happen. Flux walking can drive the core earlier or later into saturation.

The high efficiency goal for the design of the isolated DC/DC includes the need of a low switching frequency to minimize the switching losses. With low switching frequency, any voltage on the primary winding of the transformer is applied for a longer time (compared to using a higher switching frequency). Therefore, the power topology applying the lower voltage to the primary winding of the transformer — the half-bridge topology — was selected. Details can be found in Figure 45.

The applied voltage for the half bridge is exactly one half of the voltage, which would be applied using a push-pull topology. Furthermore, the half bridge is providing another simple measure to avoid flux imbalance and flux walking, simply by the use of a DC-blocking capacitor. Additionally, the half bridge eases the transformer design. On the primary side, there is only a standard single winding needed versus a tapped winding as needed with a push-pull transformer. The single winding of the half bridge is used 100% of the time. In contrast, each one of the two halves of the primary winding of the push-pull is used only 50% of the time.

	Isolated DC/DC Converter	
	Push-Pull	**Half-Bridge**
Voltage Stress of Primary Side Switches	2 x VIN	VIN
Voltage Across Primary Winding	VIN	VIN / 2
Relative V-µs (Referred to Push-Pull, Same Switching Frequency, Same ON-Time)	1	0.5
Core Utilization	Bi-Directional (Double-Ended)	Bi-Directional (Double-Ended)
Structure of Primary Winding	Center Tapped Winding	Standard Single Winding
Structure of Secondary Winding	Usually Center Tapped Winding	Standard Single Winding
Copper Utilization	50%	100%
Avoidance of Flux Imbalance	Positive Temperature Coefficient of MOSFET's RDSon	Positive Temperature Coefficient of MOSFET's RDSon, DC Blocking capacitor

Figure 45. Isolated DC/DC — Selection of Power Topology

5.7.4 Isolated DC/DC Converter — Selection of Transformer Driver

Special care was taken for the selection of the best-suited device for driving the power transformer.

Key Specifications for Selecting a Transformer Driver

- High efficiency
  - *Low-switching frequency* is a prerequisite to ensure lowest switching losses. However, the disadvantage comes when avoiding violation of the V-s limit of the transformer, while at the same time, trying to achieve the smallest solution size. This disadvantage is related to the inductance values of the transformer, which will rise with a low-switching frequency, which can directly be translated into larger physical transformer size. The same size relation applies to the capacitors needed on the input and output of the isolated power stage. However, the size impact for the capacitors is not as severe as the size impact for the transformer. There is a cost impact when trying to obtain the same physically-sized capacitor with a much larger capacitor value. A tradeoff between efficiency and solution size needs to be found.
  - *Low quiescent current (Iq)*: Due to the low output power level, the current consumption of the converter itself has a major influence on the efficiency.
- *High integration level*: needed for smallest size solution. The integration of the switches (FETs) is highly desirable.
- *Fixed switching frequency*: preferable from a noise and system accuracy perspective. The standard approach of operating the DC/DC converter in a PFM-, SKIP- or BURST-mode to achieve highest efficiency at the needed low output power level (from 5 to 10 mW) is not desirable. The result would be a mix of different frequencies, which is directly opposite of the goal of best-system accuracy performance.

After taking into account all the specifications need for a device driving the power transformer, the TPS60400 family, as shown in Figure 46, was selected.

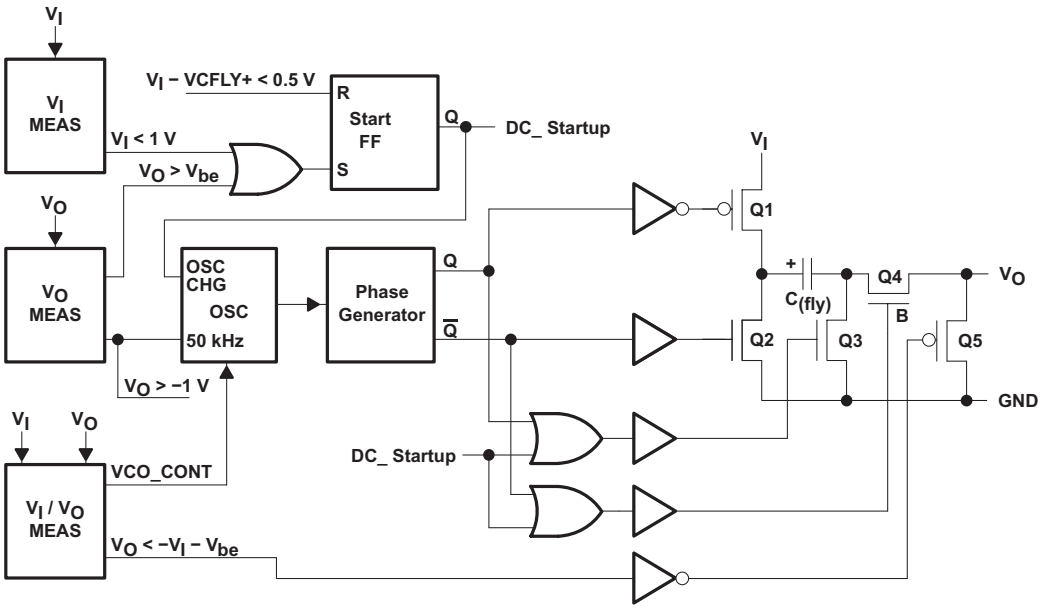


Figure 46. TPS60400 Family — Functional Block Diagram

The primary applicable and beneficial specifications of the TPS60400 device family can be summarized as follows:

- Input voltage range from 1.6 V to 5.5 V
- Small 5-pin SOT23 package
- Integrated switches (FETs)
- Internal fixed frequency oscillator (for TPS60401 to TPS60403)
- Multiple switching frequency versions, as shown in Figure 47
- Devices available with quiescent current down to 65 µA

	TPS60400	TPS60401	TPS60402	TPS60403
Switching Frequency (typ)	Variable switching frequency 50 kHz–250 kHz	20 kHz	50 kHz	250kHz
Quiescent Current (typ)	125 µA	65 µA	120 µA	425 µA

Figure 47. TPS60400 Family — Device Versions

Out of the TPS60400 family, the TPS60402 was selected. With a 50-kHz switching frequency, the TPS60402 offers a good trade-off between efficiency and solution size.

5.7.5 Isolated DC/DC Converter — Further Device Selection and Circuit Implementation

Figure 48 illustrates how the internal circuitry of U2 (TPS60402) is used to drive a half-bridge transformer.

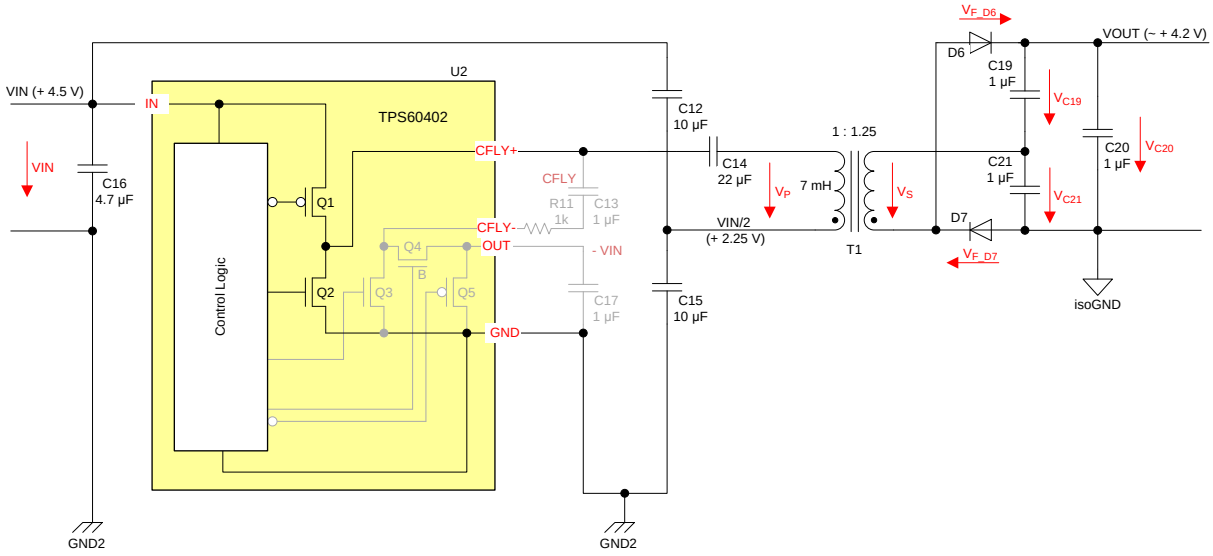


Figure 48. Simplified Schematic of Isolated DC/DC Converter

The switches (MOSFETs) Q1 and Q2 of the TPS60402 form one leg (the left leg) of the bridge. Q1 and Q2 drive the non-dot end of the transformer's T1 primary winding through the CFLY+ pin and the DC-current blocking capacitor C14 with a square-wave-like voltage. Both MOSFETs are switched ON alternately. Each MOSFET is ON for almost 50% of the period T. The basic operation of this circuitry can be divided into two main time intervals with identical length. The state of the switches, diodes, and the direction of the magnetic excursion in the core of the transformer during each of the intervals are described in Table 7.

Table 7. Half Bridge DC/DC Converter — State of Switches and Diodes During Each Time

TIME INTERVAL	Q1	Q2	Q3	Q4	VP	D6	D7	CORE DRIVE
1	**ON**	OFF	**ON**	OFF	**VIN – VIN/2**	OFF	**ON**	**A to A'**
2	Off	**ON**	OFF	**ON**	**– VIN/2**	**ON**	OFF	**A' to A**

The magnetic excursion refers to the blue line and blue dots A and A' highlighting the minor loop in Figure 44.

A small dead time between the two time intervals avoids cross conduction, respectively shoot-through of Q1 and Q2. The voltage level on the CFLY+ pin toggles between 0 V (GND2) and 4.5 V (VIN, which is the output voltage of the ripple filter).

Q3, Q4, CFLY (C13), and C17 are the remaining part of the inverting charge pump, which is the classical use case of the TPS60402. Q3, Q4, CFLY (C13), and C17 are not needed to drive the half bridge transformer, but are needed to satisfy the TPS60402 itself. The TPS60402 device expects a negative voltage on its OUT pin, requiring that the circuitry connected to the device is complete as in the typical application of the device. However, the capacitors have been minimized in value, resulting finally in an increased output voltage ripple on the OUT-pin of the device U2. This increased ripple is acceptable because this voltage is the negative voltage not used in the design at all.

R11 was connected in series to the flying capacitor C13, significantly reducing the inrush current and the continuous operating losses for the generation of the unused negative voltage. Waveforms of the charge pump's operation, simulated with TINA-TI are shown in Figure 49. The blue curve shows the CFLY+ pin of the TPS60402, internally containing the two MOSFET-switches as the left leg of the half bridge. The CFLY+ pin is toggling with a duty cycle of 50% and a frequency of 60.8 kHz between the input voltage VIN (4.5 V) and GND2 (0 V). The green curve shows the negative output voltage generated by the TPS60402, which is not further used by the complete circuitry of this design. The ripple voltage is only 320 μV_{p-p}. Similarly, the voltage across the flying capacitor (C13) shows a ripple of only 400 μV_{p-p}.

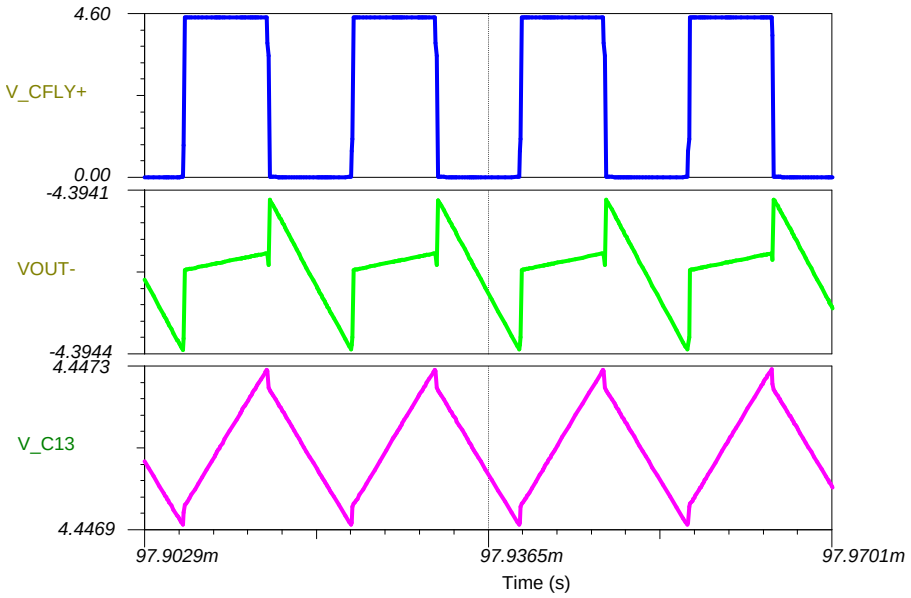


Figure 49. Charge Pump Operation

The other leg of the half bridge is formed by C12 and C15, a capacitive voltage divider keeping the dot end of the primary winding of the transformer at a constant voltage of 2.25 V (VIN / 2). The resulting voltage across the primary side of the transformer is, therefore, shown in Equation 20.

$$V_{p@1} = VIN - \frac{VIN}{2} = \frac{VIN}{2} = \frac{4.5\ V}{2} = 2.25\ V$$

$$V_{p@2} = -\frac{VIN}{2} = -\frac{4.5\ V}{2} = -2.25\ V$$

where

- $V_{p@1}$ is the voltage across the primary winding during time interval 1
- $V_{p@2}$ is the voltage across the primary winding during time interval 2

(20)

The voltages on the secondary side of the transformer can be calculated as shown in Equation 12.

$$V_{s@1} = \frac{V_{p@1}}{n}$$

$$V_{s@2} = \frac{V_{p@2}}{n}$$

where

- $V_{s@1}$ is the voltage across the secondary winding during time interval 1
- $V_{s@2}$ is the voltage across the secondary winding during time interval 2
- n is the primary-to-secondary turns ratio

(21)

Depending on the time interval and the resulting polarity on the primary winding, the voltage on the secondary winding shows up with positive and negative polarity also. Therefore, during each of the time intervals, only one of the two diodes is biased in forward direction, whereas the other diode is reverse biased. The forward-biased diode peak rectifies the voltage of the secondary winding and charges the capacitors (C19 and C21) to their respective voltages.

$$V_{C21} = V_{s@1} - V_{F\_D7}$$

$$V_{C19} = -V_{s@2} - V_{F\_D6}$$

where

- V_{F_D6} is the forward voltage drop of the diode D6
- V_{F_D7} is the forward voltage drop of the diode D7

(22)

The sum of the two voltages is the output voltage, VOUT, of this voltage-doubler circuitry.

$$VOUT = V_{C20} = V_{C19} + V_{C21} \quad (23)$$

$$VOUT = -\frac{-VIN}{2 \times n} - V_{F\_D6} + \frac{VIN}{2 \times n} - V_{F\_D7} \quad (24)$$

resulting under the assumption of:

$$V_{F\_D6} = V_{F\_D7} = V_{F\_D}$$

where

- V_{F_D} is the forward voltage drop of one diode used in the voltage doubler

in (25)

$$VOUT = \frac{VIN}{n} - 2 \times V_{F\_D} \quad (26)$$

5.7.5.1 Selection of Diodes and Transformer

The voltage stress across each diode is basically the voltage on the secondary winding, plus the voltage on the respective capacitor (C19 or C21) of the voltage doubler.

$$V_{R\_D6} > V_{s@1} + V_{C19}$$

where

- V_{R_D6} is the minimum needed reverse voltage of diode D6 (27)

To commonly simplify:

$$V_R > 2 \times \frac{V_p}{n} = \frac{VIN}{n}$$

where

- V_R is the minimum needed reverse voltage of each diode
- V_p is the voltage applied to the primary winding alternately in positive and negative direction (28)

The reverse voltage calculated by Equation 28 is by one diode forward-voltage drop larger, which usually is not a problem. In each case, the selected diode should have additional margin added to this parameter value.

The average diode current equals the output current of the converter. Because each diode is conducting for almost half of the total period, the peak current through each of the diodes is slightly higher than two times the output current of the converter. During the design of the DC/DC converter, the output current was considered to be 2 mA. Therefore, the peak current through the diodes (D6 and D7) was assumed to be in the range of 5 mA.

To avoid potential issues with an increased reverse leakage current of Schottky diodes at high temperatures, silicon diodes are used. The silicon diodes have been selected for the lowest forward voltage (V_{F_D}) drop at 5 mA, as well as for low diode capacitance to reduce conduction and switching losses.

The PMLL4153 was selected. The data sheet PMLL4153 specifies the following values for a temperature T_J of 25°C:

- $V_{F\_D\_max}$ = 700 mV @ I_{F_D} = 2 mA
- $V_{F\_D\_max}$ = 810 mV @ I_{F_D} = 10 mA
- C_{D_max} = 2 pF @ VR = 0 V and f = 1 MHz
- V_R = 50 V

$V_{F\_D\_}$ max for the above mentioned 5 mA peak forward diode current was approximated simply by averaging the two $V_{F\_D\_}$ max values given for 2 and 10 mA.

- $V_{F\_D\_max}$ (estimated) ≈ 755 mV @ I_{F_D} = 5 mA
- T_J = 25°C

Because of the diodes V_F versus I_F characteristic, the expected forward voltage at 5 mA will be in reality slightly less. Therefore, an additional design margin is provided by this approach. However, it is not sufficient to know the value at room temperature only. Since the forward voltage of silicon diode has a negative temperature coefficient, operation at the minimum operating temperature of –40°C needs to be considered as the worst case situation. Based on a –2-mV/K temperature coefficient (typical for silicon diodes) and on the before estimated maximum value at IF_D = 5 mA and Tj = 25°C, the respective value for –40°C will be 130 mV larger.

- $V_{F\_D\_max}$ (estimated) ≈ 885 mV @ IF_D = 5 mA
- T_J = –40°C

For the calculation of the required voltage on the secondary winding, the minimum needed input voltage for the LDO U4 needs to be a known value. It is especially important that U4 gets enough headroom on its input to ensure that its PSRR will be as specified in the data sheet for TPS71733. As mentioned in Section 5.6.1, the required headroom for the TPS71733 is 250 mV. Using the 3% tolerance specification given in the TPS71733 data sheet, the minimum required input voltage can be calculated as shown in Equation 29.

$$VIN_{LDO\_min} \geq 1.03 \times 3.3V + 250\,mV = 3.65\ V \quad (29)$$

where

- V_{INLDO_min} is the minimum needed input voltage of the TPS71733 to have a PSRR as specified in the TPS71733 data sheet.

The output voltage of the DC/DC converter needs to be (at least by the voltage drop of R17) larger than the calculated value.

$$VOUT_{DC/DC\_min} \geq IOUT_{LDO\_max} \times R17 + VIN_{LDO\_min} \quad (30)$$

$$VOUT_{DC/DC\_min} \geq 2mA \times 10\,\Omega + 3.65\ V = 3.67\ V$$

where

- $VOUT_{DC/DC\_min}$ is the minimum required output voltage of the isolated DC/DC converter
- $IOUT_{LDO\_max}$ is the maximum expected output current of the TPS71733 (31)

The required primary-to-secondary turns ratio n of the transformer T1 can be calculated by rearranging Equation 26.

$$n = \frac{VIN}{VOUT_{DC/DC\_min} + 2 \times V_{F\_D}} = \frac{4.5\ V}{3.67\ V + 2 \times 0.885\ V} = 0.827 = 1{:}1.209 \quad (32)$$

To provide additional margin, a turns ratio, n of 1:1.25 = 0.8, was chosen. The secondary number of turns needs to be 1.25 times the number of turns on the primary side.

Therefore, the transformer needs to be able to operate with the V-t product (also called V-s or V-µs product) applied to its primary winding, which can be calculated as shown in Equation 33.

$$Vt_{\_min} \geq V_{p\_max} \times t_{ON\_max} = \frac{VIN_{\_max}}{2} \times \frac{T_{\_max}}{2} = \frac{VIN_{\_max}}{4 \times f_{\_min}}$$

where

- $Vt_{\_min}$ is the minimum required V-t product of the transformer to avoid saturation
- $V_{p\text{-}max}$ is the maximum voltage applied to the primary winding
- t_{ON_max} is the maximum time for which a switch (Q1 or Q2 in Figure 48) is ON
- $VIN_{\_max}$ is the maximum input voltage of the isolated DC/DC converter (in this case, 4.5 V + 5% tolerance)
- $T_{\_max}$ is the maximum time of one period of the switching frequency
- $f_{\_min}$ is the minimum switching frequency; 30 kHz for TPS60402 (33)

Using the resulting numbers, the minimum needed V-t product can be calculated as shown in Equation 34.

$$Vt_{\_min} \geq \frac{1.05 \times 4.5\ V}{4 \times 30\ kHz} = 39.4\ V\mu s \quad (34)$$

To ensure staying far from saturation, which would negatively impact the efficiency, applying an additional margin is recommended. A slight reduction of the value of the magnetizing inductance can not be excluded, even if the V-s product is not (yet) violated. Transformers with V-s products larger than 45 to 50 Vµs should provide enough margin, assuming that this V-s product from the manufacturer to be valid over the needed operating temperature range.

For the purpose of this design, an optimized transformer from Wurth Electronics Midcom Inc. that matches the listed requirements was used. Short specifications for this transformer are shown in Table 8.

Table 8. Wurth Transformer Specification

TURNS RATIO n (Np:Ns)	MAGNETIZING INDUCTANCE Lm (mH)	V-t PRODUCT (Vμs)	ISOLATION (Vac, 1 MINUTE)	DIMENSIONS (mm)	ORDER NO.	OPERATING TEMPERATURE RANGE (°C)	MANUFACTURER
1:1.25	>3	100	1500	9.78 × 9.14 × 10.54	750314839	–40 to 100	Wurth Electronics Midcom Inc.

5.7.5.2 Real Implementation on the Board

Figure 48 shows a simplified schematic of the isolated DC/DC converter. The circuitry implemented on the board adds some additional components and tweaks to ease the test and enable user-specific modifications.

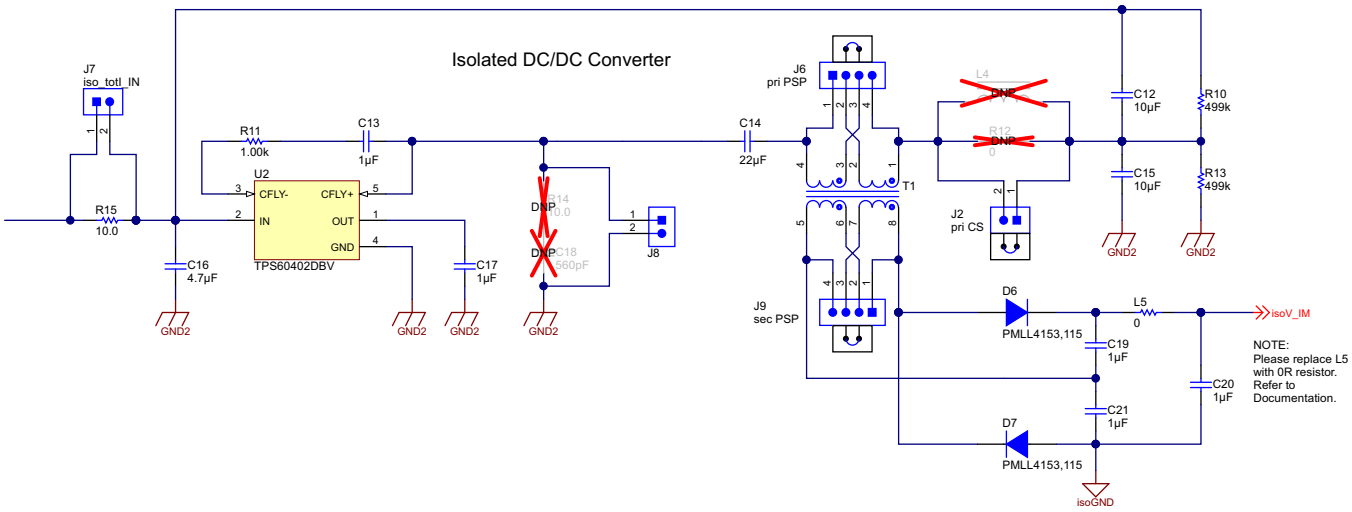


Figure 50. Isolated DC/DC — Real Implementation

The TIDA-00167 design implements a current sense resistor (R15) in front of the DC/DC converter. Using R15 provides the user an easy way for a noninvasive measurement of the current consumption of the DC/DC converter with or without the post-regulator LDOs (U4 or U7) — and possibly also with or without a connected load on the isolated side. Current measurement can be done by a voltmeter connected to the respective header (J7) where 10 mV represents 1 mA of current.

This design provides R14 and C18 as placeholders on the board to be used as snubbers for the left leg of the half bridge (Q1 and Q2 inside the TPS60402). A snubber may be needed to reduce peaking and possible ringing on the switch node of the left leg. The snubber may be needed in cases where the peaking would otherwise exceed the maximum-voltage rating of the TPS60402 or the ringing of the device would cause EMI issues. The current design does not require these components. Therefore, these components have not been populated. If these components are needed, separate testing is required to evaluate the effectiveness of the snubber and its influence on the DC/DC converter's efficiency.

The values given are placeholder values and need to be adapted according to the specific case. The value of the capacitor C18 is usually chosen so that the ringing frequency on the switch node is halved with C18 compared to the case without C18. R14 needs to be a short (or a 0-Ω resistor) for finding the right value for C18. If the best fitting capacitance value has been found and C18 has been populated with a capacitor with this optimal value, R14 can be varied to find the best compromise between ringing reduction and best efficiency. The test needs to be conducted by connecting the oscilloscope probe (high impedance, low capacitance) with the shortest possible grounding wire.

The header pins of J8 can be used as *test point* and GND2 connection for the modified use of the oscilloscope probe, similar to that what Figure 51 shows with standard test points. Using the J8 header pins provides an easy way to connect the probe in a *tip and barrel* manner to the switch node. Connecting the probe in this manner will avoid noise pickup, which otherwise happens when the probe is used with a standard ground wire and alligator clip connected.

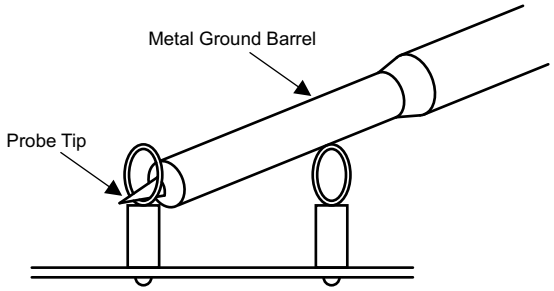


Figure 51. Tip and Barrel Method for Noise-Free Measurement

In contrast to the statement that the half bridge transformer does not need multiple or tapped windings on each side, the transformer T1 used in this design has two windings on the primary as well as on the secondary side. As can be seen in Figure 50, the windings on each side are connected in series and can be therefore considered as a single winding.

With its dual winding structure, the transformer provides an easy way to test other configurations. These configurations include paralleling the windings and using on one side a single winding, but on the other side using both windings. This approach is supported by the headers J6 and J9 and the respective jumpers, which are populated by default on the two inner pins of both headers, selecting the series connection mode of the two windings on each side. If needed, a dedicated single winding transformer can be used in series manufacturing. The headers J9 and J6 can be also used to measure the voltages across the primary and secondary winding of T1.

Header J2 provides an easy way to measure the current in the primary winding I_p. One method to measure the current in I_p is to connect a short wire loop to the header pins and using a current probe clamped on that wire loop. Another method is to use a current shunt resistor (for example 40 Ω) and measure the voltage drop across the current shunt resistor. Figure 52 and Figure 53 give examples of measurements and simulation with TINA-TI, using a 40-Ω sense resistor.

Both measurements and simulation match very well, giving confidence that other test cases (without the sense resistor) can be simulated as well. The upper curve in Figure 52 and Figure 53 shows the output voltage ripple. The lower curve shows the measured current in the primary winding I_p.

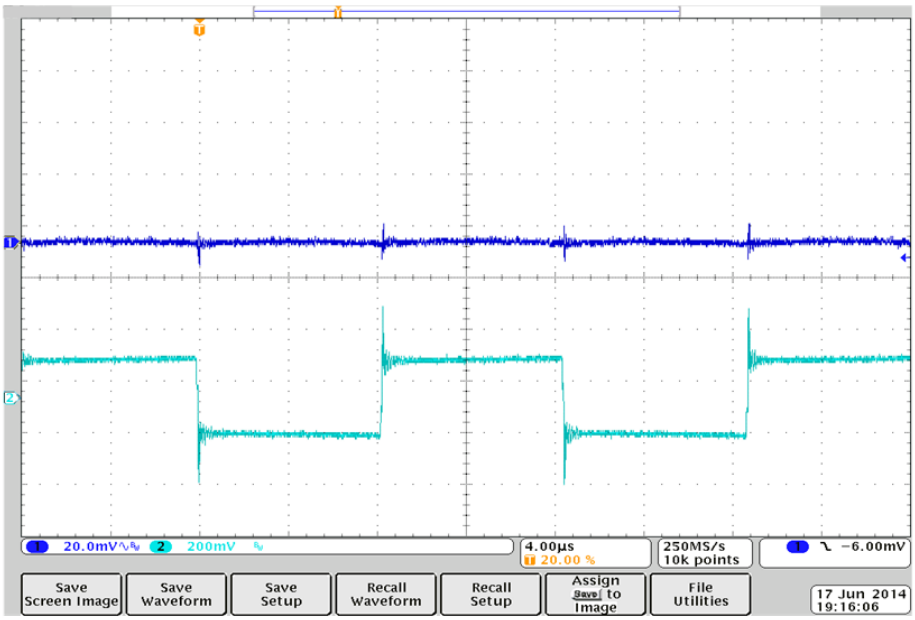


Figure 52. Current in Primary Winding — 40 Ω (Real Measurement With Oscilloscope)

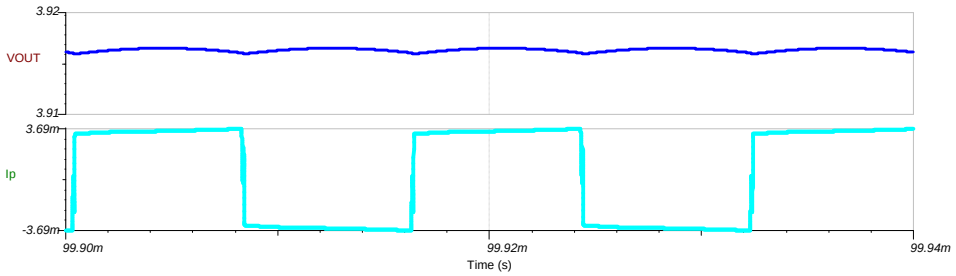


Figure 53. Current in Primary Winding — 40 Ω (Simulation with TINA-TI)

The default population is a jumper on the header J2. R12 and L4 are placeholders on the board to either test the influence of leakage inductance by populating L4, or finally shorting J2 forever by populating R12 with a 0-Ω resistor.

R10 and R13 are used to keep the capacitive divider C12 / C15 balanced to cancel out their possible tolerances.

L5 is a placeholder on the board, which can be populated with an inductor to build a ripple filter for reducing the output-ripple voltage of the DC/DC converter. Because the design relies on the high PSRR of the post-regulator LDO (U4), the ripple filter was not implemented. L5 was simply populated with a 0-Ω resistor.

6 Description of Test Points, Headers, and Jumper Settings

The board provides a number of different test points and headers to ease the measurement of the different signals. The headers and the respective jumpers can also be used for configuration of the board.

Table 9. True Test Points

TEST POINT	SPECIFIC GROUND NAME	DESCRIPTION OR ASSIGNMENT	EQUIVALENT HEADER PINS
TP4	GND	Ground for the following circuit blocks on the nonisolated side of the design: • High Input Voltage LDO • Load Switch • Input of Ripple Filter • Post-Regulator LDOs on nonisolated side	Equivalent to: • J20-p2 • J10-p2 • J19-p2
TP5	isoGND	Ground for the following circuit blocks on the isolated side of the design: • Secondary Side of Isolated DC/DC Converter • Post-Regulator LDOs on isolated side	Equivalent to: • J15-p1 • J11-p2 • J18-p2
TP7	GND2	Ground for the following circuit blocks on the nonisolated side of the design: • Output of Ripple Filter • Primary Side of Isolated DC/DC Converter	Equivalent to: • J8-p2

Table 10. Headers (Respective Jumpers Must Not Be Populated for Current Measurements)

HEADER	PIN	DESCRIPTION
J4	1 → 2	High-voltage LDO (U1) input current measurement with voltmeter (200 mV/mA)
J5	1 → 2	Input voltage after Loop Protection
J21	1 → 2	High-voltage LDO (U1) input current measurement with ammeter Active current-limiter circuit is disabled by ammeter
J3	2 → GND	High-voltage LDO (U1): power-good signal
J7	2 → GND2	Input voltage of Isolated DC/DC converter
J7	1 → GND2	Ripple Filter: Output voltage
J7	1 → 2	Isolated DC/DC converter's input current measurement with voltmeter (10 mV/mA)
J8	1 → 2	Isolated DC/DC converter: switch node voltage (left leg of half bridge) measurement with oscilloscope
J2	1 → 2	Transformer T1 - measurement of primary winding current with oscilloscope: either using a short wire loop connected to J2 and measure with current probe or use up to 40 Ω resistor on J2 and measure with high impedance probe
J9	2 → 3	Transformer T1 - measurement of secondary winding current with oscilloscope: either using a short wire loop connected to J9 and measure with current probe or use up to 40 Ω resistor on J9 and measure with high impedance probe
J12	1 → 2	Post-regulator LDOs (U3 or U6) on nonisolated side: Input current measurement with voltmeter; LDO selection depends on jumper setting on J16 (10 mV/mA)
J12	1 → GND	Output voltage of the load switch (U5); almost equals the output voltage of the high voltage LDO (U1)
J12	2 → GND	Post-regulator LDOs (U3 or U6) on nonisolated side: input voltage measurement; LDO selection depends on jumper setting on J16
J14	2 → GND	High-voltage LDO (U1): power-good signal
J14	1 → GND	Low-noise LDO U3 on nonisolated side: Enable signal
J13	1 → 2	Post-regulator LDOs (U4 or U7) on isolated side: Input current measurement with voltmeter; LDO selection depends on jumper setting on J17 (10 mV/mA)
J13	1 → isoGND	Isolated DC/DC converter: output voltage
J13	2 → isoGND	Post-regulator LDOs (U4 or U7) on isolated side: input voltage measurement; LDO selection depends on jumper setting on J17
J10	1 → 2	Low Iq post regulator (U6) on nonisolated side: output voltage
J19	1 → 2	Low-noise, high-PSRR post regulator (U3) on nonisolated side: output voltage
J11	1 → 2	Low Iq post regulator (U7) on isolated side: output voltage
J18	1 → 2	Low Noise, High PSRR Post Regulator (U4) on Isolated Side: output voltage
J15	2 → isoGND	Low-noise LDO U4 on isolated side: Enable signal

Table 11. Jumper Settings

HEADER	DEFAULT SETTING	RESULT WHEN POPULATED
J4		Current-limiting resistor: disabled
J20	Populated	Connected 4 – 20 mA DAC's internal current sense resistor not protected – standard configuration when used for other applications than 4 – 20 mA loop powered transmitters
J21		Active Current Limiter: disabled (shorted)
J3		Load switch (U5) enabled by power good of high-voltage LDO (U1)
J6	Populated (on pins 2 and 3)	Transformer T1 Primary Windings: connected in series
J9	Populated (on pins 2 and 3)	Transformer T1 Secondary Windings: connected in series
J2	Populated	Transformer T1 Primary: directly connected to right leg of half bridge, not able to sense primary winding current Ip
J16	Populated	Post-regulator LDOs selection on nonisolated side: • on pins 1 and 2: Low-noise LDO (U3) • on pins 2 and 3: Low-Iq LDO (U6)
J14		Low-noise LDO (U3) on nonisolated side (provided it is selected by J16): controlled by power good of high-voltage LDO (U1) otherwise always ON (when J14 is not populated)
J17	Populated	Post-regulator LDOs selection on isolated side: • on pins 1 and 2: Low-noise LDO (U4) • on pins 2 and 3: Low-Iq LDO (U7)
J15		Low-noise LDO (U4) on isolated side (provided it is selected by J17): disabled otherwise always ON (when J14 is not populated)

7 Simulation Results

7.1 DC/DC Converter — All Waveforms

The isolated DC/DC converter has been simulated using TINA-TI. All important waveforms have been probed and are shown in Figure 54. The simulation is based on an input voltage of 4.5 V and a constant output current of 2 mA. An additional explanation of the simulated signals can be found in Table 12.

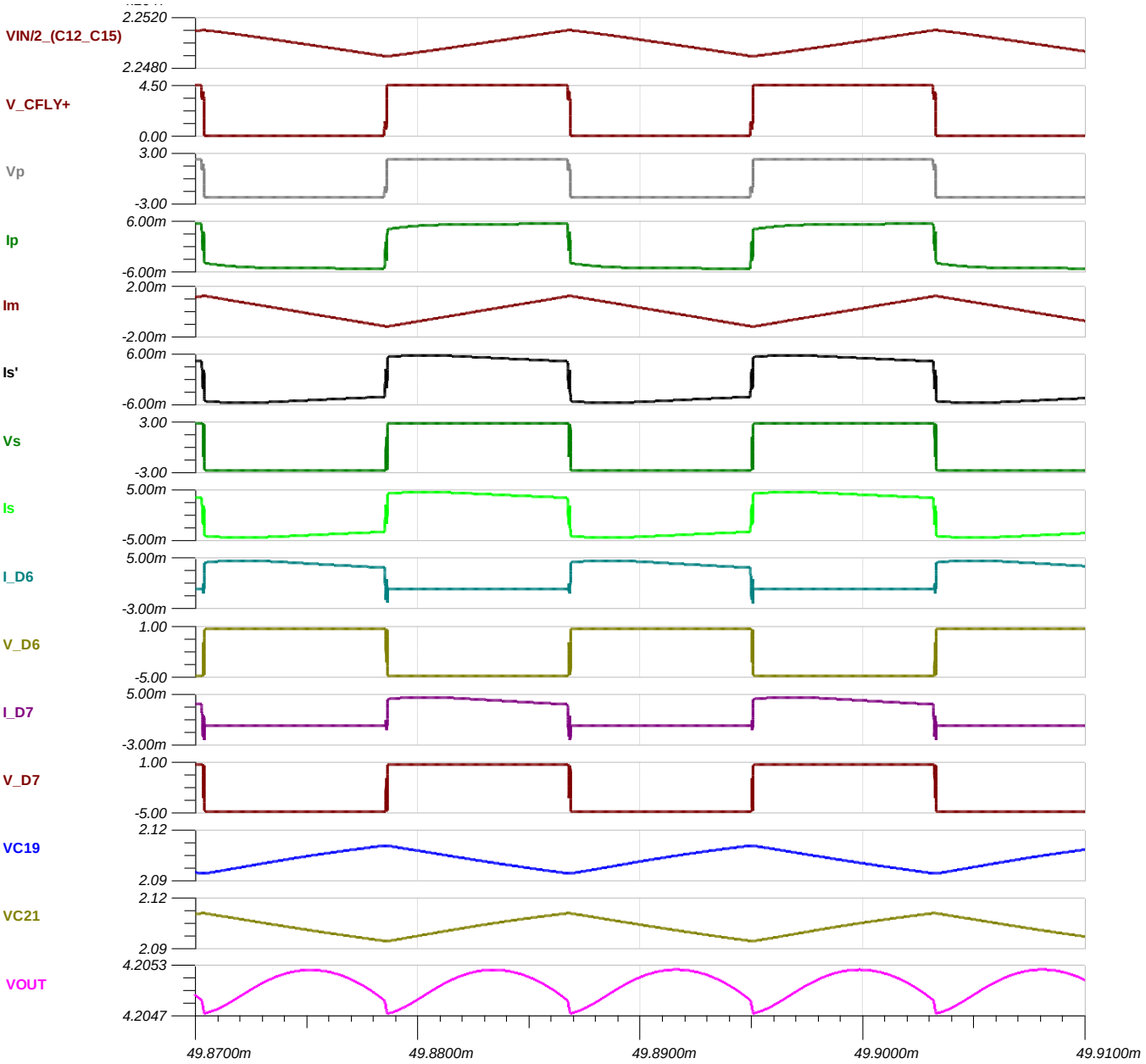


Figure 54. DC/DC Converter — All Waveforms

Table 12. List of Simulated Signals

SIGNAL NAME	DESCRIPTION
VIN/2_(C12_C15)	Voltage on the midpoint of the half bridge's right leg (C12 and C15)
V_CFLY+	Switch node voltage of left leg (Q1 and Q2 inside U2) of the half bridge
Vp	Voltage across primary winding (between pin 1 and 4 of header J6)
Ip	Current through primary winding of T1
Im	Magnetizing Current in Primary Winding of T1; cannot be measured; see Figure 43
Is'	Reflected current from the secondary winding; cannot be measured; see Figure 43
Vs	Voltage across secondary winding (between pin 1 and 4 of header J9)
Is	Current through secondary winding of T1
I_D6	Current through Diode D6
V_D6	Voltage across Diode D6
I_D7	Current through Diode D7
V_D7	Voltage across Diode D7
VC19	Voltage across C19 (charged through D6)
VC21	Voltage across C20 (charged through D7)
VOUT	Output voltage of the DC/DC converter, see Equation 23

8 Test Setup and Results

8.1 Pre-Compliance Conducted Noise Test (EN 55011)

Pre-compliance tests have evaluated the performance with different loop-input voltages on J1. The noise of each single wire of the cable was measured separately. The used board was using the scaled-down ripple filter configuration as shown in the schematics (Figure 26 and Figure 71). A 1.65-kΩ load resistance was connected on the board's isolated 3.3-V output, resulting in an output current of 2 mA. The board's isoGND was earthed at the respective terminal of the load.

8.1.1 Pre-Compliance Conducted Noise Measurement — Test Setup

The test setup was done according to Figure 55.

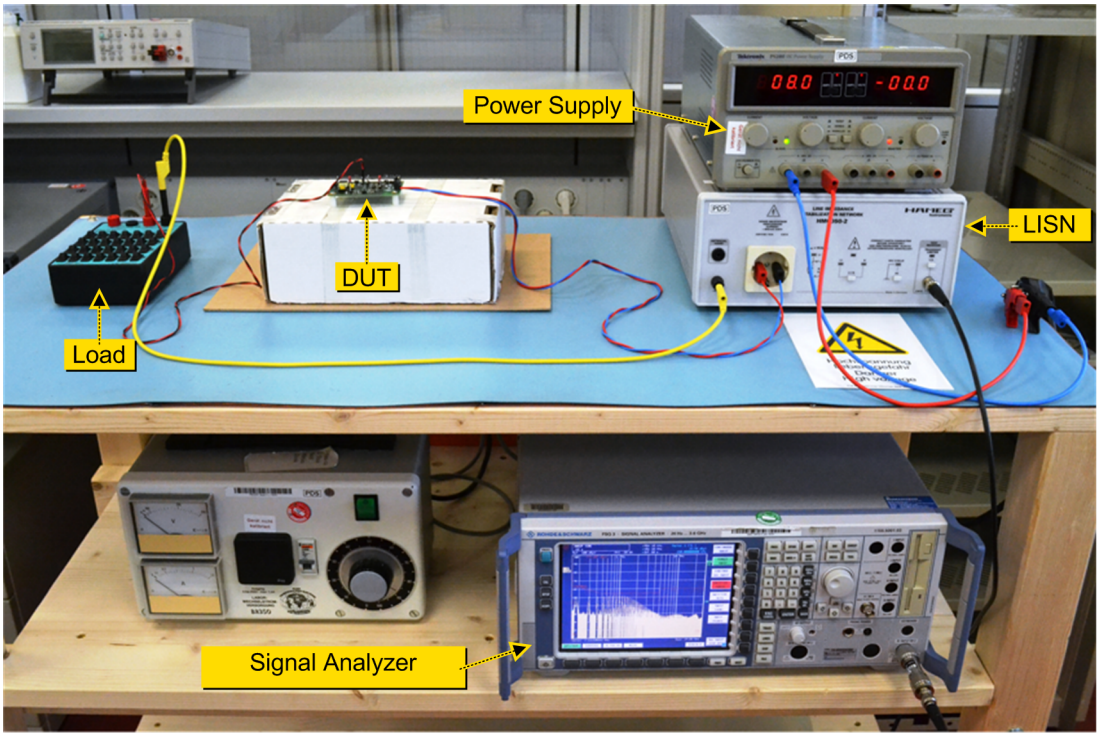


Figure 55. Pre-Compliance Conducted Noise Measurement — Test Setup

Table 13. Equipment Used in Pre-Compliance Conducted Noise Measurement

Signal Analyzer	FSQ 3 20 Hz to 3.6 GHz	Rohde and Schwarz GmbH and Co. KG
LISN	HM6050-2	Hameg Instruments
Power Supply	PS280	Tektronix
Load (Mini-Decade)	R1-3000	CMT

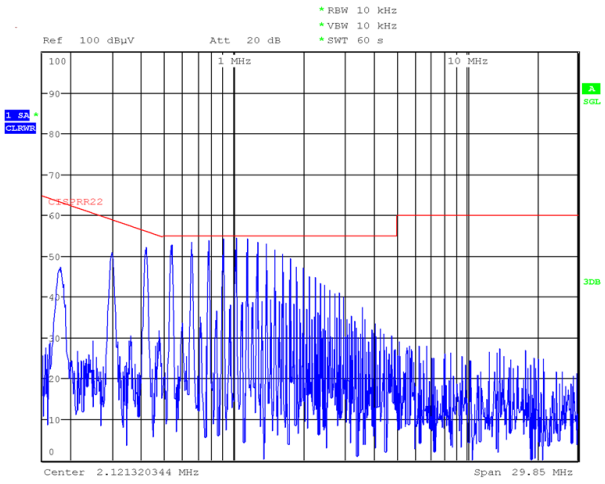
8.1.2 Pre-Compliance Conducted Noise Measurement — Results

The tests have been done for a frequency range from 150 kHz to 30 MHz, using the quasi-peak values given in EN 55011 for class B, group 1 devices as limit. The limit is shown in Figure 56, Figure 57, and Figure 58 as a red curve.

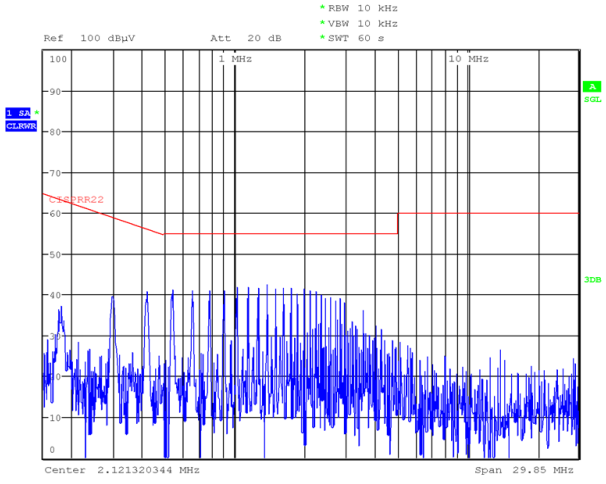
A purely informal test was done first to show the difference in noise between a nonearthed load versus an earthed load.

Table 14. Pre-Compliance Conducted Noise Measurement — Results

FIGURE	MEASURED WIRE ON LISN	INPUT	FILTER (POPULATION)	LOAD
Figure 56	L1	8 V	Full	Earthed
				Nonearthed
Figure 57	L1		Scaled-down	Earthed
	N			
Figure 58	L1	33 V		
	N			

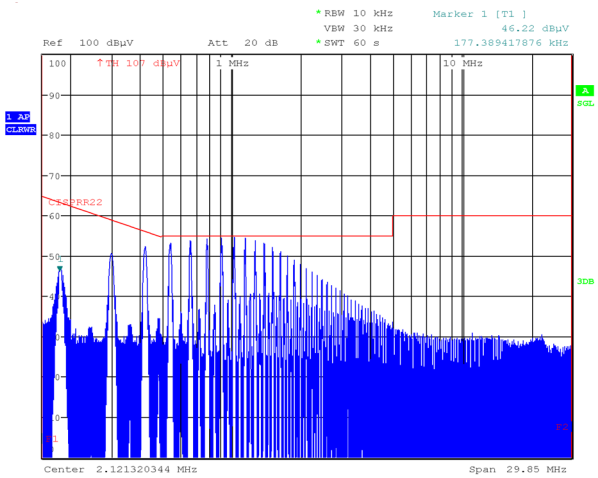


Conducted Noise on “L1”, 8V Loop Input, Full Ripple Filter, **Earthed Load**

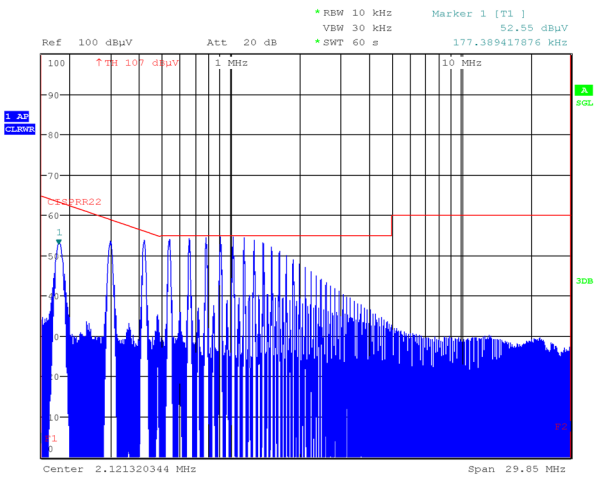


Conducted Noise on “L1”, 8V Loop Input, Full Ripple Filter, **Non-Earthed Load**

Figure 56. Conducted Noise with 8-V Loop Voltage and Full Filter

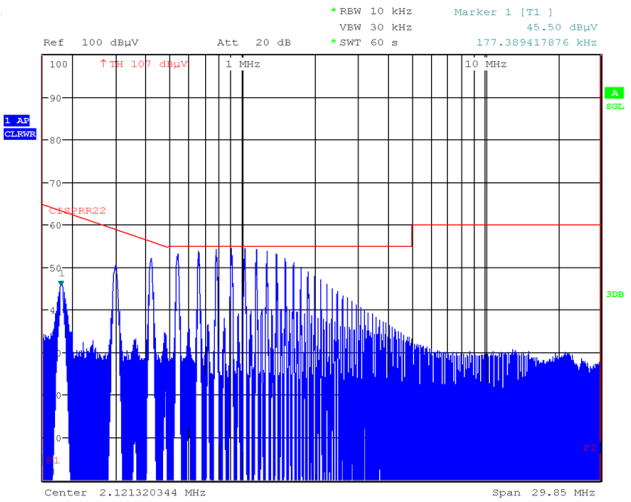


Conducted Noise **on "L1"**, 8V Loop Input, Scaled-Down Ripple Filter, Earthed Load

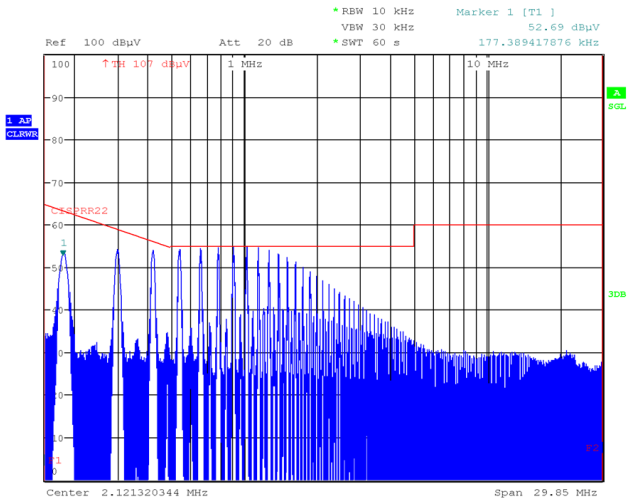


Conducted Noise **on "N"**, 8V Loop Input, Scaled-Down Ripple Filter, Earthed Load

Figure 57. Conducted Noise with 8-V Loop Voltage and Scaled Down Filter



Conducted Noise **on "L1"**, 33V Loop Input, Scaled-Down Ripple Filter, Earthed Load



Conducted Noise **on "N"**, 33V Loop Input, Scaled-Down Ripple Filter, Earthed Load

Figure 58. Conducted Noise with 33-V Loop Voltage and Scaled Down Filter

8.2 Isolated DC/DC Converter — Specific Measurements

The isolated DC/DC Converter has been evaluated in depth. A variable input voltage from 3 to 5.2 V has been applied on pin 2 of header J7, referenced to TP7 (GND2). The jumper on J7 was not populated, and R15 had been removed to ensure than no current was flowing back into the ripple filter, load switch, and high-voltage LDO. The jumper belonging to J17 had been removed to disconnect the post-regulator LDOs of the isolated side completely from the output of the DC/DC converter.

The output of the DC/DC converter was loaded by constant current ranging from no load (10 µA) to 3 mA, in steps of 250 µA.

The test was conducted at –40°C, 25°C, and 85°C.

The results of this evaluation are presented in Figure 59 to Figure 70. While engineers are familiar with interpreting efficiency curves (Figure 59 to Figure 61), the way of presenting results as used in Figure 62 to Figure 70 was especially chosen for this design. These images provide an easy way to determine the optimized operating point of the converter for a given output current when a minimum output voltage needs to be achieved (to provide enough headroom voltage for the post-regulator LDO) while not exceeding a dedicated input current budget.

8.2.1 Efficiency Measurements (Input Voltage VIN as Parameter)

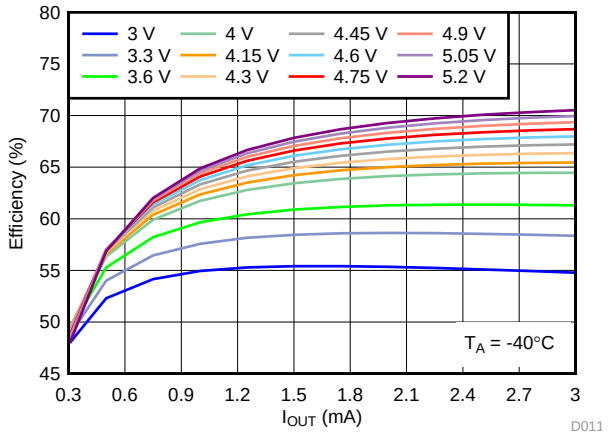


Figure 59. Efficiency vs. Output Current IOUT at –40°C

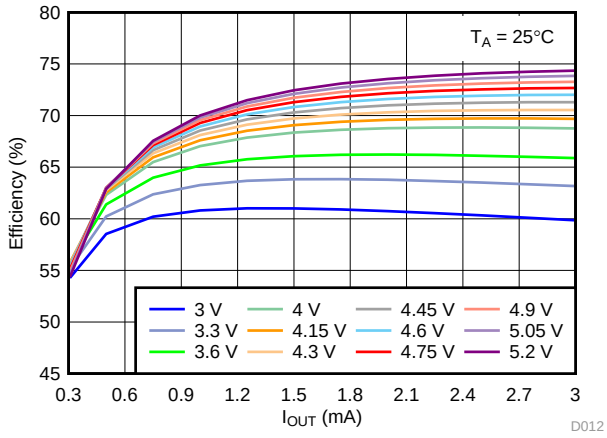


Figure 60. Efficiency vs. Output Current IOUT at 25°C

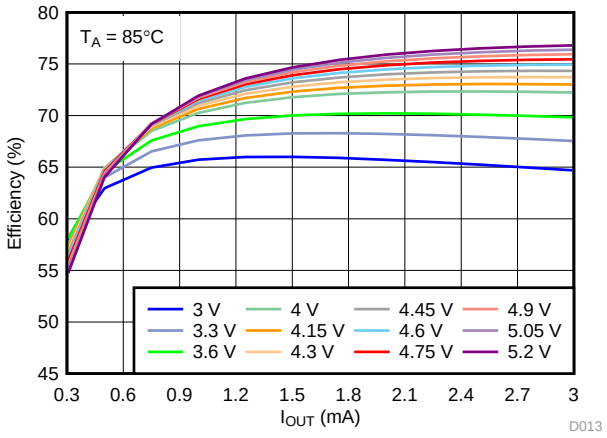


Figure 61. Efficiency vs. Output Current IOUT at 85°C

8.2.2 Output Voltage and Input Current versus Output Current Measurements (Input Voltage VIN as Parameter)

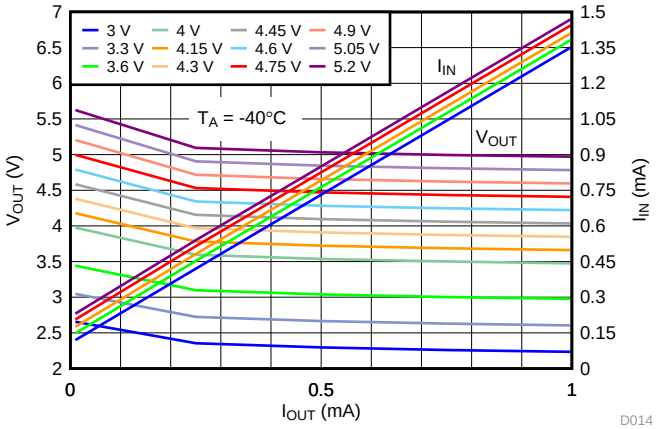


Figure 62. Output Voltage VOUT and Input Current IIN vs. Output Current IOUT (0 to 1 mA) at –40°C

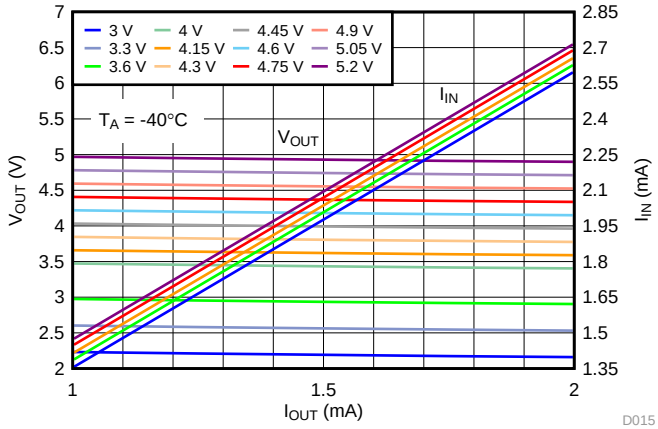


Figure 63. Output Voltage VOUT and Input Current IIN vs. Output Current IOUT (1 to 2 mA) at –40°C

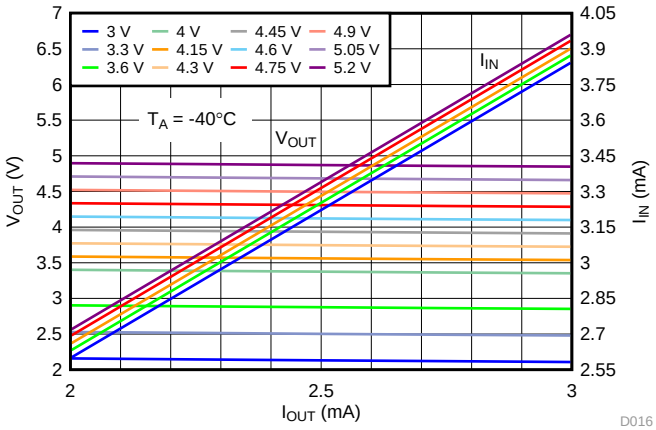


Figure 64. Output Voltage VOUT and Input Current IIN vs. Output Current IOUT (2 to 3 mA) at –40°C

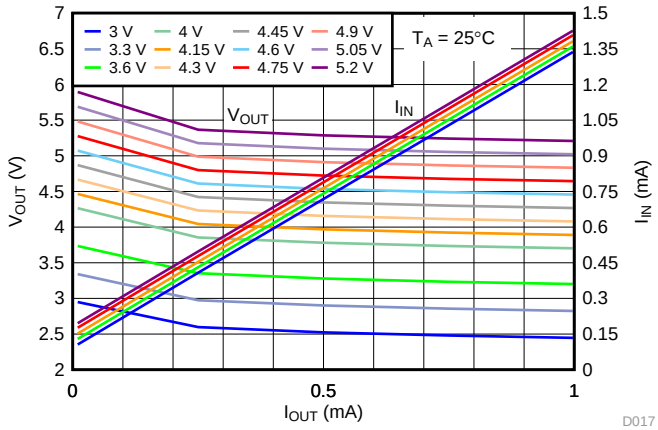


Figure 65. Output Voltage VOUT and Input Current IIN vs. Output Current IOUT (0 to 1 mA) at 25°C

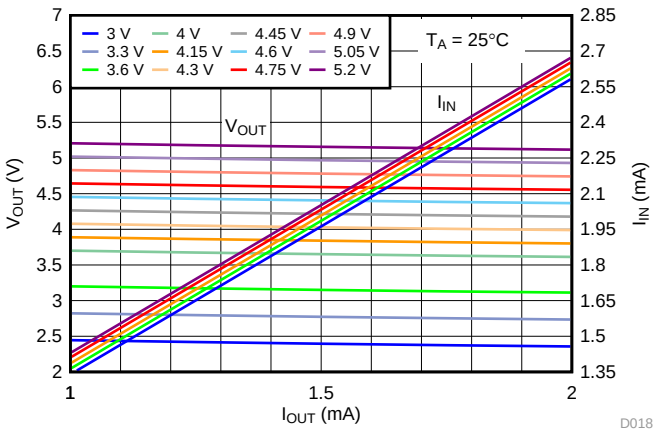


Figure 66. Output Voltage VOUT and Input Current IIN vs. Output Current IOUT (1 to 2 mA) at 25°C

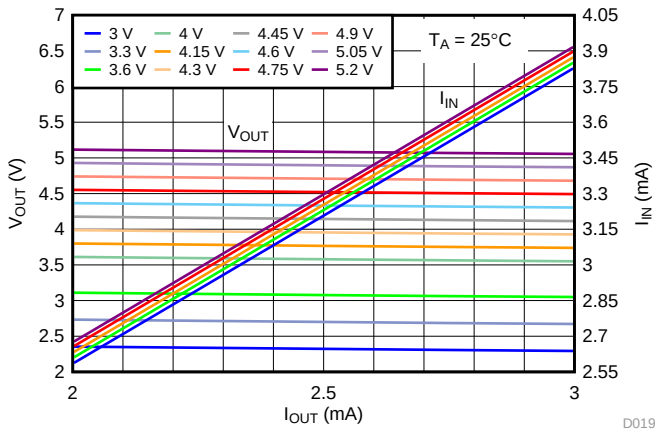


Figure 67. Output Voltage VOUT and Input Current IIN vs. Output Current IOUT (2 to 3 mA) at 25°C

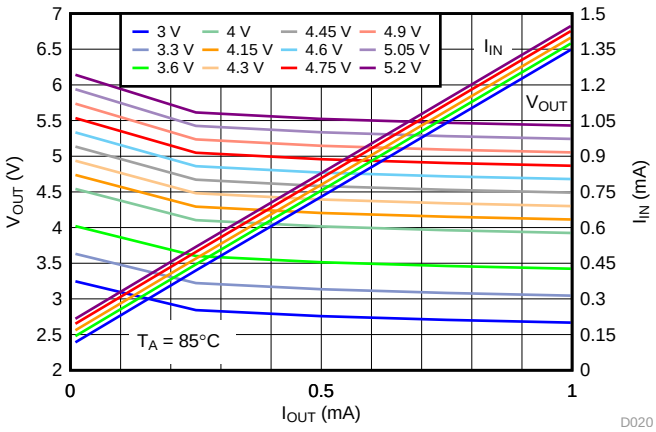


Figure 68. Output Voltage VOUT and Input Current IIN vs. Output Current IOUT (0 to 1 mA) at 85°C

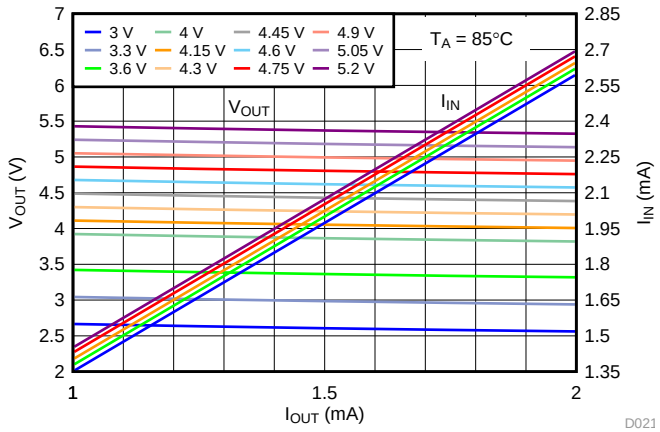


Figure 69. Output Voltage VOUT and Input Current IIN vs. Output Current IOUT (1 to 2 mA) at 85°C

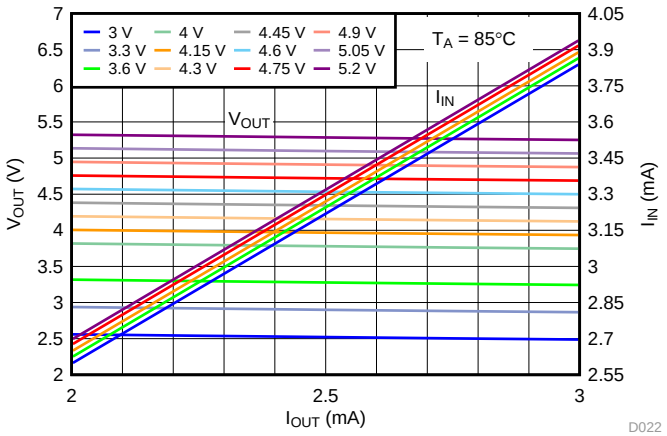


Figure 70. Output Voltage VOUT and Input Current IIN vs. Output Current IOUT (2 to 3 mA) at 85°C

9 Design Files

9.1 Schematics

To download the Schematics, see the design files at TIDA-00167.

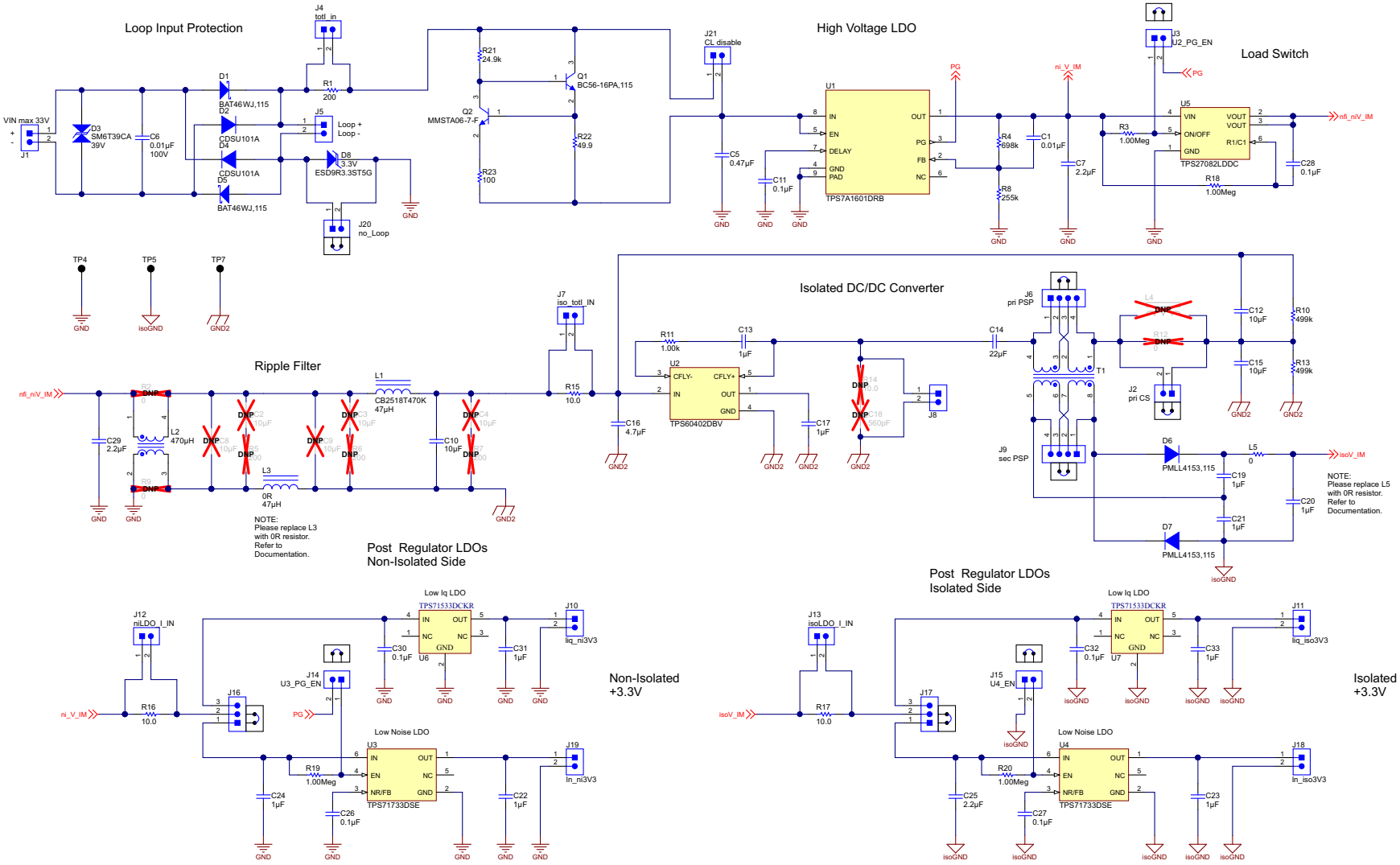


Figure 71. TIDA-00167 Complete Schematic

9.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00167.

Table 15. BOM

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER (1)	MFG	ALTERNATE PART NUMBER	ALTERNATE MFG
!PCB1	1		Printed Circuit Board		TIDA-00167	Any		
C1	1	0.01uF	CAP, CERM, 0.01uF, 10V, +/-10%, X5R, 0402	0402	GRM155R61A103KA01D	MuRata		
C5	1	0.47uF	CAP, CERM, 0.47uF, 100V, +/-10%, X7R, 0805	0805	GRM21BR72A474KA73L	MuRata		
C6	1	0.01uF	CAP, CERM, 0.01uF, 100V, +/-10%, X7R, 0603	0603	GRM188R72A103KA01D	MuRata		
C7, C29	2	2.2uF	CAP, CERM, 2.2uF, 16V, +/-10%, X5R, 0402	0402	C1005X5R1C225K050BC	TDK		
C10, C12, C15	3	10uF	CAP, CERM, 10uF, 10V, +/-10%, X7R, 0805	0805	GRM21BR71A106KE51L	MuRata		
C11, C28	2	0.1uF	CAP, CERM, 0.1uF, 16V, +/-10%, X7R, 0603	0603	GRM188R71C104KA01D	MuRata		
C13, C19, C20, C21, C22, C23, C24, C31, C33	9	1uF	CAP, CERM, 1uF, 10V, +/-10%, X5R, 0402	0402	GRM155R61A105KE15D	MuRata		
C14	1	22uF	CAP, CERM, 22uF, 10V, +/-10%, X5R, 1206	1206	GRM31CR61A226KE19L	MuRata		
C16	1	4.7uF	CAP, CERM, 4.7uF, 10V, +/-10%, X5R, 0603	0603	C0603C475K8PACTU	Kemet		
C17	1	1uF	CAP, CERM, 1uF, 10V, +/-10%, X7R, 0603	0603	GRM188R71A105KA61D	MuRata		
C25	1	2.2uF	CAP, CERM, 2.2uF, 10V, +/-10%, X7R, 0603	0603	GRM188R71A225KE15D	MuRata		
C26, C27, C30, C32	4	0.1uF	CAP, CERM, 0.1uF, 16V, +/-10%, X7R, 0402	0402	GRM155R71C104KA88D	MuRata		
D1, D5	2	100V	Diode, Schottky, 100V, 0.25A, SOD-323F	SOD-323F	BAT46WJ,115	NXP Semiconductor		
D2, D4	2	90V	Diode, Switching, 90V, 0.1A, SOD-523F	SOD-523F	CDSU101A	Comchip Technology		
D3	1	39V	Diode, TVS, Bi, 39V, 600W, SMB	SMB	SM6T39CA	ST Microelectronics		None
D6, D7	2	75V	Diode, Fast Rectifier, 75V, 0.2A, 3.7x1.6x1.6mm	3.7x1.6x1.6mm	PMLL4153,115	NXP Semiconductor		
D8	1	3.3V	Diode, TVS, Uni, 3.3V, 0.15W, SOD-923	SOD-923	ESD9R3.3ST5G	ON Semiconductor		
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	BandF Fastener Supply		
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone		
J1	1		Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	7.0x8.2x6.5mm	ED555/2DS	On-Shore Technology		
J2, J3, J4, J5, J7, J8, J10, J11, J12, J13, J14, J15, J18, J19, J20, J21	16		Header, 100mil, 2x1, Tin, TH	Header 2x1	90120-0122	Molex		

(1) Unless otherwise noted in the Alternate PartNumber or Alternate Manufacturer columns, all parts may be substituted with equivalents.

Table 15. BOM (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER (1)	MFG	ALTERNATE PART NUMBER	ALTERNATE MFG
J6, J9	2		Header, 4x1, 100mil, Tin, TH	Header, 4x1, 100mil, TH	PEC04SAAN	Sullins Connector Solutions		
J16, J17	2		Header, 100mil, 3x1, Tin, TH	Header, 3 PIN, 100mil, Tin	PEC03SAAN	Sullins Connector Solutions		
L1, L3	2	47uH	Inductor, Wirewound, Ferrite, 47uH, 0.11A, 1.235 ohm, SMD	2.5x1.8x1.8mm	CB2518T470K	Taiyo Yuden		
L2	1	470uH	Coupled inductor, 470uH, 0.1A, 0.35 ohm, +/-30%, SMD	5.0x3.3x3.3mm	DR221-474AE	Bourns		
L5	1	0	RES, 0 ohm, 5%, 0.1W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale		
Q1	1	V	Transistor, NPN, 80V, 1A, SOT1061	SOT1061	BC56-16PA,115	NXP Semiconductor		
Q2	1	0.25V	Transistor, NPN, 80V, 0.5A, SOT-323	SOT-323	MMSTA06-7-F	Diodes Inc.		
R1	1	200	RES, 200 ohm, 1%, 0.25W, 1206	1206	CRCW1206200RFKEA	Vishay-Dale		
R3, R19, R20	3	1.00Meg	RES, 1.00Meg ohm, 1%, 0.063W, 0402	0402	CRCW04021M00FKED	Vishay-Dale		
R4	1	698k	RES, 698k ohm, 1%, 0.1W, 0603	0603	CRCW0603698KFKEA	Vishay-Dale		
R8	1	255k	RES, 255k ohm, 1%, 0.1W, 0603	0603	CRCW0603255KFKEA	Vishay-Dale		
R10, R13	2	499k	RES, 499k ohm, 1%, 0.063W, 0402	0402	CRCW0402499KFKED	Vishay-Dale		
R11	1	1.00k	RES, 1.00k ohm, 1%, 0.063W, 0402	0402	CRCW04021K00FKED	Vishay-Dale		
R15, R16, R17	3	10.0	RES, 10.0 ohm, 1%, 0.1W, 0603	0603	CRCW060310R0FKEA	Vishay-Dale		
R18	1	1.00Meg	RES, 1.00Meg ohm, 1%, 0.1W, 0603	0603	CRCW06031M00FKEA	Vishay-Dale		
R21	1	24.9k	RES, 24.9k ohm, 1%, 0.25W, 1206	1206	CRCW120624K9FKEA	Vishay-Dale		
R22	1	49.9	RES, 49.9 ohm, 1%, 0.25W, 1206	1206	CRCW120649R9FKEA	Vishay-Dale		
R23	1	100	RES, 100 ohm, 1%, 0.25W, 1206	1206	CRCW1206100RFKEA	Vishay-Dale		
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9 (2)	9	1x2	Shunt, 100mil, Gold plated, Black	Shunt	969102-0000-DA	3M	SNT-100-BK-G	Samtec
T1	1	3mH	Transformer, 3mH, SMT	9.78x10.54x9.14 mm	750314839	Wurth Elektronik eiSos		
TP4, TP5, TP7	3	Black	Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone		
U1	1		60-V, 5-µA IQ, 100-mA, Low-Dropout Voltage Regulator with Enable and Power-Good, DRB0008B	DRB0008B	TPS7A1601DRB	Texas Instruments		None
U2	1		UNREGULATED 60-mA CHARGE PUMP VOLTAGE INVERTER, DBV0005A	DBV0005A	TPS60402DBV	Texas Instruments		None

(2) Shunts (Jumpers) SH-J1 to SH-J9 needs to be populated as shown in the schematic. The number in their designators are not related to the numbers used in the headers' J2 to J21 designators.

Table 15. BOM (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER (1)	MFG	ALTERNATE PART NUMBER	ALTERNATE MFG
U3, U4	2		Low Noise, High-Bandwidth PSRR Low-Dropout 150mA Linear Regulator, DSE0006A	DSE0006A	TPS71733DSE	Texas Instruments		None
U5	1		1.2V - 8V, 3A PFET Load Switch with Configurable Slew Rate, Fast Transient Isolation and Hysteretic Control, DDC0006A	DDC0006A	TPS27082LDDC	Texas Instruments		None
U6, U7	2		Single Output LDO, 50 mA, Fixed 3.3 V Output, 3 to 24 V Input, 5-pin SC70 (DCK), -40 to 85 degC, Green (RoHS and no Sb/Br)	DCK0005A	TPS71533DCKR	Texas Instruments	Equivalent	None
C2, C3, C4, C8, C9	0	10uF	CAP, CERM, 10uF, 10V, +/-10%, X7R, 0805	0805	GRM21BR71A106KE51L	MuRata		
C18	0	560pF	CAP, CERM, 560pF, 50V, +/-10%, X7R, 0402	0402	GRM155R71H561KA01D	MuRata		
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A		
L4	0	33uH	Inductor, Wirewound, Ferrite, 33uH, 0.13A, 0.7 ohm, SMD	2.5×1.8×1.8mm	CB2518T330K	Taiyo Yuden		
R2, R9, R12	0	0	RES, 0 ohm, 5%, 0.1W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale		
R5, R6, R7	0	200	RES, 200 ohm, 1%, 0.063W, 0402	0402	CRCW0402200RFKED	Vishay-Dale		
R14	0	10.0	RES, 10.0 ohm, 1%, 0.063W, 0402	0402	CRCW040210R0FKED	Vishay-Dale		

NOTE: L3 replaced by RES, 0 ohm, 5%, 0.125W, 0805, CRCW08050000Z0EA, Vishay-Dale.

9.3 Layer Plots

To download the layer plots, see the design files at TIDA-00167.

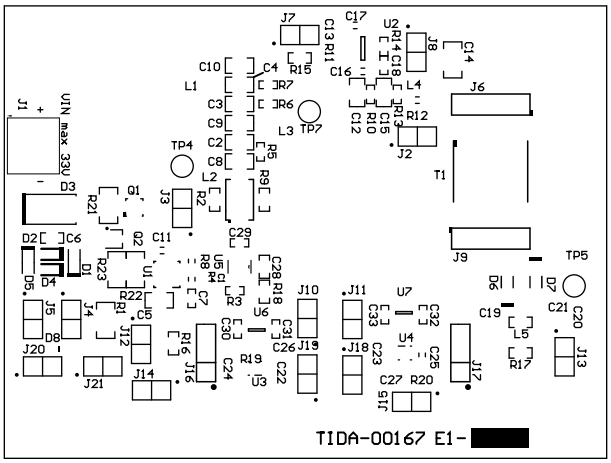


Figure 72. Top Overlay

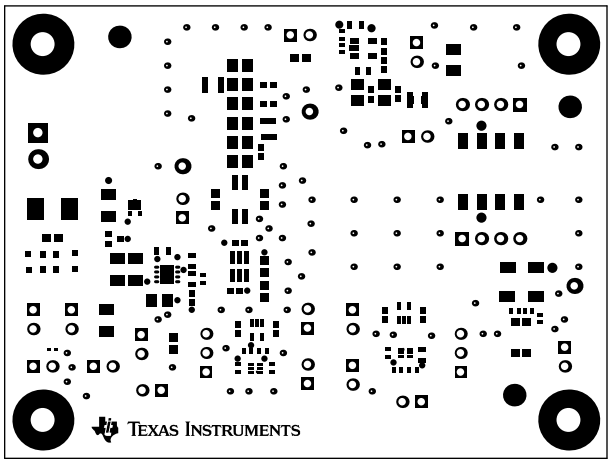


Figure 73. Top Solder Mask

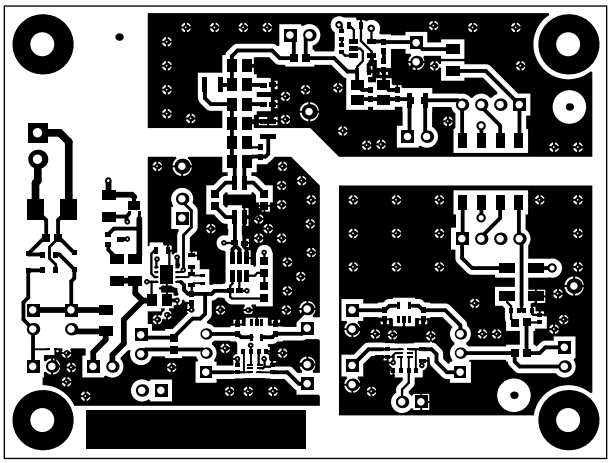


Figure 74. Top Layer

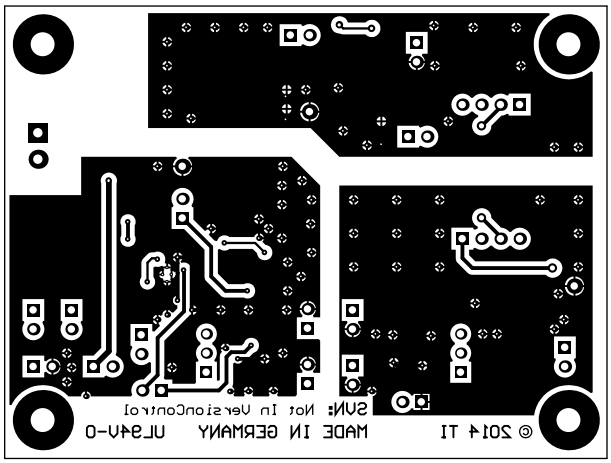


Figure 75. Bottom Layer

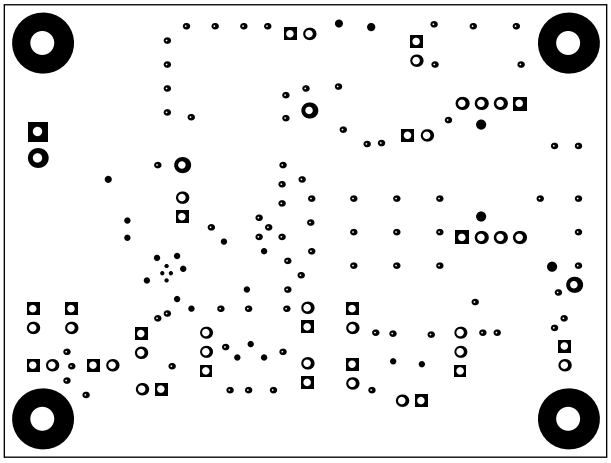


Figure 76. Bottom Solder Mask

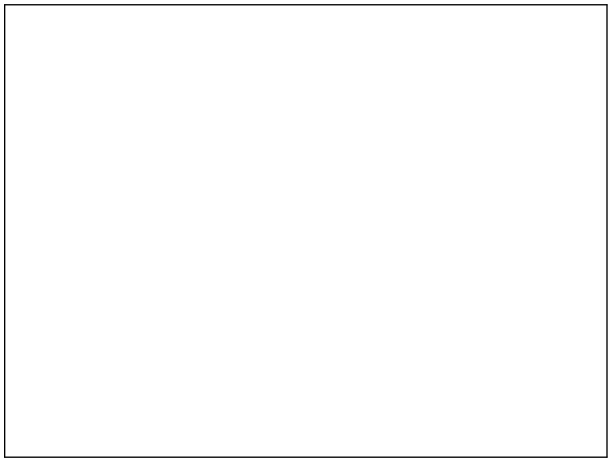
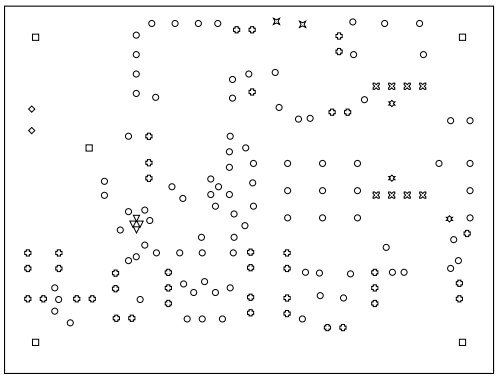


Figure 77. Bottom Overlay



Symbol	Hit Count	Tool Size	Plated	Hole Type
▽	4	7.874mil (0.2mm)	PTH	Round
○	94	10mil (0.254mm)	PTH	Round
□	1	15mil (0.381mm)	PTH	Round
⌑	2	18mil (0.457mm)	PTH	Round
✡	3	28mil (0.711mm)	PTH	Round
⊠	8	39.37mil (1mm)	PTH	Round
✪	41	40mil (1.016mm)	PTH	Round
◇	2	50mil (1.27mm)	PTH	Round
□	4	125.984mil (3.2mm)	PTH	Round
	159 Total			

Drill Table

Figure 78. Drill Drawing

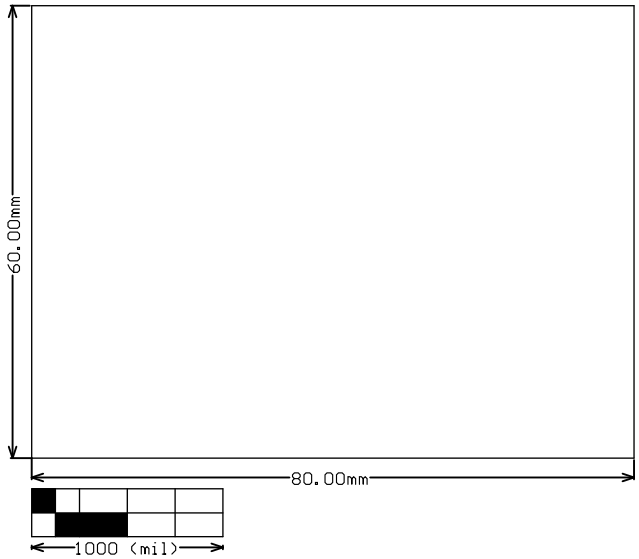


Figure 79. Board Dimensions

9.4 Altium Project

To download the Altium project files, see the design files at TIDA-00167.

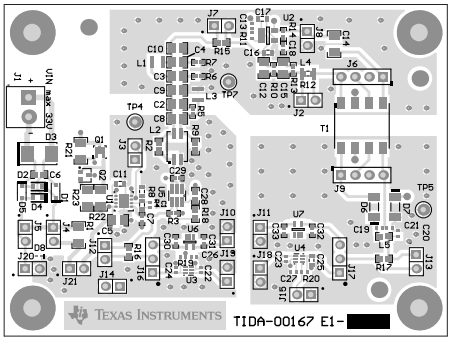


Figure 80. Top Components and Silkscreen

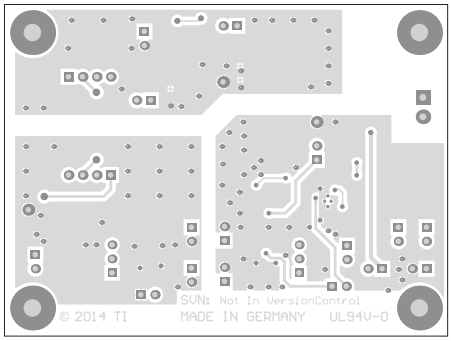


Figure 81. Bottom Components and Silkscreen

9.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00167.

9.6 Assembly Drawings

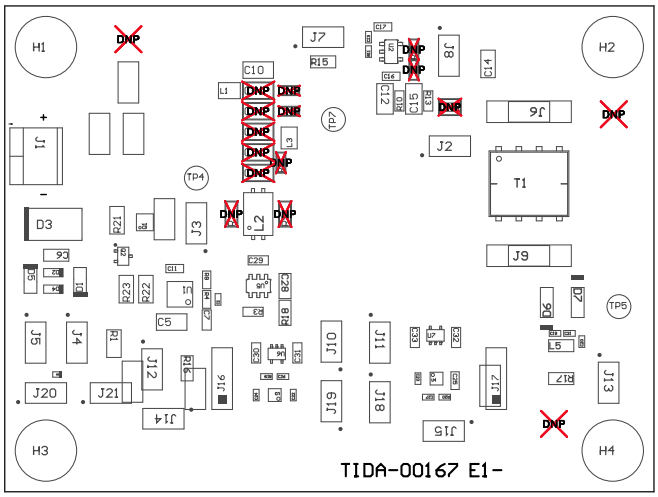


Figure 82. Top Assembly Drawing

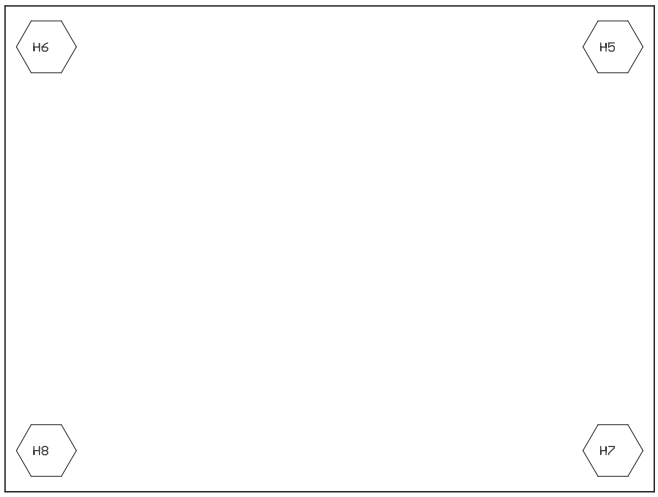


Figure 83. Bottom Assembly Drawing

10 References

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12. Data Sheet, *TPS7A1601 60-V, 5-µA IQ, 100-mA, Low-Dropout Voltage Regulator with Enable and Power Good*, (SBVS171).
13. Data Sheet, *TPS60400, TPS60401, TPS60402, TPS60403 UNREGULATED 60-mA CHARGE PUMP VOLTAGE INVERTER* (SLVS324).
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15. Data Sheet, *TPS715xx 50 mA, 24 V, 3.2-µA Supply Current Low-Dropout Linear Regulator in SC70 Package* (SLVS338).
16. Data Sheet, *PMLL4153 High-speed diode* (PMLL4153).
17. Data Sheet, *SMD Switching Diode CDSU101A (Lead-free Device) High Speed* (CDSU101A).
18. Data Sheet, *BAT46WJ Single Schottky Barrier Diode* (BAT46WJ).

11 About the Author

JÜRGEN SCHNEIDER is a systems engineer at Texas Instruments where he is responsible for developing TI-Designs for the industrial automation segment. He holds a Dipl.-Ing. (FH) degree in Industrial Electronics and he worked 13 years as a design engineer for semiconductor manufacturing equipment, telemetry systems and electro-medical devices before he joined TI in 1999. With TI he worked as an analog field specialist, FAE, and systems engineer for power solutions. He presents at technical conferences and seminars, is one of the presenters of the industry-wide known TI Power Supply Design Seminar, and was elected as Member, Group Technical Staff.

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