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TIDA-00287 2-Port USB 3.0 Hub Reference Design

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Design Resources

TPD6E05U06	IEC ESD Protection Diodes
TUSB8020B	2-Port USB Hub
TPS2553	Power Distribution Switch
TLV70033	LDO Linear Regulator
LM3674	600-mA Buck Converter

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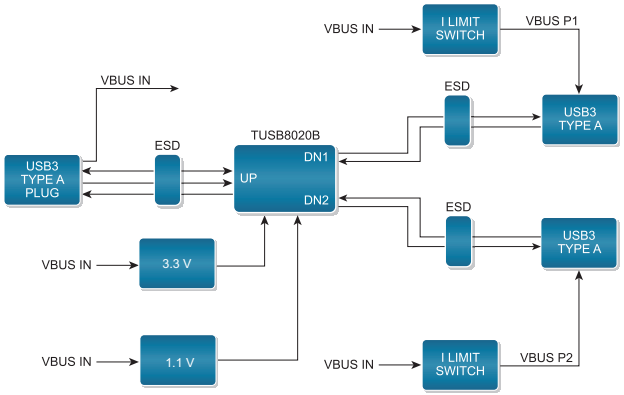
Design Features

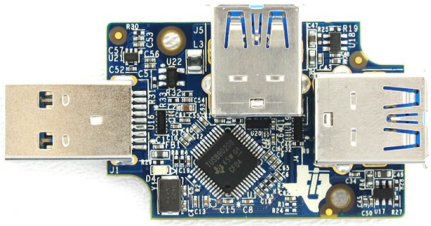
The TIDA-00287 is a fully functioning 2-port USB 3.0 hub:

- Supports individual port power control
- ESD protection on both upstream and downstream ports
- Operates as a bus-powered device (all power being supplied by the upstream host or hub)
- Supports operation as a USB 3.0 and USB 2.0 device

Featured Applications

- Computer systems
- Docking stations
- Monitors
- Set-top boxes





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1 Circuit Description

The USB 3.0 Hub Design is a two-port USB 3.0 compliant hub. It provides simultaneous SuperSpeed and high-speed/full-speed connections on the upstream port and provides SuperSpeed, high-speed, full-speed, or low-speed connections on the downstream ports. The hub design provides power control for each downstream port and overcurrent protection

2 Theory of Operation

A block diagram of the design in Figure 1 shows a USB 3.0 Hub with a Type A plug upstream port and two USB 3.0 Type A downstream ports. Power for the design is shown as well as ESD protection elements on the upstream and downstream sides of the hub. Downstream port current limiting is provided by two TPS2553 (Adjustable Current-Limited Power-Distribution Switch) devices.

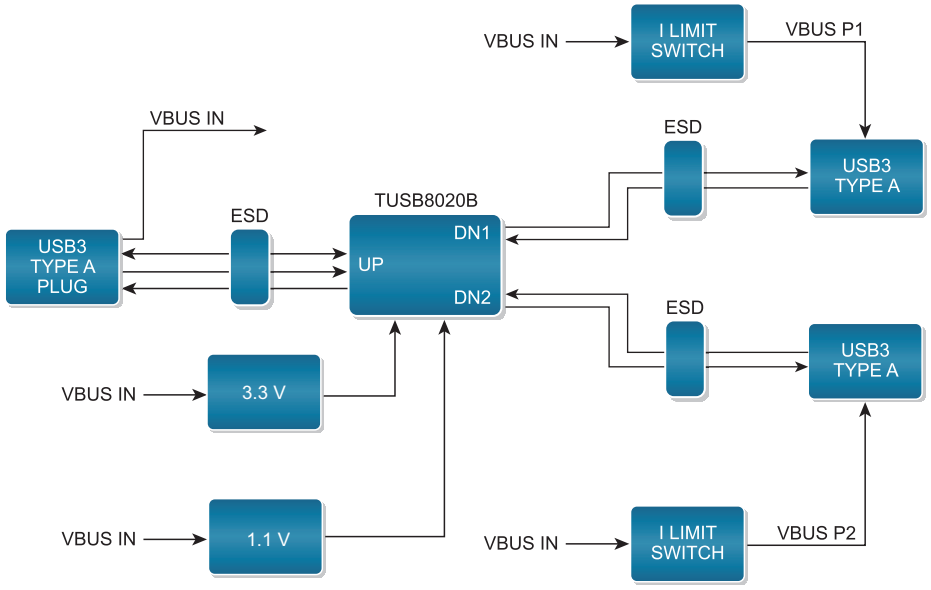

Figure 1. TIDA-00287 Functional Block Diagram

2.1 TUSB8020B

The TUSB8020B is a two port USB 3.0-compliant hub device. It provides SuperSpeed and high/full speed connections on the upstream port. It also supports SuperSpeed, high/full speed or low-speed connections on the downstream ports. When the upstream port is connected to an environment that supports only high-speed or full-speed/low-speed connections, SuperSpeed is disabled on the downstream ports. When the upstream port is connected to an environment that supports only full-speed/low-speed connections, SuperSpeed and high-speed are both disabled on the downstream ports.

The hub supports overcurrent protection and battery charging as well as either ganged switching or per port power switching.

The USB 3.0 hub is configured with the de-assertion of RESET. Refer to Table 1 for the default values.

Table 1. TUSB8020B Power-on Reset Settings

TUSB8020B Function	Status
Downstream port power management	Enabled
Power control signal polarity	Signals are active high
Power port control	Ganged Power control supported

2.2 System Power

The main power on the board is 5 V and is supplied by the upstream USB port. Figure 2 shows the configuration of the board's power system. The 5 V coming from the upstream USB port is regulated down to 3.3 V through a TLV70033 LDO regulator. An LM3674 switching regulator is used to supply 1.1-V power for the core voltage to the TUSB8020B. The 5-V power is also passed to the TPS2553 current-limiting switches that supply power to the down-stream ports.

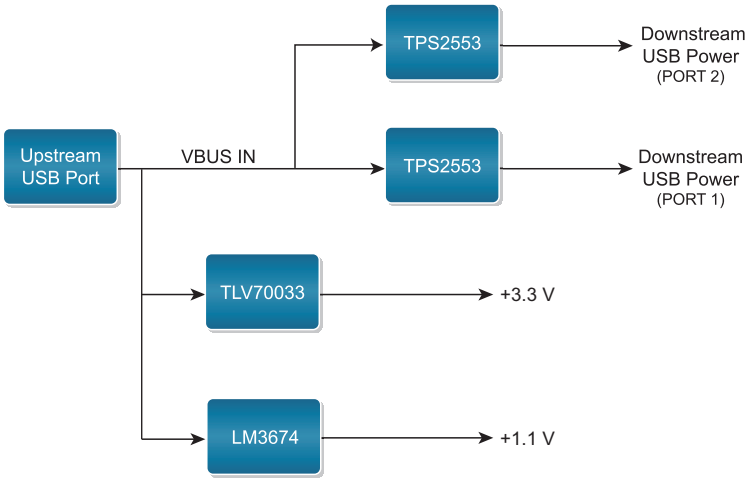

Figure 2. Power Subsystem

2.3 Downstream USB Power Delivery

USB power for downstream ports is provided by two TPS2553 (Adjustable Current-Limited Power-Distribution Switch). These switches are controlled by the USB hub chip, and have adjustable current limits on the outputs. This design is set for a current limit of 901.5 mA (typical).

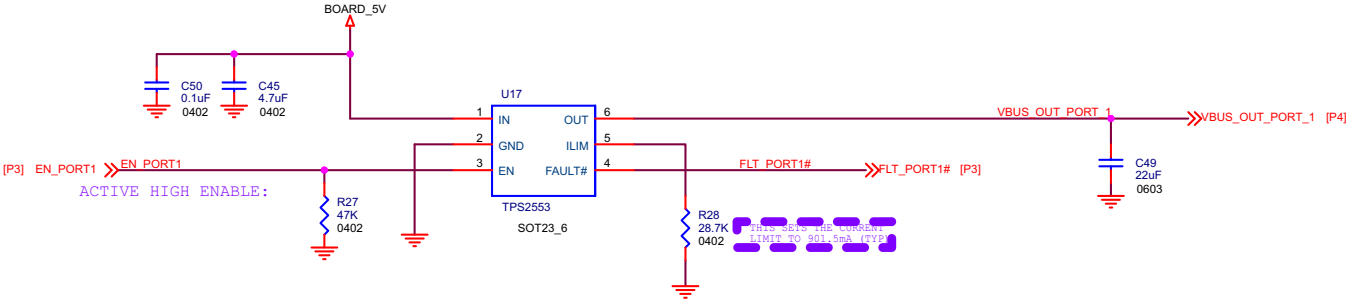

Figure 3. Downstream Power Delivery

3 Component Selection

All components contained in this design are chosen to provide a low-cost solution when purchased in large quantities, while minimizing component count and maintaining performance to satisfy the design criteria.

3.1 Hub Selection

The TUSB8020B was chosen as a low cost 2 port USB 3.0 hub. It supports both USB 3.0 and USB 2.0 for both upstream and downstream ports. Battery charging can be supported as can be per-port or ganged power switching. An OTP ROM is included for custom 3rd party VID/PID and device configuration. There are no special drivers required for this hub.

3.2 Downstream Power Switches

This design uses two TPS2553 current-limited power distribution switches. These parts have adjustable current limits that can be set by an external resistor. Both ports have been designed to deliver ~900 mA. It should be noted that some USB 3.0 ports can supply far in excess of the minimum 900-mA current. If the upstream USB 3.0 port that the hub is plugged into can provide in excess of 1.8 A, then both downstream ports will support the full 900 mA of current.

3.3 ESD Components

ESD protection for all USB ports is supplied by the TPD6E05U06 devices. This part provides ESD protection for 3 differential pairs at data speeds of up to 6GBps and has low capacitance of 0.5 pF. Each USB port uses one of these parts to protect the port. The package allows for *straight through* routing and is placed as close to the USB connector as possible. Application of ESD protection is recommended.

3.4 2-Port Power

The main power for the board is +5 V. This is supplied from the upstream USB port only. The voltages for the hub are generated from 2 different regulators. U21 (TLV70033) takes the BOARD_5V and regulates it down to 3.3 V (refer to Figure 4). The TLV70033 is an LDO that is capable of supplying 200 mA. U22 (LM3674) generates the 1.1-V power rail used for the TUSB8020B core voltage. Figure 5 shows schematics of the power supply circuitry for the hub. The circuit was designed using TI's Webench Design Tool, and selected for the small PCB footprint and low component cost.

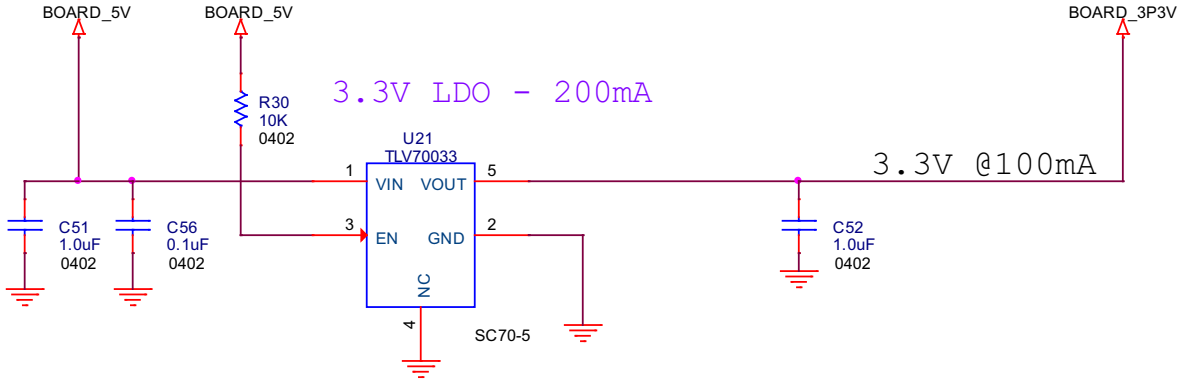

Figure 4. TUSB8020B Power Supply (TLV70033)

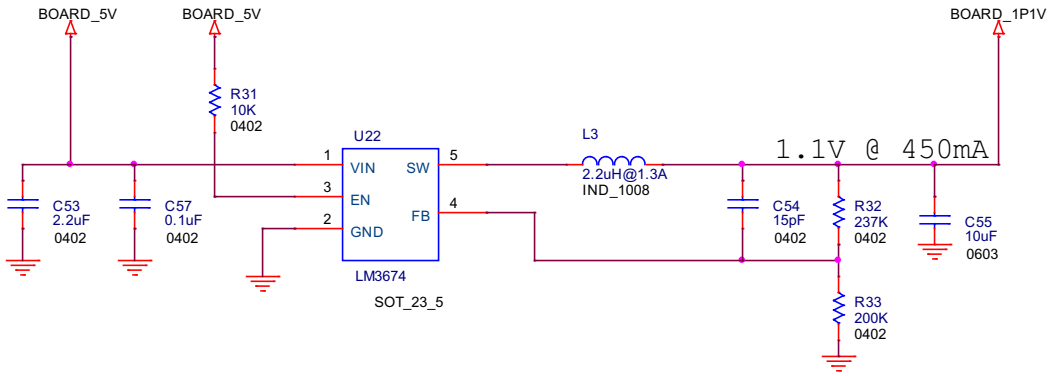

Figure 5. TUSB8020B Power Supply (LM3674)

4 PCB Design

The PCB stack-up design was chosen to accommodate the 90-Ω impedance of USB 3.0 signal traces. A trace width of 4.4 mils and differential pair spacing of 5 mils is used with this layout. All USB 3.0 traces are routed on the top side of the board and references a solid ground plane that is layer 2. Layer 3 is the power layer and includes the 5- and 1.1-V supplies. The bottom side, layer 4, is where the 3.3-V supply is routed as well as all other traces. To simplify the assembly process, all components are placed on the top side of the board. Figure 6 through Figure 11 show the layout for all 4 layers as welll as the silk screens

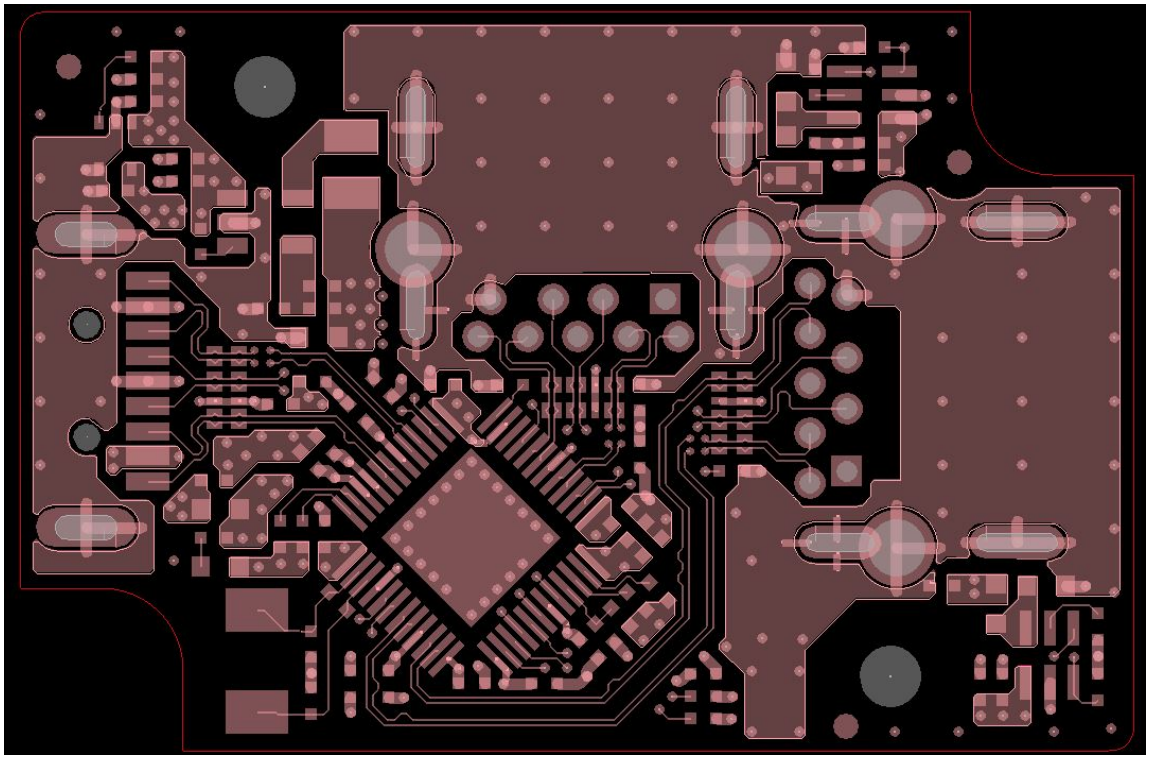

Figure 6. Top Layer – USB 3.0 Routes

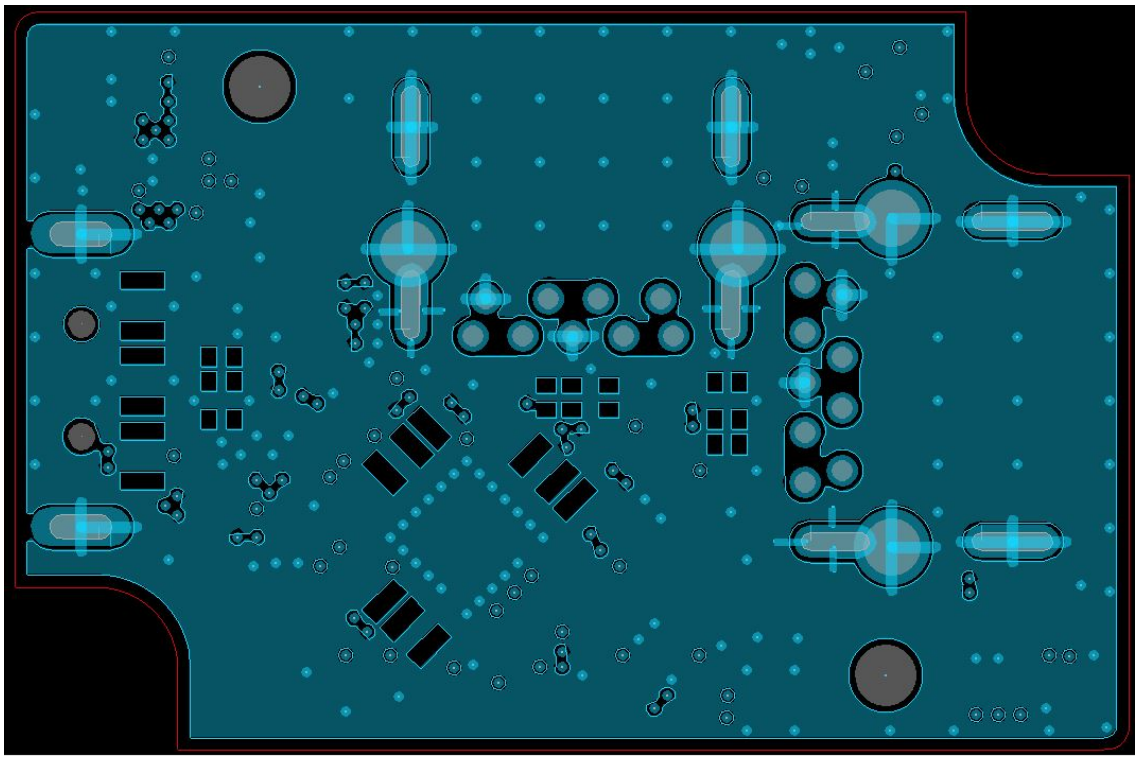

Figure 7. Layer 2 – Ground Plane

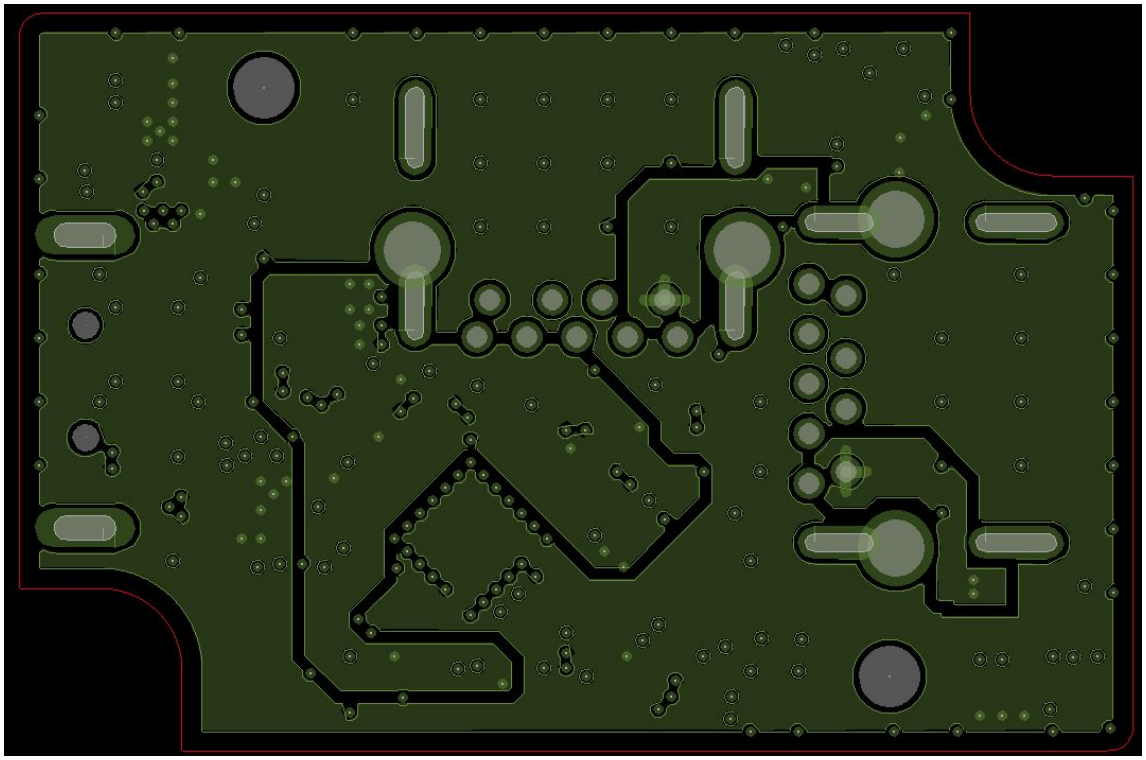

Figure 8. Layer 3 – Power Plane (+5 V and +1.1 V)

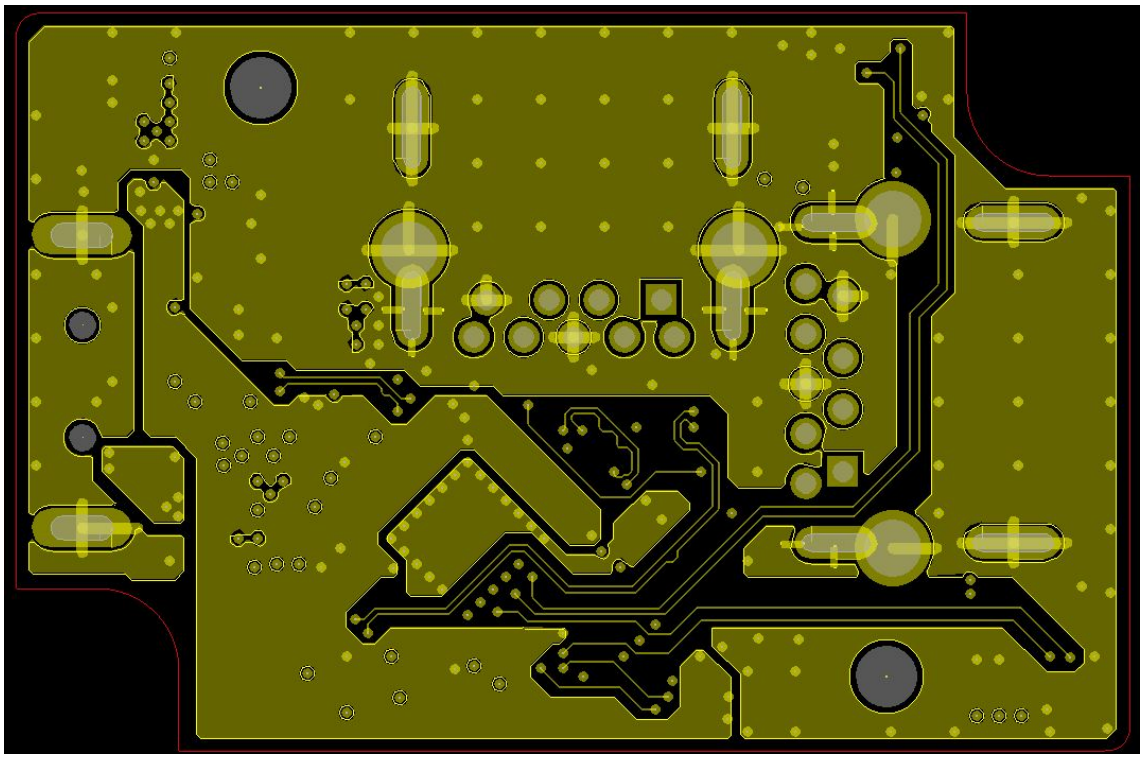

Figure 9. Bottom Side - +3.3-V Power and Routing

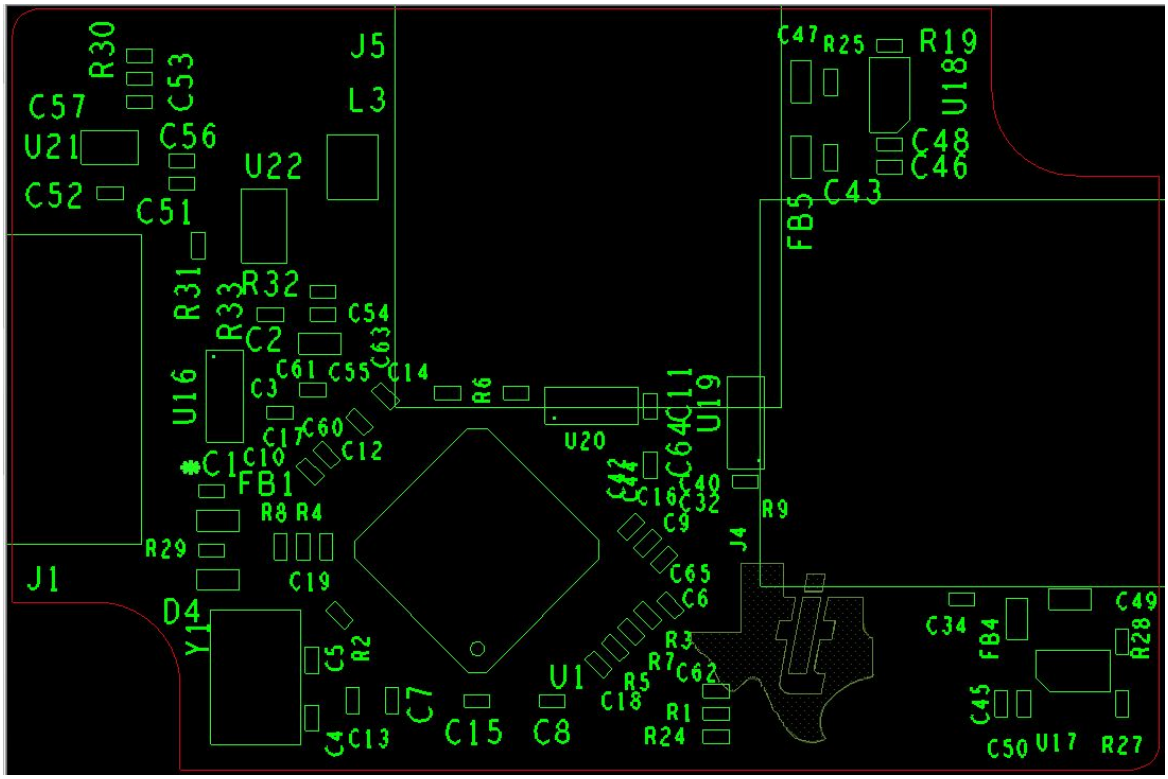

Figure 10. Top Side Silk Screen

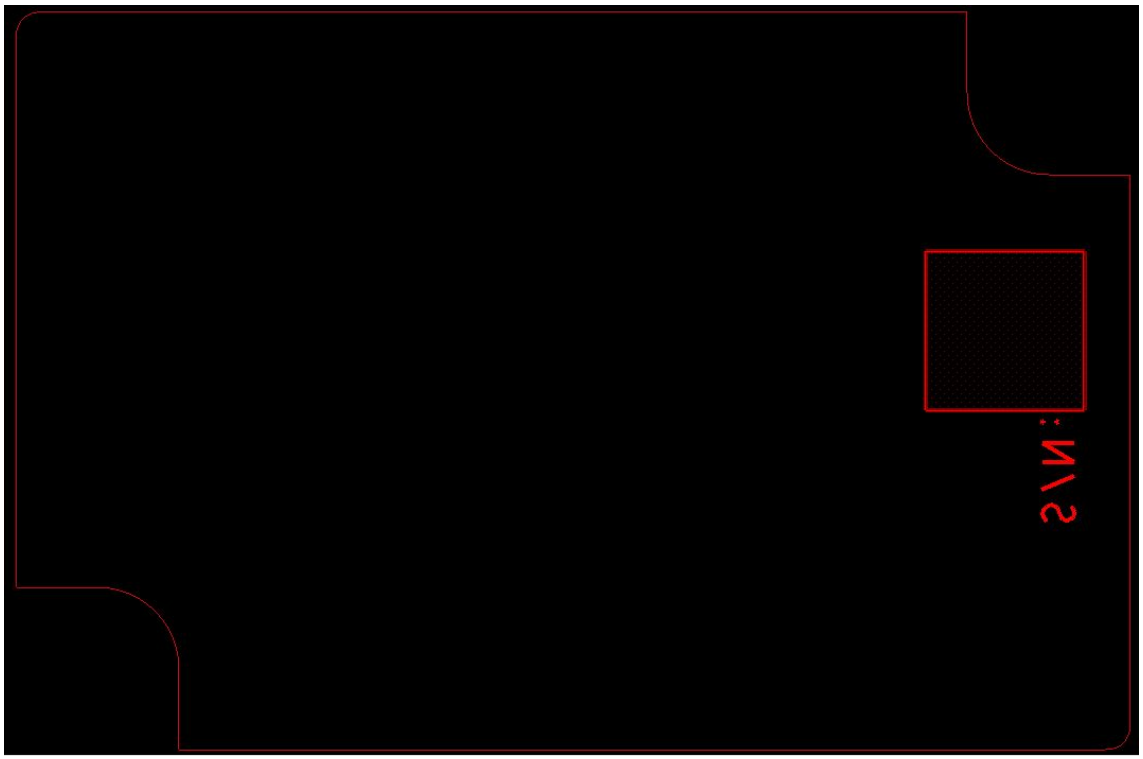

Figure 11. Bottom Side Silk Screen

4.1 Layout Guidelines

All USB 3.0 and USB 2.0 lines must be routed as controlled impedance, high-speed differential pairs. Minimize the use of vias and 90 degree corners in the routing of the high-speed lines. Assure the high-speed lines reference a solid ground plane and the plane is void of cuts and splits to prevent impedance discontinuities. ESD connection points need to be placed *in-line* with the high-speed signal traces to reduce reflections caused by routing discontinuities.

4.2 PCB Stack-up

Figure 12 shows the PCB stack-up used for the TIDA-00287 reference design.

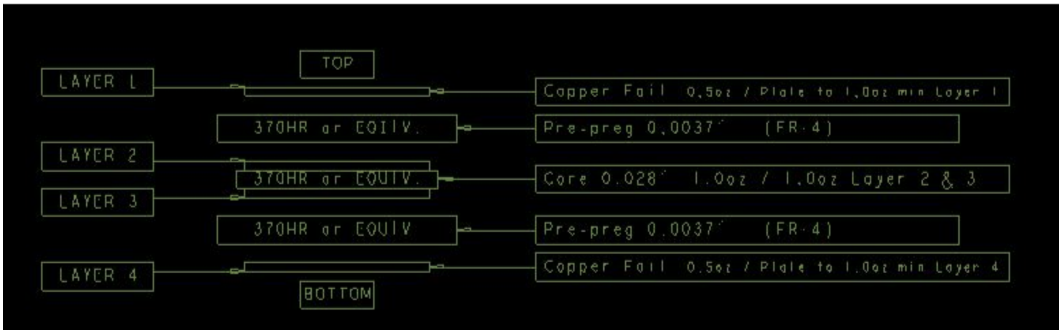

Figure 12. PCB Stack-up

5 Verification and Measured Performance

5.1 Compliance Testing

5.1.1 USB 2.0 – Downstream Port 1

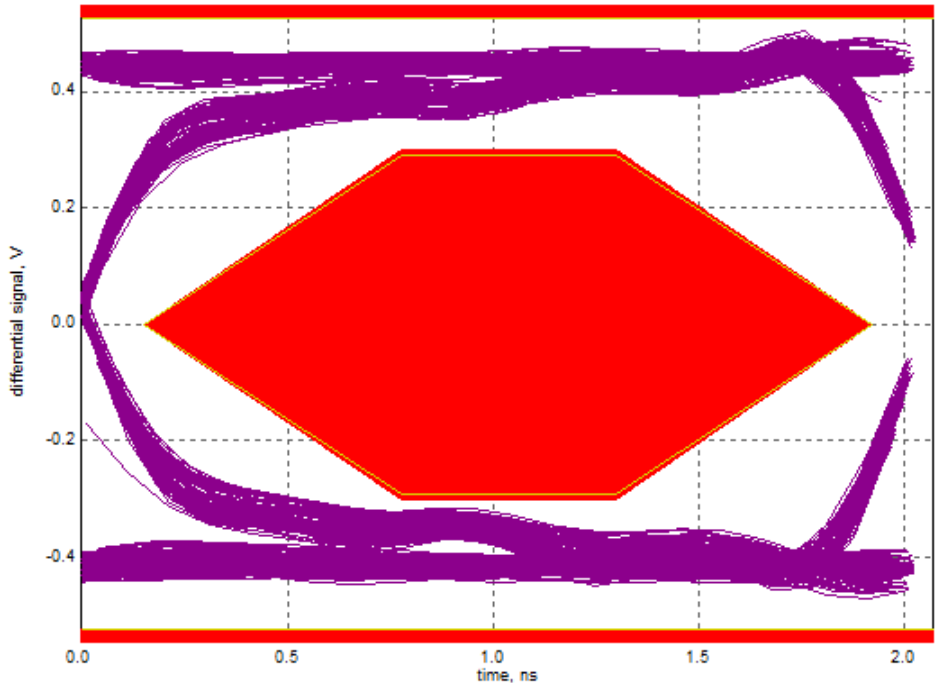

Figure 13. USB 2.0 Downstream Signal Quality Eye Diagram - Port 1

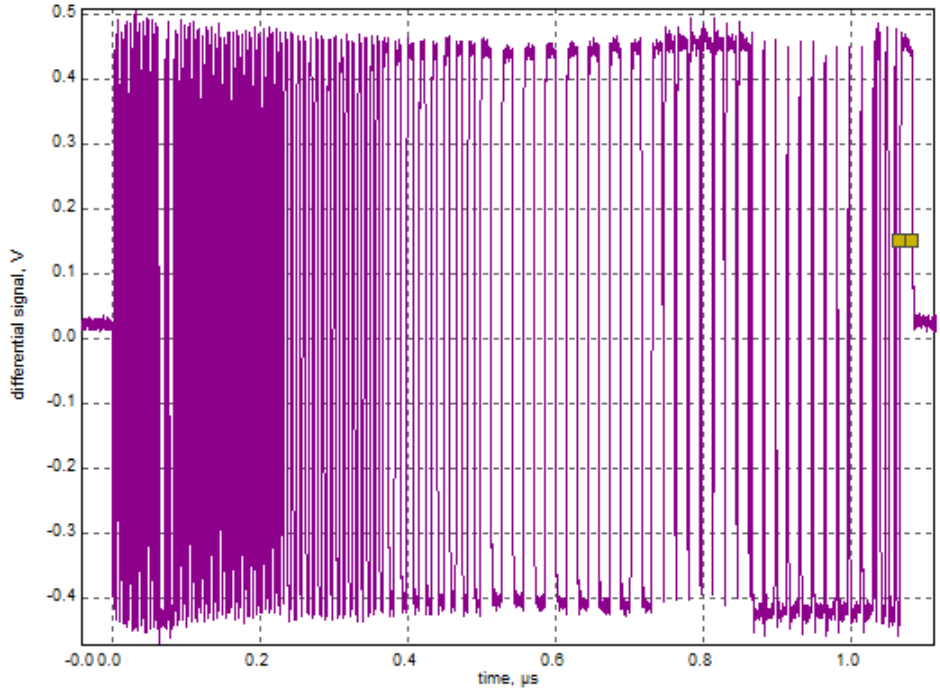

Figure 14. USB 2.0 Downstream Signal Quality Plot - Port 1

5.1.2 USB 2.0 – Downstream Port 2

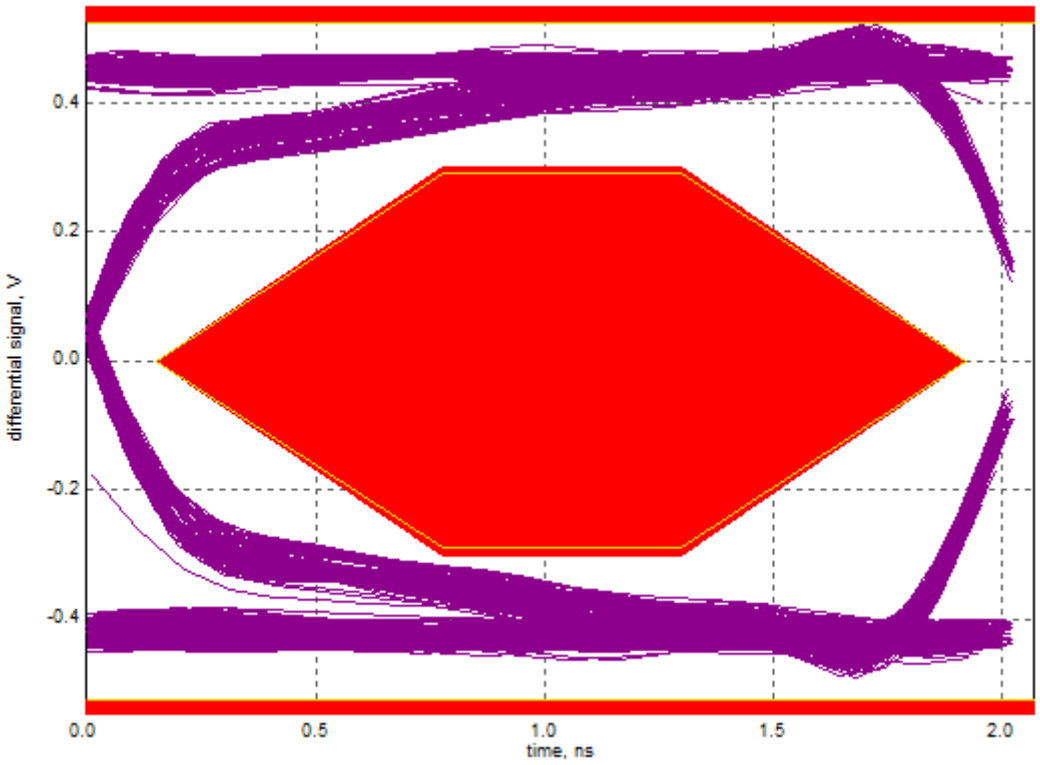

Figure 15. USB 2.0 Downstream Signal Quality Eye Diagram - Port 2

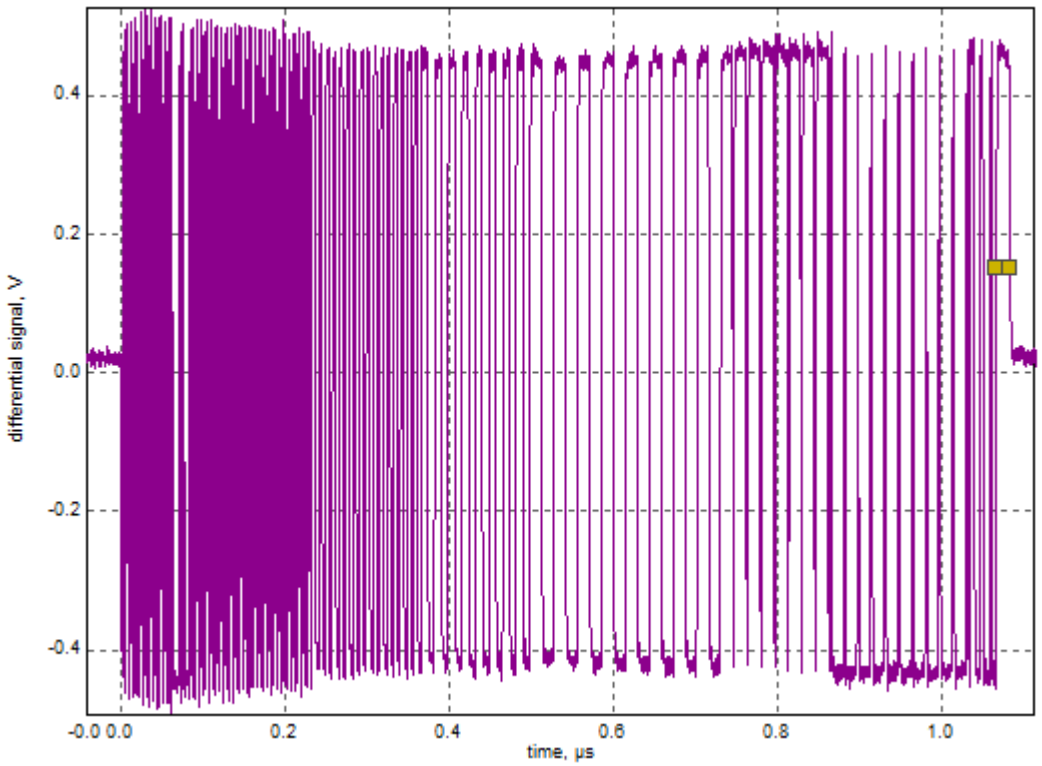

Figure 16. USB 2.0 Downstream Signal Quality Plot - Port 2

5.1.3 USB 2.0 – Downstream Port 1 without ESD Protection

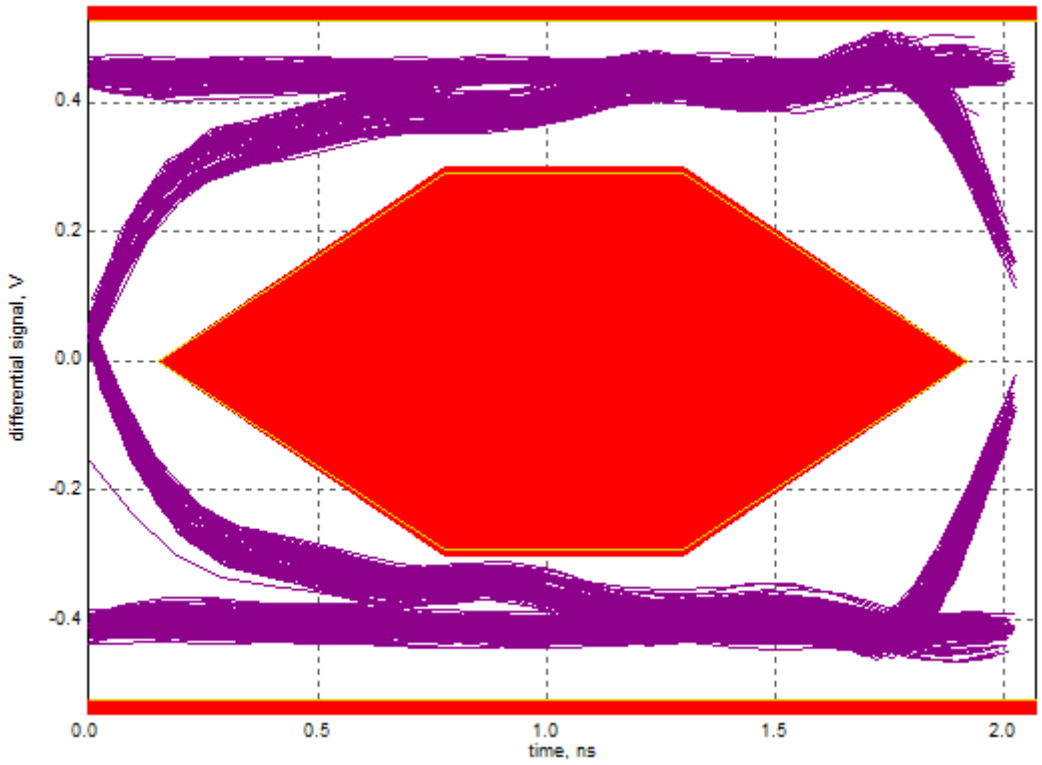

Figure 17. USB 2.0 Downstream Signal Quality Eye Diagram - Port 1 Without ESD Protection Device

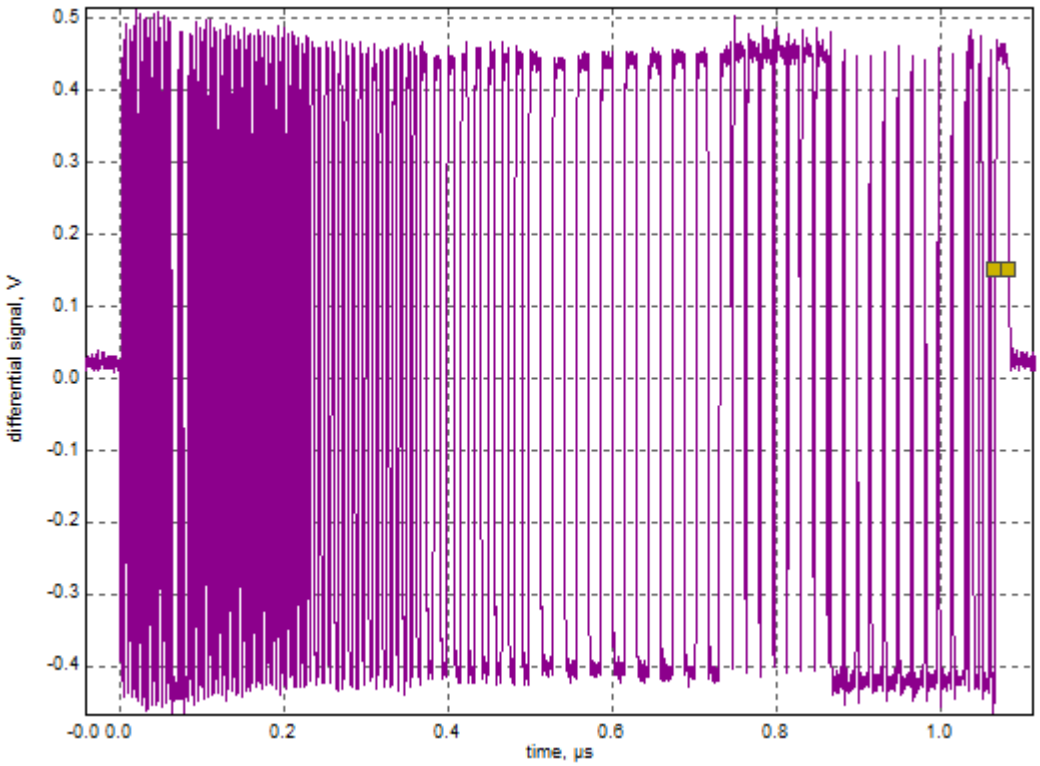

Figure 18. USB 2.0 Downstream Signal Quality Plot - Port 1 Without ESD Protection Device

5.1.4 USB 2.0 – Downstream Port 2 without ESD Protection

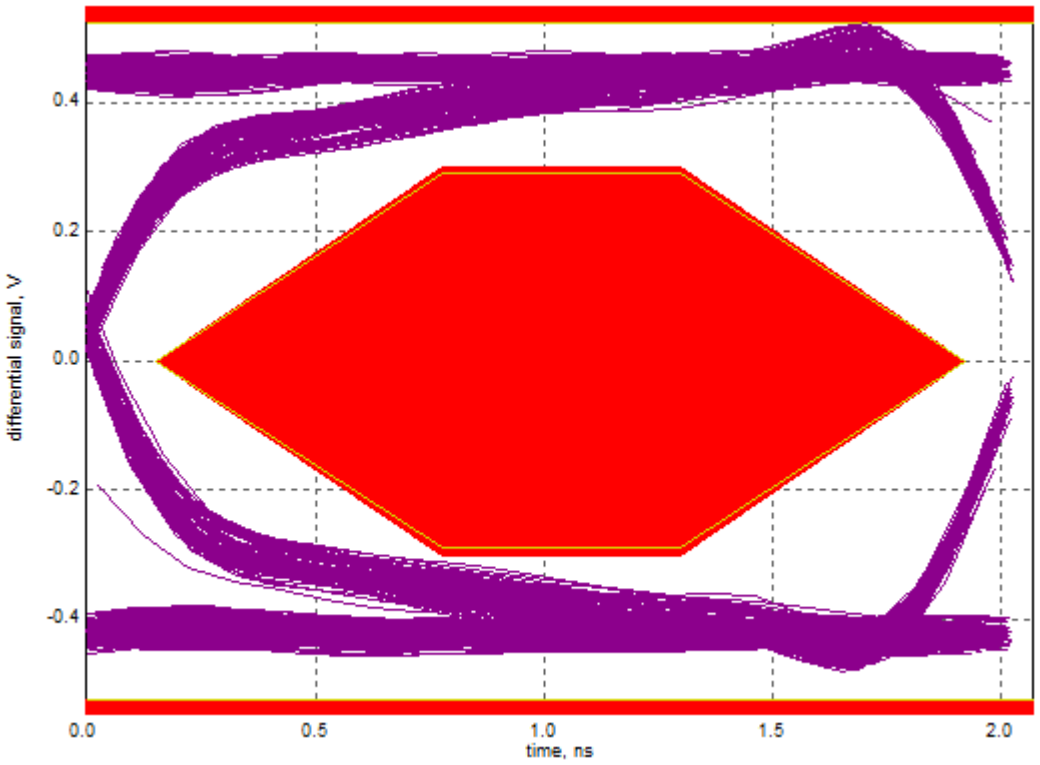

Figure 19. USB 2.0 Downstream Signal Quality Eye Diagram - Port 2 Without ESD Protection Device

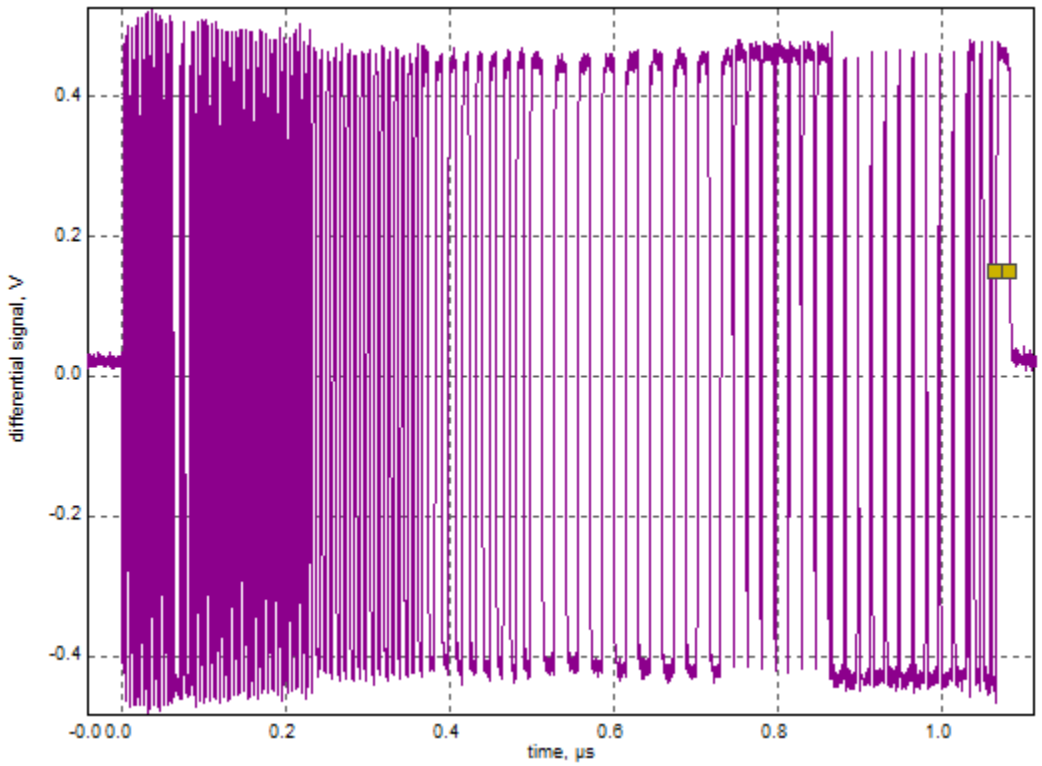

Figure 20. USB 2.0 Downstream Signal Quality Plot - Port 2 Without ESD Protection Device

5.1.5 USB 3.0 – Downstream Port 1

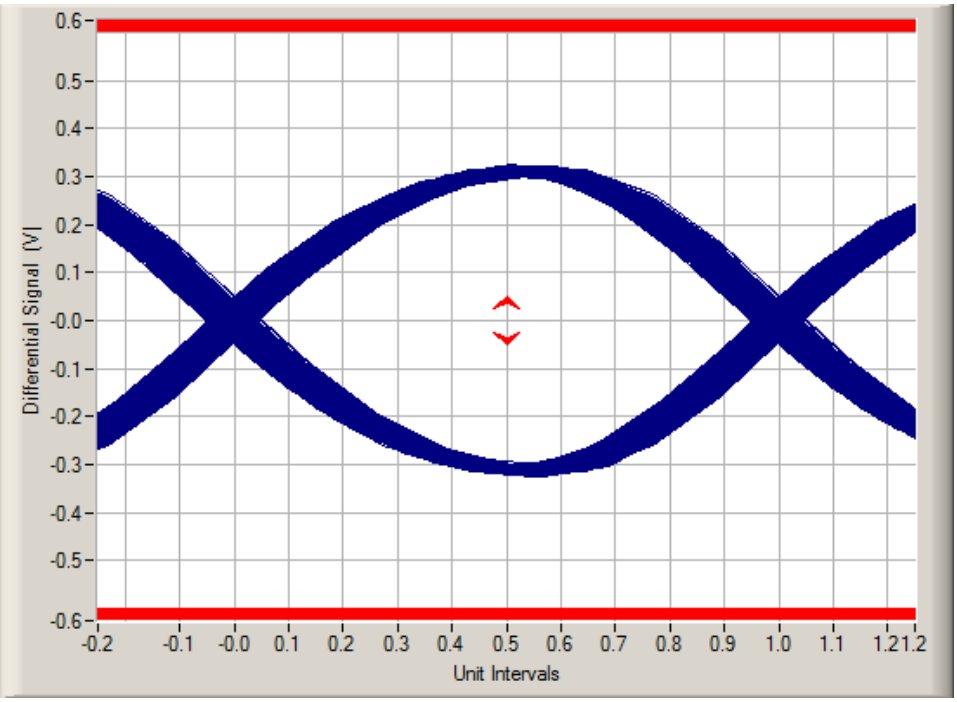

Figure 21. USB 3.0 Downstream CP1 Eye Diagram - Port 1

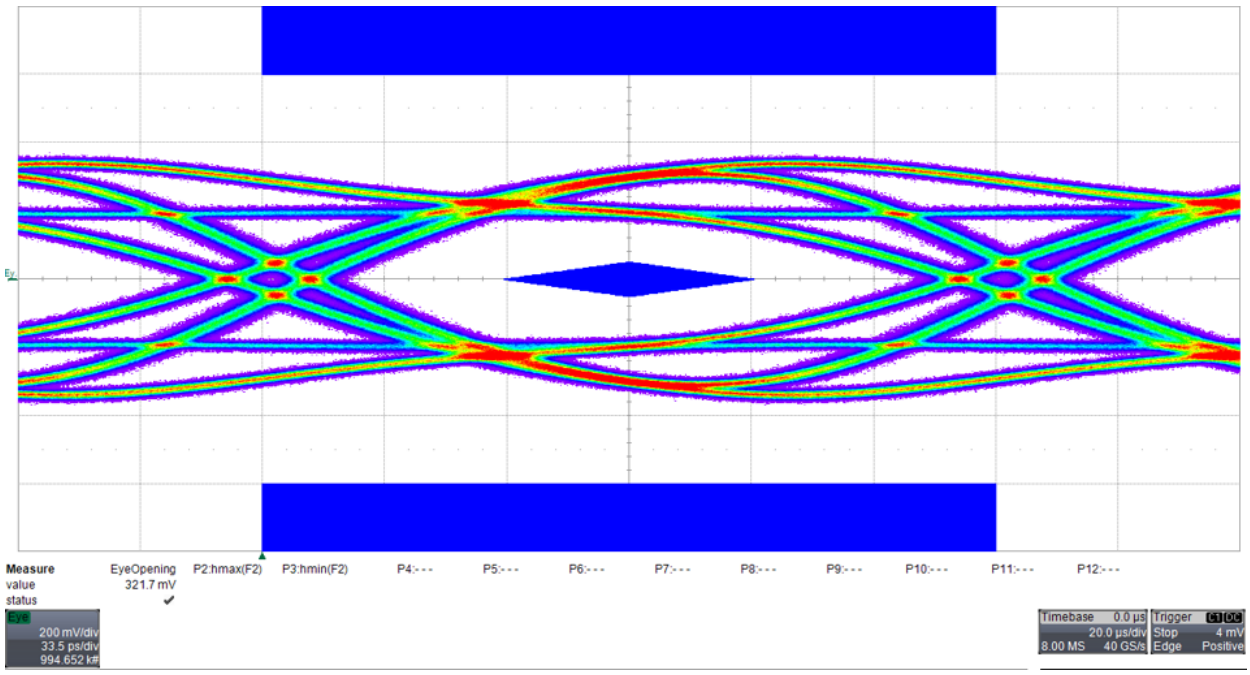

Figure 22. USB 3.0 Downstream CP0 Eye Diagram - Port 1

5.1.6 USB 3.0 – Downstream Port 2

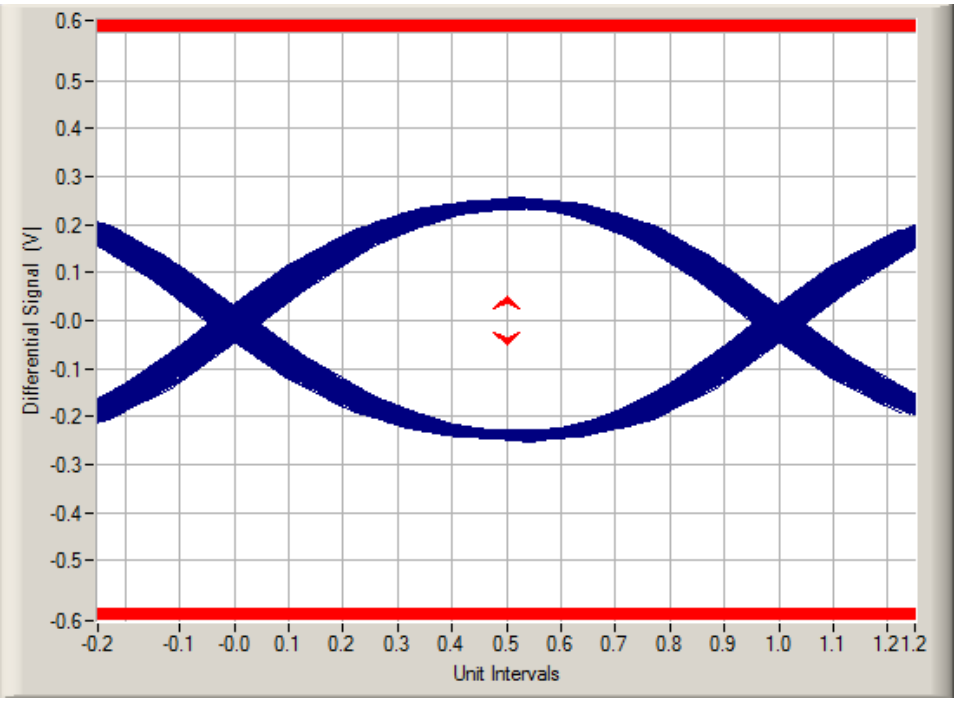

Figure 23. USB 3.0 Downstream CP1 Eye Diagram - Port 2

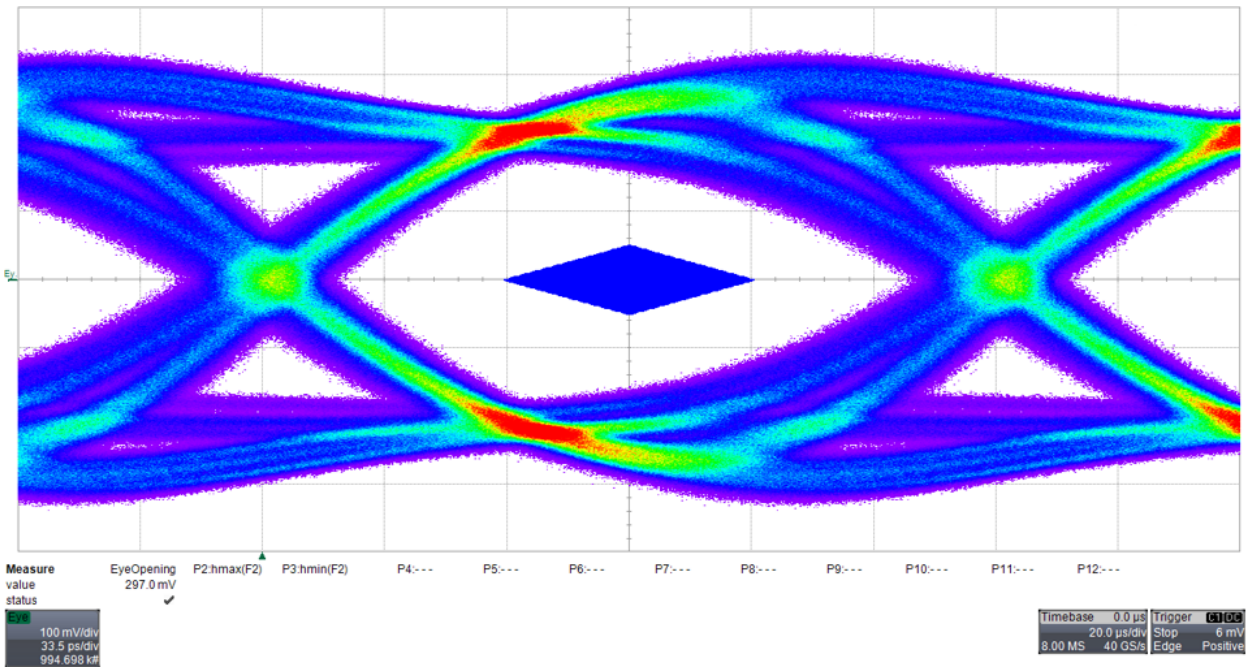

Figure 24. USB 3.0 Downstream CP0 Eye Diagram - Port 2

6 Design Options

This section discusses different design *options* that were evaluated for this project to give the designer flexibility to modify the design.

6.1 ESD Protection

We chose the TPD6E05U06 part to provide ESD protection on this design. It was also chosen due to its small size, capability to provide protection of up to 3 differential pairs, and low capacitance. The package allows for *flow-through* routing. Another option is using 3 single package parts for each USB connector (TPD2EUSB30). This allows more flexibility in board routing.

6.2 TUSB8020B Options

The TUSB8020B has an interface for an optional I2C EEPROM or SMBUS host. This can be used for storing vendor information and other *start-up* parameters. An I2C EEPROM like the AT24C04 or a SMBUS host can be connected to the serial interface for this purpose, but is not a design requirement. In this design a 24-MHz fundamental frequency crystal was used to generate the clock (CTS Frequency Controls #445C25D24M00000). Optionally, a 24-MHz oscillator can be used and connected to XI pin (pin 38). Table 2 lists the options for the TUSB8020B that are set at the rising edge of the Grst# pin (pin 11).

Table 2. Power-on Reset Options

Signal Name (Pin #)	Default	Condition
SMBUSz/SS_DN2 (pin 22)	Pull-Up	0 = SMBbus enabled
		1 = I2C enabled
FPMGT/SMBA1/SS_UP (pin 36)	Pull-Up	0 = downstream power switching supported
		1 = downstream power switch not supported
PWRCTL_POL/SS_DN1 (pin 21)	Pull-Down	0 = PWRCTL polarity is active high
		1 = PWRCTL polarity is active low
GANGED/SMBA2/HS_UP (pin 35)	Pull-Up	0 = Individual port power control supported
		1 = Ganged power control supported
PWRCTL/BATEN(pins 4 and 6)	Pull-Down	0 = Battery charging not supported
		1 = Battery charging supported

6.3 Power Delivery Options

TI has many options for providing power to downstream USB ports. In the reference design, the TPS2553 is used to reduce component count. This part has an adjustable current limit that is controlled by an external resistor. R28 is used to set the current limit on downstream port 1, and R25 for port 2. The equation used to calculate the current limit is as follows:

$$I_{OSnom}(mA) = \frac{23950\ V}{R_{ILIM}^{0.977}k\Omega} \quad (1)$$

6.4 Power Options

The TUSB8020B requires 1.1 V for core logic and 3.3 V for I/O logic. The current requirements can be seen in the datasheet (SLLSEF6), and TI has many power solutions. Since 3.3 V has a low-power requirement, a low-cost, low-component-count LDO was used to step down the BOARD_5V to 3.3 V. The 1.1-V power rail is generated by an LM3674 – step down switching regulator.

7 Schematic

Figure 25 through Figure 30 illustrate the electrical schematics for the TUSB8020B.

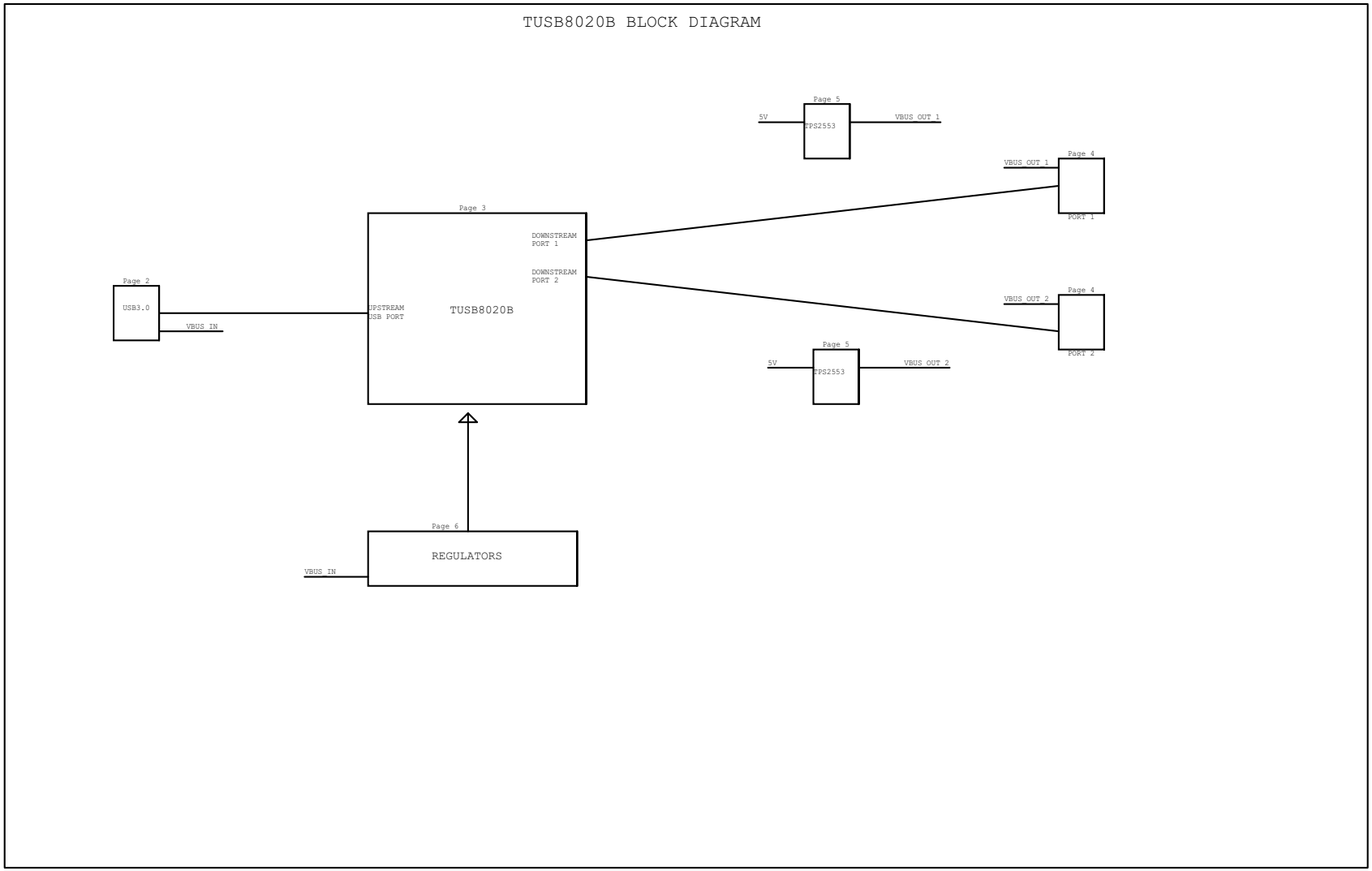

Figure 25. Schematic (1 of 6)

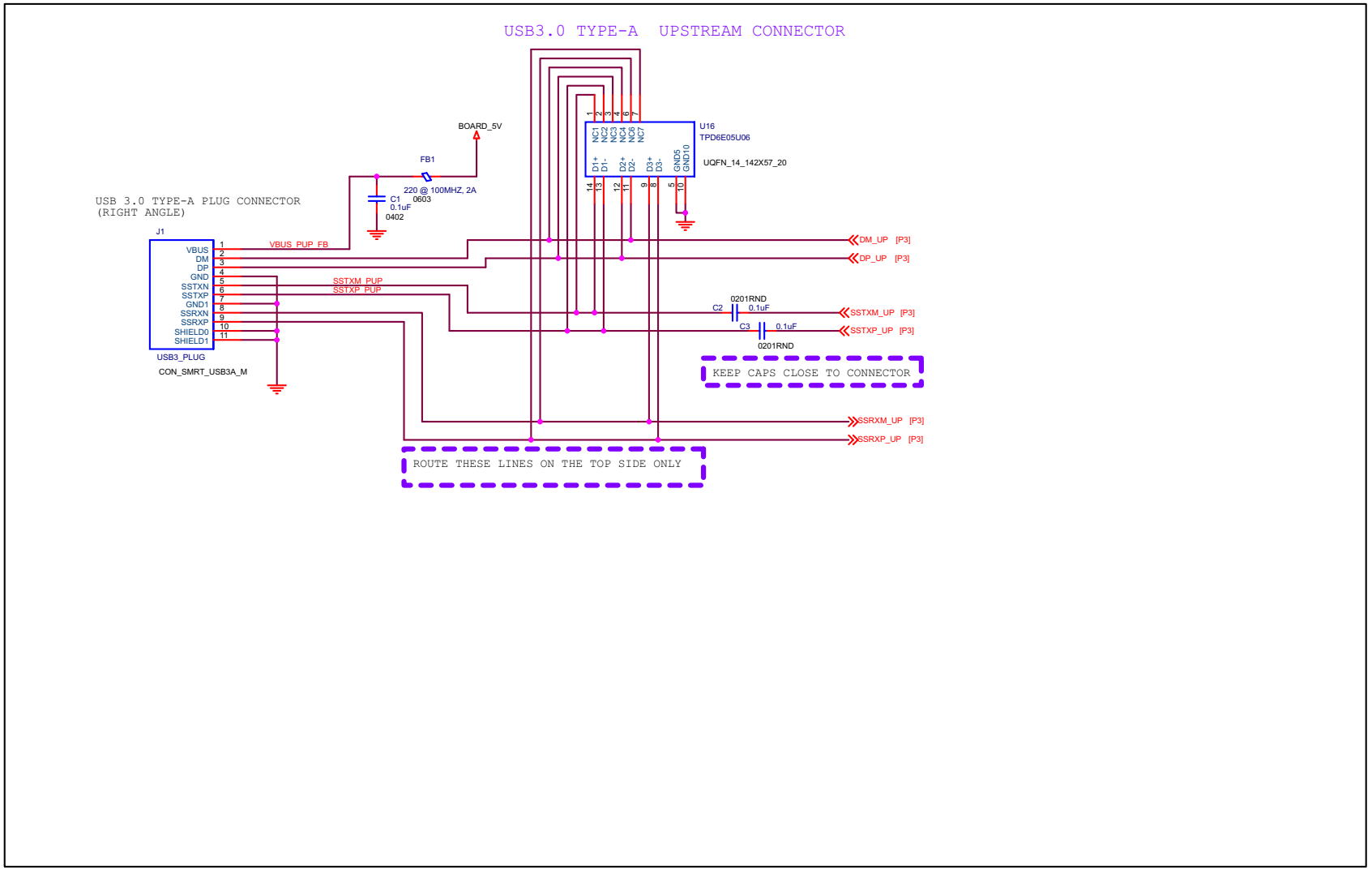

Figure 26. Schematic (2 of 6)

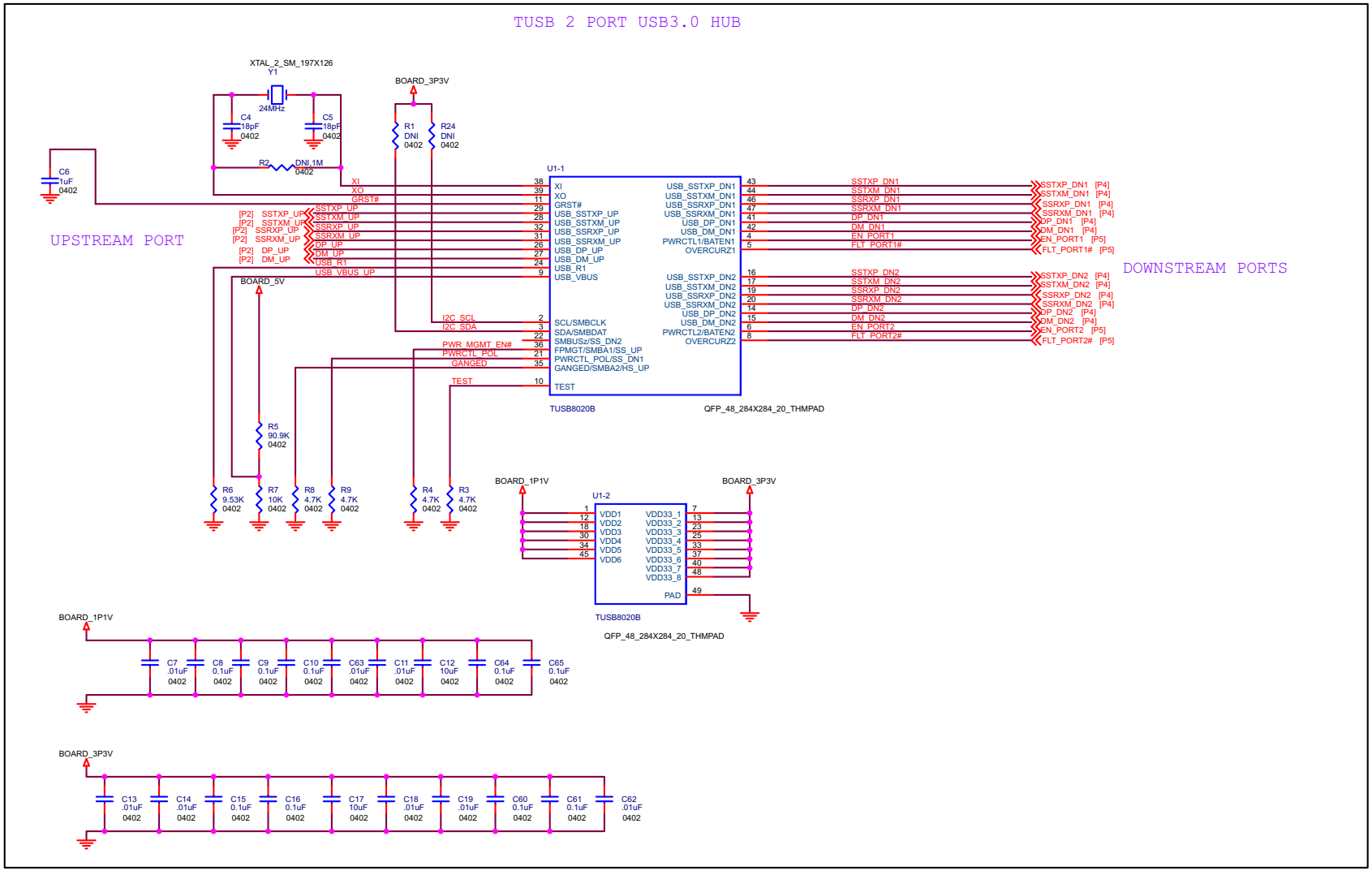

Figure 27. Schematic (3 of 6)

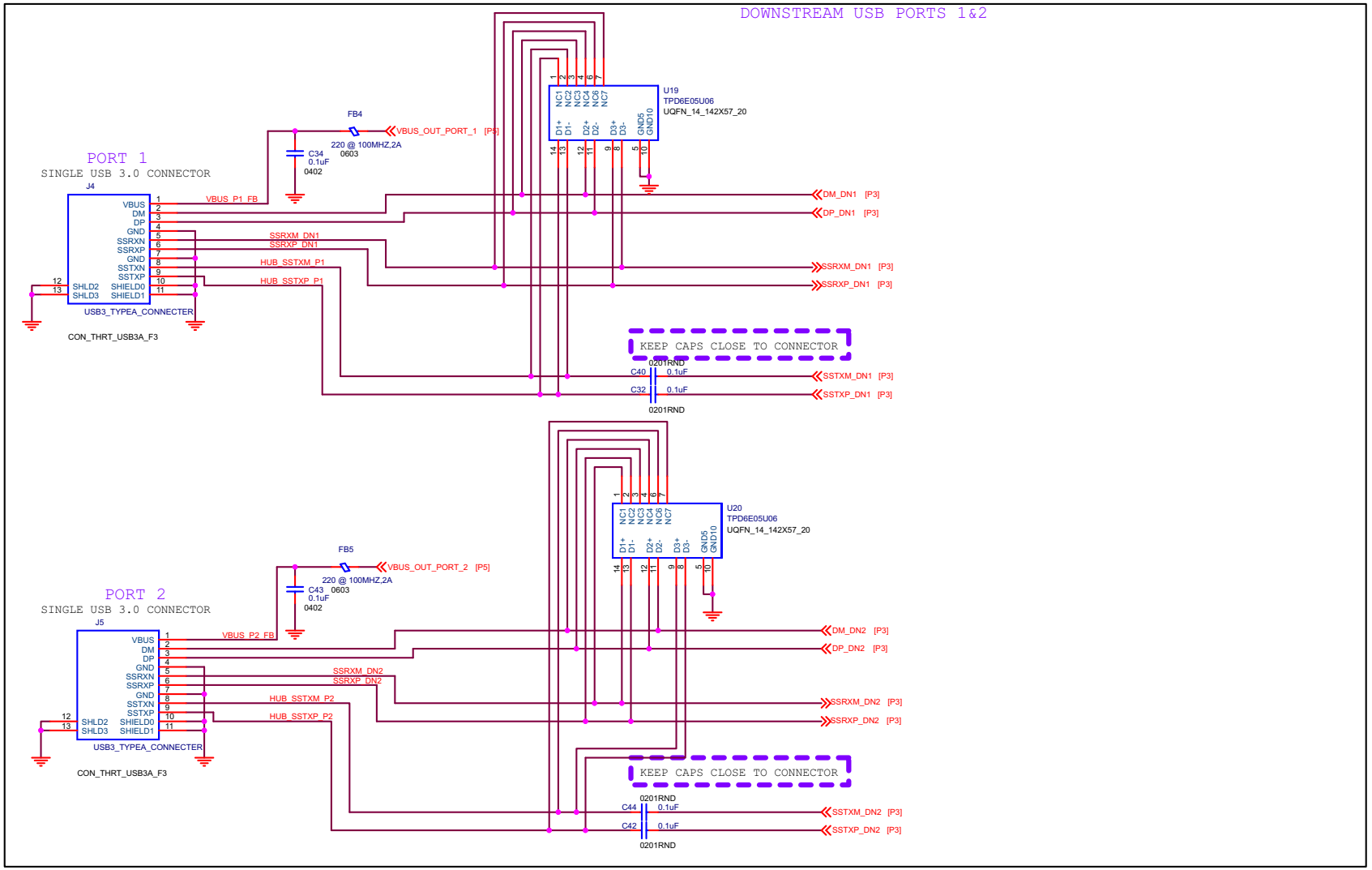

Figure 28. Schematic (4 of 6)

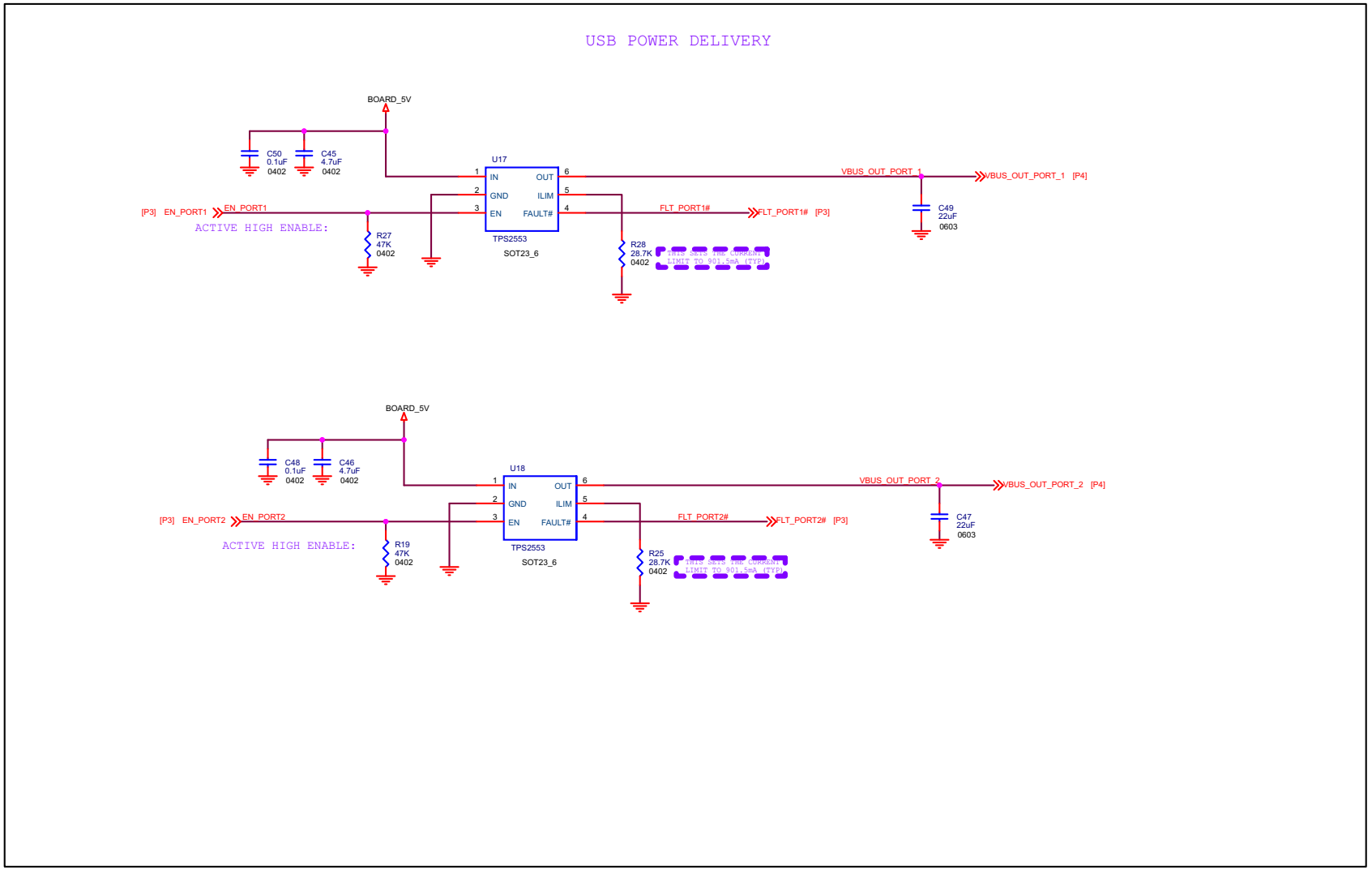

Figure 29. Schematic (5 of 6)

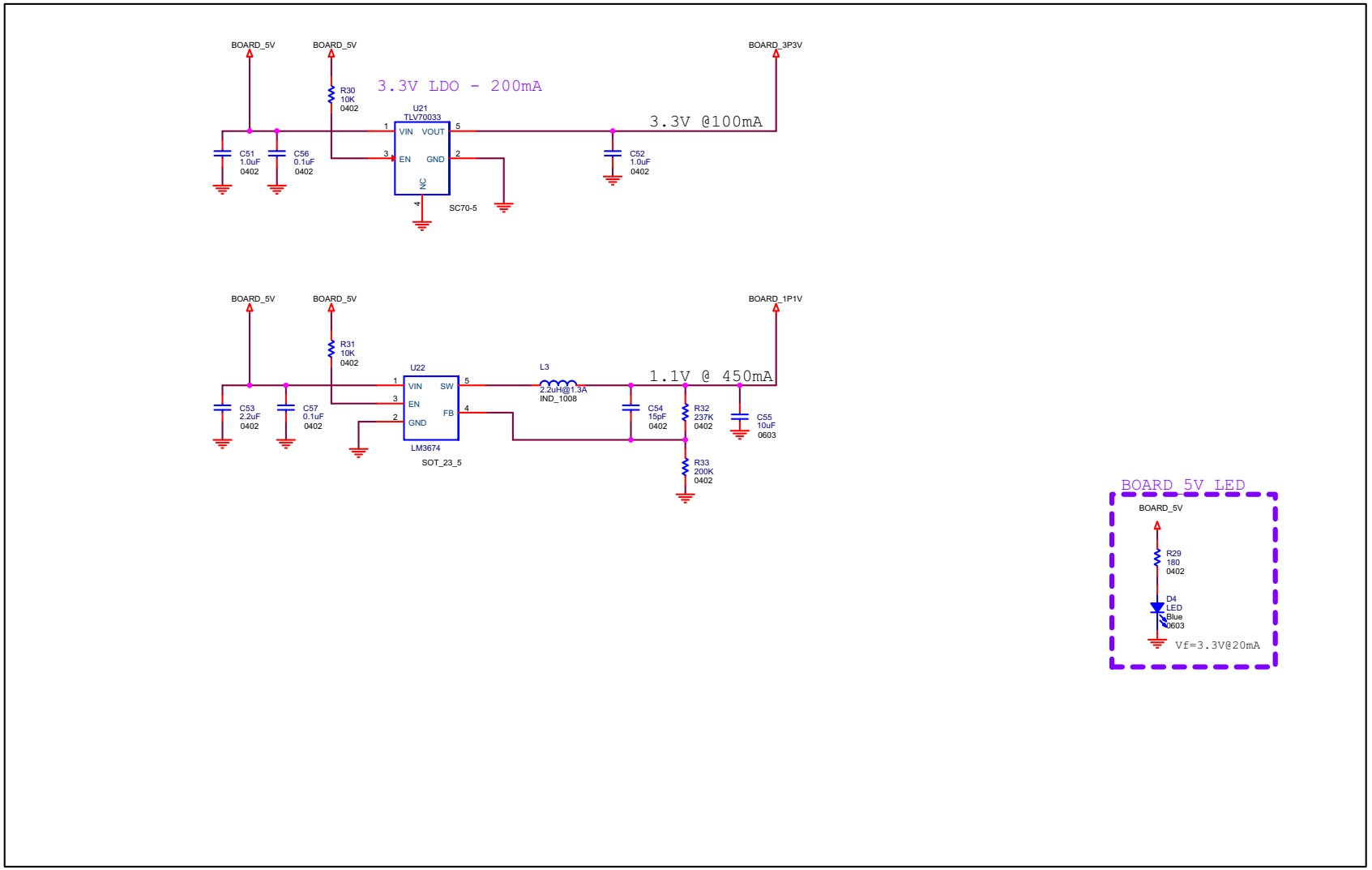

Figure 30. Schematic (6 of 6)

8 Bill of Materials

Table 3 lists the BOM for this reference design.

Table 3. Bill of Materials

Item	Qty	Reference	Value	Part Description	Manufacturer	Manufacturer Part Number	PCB Footprint
1	16	C1,C8,C9,C10,C15,C16,C34,C43,C48,C50,C56,C57,C60,C61,C64,C65	0.1uF	cap 0402, 0.1uF, +/- 10%, X7R, 16V	TDK Corporation	C1005X7R1C104K	0402
2	6	C2,C3,C32,C40,C42,C44	0.1uF	cap 0201, 0.1uF, +/- 20%, X5R, 6.3V	TDK Corporation	C0603X5R0J104M030BC	0201RND
3	2	C4,C5	18pF	cap 0402, 18pF, +/- 5%, COG (NPO), 50V	Murata Electronics North America	GRM1555C1H180JZ01D	0402
4	3	C6,C51,C52	1uF	cap 0402, 1uF, +/- 10%, X5R, 10V	Taiyo Yuden	LMK105BJ105KV-F	0402
5	8	C7,C11,C13,C14,C18,C19C62,C63	.01uF	cap 0402, 0.1uF, +/- 10%, X7R, 50V	Murata Electronics North America	GRM155R71H103KA88D	0402
6	2	C12,C17	10uF	cap 0402, 10uF, +/- 20%, X5R, 6.3V	Samsung	CL05A106MQ5NUNC	0402
7	2	C45,C46	4.7uF	cap 0402, 4.7uF, +/- 10%, X5R, 6.3V	TDK Corporation	C1005X5R0J475K	0402
8	2	C47,C49	22uF	cap 0603, 22uF, +/- 20%, X5R, 6.3V	TDK Corporation	C1608X5R0J226M	0603
10	1	C53	2.2uF	cap 0402, 2.2uF, +/- 20%, X5R, 6.3V	TDK Corporation	C1005X5R0J225M	0402
11	1	C54	15pF	cap 0402, 15pF, +/- 5%, COG, 50V	Venkel	C0402COG500-150JNE	0402
12	1	C55	10uF	cap 0603, 10uF, +/- 20%, X5R, 6.3.V	TDK Corporation	C1608X5R0J106M080AB	0603
13	1	D4	LED - Blue	LED BLUE, 0805, 104MCD, 20mA	Lite-On Inc.	LTST-C170TBK	0805
15	3	FB1,FB4,FB5	220 @ 100MHZ,2A	EMI Filter Beads, 220 Ohms, 25%	MuRata	BLM18EG221SN1D	0603
16	1	J1	USB3_PLUG	USB 3.0 - A Type R/A	Assmann	A-USB/3-A-LP/SMT-R	CON_SMRT_USB3A_M
17	2	J4,J5	USB3_TYPEA_CONNECTOR	Connectors USB 3.0, Super Speed USB - A, Receptacle	FCI	10117835-002LF	USB - A, Receptacle
18	1	L3	2.2uH@1.3A	INDUCTOR 2.2UH 20% 1.3A 1008	Murata	LQM2HPN2R2MG0L	IND_1008
19	2	R1,R24	DNI	DNI	DNI	DNI	0402
20	1	R2	DNI,1M	DNI	DNI	DNI	0402
21	3	R7,R30,R31	10K	RES 0402, 10K, +/- 1%, 1/10W	Panasonic Electronic Components	ERJ-2RKF1002	0402
22	4	R3,R4,R8,R9	4.7K	RES 0402, 4.7K, +/- 1%, 1/16w	Vishay Dale	CRCW04024K70FKED	0402
23	1	R5	90.9K	RES 0402, 90.9K, +/- 1%, 1/16W	Yageo	RC0402FR-0790K9L	0402
24	1	R6	9.53K	RES 0402, 9.53K, +/- 1%, 1/16w	Vishay Dale	CRCW04029K53FKED	0402
25	2	R19,R27	47K	RES 0402, +/- 1%, 1/10W	Panasonic Electronic Components	ERJ-2RKF4702X	0402
26	2	R25,R28	28.7K	RES 0402, 28.7k, +/- 1%, 1/16w	Venkel	CR0402-16W-2872FT	0402
27	1	R29	180	RES 0402, 180, +/- 1%, 1/16W	Panasonic Electronic Components	ERJ-2RKF1800X	0402
28	1	R32	237K	RES 0402, 237K, +/- 1%, 1/10W	Panasonic Electronic Components	ERJ-2RKF2373X	0402
29	1	R33	200K	RES 0402, 200K, +/- 1%, 1/16W	Panasonic Electronic Components	ERJ-2RKF2003X	0402
30	1	U1	TUSB8020B	Two-Port USB Hub	TEXAS INSTRUMENTS	TUSB8020B	QFP_48_284X284_20_THMPAD
31	3	U16,U19,U20	TPD6E05U06	IEC ESD protection diodes	TEXAS INSTRUMENTS	TPD6E05U06RVZ	UQFN_14_142X57_20
32	2	U17,U18	TPS2553	Power Distribution Switch	TEXAS INSTRUMENTS	TPS2553DBV	SOT23_6
33	1	U21	TLV70033	LDO linear regulator	TEXAS INSTRUMENTS	TLV70033DCK	SC70-5
34	1	U22	LM3674	600 mA Buck Converter	TEXAS INSTRUMENTS	LM3674MF-ADJ/NOPBTR-ND	SOT_23_5
35	1	Y1	24MHz	24 MHz Crystal	CTS Freq Controls	445C25D24M00000	XTAL_2_SM_197X126

9 Acknowledge and References

1. *USB 3.0 Electrical Compliance Test Specification*
2. *Agilent DSA91304A USB 3.0 Receiver Testing*

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