TIDA-00346 Design Considerations

Some implementations and use-cases of the TDA3x call for an inexpensive power supply without certain features that are required for other systems. This power supply design provides appropriate rails and proper sequencing for a medium use case for the TDA3x processor. In addition, this reference design contains a supply for DDR memory, a supply for a CAN transceiver and a simple switched load that can be used for testing the onboard supplies.

Each of the power supplies for the TDA3x must be sequenced during power up and power down. For this reason, any DC/DC converter that we choose must have an enable input or a switched output. All supplies must be automotive qualified and all switching frequencies should be outside of the AM band.

For the off-battery supply, a TPS54240-Q1 was chosen. This will accommodate a battery input of up to 42V. Substituting a footprint compatible TPS54260-Q1 will increase the maximum input voltage to 60V. A 340 kohm resistor sets the switching frequency at 360 kHz. Feedback resistors of 31.6k and 10.0k set the output voltage to 3.3V. This 3.3V rail will be the input to all other converters. To be able to sequence the 3.3V, it is passed through one channel of a TPS22968-Q1 analog switch.

A TPS54122-Q1 dual output supply is used for the 1.8V and 1.06V rails. The buck is used for the high current 1.06V core rail while the LDO provides the low current 1.8V rail. The 1.8V digital is utilized directly, while the 1.8V analog supply passes through the second channel of the TPS22968-Q1 analog switch (for correct sequencing).

TPS62262-Q1 was chosen for its high efficiency and the 2.2MHz switching frequency that reduces radio noise and decreases the size of external components. This is a very simple implementation utilizing the recommended 2.2uH inductor and a fixed 1.2V output.

Sequencing for the different supplies described above is achieved with a logic circuit utilizing two LM3880-Q1 sequencers and a couple of logic gates.

Power Up Sequence: When the TPS3808-Q1 power rail supervisor senses that the battery input voltage (Vin_P) is above 4.8V, the nRST output transitions from a low to a high. This causes the output of the OR gate to transition to a high, enabling the first sequencer (U1). This sequencer turns on three supplies in order using FLAG1, FLAG2 and FLAG3. When the last of these, FLAG3 (EN_4) goes high, the output of the AND gate transitions to a high and enables the second sequencer (U3). This enables three more supply rails and power up is complete.

Power Down Sequence: When the TPS3808-Q1 power rail supervisor senses that the battery input (Vin_P) voltage falls below 4.8V, the nRST output transitions from a high to a low. This causes the output of the AND gate to transition to a low, disabling the second sequencer (U3). This sequencer turns off three supplies in the reverse order using FLAG1, FLAG2 and FLAG3. When the last of these, FLAG1 (EN_5) goes low, the output of the OR gate transitions to a low and disables the first sequencer (U1). This disables three more supply rails and power down is complete.

The power down sequence requires that even though Vin_P has dropped, Vin must be held up long enough for the sequence to complete. For some loads, this may require additional capacitance be added on the Vin rail. This can be done using TP91. An alternate power down method would be to assert the master reset on the TPS3808-Q1. If a power down signal is available in the system, this would be a preferred method to initiate shutdown. The sequence would be the same, but it would not require additional capacitance. If the master reset is used, the power good threshold for the supervisor can be decreased to allow the entire system to operate down to a 4V battery input.

This concludes the design considerations for the TDA3 power supply. What follows is a description of the additional (optional) circuitry that has been included in this reference design.

For many automotive systems, a CAN transceiver is required. For this, a 5V rail has been provided. This supply is built with a TPS61071-q1 boost converter. The 5V rail is boosted off of the 3.3V rail so that the battery input can be allowed to fall below 5V.

For a design requiring DDR memory, a complete power supply and termination regulator is included. By changing the feedback resistors on the TPS79901-Q1 LDO, a VDDQ output voltage of 1.1V to 3.5V can be achieved. By configuring the input jumper for the TPS51200-Q1 termination regulator input, a VTT is made available that will accommodate multiple memories types: DDR, DDR2, DDR3, DDR3L, DDR4, LPDDR2 and LPDDR3.

To make this design easier to test, a “programmable” switched load is incorporated on the board. This circuit utilizes a TLS555-Q1 timer and a UCC27324 low-side MOSFET driver to create a repeating load pulse. The frequency of the load pulse is set to 30-40 Hz with a duty cycle of about 5%. R903, R904 and R905 are the load resistors for the 3.3V, 1.06V and 1.2V rails. Using the load resistor values shown in the schematic will result in load current pulses of 1A, 1.5A, and 120mA, respectively. Only one of these load resistors should be populated at any one time. The slope of the turn on and turn off edges of the control pulse can individually be controlled by adjusting the value of R906 and R907.

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