TI Designs

SSD Power Delivery Design Guide

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Design Resources

TIDA-00399	Tool Folder Containing Design Files
TPS22954	Product Folder
TPS62085	Product Folder
TPS62086	Product Folder
TPS62087	Product Folder
TMP103	Product Folder
TPD2E009	Product Folder
TPS22922	Product Folder
TPS22964C	Product Folder
TPS22920	Product Folder
TPS22914	Product Folder
TPS7A4501	Product Folder
TPL0102-100	Product Folder

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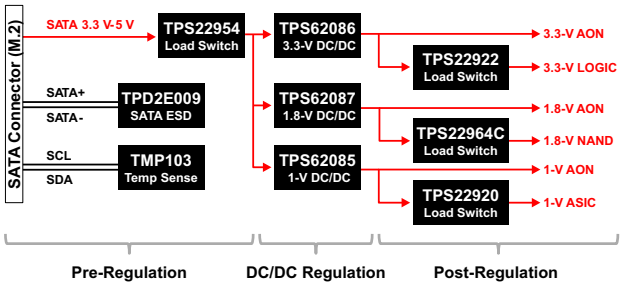
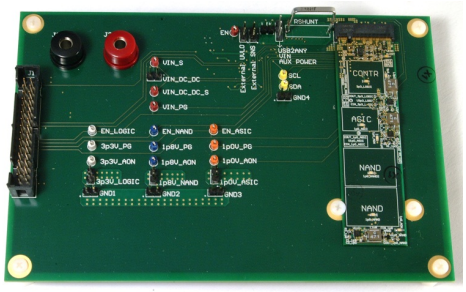
Design Features

- Size-optimized Solution For M.2 Form Factor
- Complete Power Solution For Standard 3.3-V, 1.8-V, And 1-V Rails Up To 3 A
- Slew Rate Control On All Switched Power Rails To Limit Inrush Current
- Programmable Undervoltage And “Power Good” Thresholds For Real-World Emulation
- Overtemperature Protection With Software
- Quick Output Discharge (QOD) Safely Discharges All Rails, Even When Input Power Is Lost

Featured Applications

- Client-Side Solid State Drives (SSDs)
- Enterprise SSDs





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1 System Description

SSD Power Delivery is composed of two boards: an interposer board and a daughter card. The daughter card mimics the physical appearance of an SSD with components placed accordingly. The interposer provides an interface to the daughter card and implements circuits for programmable input voltage, undervoltage threshold, and “power good” threshold.

Load switches offer many advantages when compared to a discrete solution using field-effect transistors (FETs). Load switches ubiquitously offer controlled turn-on, which limits the damaging effects of inrush current. These load switches have very low leakage current when disabled and draw minimal power when enabled, which greatly improves battery life in portable applications. They are cost- and size-optimized to replace discrete solutions where channel density and space is critical. Many load switches offer a Quick Output Discharge (QOD) feature, which dissipates any residual energy on the output after the switch is disabled. Other load switches offer reverse current protection to protect upstream circuitry in the event that the supply potential dips. Learn more about load switches on ti.com.

1.1 TPS22954

The TPS22954 load switch is used as a pre-regulation switch. The input power to the SSD attaches to V_{IN}, and the output of the switch, V_{OUT}, ties to the input of the DC/DC converters. TPS22954 also has an open drain “power good” (PG) indication, which is pulled high by an external resistor when V_{OUT} rises above a user-defined threshold. In this application, the PG signal enables the DC/DC converters.

The purpose of this switch is to limit the input leakage current while the SSD is off, which prolongs battery life in portable applications. The integrated “power good” functionality eliminates the need for a separate supervisor circuit. Inrush current can be decreased by changing the slew rate of the device with the external CT capacitor.

TPS22954 also implements a Quick Output Discharge (QOD) function. This device is designed to discharge large capacitive loads. This application has 30 µF of downstream capacitance, which would otherwise hold charge after the switch is disabled. With QOD, however, the output is safely discharged even when input power to the device is lost.

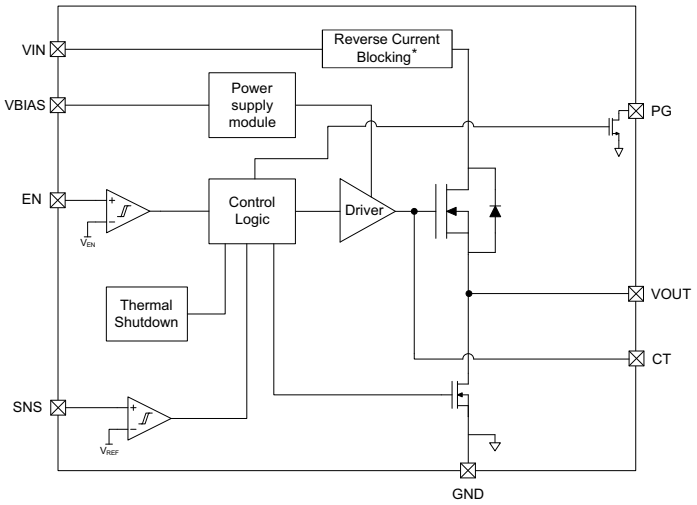


Figure 1. Functional Block Diagram of TPS22954

1.2 TPS62085, TPS62086, and TPS62087

The TPS62085 (and TPS62086 and TPS62087) is a high-efficiency DC/DC converter capable of providing up to 3 A, and maintains efficiency across all loads with a DCS-Control™ Topology. The TPS62085, TPS62086, and TPS62087 implement an adjustable, fixed-3.3-V, and fixed-1.8-V output, respectively.

Each converter is powered from the output of the TPS22954 pre-regulation load switch, and enabled by its "power good" output. Power good prevents the converters from starting up with insufficient voltage and greatly reduces the risk of a brown-out condition.

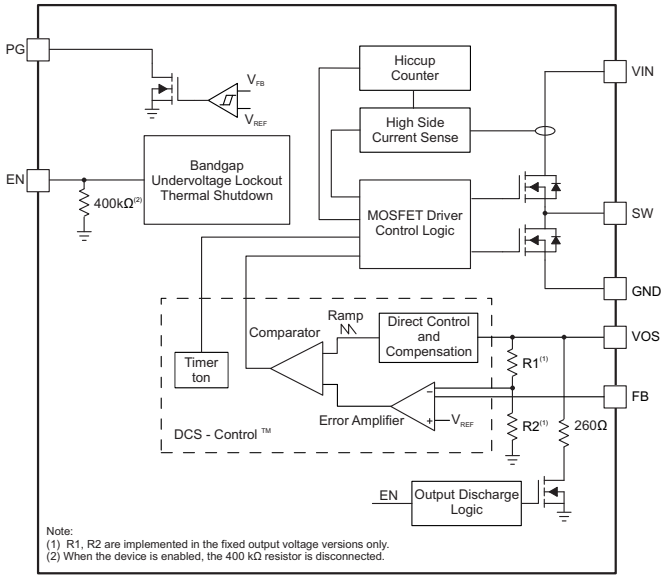
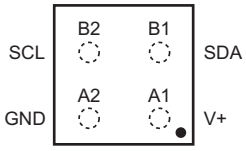


Figure 2. Functional Block Diagram of TPS62085, TPS62086, and TPS62087 Step-Down Converter

1.3 TMP103

The TMP103 temperature sensor monitors the temperature of the daughter card. The sensor has a 1°C resolution across –10°C to +100°C. Configuration registers exist for high and low temperature limits. If the current temperature is higher than the limit, a fault flag is set in the status register, and the system shuts down via software to protect itself from damage by overtemperature. Because of its small size and multiple device access (MDA) commands, several TMP103 can be included to monitor multiple sites during operation.



PIN DESCRIPTIONS

PIN		
NO.	NAME	DESCRIPTION
A1	V+	Supply voltage
A2	GND	Ground
B1	SDA	Input/output data pin
B2	SCL	Input clock pin

Figure 3. TMP103 Temperature Sensor with Two-Wire Interface

1.4 TPD2E009

The TPD2E009 is a 2-channel electrostatic discharge (ESD) solution for high-speed differential interfaces. The TPD2E009 is intended to protect a serial ATA (SATA) controller from ESD events. The ESD protection meets or exceeds IEC61000-4-2 (lightning, level 4). Several devices can be used for systems with multiple differential signal pairs.

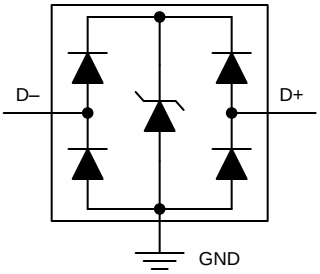


Figure 4. Functional Diagram of TPD2E009

1.5 TPS22922

The TPS22922 post-regulation load switch is used for switching the 3.3-V power to the SSD controller. This switch implements Quick Output Discharge (QOD), which pulls the rail low when the device is off, reducing the risk of errors caused by subsystems not disabling properly. The low leakage current of this device limits the wasted power when the controller is disabled.

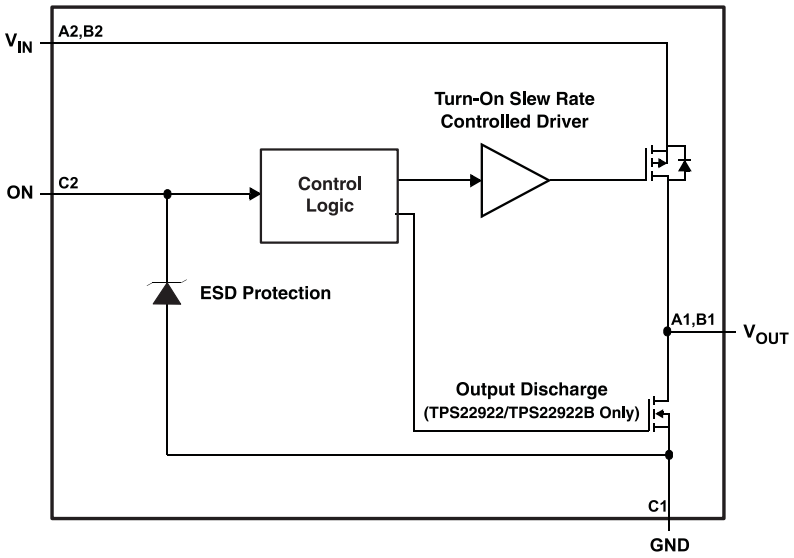


Figure 5. Functional Block Diagram of TPS22922

1.6 TPS22964C

The TPS22964C post-regulation load switch is used for switching the 1.8-V power to the NAND flash memory. The switch implements Quick Output Discharge (QOD), which pulls the rail low when the device is off, reducing the risk of errors caused by subsystems not disabling properly. The low leakage of this device limits the wasted power when the flash is disabled.

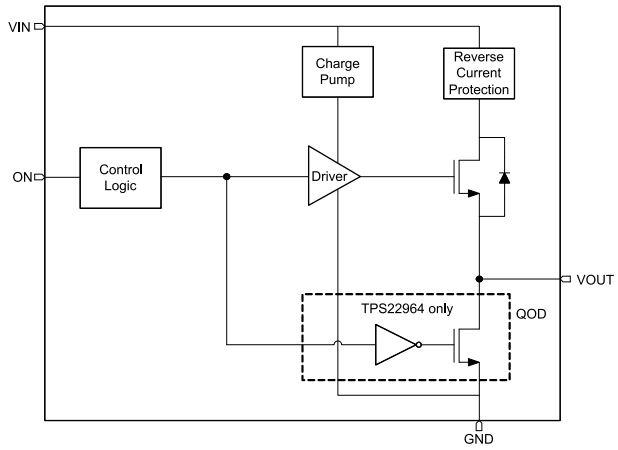


Figure 6. Functional Block Diagram of TPS22964C

1.7 TPS22920

The TPS22920 post-regulation load switch is used for switching the 1-V power to the flash ASIC. The switch implements Quick Output Discharge (QOD), which pulls the rail low when the device is off, reducing the risk of errors caused by subsystems not disabling properly. The low leakage of this device limits the wasted power when the ASIC is disabled.

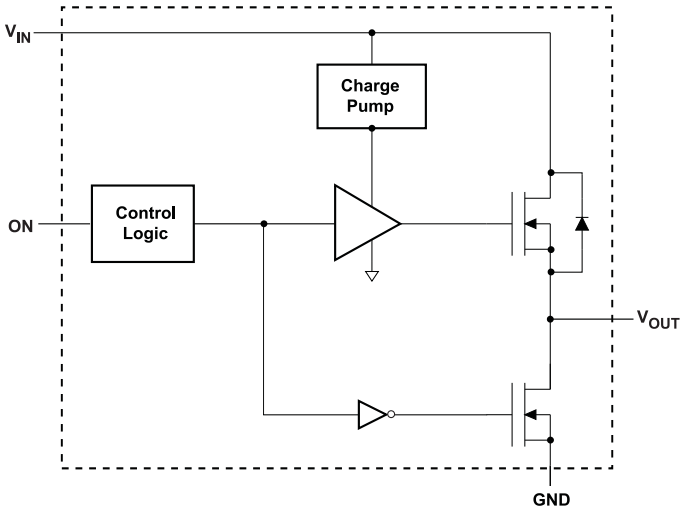


Figure 7. Functional Block Diagram of TPS22920

1.8 TPS22914

The TPS22914 load switch has a supporting role on the daughter card. The switch uses 3.3-V power from the USB2ANY to drive the blue LEDs on the daughter card. The small package size is optimal for space-constrained applications.

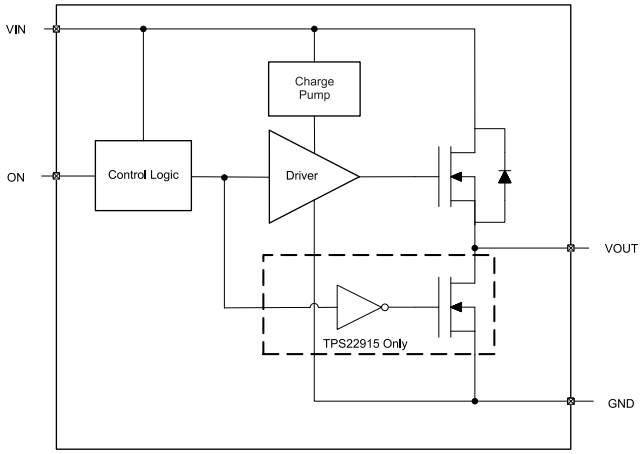


Figure 8. Functional Block Diagram of TPS22914

1.9 TPS7A4501

The TPS7A4501 low-dropout (LDO) regulator is used on the interposer board for programmable input voltage. The 5-V input from the USB2ANY is passed through the pass element, and a TPL0102-100 digital potentiometer is used as a programmable resistor divider between OUT and SENSE/ADJ to set the output voltage. The programming resolution is limited by the TPL0102-100 voltage divider. This circuit is designed to be used for low current because the USB2ANY can only supply 100 mA on its 5-V rail.

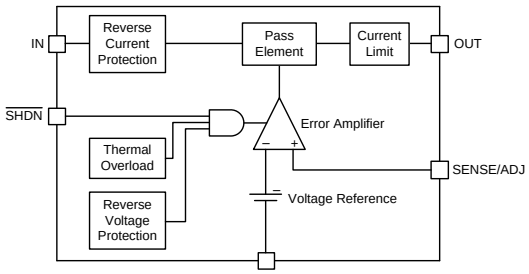


Figure 9. Functional Block Diagram of TPS7A4501

1.10 TPL0102-100

The TPL0102-100 digital potentiometer is used in several applications on the interposer board for system-level testing. These applications include the programmable input voltage, undervoltage threshold, and “power good” threshold. Each application uses the TPL0102-100 in its voltage divider mode. The high-to-low (end-to-end) resistance of 100 kΩ can be divided by the 256 available taps.

One TPL0102-100 is used for the programmable input voltage circuit by attaching the high side (HA) to the output of the TPS7A4501 LDO (OUT), the low side (LA) to ground, and the wiper (WA) to the feedback pin of the LDO (SENSE/ADJ). The range and sensitivity of this circuit is increased by adding a high-side resistor between OUT and HA, and a low-side resistor between LA and GND.

The other TPL0102-100 is used for programmable undervoltage and power good thresholds on the TPS22954 pre-regulation load switch. For undervoltage, the high side (HA) is connected to the input (V_{IN}), the low side (LA) to ground, and the wiper (WA) to the enable signal (EN). For power good, the high side (HB) is connected to the output (V_{OUT}), the low side (LB) to ground, and the wiper (WB) to the feedback pin (SNS).

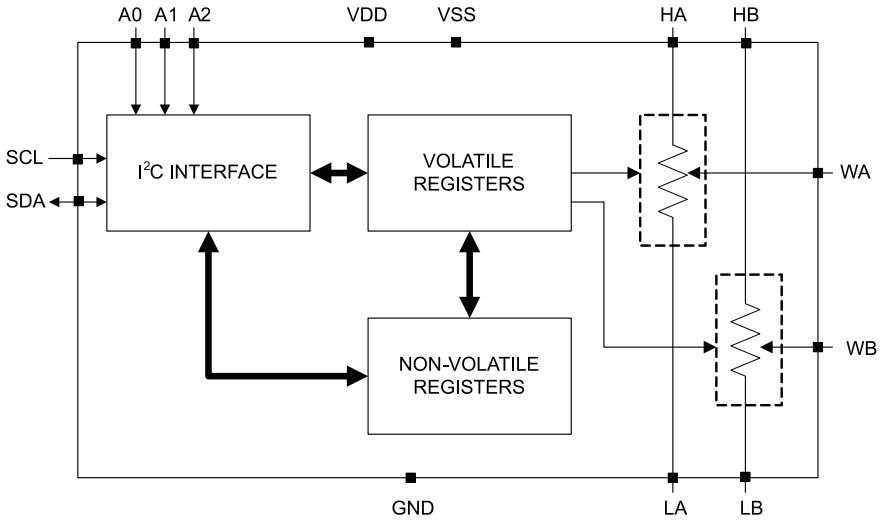


Figure 10. Functional Block Diagram of TPL0102-100

2 System Electrical Characteristics

Table 1 shows the electrical specifications of this design.

Table 1. System Electrical Specifications

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
System Input	VIN input voltage range		2.5		5	V
	Input current	V_{IN} = 5 V		3		A
	Efficiency	V_{IN} = 5 V $R_{L,\ 3.3}$ = 1.65 Ω $R_{L,\ 1.8}$ = 0.72 Ω $R_{L,\ 1.0}$ = 0.33 Ω		91.1		%
TPS62086 3.3-V Output	Output current	V_{IN} = 5 V			2	A
TPS62087 1.8-V Output	Output current	V_{IN} = 5 V			2.5	A
TPS62085 1-V Output	Output current	V_{IN} = 5 V			3	A
Free-air Temperature Range			–40		85	°C

3 Block Diagram

SSD Power Delivery implements a typical power tree in a Solid-State Drive (SSD). The power path is marked in red in Figure 11. Each DC/DC converter output is split into two rails: an “Always On” (AON) rail for low current standby power, and a switched rail for high-current operation. The 3.3-V rail is intended for a SATA interface controller, the 1.8-V rail for NAND memory, and the 1-V rail for a memory management ASIC. The system can provide up to 15 W to the SSD controller, ASIC, and NAND flash memory. Load switches are used to turn the high-current rails on and off. The benefit of using load switches for these rails is described in detail in the following sections.

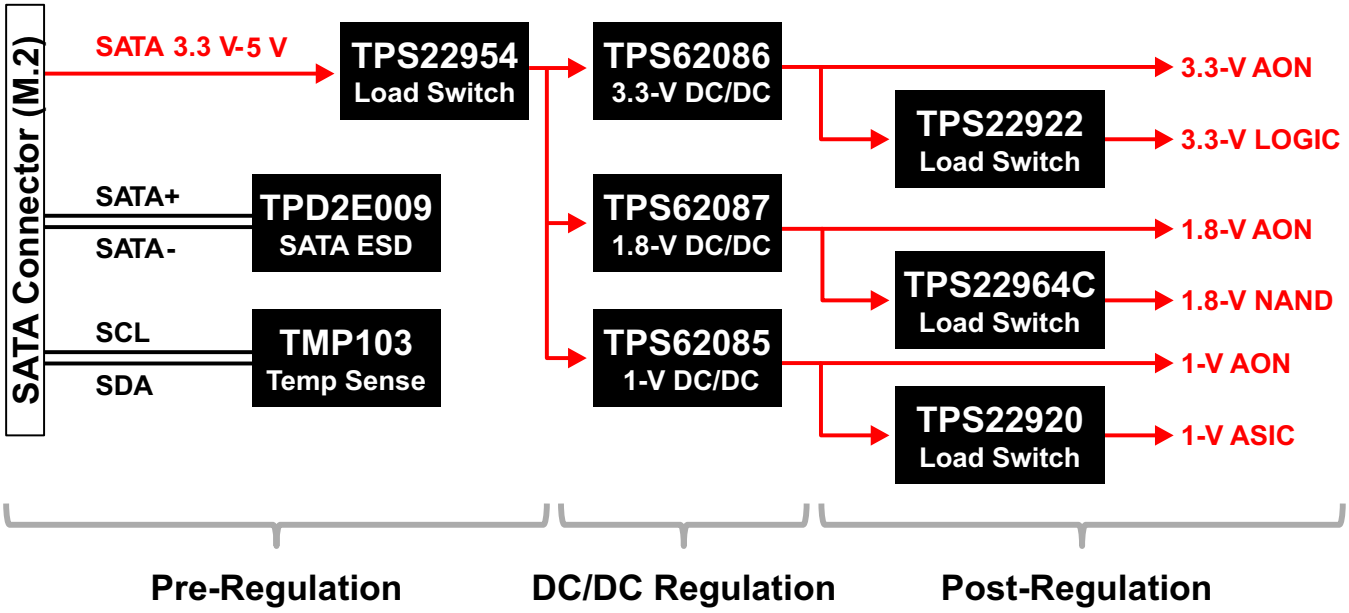


Figure 11. Block Diagram of SSD Power Delivery Solution

4 System Design Theory

The daughter card's pre-regulation load switch, TPS22954, has several purposes. One is to reduce the system leakage current to the order of single microamperes (μA), greatly prolonging battery life in portable applications. Another purpose is the integrated "power good" functionality, which enables the DC/DC converters once their input voltage (the output of the switch) is sufficiently high. Inrush current can also be controlled by changing the slew rate of the device with the external CT capacitor.

Each post-regulation load switch on the daughter card was chosen based upon the voltage and current rating of their respective rails. The design goals include minimizing voltage drop from input to output and minimizing generated heat.

The interposer board acts as an interface between the system controller (USB2ANY) and the daughter card. The main purpose of this board is to break out signals from the daughter card to test points so that they may be observed without probing the daughter card directly. However, the interposer board has a few interesting circuits of its own, described in the following subsections. Although these circuits may not be included as part of an actual system, they help test the core design functionality as shown in the daughter card block diagram. Among these circuits are a circuit for programmable input voltage from a single 5-V input rail, a circuit for a programmable undervoltage lockout (UVLO) level, and a circuit for a programmable "power good" (PG) level.

4.1 TPS22954 Undervoltage Lockout

The TPS22954 pre-regulation load switch can be turned on and off with its enable (EN) pin. In applications where GPIO resources are limited, the EN pin can be tied to the input voltage V_{IN}, or more practically, a voltage divider can be used between V_{IN} and GND.

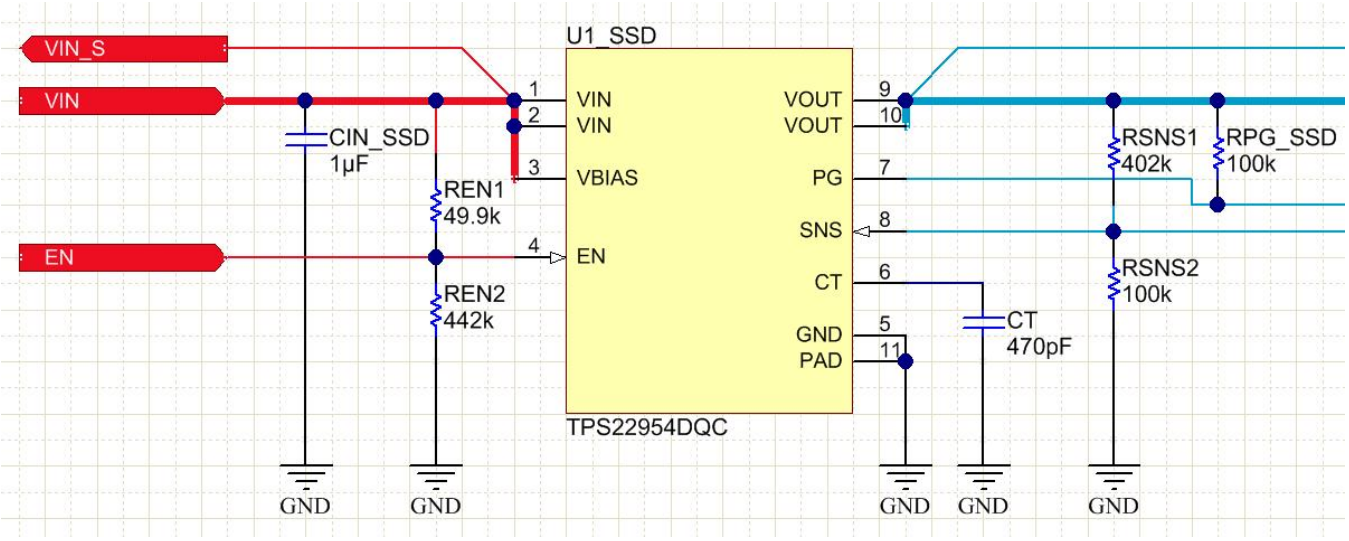


Figure 12. TPS22954 Pre-Regulation Load Switch as Designed in SSD Power Delivery

TPS22954 has a typical enable threshold of $V_{IH,EN}$ = 700 mV and disable threshold of $V_{IL,EN}$ = 600 mV. When the voltage on EN rises above 700 mV, the switch turns on; when the voltage falls below 600 mV, the switch turns off. A resistor divider from V_{IN} to EN can help set the input voltage at which the switch turns on and off (assuming zero leakage into EN):

$$V_{EN} = (V_{IN}) / (1 + R_{EN1} / R_{EN2})$$

$$V_{IN} = (V_{EN}) (1 + R_{EN1} / R_{EN2})$$

$$V_{IN,\,disable} = (V_{IL,EN}) (1 + R_{EN1} / R_{EN2}) = (600mV) (1 + R_{EN1} / R_{EN2})$$
$$V_{IN,\,enable} = (V_{IH,EN}) (1 + R_{EN1} / R_{EN2}) = (700mV) (1 + R_{EN1} / R_{EN2}) \quad (1)$$

The leakage current through the divider can be calculated from the input voltage and total divider resistance:

$$I_{IN} = V_{IN} / (R_{EN1} + R_{EN2}) \quad (2)$$

The voltage divider can be used to create an undervoltage lockout (UVLO) functionality by specifying the nominal input voltage, the maximum divider leakage current, and at least one of four remaining undetermined parameters.

4.1.1 Design Example

Suppose that you want to design a divider for a 5-V input system with 5-µA maximum leakage current that turns on at 3 V:

Table 2. Design Target Specification for UVLO

INPUT VOLTAGE V_{IN} (V)	INPUT LEAKAGE $I_{IN,\ max}$ (µA)	TURN-ON VOLTAGE $V_{IN,\ enable}$ (V)	TURN-OFF VOLTAGE $V_{IN,\ disable}$ (V)	R_{EN1} (Ω)	R_{EN2} (Ω)
5	5	3	Calculated	Calculated	Calculated

The ratio of resistances can be determined by using the turn-on voltage, and the (minimum) sum of the resistances can be determined by using the input voltage and maximum leakage:

$$R_{EN1} / R_{EN2} = (V_{IN,\ enable}) / (700mV) - 1 = (3V) / (0.7V) - 1 = 3.286$$

$$R_{EN1} + R_{EN2} \geq (V_{IN}) / (I_{IN,\ max}) = (5V) / (5\mu A) = 1M\Omega$$

$$R_{EN1,\ min} = 767k\Omega$$
$$R_{EN2,\ min} = 233k\Omega \quad (3)$$

Finally, the turn-off voltage is determined from the enable voltage:

$$V_{IN,\ disable} = (V_{IN,\ enable})(600mV / 700mV) = 2.57V \quad (4)$$

Table 3. Final Parameter Values for UVLO Specification

INPUT VOLTAGE V_{IN} (V)	INPUT LEAKAGE $I_{IN,\ max}$ (µA)	TURN-ON VOLTAGE $V_{IN,\ enable}$ (V)	TURN-OFF VOLTAGE $V_{IN,\ disable}$ (V)	R_{EN1} (Ω)	R_{EN2} (Ω)
5	5	3	2.57	767 k	233 k

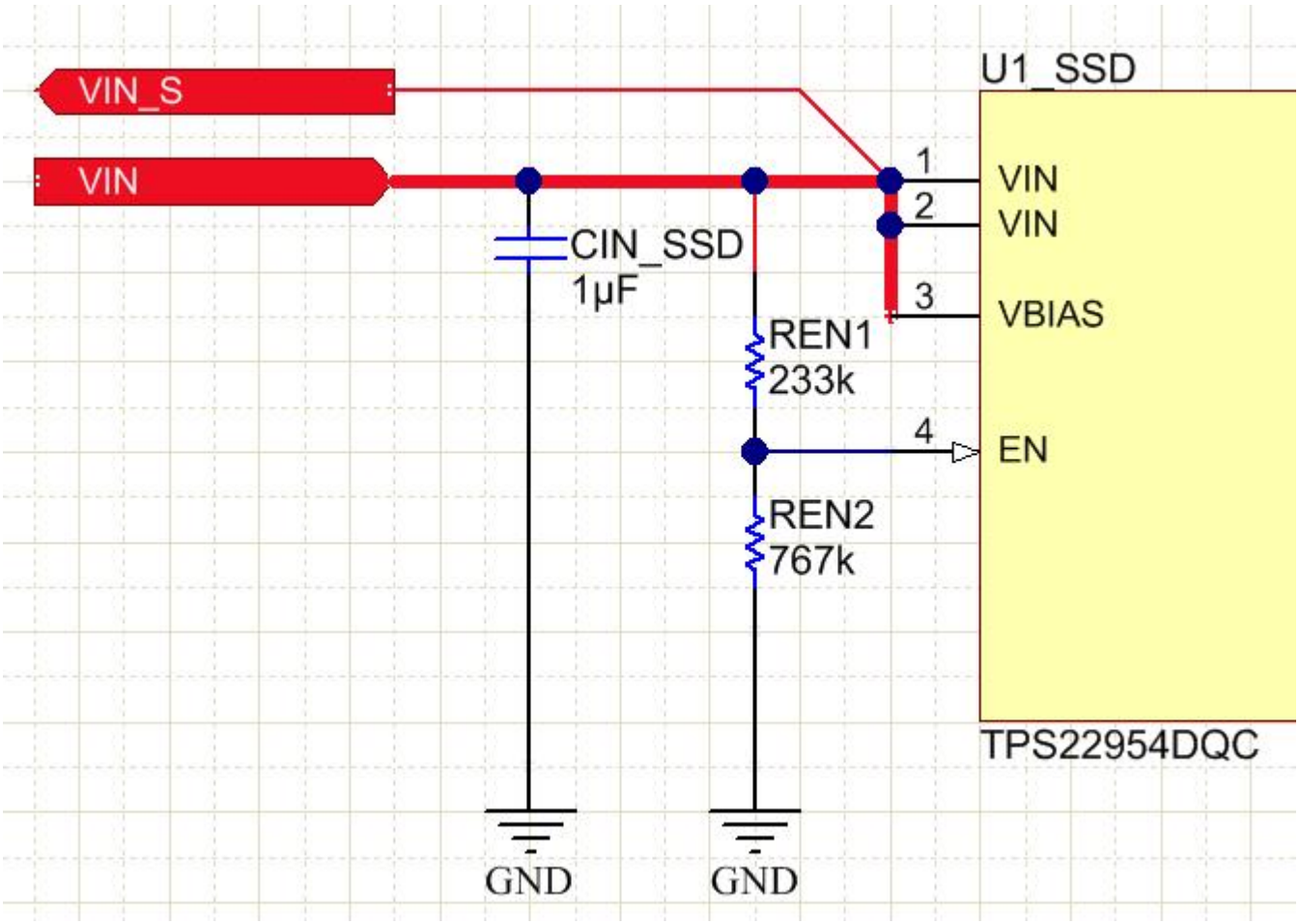


Figure 13. Final Circuit for UVLO Specification

4.2 TPS22954 Power Good

The TPS22954 pre-regulation load switch has an integrated “power good” (PG) signal that enables the downstream DC/DC converters. The PG pin is an open-drain output that is pulled up to the output voltage V_{OUT} using a pull-up resistor between V_{OUT} and PG. PG is pulled high when the voltage on the SNS pin rises above its rising threshold. In a typical application, a voltage divider between V_{OUT} and GND is used for the SNS input.

The design methodology is very similar to the previous UVLO design. The typical enable threshold is $V_{IH,SNS}$ = 515 mV, and the disable threshold is $V_{IL,SNS}$ = 455 mV.

$$V_{SNS} = (V_{OUT}) / (1 + R_{SNS1} / R_{SNS2})$$

$$V_{OUT} = (V_{SNS})(1 + R_{SNS1} / R_{SNS2})$$

$$V_{OUT,\ power\ bad} = (V_{IL})(1 + R_{SNS1} / R_{SNS2}) = (455mV)(1 + R_{SNS1} / R_{SNS2})$$
$$V_{OUT,\ power\ good} = (V_{IH})(1 + R_{SNS1} / R_{SNS2}) = (515mV)(1 + R_{SNS1} / R_{SNS2}) \quad (5)$$

4.2.1 Design Example

Suppose that you want to design a “power good” divider for a 5-V input system with 5-µA maximum leakage current that turns on at 4 V:

Table 4. Design Target Specification for Power Good

OUTPUT VOLTAGE V_{OUT} (V)	OUTPUT LEAKAGE $I_{OUT,\ max}$ (µA)	TURN-ON VOLTAGE $V_{OUT,\ power\ good}$ (V)	TURN-OFF VOLTAGE $V_{OUT,\ power\ bad}$ (V)	R_{SNS1} (Ω)	R_{SNS2} (Ω)
5	5	4	Calculated	Calculated	Calculated

The ratio of resistances can be determined using the turn-on voltage, and their (minimum) sum using the input voltage and leakage:

$$R_{SNS1} / R_{SNS2} = \left(V_{OUT,\ power\ good}\right) / \left(515mV\right) - 1 = \left(4V\right) / \left(0.515V\right) - 1 = 6.767$$

$$R_{SNS1} + R_{SNS2} \geq \left(V_{OUT}\right) / \left(I_{OUT,\ max}\right) = \left(5V\right) / \left(5\mu A\right) = 1M\Omega$$

$$\begin{aligned} R_{SNS1,\ min} &= 871k\Omega \\ R_{SNS2,\ min} &= 129k\Omega \end{aligned} \tag{6}$$

Finally, the turn-off voltage is determined from the turn-on voltage:

$$V_{OUT,\ power\ bad} = \left(V_{OUT,\ power\ good}\right)\left(455mV / 515mV\right) = 3.53V \tag{7}$$

Table 5. Final Parameter Values for Power Good Specification

OUTPUT VOLTAGE V_{OUT} (V)	OUTPUT LEAKAGE $I_{OUT,\ max}$ (µA)	TURN-ON VOLTAGE $V_{OUT,\ power\ good}$ (V)	TURN-OFF VOLTAGE $V_{OUT,\ power\ bad}$ (V)	R_{SNS1} (Ω)	R_{SNS2} (Ω)
5	5	4	3.53V	871k	129k

The pull-up resistor on PG (RPG) must be chosen based on the system configuration as well. When SNS increases past its rising threshold, the PG pin becomes high impedance, and the voltage on PG is determined by the input leakage current of any subsequent circuits. The resistance of RPG should be high to reduce leakage during turn-on, but low to ensure PG is pulled up to a valid logic level.

$$\begin{aligned} I_{PG} &= \left(V_{OUT}\right) / \left(R_{PG}\right) && \left(V_{PG} \approx 0V, V_{OUT} < V_{OUT,\ power\ good}\right) \\ V_{PG} &= V_{OUT} - \left(R_{PG}\right)\left(I_{LEAK}\right) && \left(V_{OUT} \geq V_{OUT,\ power\ good}\right) \end{aligned} \tag{8}$$

For example, if the downstream circuit requires a valid high logic threshold of at least 1.2 V with 50-nA leakage current, the pull-up resistance can be at most

$$R_{PG} \leq \left(V_{OUT} - V_{PG}\right) / \left(I_{LEAK}\right) = \left(5V - 1.2V\right) / \left(50nA\right) = 76k\Omega \tag{9}$$

This resistance sets the minimum peak leakage during turn-on to be

$$I_{PG,\ peak} = \left(V_{OUT,\ power\ good}\right) / \left(R_{PG}\right) = \left(4V\right) / \left(76k\Omega\right) = 52.6\mu A \tag{10}$$

This equation is the peak value of current through RPG just before the PG pin goes to high impedance. If the output of the switch is assumed to turn on linearly, the minimum average current into PG during turn-on will be half of the calculated value, or 26.3 µA. In applications where the device will not turn on and off frequently, this current will be minuscule compared to the leakage through R_{SNS1} and R_{SNS2} over time.

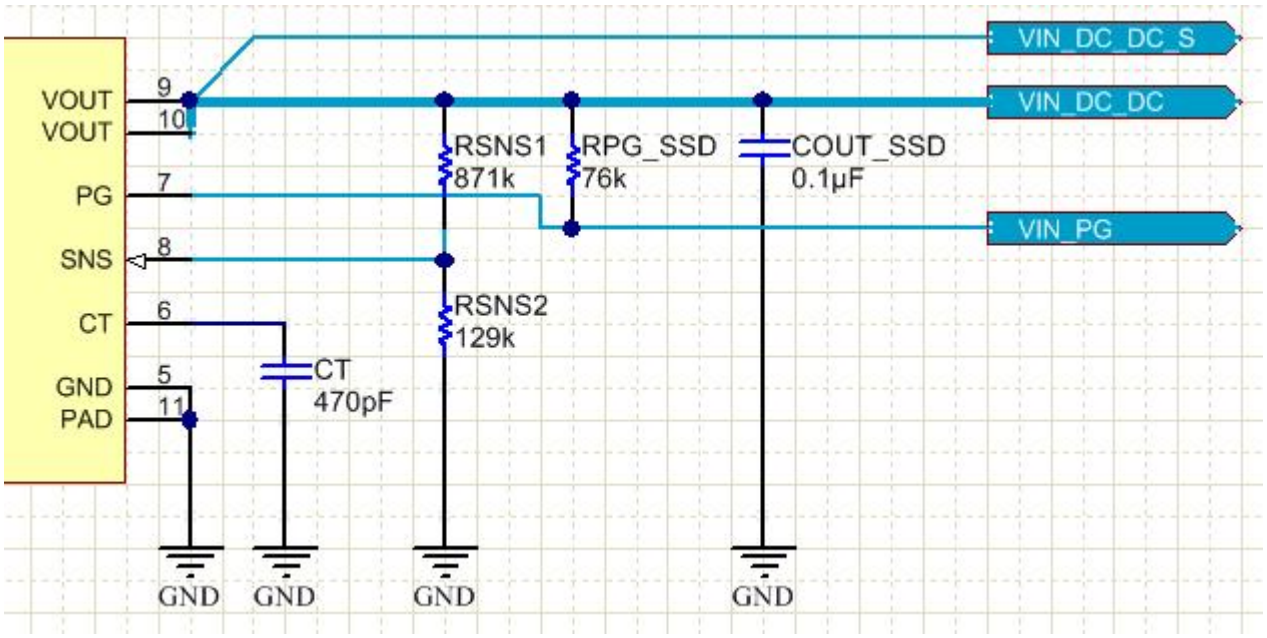


Figure 14. Final Circuit for Power Good Specification

Figure 15 shows the final circuit as designed:

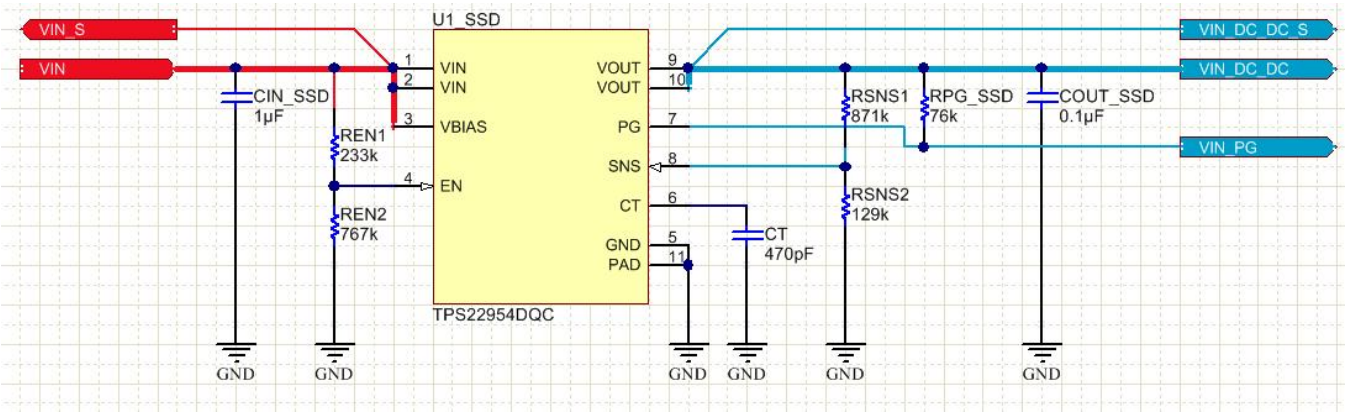


Figure 15. Final Design for UVLO and Power Good

During normal operation, the following will occur:

1. When the input voltage V_{IN} rises above 3 V, EN passes its V_{IH} (rising) threshold, the switch begins to turn on, and V_{OUT} rises to the level of V_{IN}.
2. When the output voltage V_{OUT} rises above 4 V, SNS passes its V_{IH} (rising) threshold, the PG pins goes high impedance, and the voltage on PG floats to a valid logic high.
3. If the output voltage decreases below 3.53 V (due to input voltage sagging or high current on the output), SNS falls below its V_{IL} (falling) threshold, the PG pin pulls low, and the downstream circuits disable.
4. If the input voltage decreases below 2.57 V (due to upstream supply sagging), EN falls below its V_{IL} (falling) threshold, and the switch turns off.

The range of 3.5 V to 2.5 V was chosen as a “dead zone” for device limits and thermal considerations. Because V_{BIAS} is tied to V_{IN}, the minimum input voltage is limited to 2.5 V, as shown in the TPS22954 datasheet. The ON-resistance (R_{ON}) of the switch increases at lower V_{BIAS}, which causes the device to heat more with the same amount of input current. Because the DC/DC converters are operating at constant power, the system input current increases at lower voltage as well. This two-fold effect (higher resistance, higher current) causes the switch to heat up much more quickly. To protect itself, the switch can shut off the DC/DC converters with the “power good” signal before the voltage decreases too much.

4.3 TPS22954 Inrush Current Limiting

A large amount of inrush current can flow when a voltage is suddenly applied to a load. This current charges any downstream parasitic capacitance and input capacitance to other circuits. Inrush current spikes can cause the supply voltage to sag, causing brown-out conditions and other unwanted behavior. In its simplest form, inrush current can be modeled as the product of the total load capacitance (parasitic or otherwise) and the change in load voltage with respect to time:

$$I_{inrush} = C_L \cdot (dV_L / dt) \tag{11}$$

I_{inrush} = inrush current — A

C_L = total load capacitance — µf

dV_L / dt = rate of change of load voltage — V / µs

The inrush current can be reduced by either reducing the load capacitance or the rate at which the load voltage changes. The capacitance is typically dominated by input capacitance to other circuits, which is fixed in application. The only practical solution is to limit the rate at which the load voltage changes. A high rate turns the system on quickly, but a low rate limits the inrush current.

The TPS22954 pre-regulation load switch has a controlled turn-on, which causes the output voltage to rise linearly with constant slope. The rate at which the output voltage rises is controlled by the CT pin. In the simplified model, a constant current source charges the CT pin, and the resulting voltage turns on the gate of the pass FET. Adding an external capacitor between the CT pin and GND causes the gate to charge more slowly and the output to rise more slowly. A detailed guide is available in the TPS22954 datasheet. The approximate formula for slew rate as a function of CT capacitance is

$$SR = 0.35 \cdot CT + 20 \tag{12}$$

SR = slew rate — µs / V

CT = capacitance between CT and GND — pF

The units for the constant 20 are microseconds per volt — µs / V

The units for the constant 0.35 are microseconds per volt-picofarad — µs / (V · pF)

The inrush current can then be calculated directly from the slew rate, independent of the voltage:

$$I_{inrush} = C_L / SR \quad (13)$$

I_{inrush} = inrush current in amps A

C_L = total load capacitance in microfarads µf

SR = slew rate in microseconds per volt µs / V

4.3.1 Design Example

In SSD Power Delivery, the pre-regulation switch controls the inrush current into the DC/DC converters' input capacitors. The total load capacitance is CL = 3 · 10 µF = 30 µF. A value of CT = 470 pF balances inrush current and turn-on time. The slew rate can be calculated from the CT capacitance:

$$SR = 0.35 \cdot 470 + 20 = 184.5 \mu s / V \quad (14)$$

The inrush current during turn-on can be calculated from the slew rate:

$$I_{inrush} = (30 \mu F) / (184.5 \mu s / V) = 0.163 A \quad (15)$$

The total rise time of the system can be calculated if the change in voltage is specified:

$$t_{rise,\ general} = \Delta V \cdot SR \quad (16)$$

The rise time of a load switch is given as the amount of time for the output voltage to rise from 10% to 90% of its final value to account for any non-linearity at either end of the voltage ramp. For example, suppose the input to the system is 5 V. The rise time is the amount of time the output voltage takes to rise from 10% of 5 V to 90% of 5 V:

$$t_{rise,\ typical} = ((90\%)(5\ V) - (10\%)(5\ V)) \cdot 184.5 \mu s / V = 738 \mu s \quad (17)$$

The calculated value is within 5% of 767 µs measured on a typical device at 25°C. Lot-to-lot variations between devices and stray parasitic capacitance on CT can cause the rise time to vary by a few percentage points. Users should design the slew rate with an upper bound given by the maximum rise time, and lower bound given by maximum inrush current.

For example, suppose we want to design the CT capacitance based on the following constraints:

Table 6. Design Target Specification for Inrush Current

INPUT VOLTAGE V_{IN} (V)	MAXIMUM RISE TIME $t_{rise,\ max}$ (µs)	MAXIMUM INRUSH CURRENT $I_{inrush,\ max}$ (A)	LOAD CAPACITANCE C_L (µF)	CT CAPACITANCE CT (pF)
5	800	0.2	30	Calculated

The maximum slew rate is calculated from the maximum rise time:

$$SR \le t_{rise,\ max} / \Delta V = (800 \mu s) / ((90\%)(5V) - (10\%)(5V)) = 200 \mu s / V \quad (18)$$

The minimum slew rate is calculated from the maximum inrush current:

$$SR \ge C_L / I_{inrush} = (30 \mu F) / (0.2\ A) = 150 \mu s / V \quad (19)$$

The range of CT capacitance can then be calculated:

$$150\mu s / V \le SR \le 200\mu s / V$$

$$150\mu s / V \le (0.35\mu s / V \cdot pF) \cdot CT + 20\mu s / V \le 200\mu s / V$$

$$130\mu s / V \le (0.35\mu s / V \cdot pF) \cdot CT \le 180\mu s / V$$

$$371\,pF \le CT \le 514\,pF \quad (20)$$

A nominal value of CT = 470 pF would be acceptable for this application.

Table 7. Final Parameter Values for Inrush Current Specification

INPUT VOLTAGE V_{IN} (V)	MAXIMUM RISE TIME $t_{rise,\ max}$ (µs)	MAXIMUM INRUSH CURRENT $I_{inrush,\ max}$ (A)	LOAD CAPACITANCE C_L (µF)	CT CAPACITANCE CT (pF)
5	800	0.2	30	470

4.4 Output Voltage Rail Load Switches

Table 8. Load Switch Characteristics at Design Goal Targets

DEVICE	V_{IN} (V)	I_{OUT} (A)	R_{ON} (mΩ)	Θ_{JA} (1) (°C/W)	V_{DROP} (mV, %)	P_{DISS} (mW)	ΔT (°C)
TPS22922	3.3	2	22	125.1	44 (1.3%)	88	11
TPS22964C	1.8	2.5	17	132	42.5 (2.4%)	106.25	14
TPS22920	1	3	6.5	130	19.5 (1.95%)	58.5	7.6

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* (SPRA953).

Each DC/DC output voltage rail has an associated post-regulation load switch. The 3.3-V, 1.8-V, and 1-V rail are designed to handle 2 A, 2.5 A, and 3 A, respectively. The design goal is to place a voltage burden of less than 2.5% of the rail voltage at the rated load. This limits the maximum ON-Resistance (R_{ON}) to:

$$R_{ON} \le (0.025)\ (V_{IN} / I_{OUT}) \quad (21)$$

The other design goal is to maximize the thermal performance by keeping the thermal rise (above ambient temperature) less than 15°C. The thermal rise is directly proportional to R_{ON}, the square of the load current I_{OUT}, and the thermal resistance Θ_{JA}.

$$\Delta T = (R_{ON} \cdot {I_{OUT}}^2)\ (\Theta_{JA}) \le 15°C$$

$$\Theta_{JA} \le (15°C) / (R_{ON} \cdot {I_{OUT}}^2) \quad (22)$$

Based on these requirements, the TPS22922, TPS22964C, and TPS22920 were chosen for the 3.3-V, 1.8-V, and 1-V rails, respectively.

4.5 Interposer—Programmable Input Voltage

On the interposer board, the programmable input voltage simulates variable system input voltage in the application, without requiring a separate power supply. The circuit uses the TPS7A4501 LDO and TPL0102-100 Digital Potentiometer to regulate the USB2ANY 5-V supply to any voltage between 2.5 V and 5 V. The digital potentiometer acts as a voltage divider between the output and feedback (ADJ) pin of the LDO. The LDO increases the resistance of the pass element (thus decreasing the output voltage) until the voltage at the ADJ pin is 1.21 V.

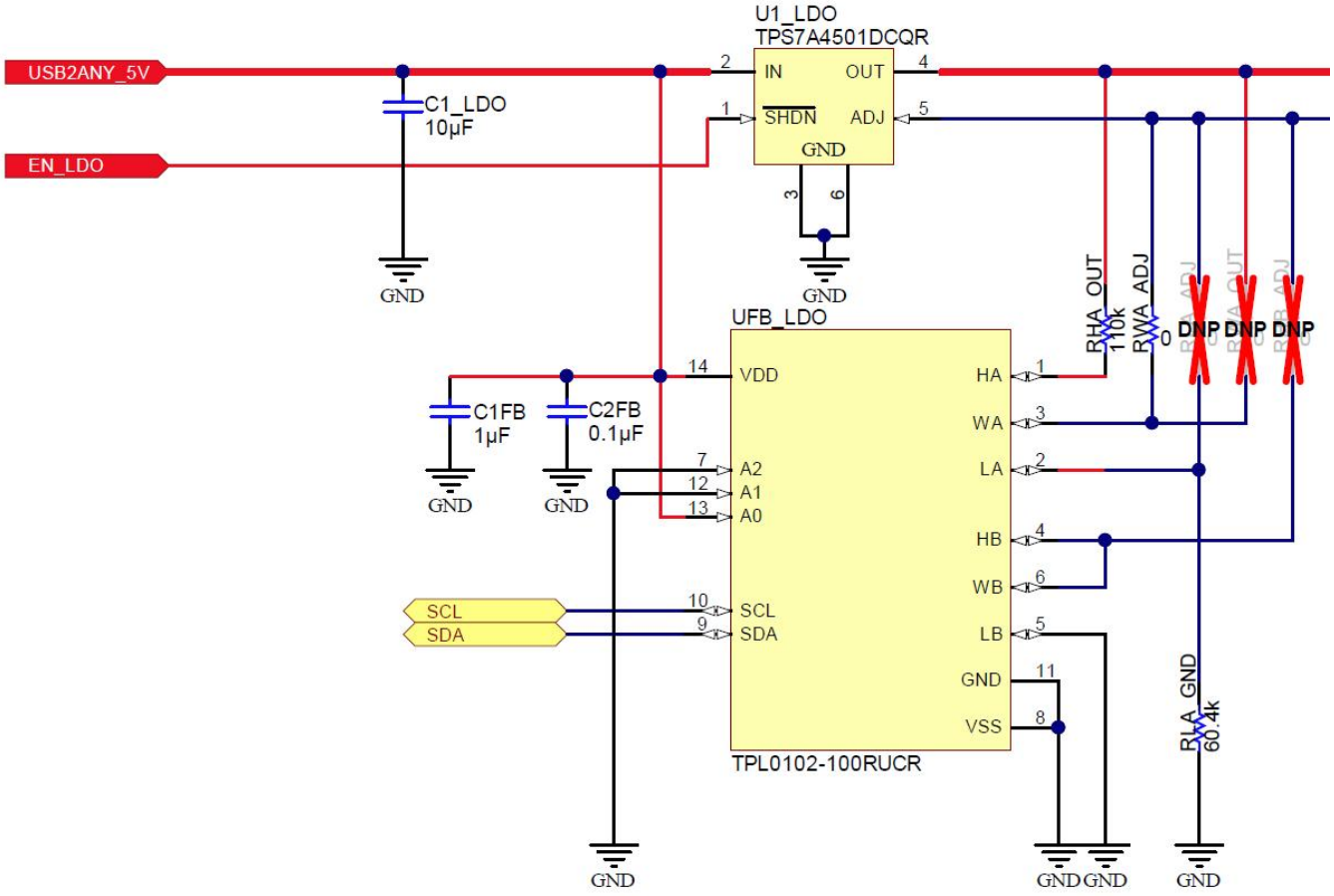


Figure 16. Programmable Input Voltage Circuit

The additional resistors RHA_OUT (110 kΩ) and RLA_GND (60.4 kΩ) center the wiper of the digital potentiometer closer to the 1.21-V feedback voltage of the LDO. Because the high-to-low (end-to-end) resistance of the TPL0102-100 is 100 kΩ, this sets bounds on the ratio of high- to low-leg resistance:

$$R_{HIGH} / R_{LOW} = (110k\Omega + 100k\Omega) / (60.4k\Omega) = 3.477 = \alpha_{max}$$

$$R_{HIGH} / R_{LOW} = (110k\Omega) / (100k\Omega + 60.4k\Omega) = 0.686 = \alpha_{min} \quad (23)$$

The output voltage of the LDO can be calculated as

$$V_{ADJ} = 1.21V = (V_{OUT}) / (1 + R_{HIGH} / R_{LOW})$$

$$V_{OUT} = (1.21V)(1 + R_{HIGH} / R_{LOW}) \quad (24)$$

The bounds on the output voltage of the LDO are

$$V_{OUT,\,max} = (1.21V)(1 + \alpha_{max}) = (1.21V)(1 + 3.477) = 5.417V$$

$$V_{OUT,\,min} = (1.21V)(1 + \alpha_{min}) = (1.21V)(1 + 0.686) = 2.040V \quad (25)$$

Because the maximum output voltage is greater than the input voltage, the “true” maximum voltage is limited to 5 V by the input. Wide margins allow fine-tuning without running out of codes and while maintaining good resolution.

5 System Setup

The following steps detail how to set up the system and the results of basic functional testing.

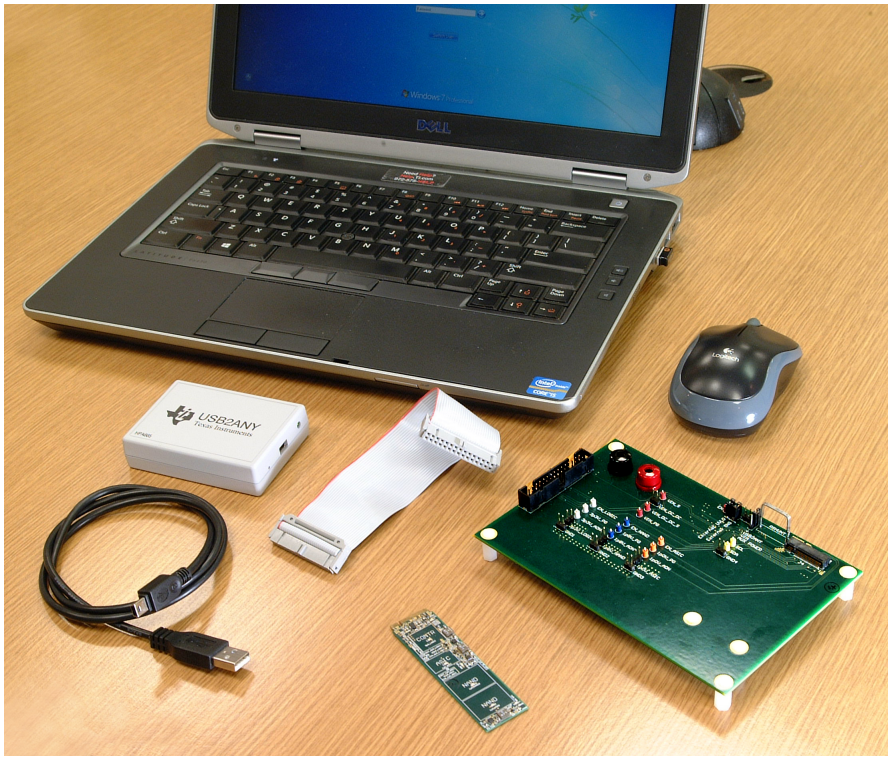


Figure 17. SSD Power Delivery System and Required Components

5.1 Standard Operation using USB2ANY

1. Connect one end of the USB cable to the computer, and connect the other end to the USB2ANY.

Figure 18. The USB2ANY is Connected to the Computer

2. Wait for Windows to detect and install drivers for the USB2ANY.

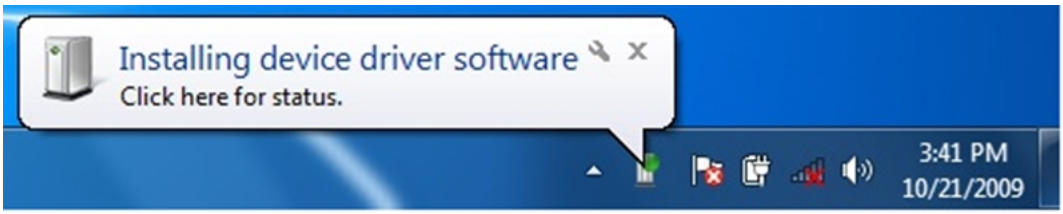


Figure 19. The Drivers of the USB2ANY are Installed Automatically

3. Connect one end of the ribbon cable to the USB2ANY, and connect the other end to the interposer board.

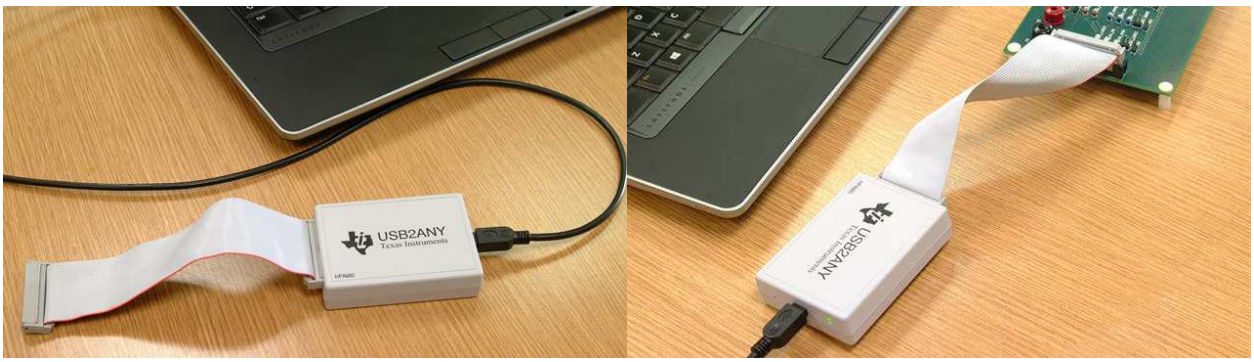


Figure 20. The Ribbon Cable is Connected Between the USB2ANY and Interposer Board

4. Plug the SSD daughter card fully into the socket on the interposer board at a 30° angle. Gently depress the daughter card and use the holding screws to grasp the edges of the board.

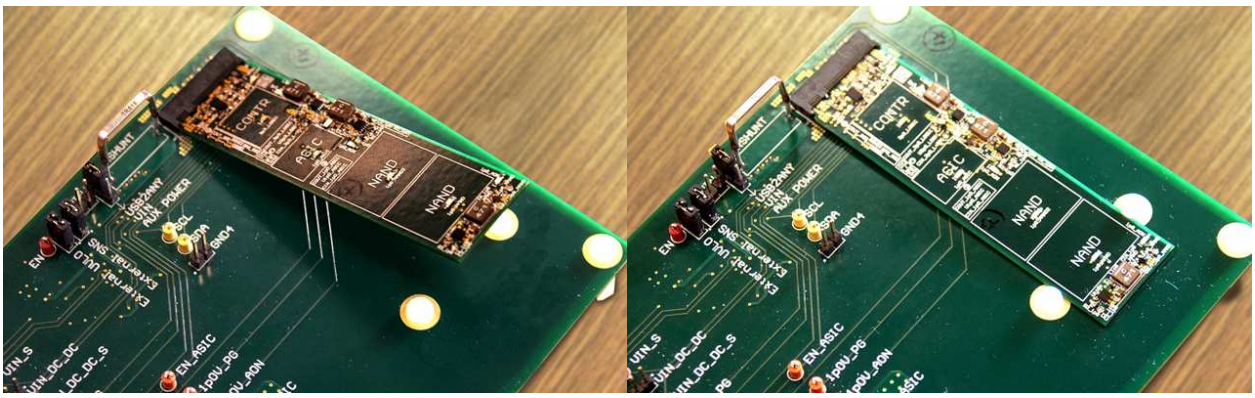


Figure 21. Inserting the Daughter Card

5. Verify that the “External UVLO” and “External SNS” jumpers are populated, and the input voltage jumper is set between “USB2ANY” and “VIN”.

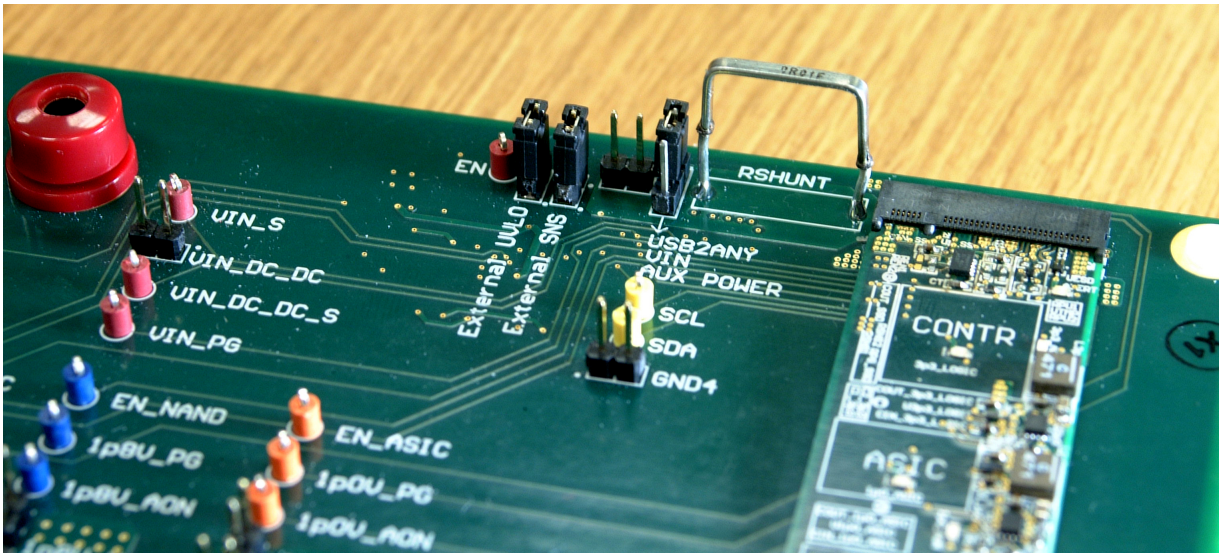


Figure 22. Jumper Settings for USB2ANY-Powered Application

6. Start the software. If everything is connected properly, the status indication box will change from “Initializing…” to “Status OK”. Otherwise, an error text will appear to diagnose connection problems.

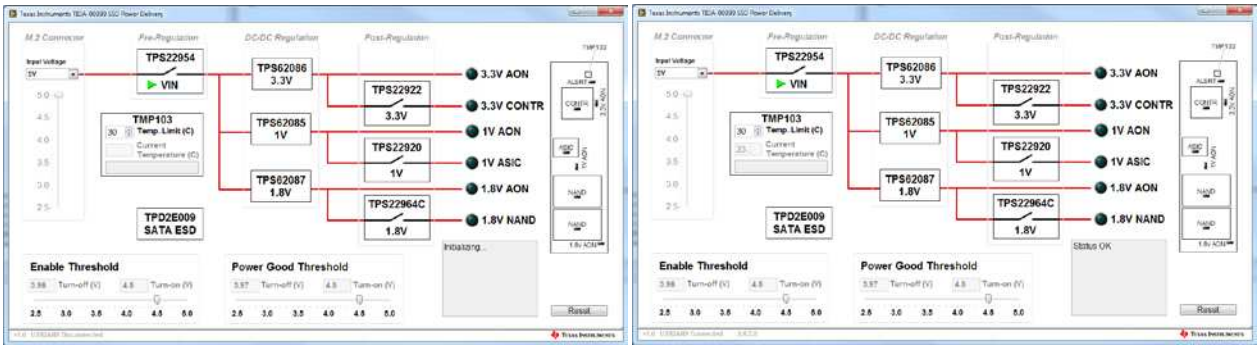


Figure 23. The Software is Initialized and Everything is Connected Properly

7. Press the button labeled “VIN” to enable the TPS22954 pre-regulation load switch and DC/DC converters. Three LEDs representing the “Always On” rails light up.

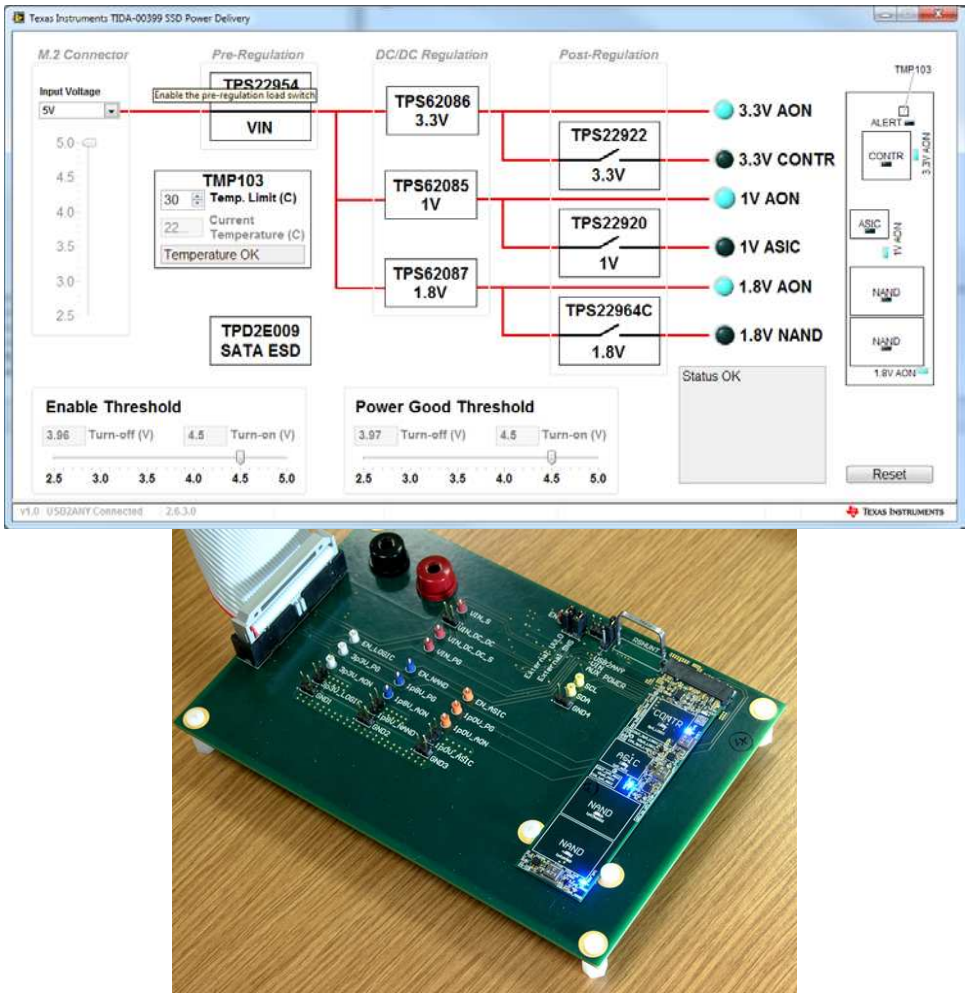


Figure 24. The "Always On" Rails are Enabled

8. Press any of the post-regulation switches to enable the corresponding high-current rail.

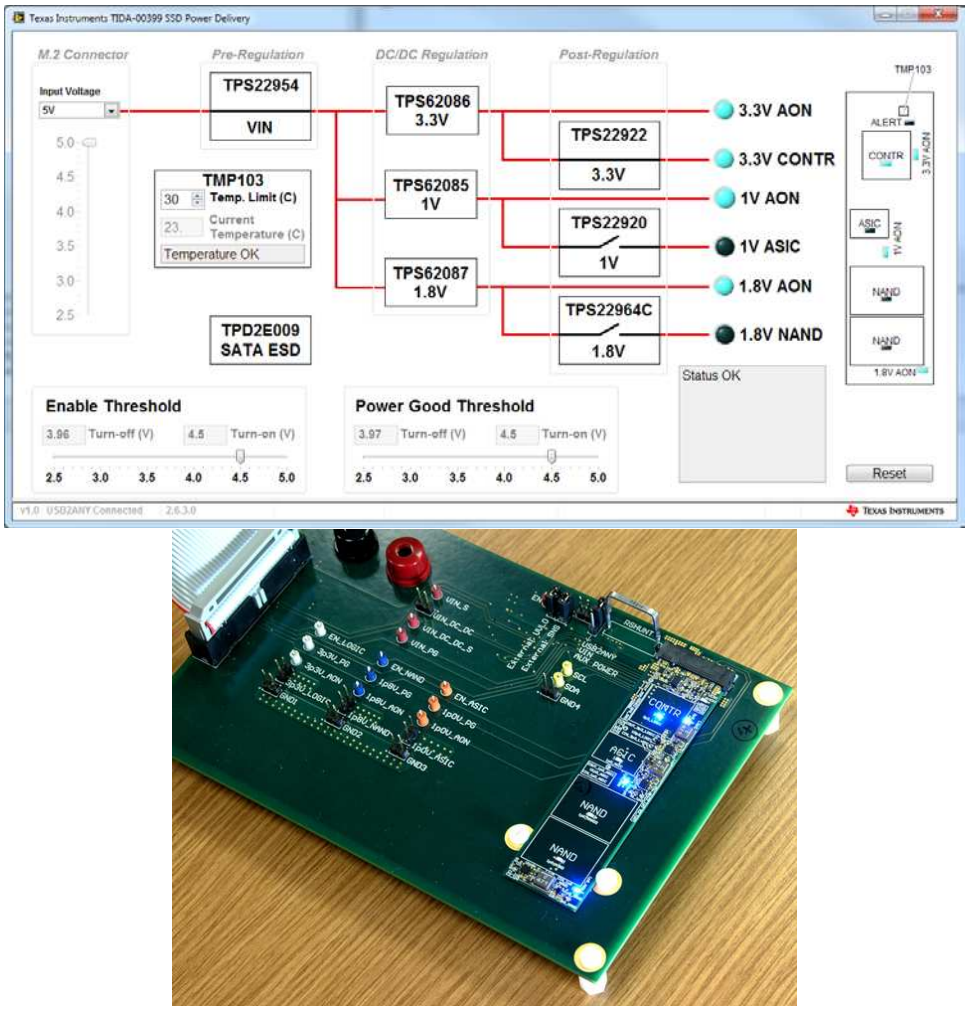


Figure 25. The 3.3-V Controller Power is Enabled

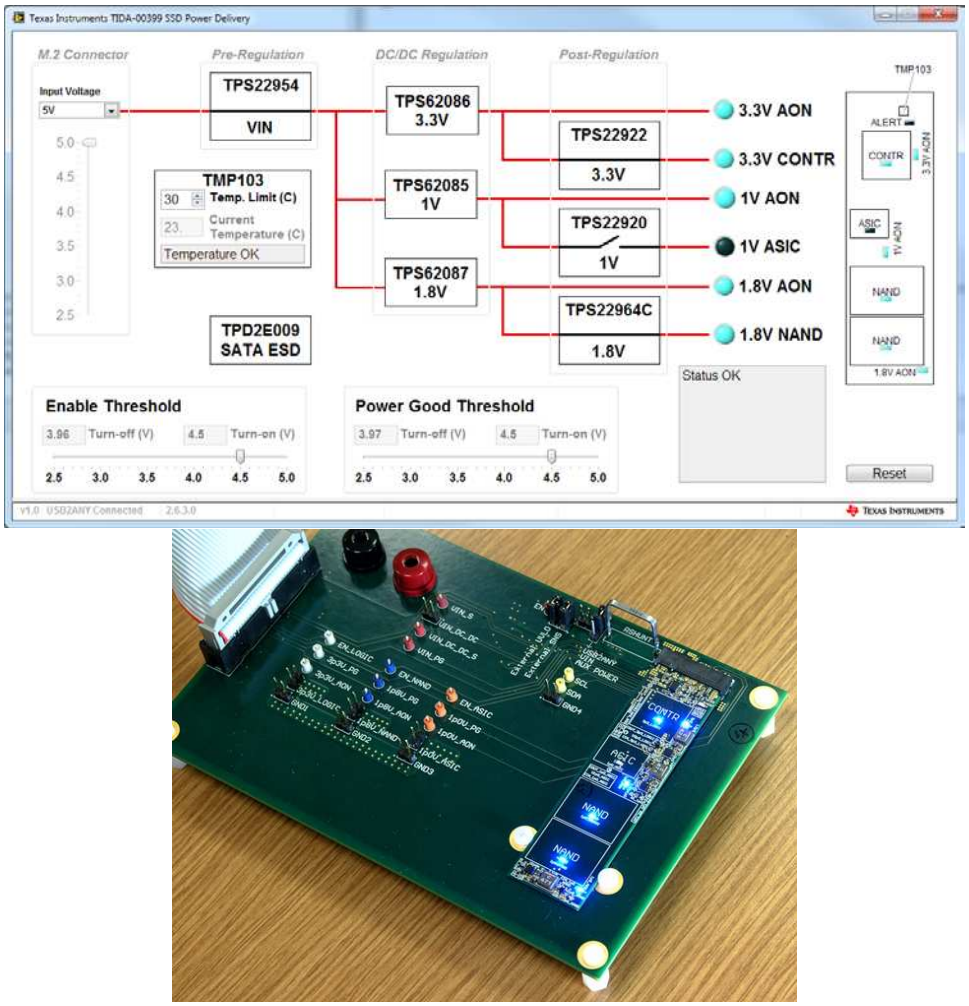


Figure 26. The 1.8-V NAND Power is Enabled

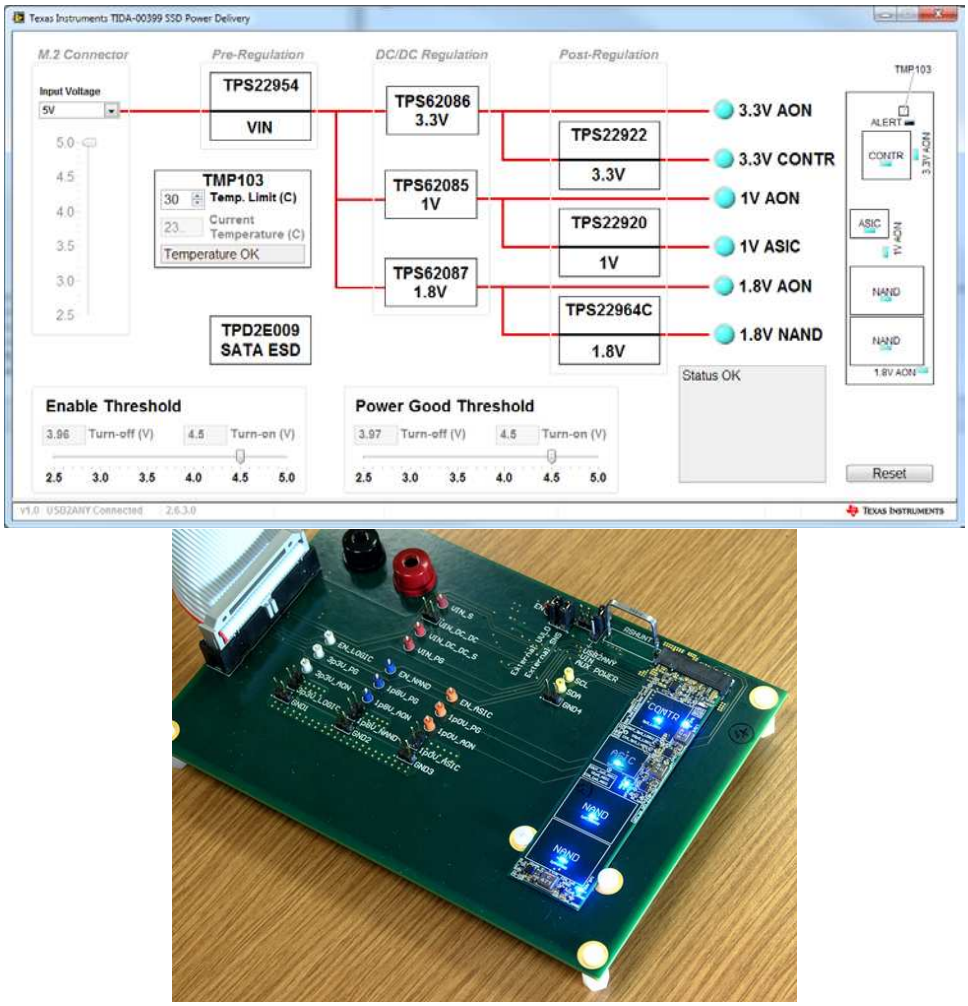


Figure 27. The 1-V Memory ASIC Power is Enabled

5.2 Operation using Auxiliary Power

The system can also be powered using auxiliary power, which allows for high-current testing that would otherwise be impossible by solely using the USB2ANY. To use auxiliary power, follow steps 1-4 above, then use the steps below as an alternative to step 5:

5a. Connect the auxiliary power supply to the interposer board. Users can set the power supply to any voltage between 0 V and 5 V.

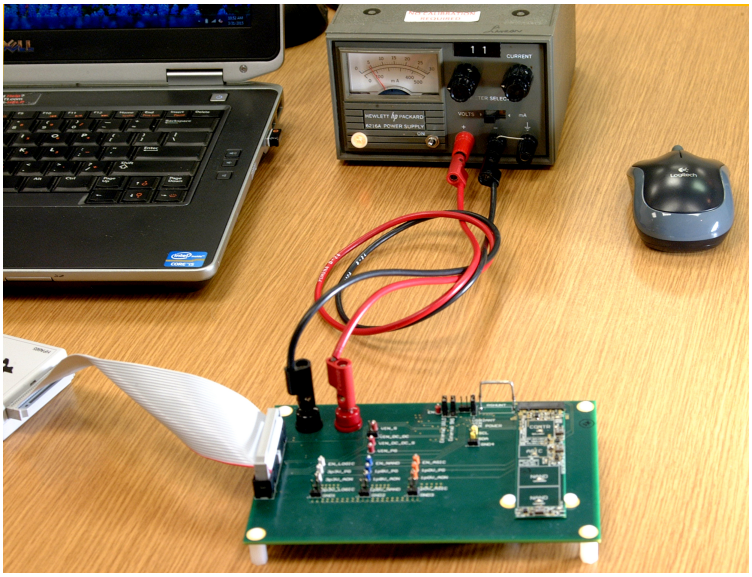


Figure 28. Auxiliary Power Supply Connected to Interposer Board

5b. Verify that the “External UVLO” and “External SNS” jumpers are populated and that the input voltage jumper is set between “VIN” and “AUX POWER”.

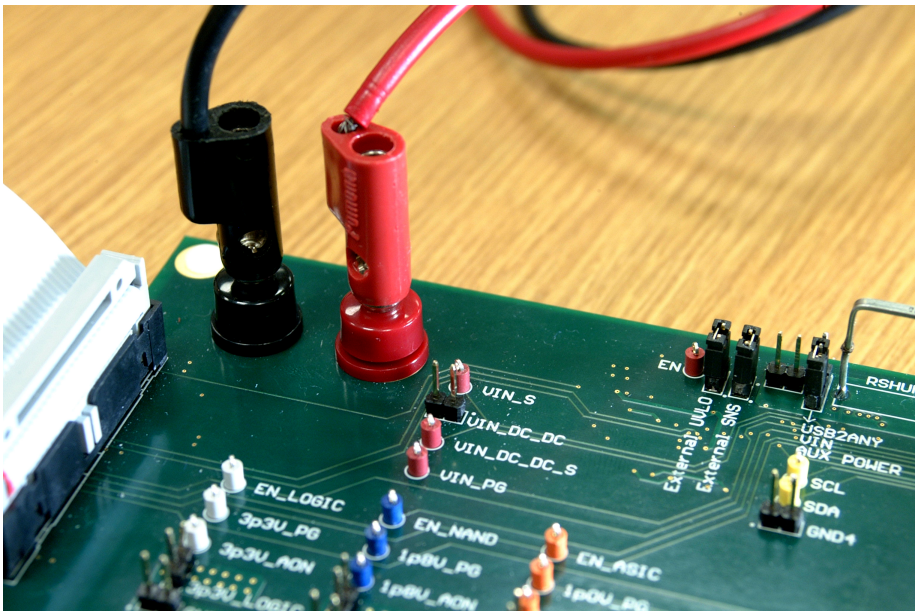


Figure 29. Jumper Settings and Auxiliary Power Supply Connections

From here, follow the remaining steps as usual.

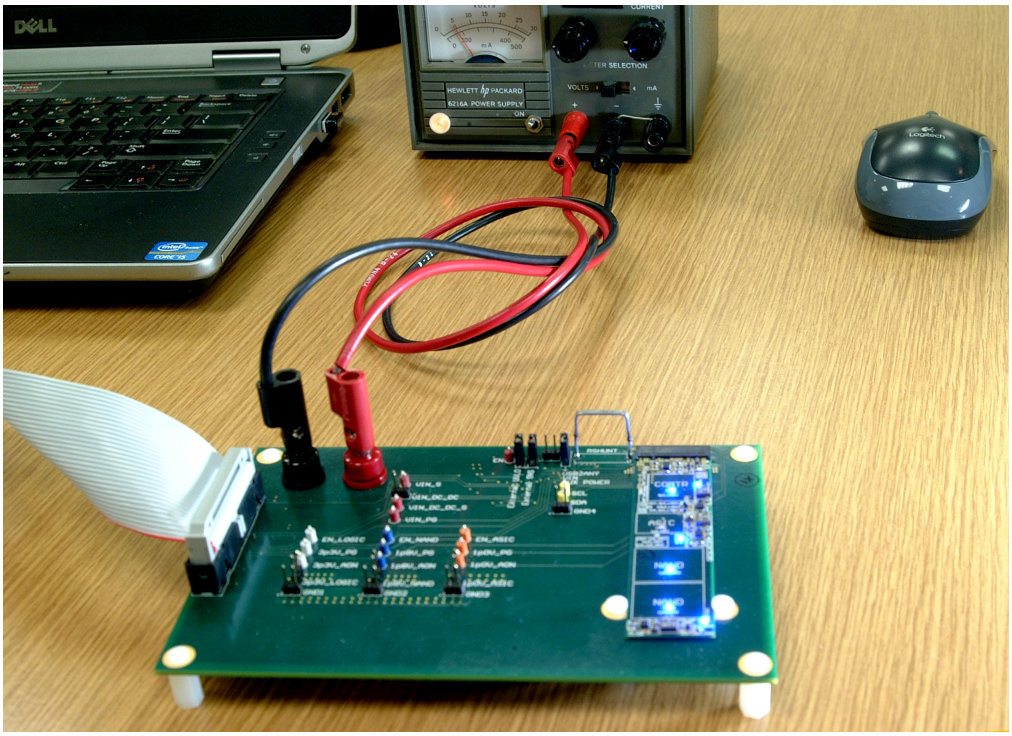


Figure 30. SSD Power Delivery Powered by Auxiliary Power Supply

6 Test Data

6.1 DC/DC Converter Efficiency

Each DC/DC converter was independently tested across load current, and the ratio of output power to input power (P_{OUT} / P_{IN}) was recorded. Each converter was tested at an input voltage of 5 V. The TPS62085 (1 V) and TPS62087 (1.8 V) were also tested at an input voltage of 3.3 V. The TPS62086 (3.3 V) was not tested at an input voltage of 3.3 V because no regulation occurs and the device acts as a pass-through. The input and output voltages were measured using a low-inductance probe across the input and output capacitors, respectively. The input and output currents were measured from the sourcemeter (SMU) providing the input and load, respectively.

Table 9. Efficiency Versus Load Current, VIN = 5 V

LOAD CURRENT (A)	TPS62085 1 V EFFICIENCY (%)	TPS62087 1.8 V EFFICIENCY (%)	TPS62086 3.3 V EFFICIENCY (%)
0.01	81.4%	85.0%	90.3%
0.02	82.6%	86.3%	89.2%
0.05	82.4%	87.2%	88.4%
0.1	80.9%	89.9%	89.0%
0.2	82.5%	89.8%	90.8%
0.5	86.3%	90.5%	93.5%
1	89.0%	91.8%	94.7%
2	87.9%	91.4%	94.4%
3	85.8%	89.9%	92.2%

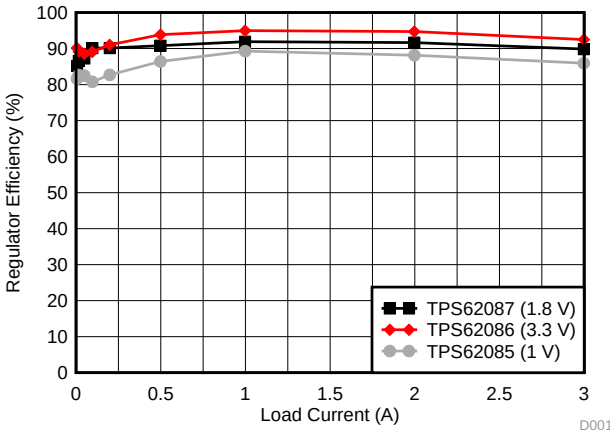


Figure 31. DC/DC Converter Efficiency at VIN = 5 V

Table 10. Efficiency Versus Load Current, VIN = 3.3 V

LOAD CURRENT (A)	TPS62085 1 V EFFICIENCY (%)	TPS62087 1.8 V EFFICIENCY (%)
0.01	81.4%	85.0%
0.02	82.6%	86.3%
0.05	82.4%	87.2%
0.1	80.9%	89.9%
0.2	82.5%	89.8%
0.5	86.3%	90.5%
1	89.0%	91.8%
2	87.9%	91.4%
3	85.8%	89.9%

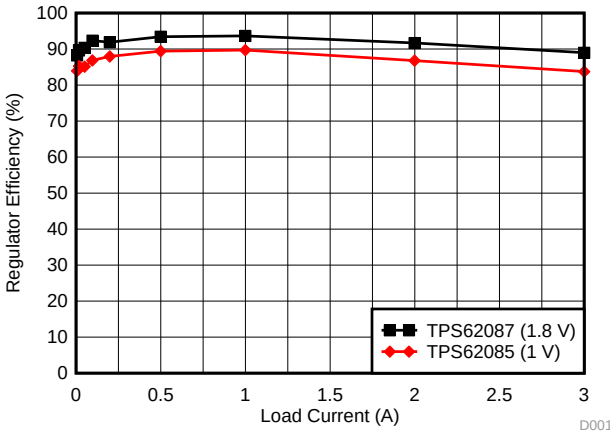


Figure 32. DC/DC Converter Efficiency at VIN = 3.3 V

6.2 DC/DC Converter Ripple and Step Response

The output of each DC/DC converter was observed to measure the peak-to-peak ripple during a 0.1-A to 3-A load step, and full load operation. From the following figures, the first five show each converter's load step response, and the last five show the output ripple at full load. At full load, the frequency of the ripple was measured to be approximately 3 MHz.

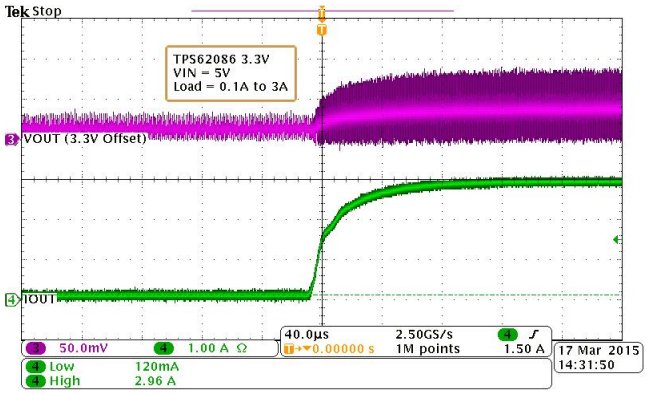


Figure 33. TPS62086 3.3-V load step response, VIN = 5 V, IOUT = 0.1 A to 3 A

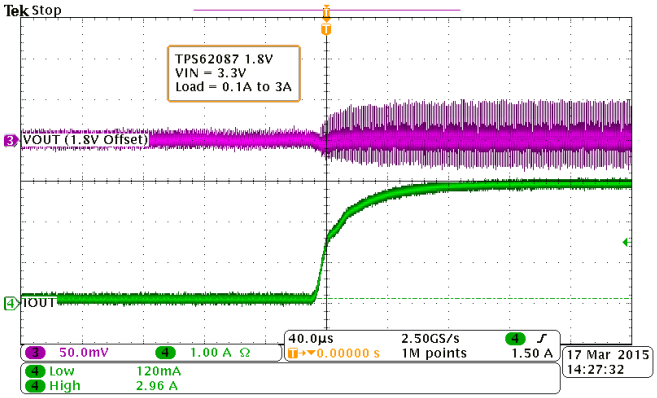


Figure 34. TPS62087 1.8-V load step response, VIN = 3.3 V, IOUT = 0.1 A to 3 A

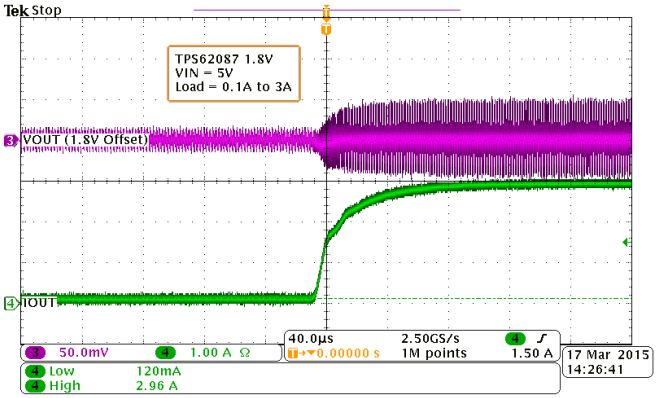


Figure 35. TPS62087 1.8-V load step response, VIN = 5 V, IOUT = 0.1 A to 3 A

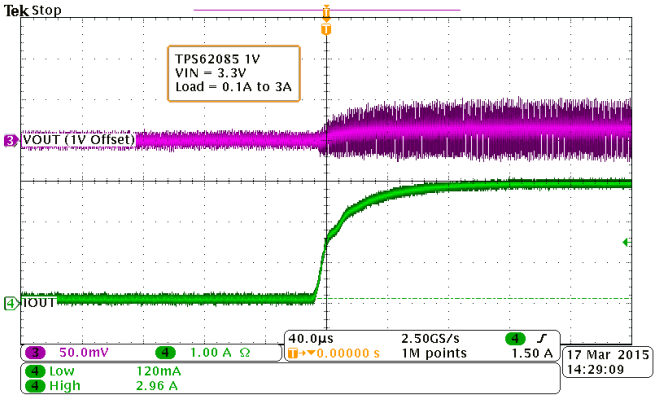


Figure 36. TPS62085 1-V load step response, VIN = 3.3 V, IOUT = 0.1 A to 3 A

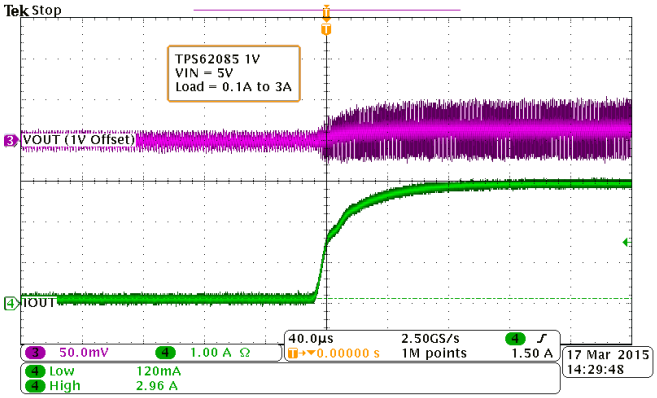


Figure 37. TPS62085 1-V load step response, VIN = 5 V, IOUT = 0.1 A to 3 A

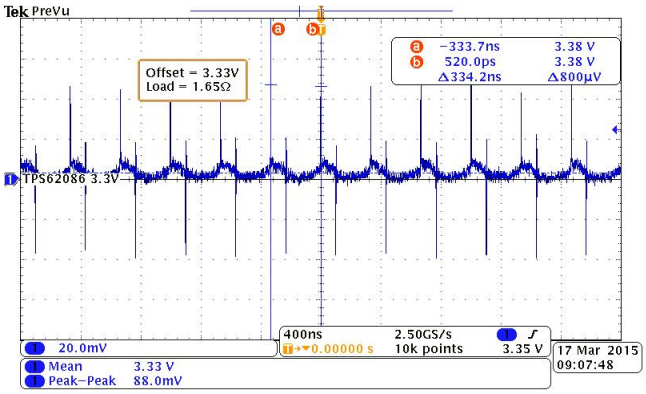


Figure 38. TPS62086 3.3-V Output Ripple, VIN = 5 V, IOUT = 2 A

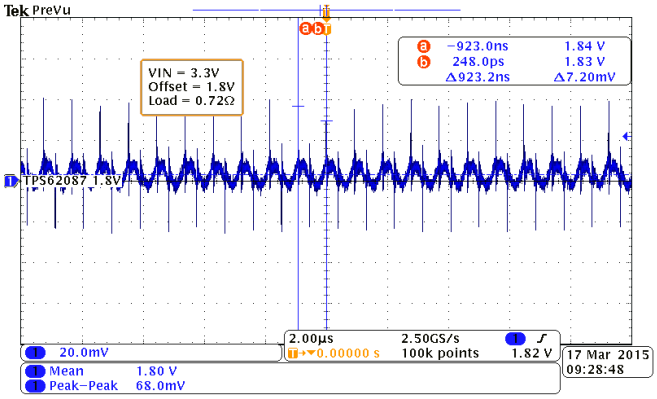


Figure 39. TPS62087 1.8-V Output Ripple, VIN = 3.3 V, IOUT = 2.5 A

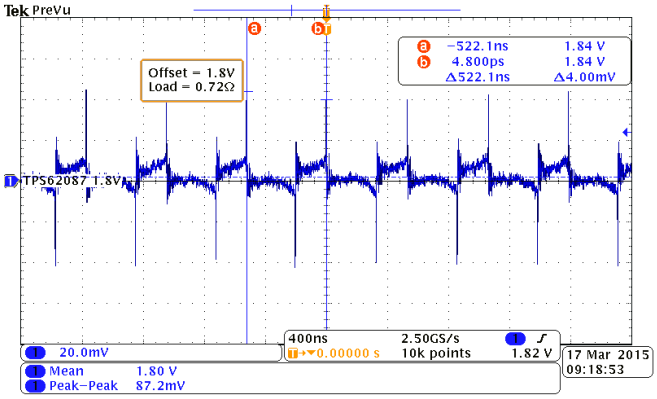


Figure 40. TPS62087 1.8-V Output Ripple, VIN = 5 V, IOUT = 2.5 A

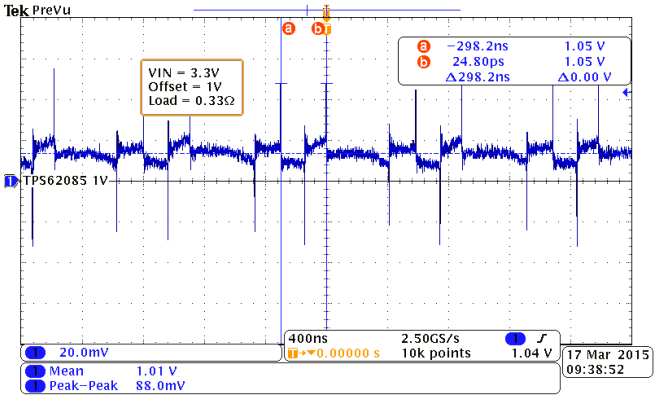


Figure 41. TPS62085 1-V Output Ripple, VIN = 3.3 V, IOUT = 3 A

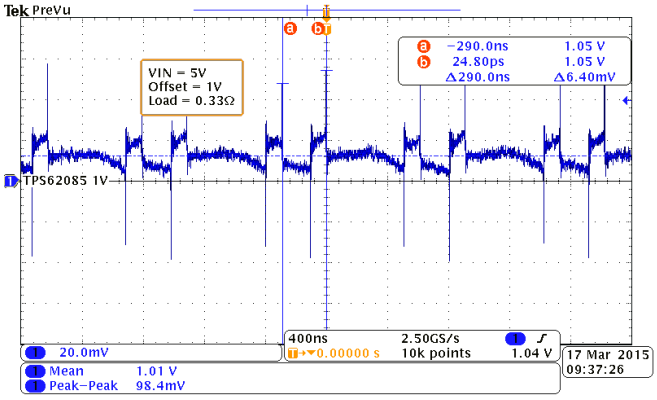


Figure 42. TPS62085 1-V Output Ripple, VIN = 5 V, IOUT = 3 A

6.3 Load Switch Startup and Shutdown Waveforms

Table 11. Load Conditions for Startup and Shutdown Waveforms

DEVICE	NOMINAL VOLTAGE (V)	LOAD
TPS22954	3.3	4.27 A
	5	2.82 A
TPS22922	3.3	1.65 Ω (2 A)
TPS22964C	1.8	0.72 Ω (2.5 A)
TPS22920	1	0.33 Ω (3 A)

The output of the TPS22954 pre-regulation load switch is connected to the SNS pin through a resistor divider. During normal operation, the DC/DC converter ripple can be observed on V_{OUT}, and consequently SNS as well. TPS22954 was designed with hysteresis on SNS to prevent the “power good” signal PG from going low due to ripple on SNS. The following figures show the ripple rejection.

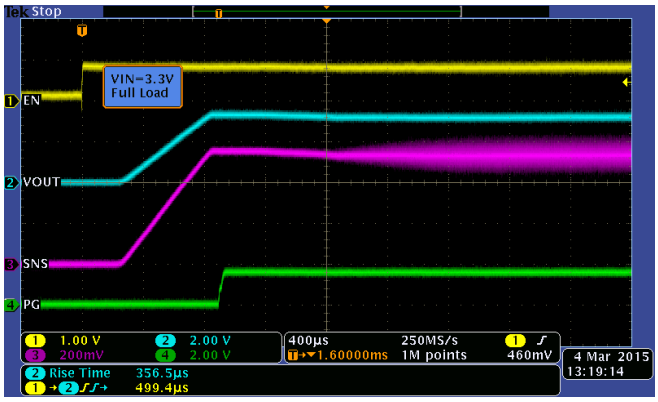


Figure 43. TPS22954 Startup at VIN = 3.3 V, IOUT = 4.27 A

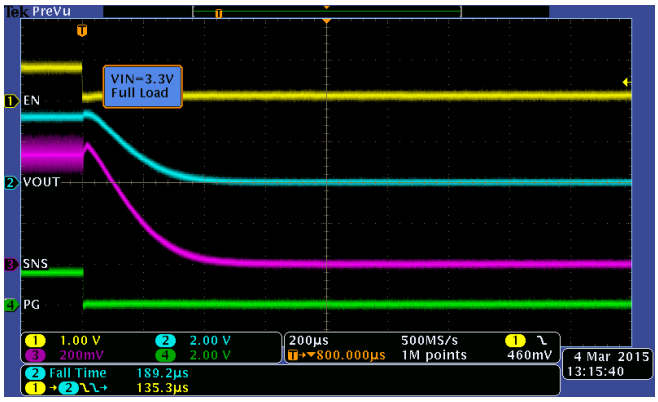


Figure 44. TPS22954 Shutdown at VIN = 3.3 V, IOUT = 4.27 A

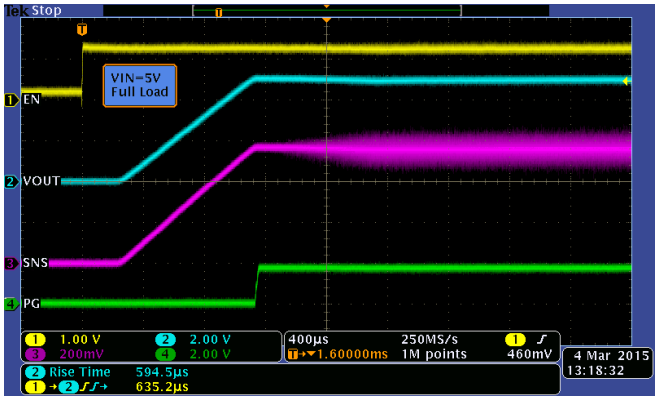


Figure 45. TPS22954 Startup at VIN = 5 V, IOUT = 2.82 A

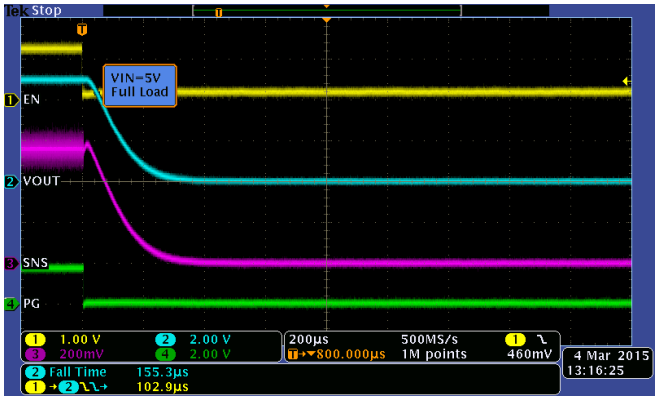


Figure 46. TPS22954 Shutdown at VIN = 5 V, IOUT = 2.82 A

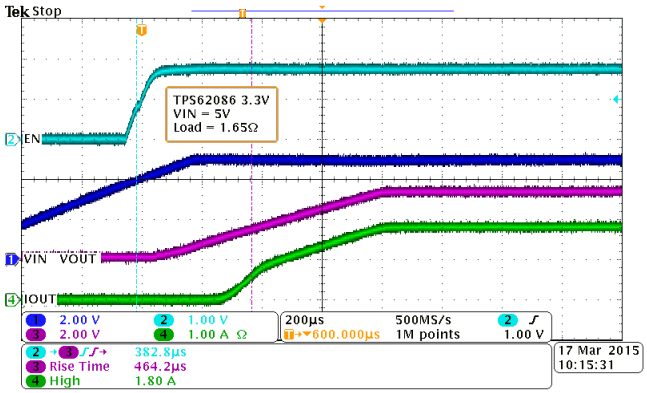


Figure 47. TPS62086 3.3-V Startup at VIN = 5 V, RL = 1.65 Ω, IOUT = 2 A

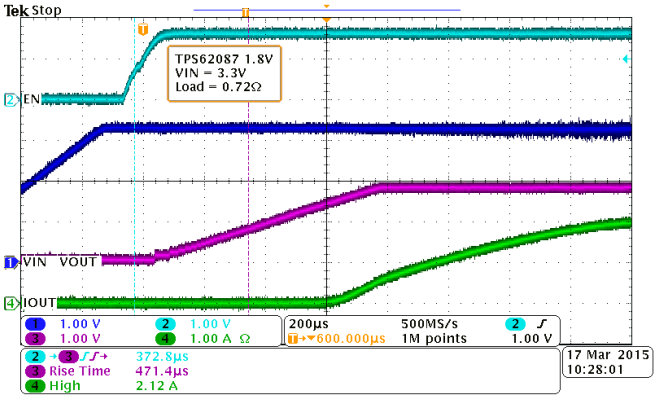


Figure 48. TPS62087 1.8-V Startup at VIN = 3.3 V, RL = 0.72 Ω, IOUT = 2.5 A

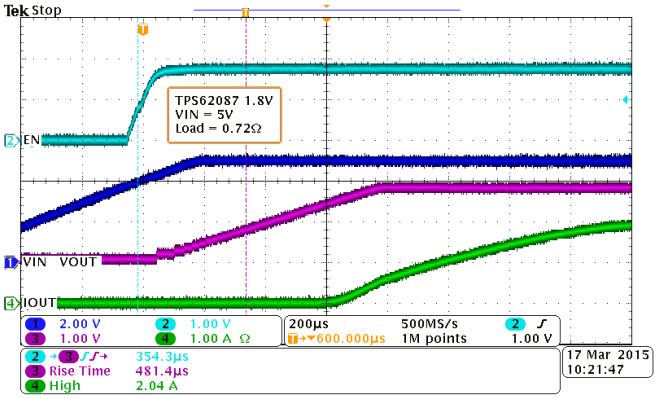


Figure 49. TPS62087 1.8-V Startup at VIN = 5 V, RL = 0.72 Ω, IOUT = 2.5 A

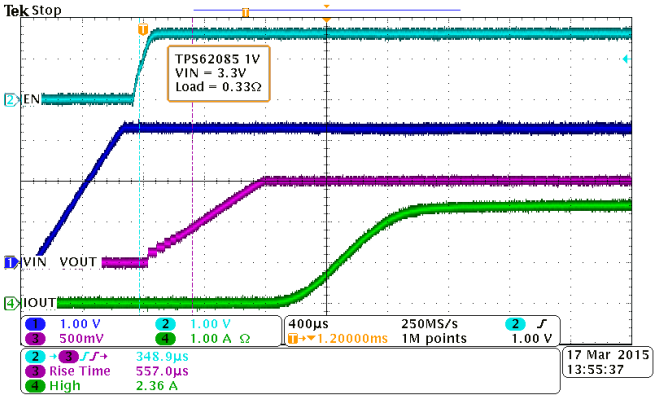


Figure 50. TPS62085 1-V Startup at VIN = 3.3 V, RL = 0.33 Ω, IOUT = 3 A

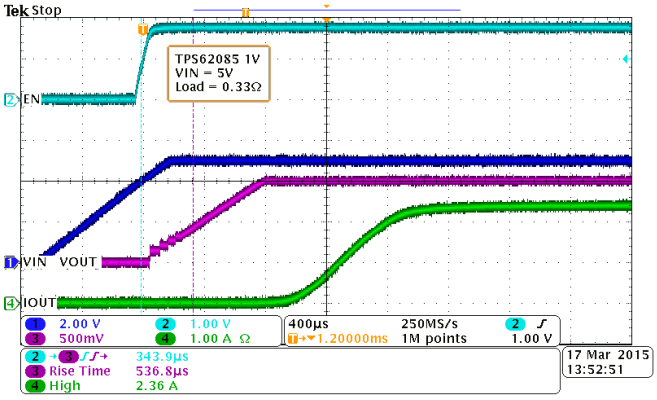


Figure 51. TPS62085 1-V Startup at VIN = 5 V, RL = 0.33 Ω, IOUT = 3 A

6.4 Load Switch Timing

Each load switch was independently observed for turn-on and turn-off performance. The parameters shown in Figure 52 were measured on each load switch at full load. Table 12 shows the summarized results.

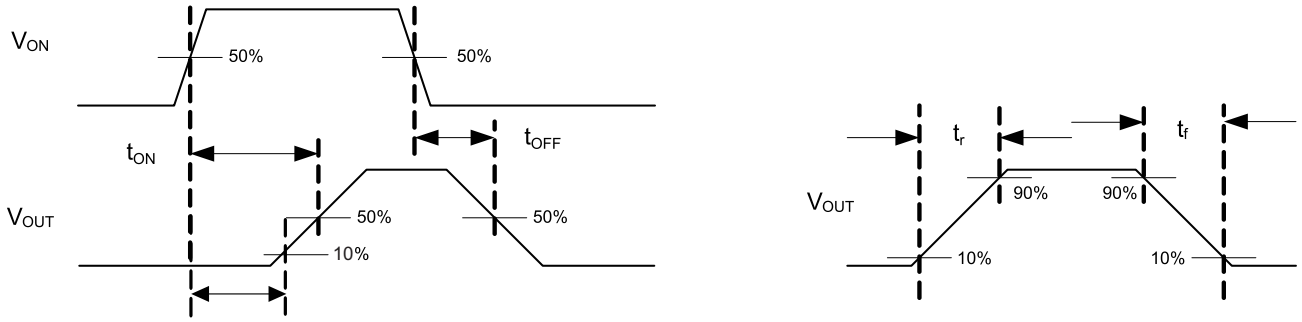


Figure 52. Definition of Load Switch Timing Parameters

Table 12. Timing Characteristics of SSD Power Delivery Load Switches

DEVICE	V_{IN} (V)	t_R (µs)	t_{ON} (µs)	t_D (µs)	t_F (µs)	t_{OFF} (µs)
TPS22954 (CT = 470pF)	5	624.1	634.9	291.2	150.4	101.8
	3.3	407.1	522.4	289.2	217.6	149.1
TPS22922	3.3	36.5	42.9	24.1	1.02	4.49
TPS22964C	1.8	779.2	1012	718.6	0.83	2.49
TPS22920	1	510.2	1009	745.1	2.65	13.94

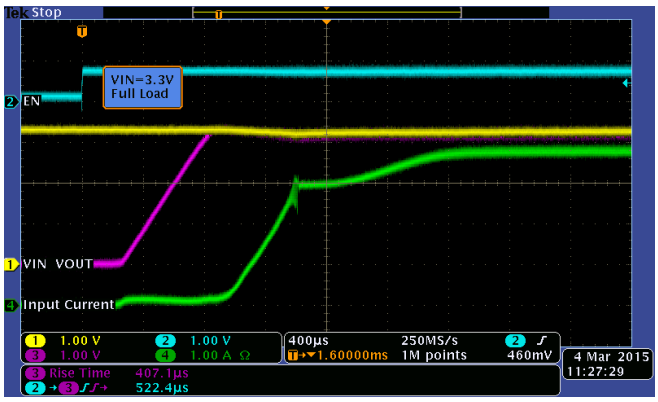


Figure 53. TPS22954 t_R, t_{ON} Measurement at VIN = 3.3 V

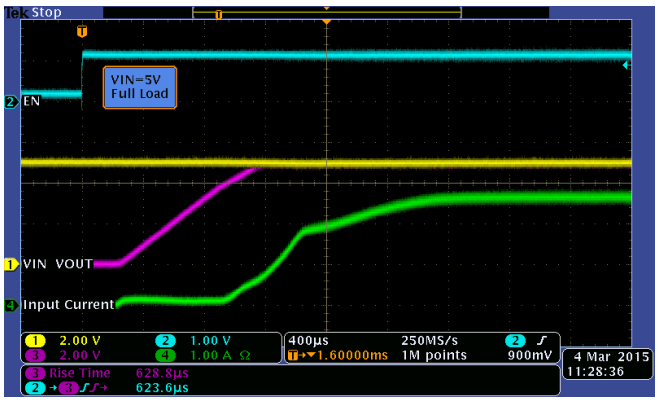


Figure 54. TPS22954 t_R, t_{ON} Measurement at VIN = 5 V

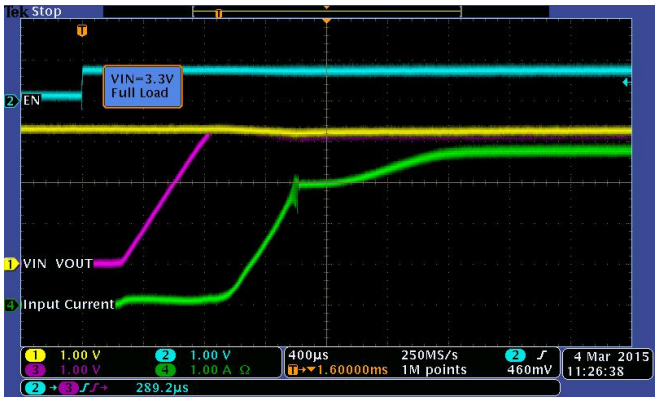


Figure 55. TPS22954 t_D Measurement at VIN = 3.3 V

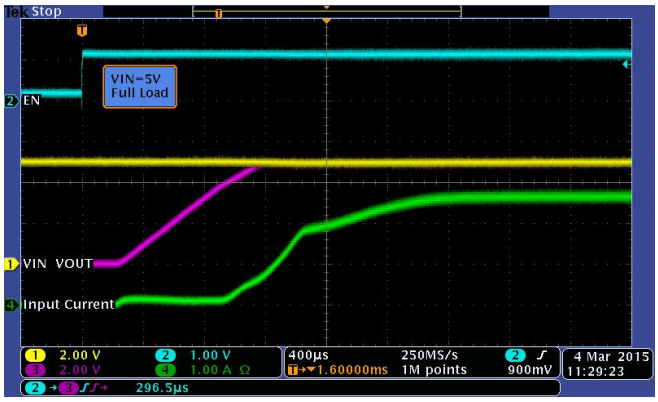


Figure 56. TPS22954 t_D Measurement at VIN = 5 V

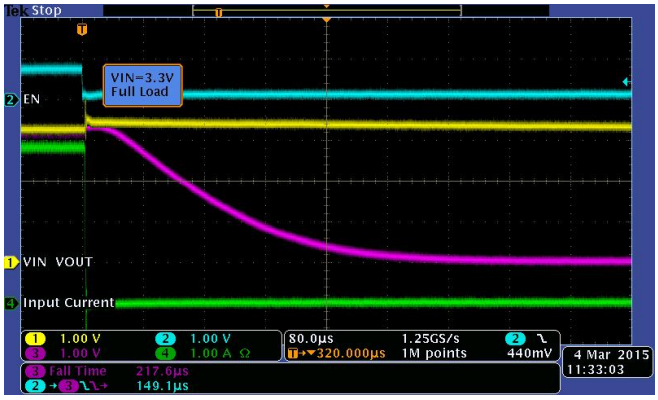


Figure 57. TPS22954 t_F, t_{OFF} Measurement at VIN = 3.3 V

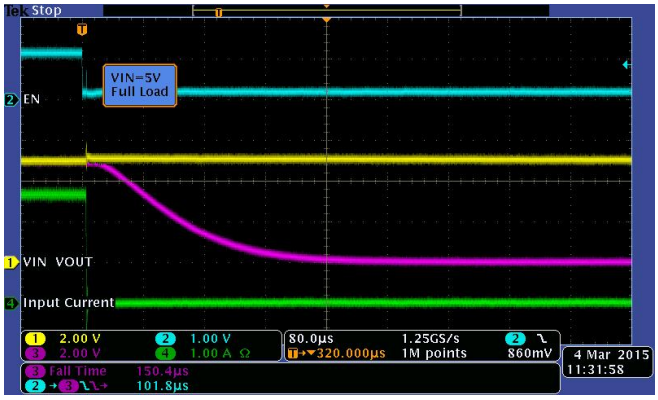


Figure 58. TPS22954 t_F, t_{OFF} Measurement at VIN = 5 V

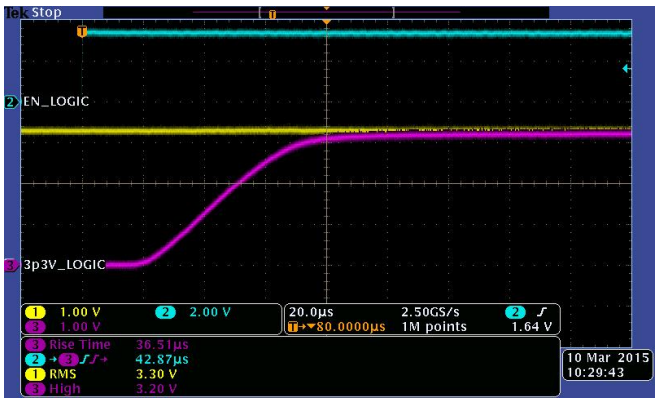


Figure 59. TPS22922 t_R, t_{ON} Measurement at VIN = 3.3 V, RL = 1.65 Ω, IOUT = 2 A

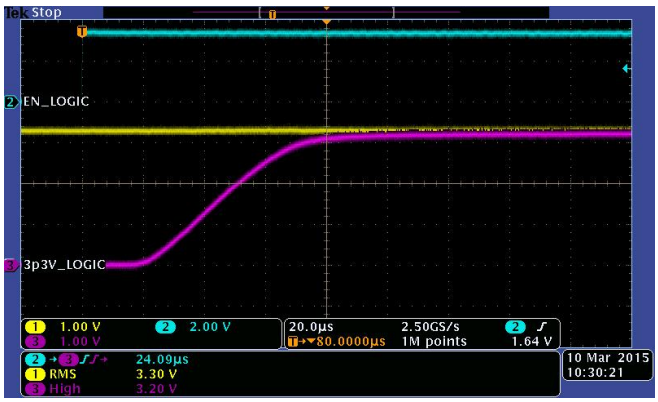


Figure 60. TPS22922 t_D Measurement at VIN = 3.3 V, RL = 1.65 Ω, IOUT = 2 A

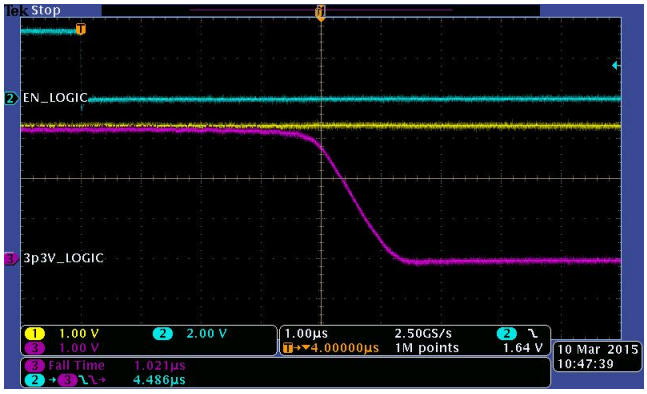


Figure 61. TPS22922 t_F, t_{OFF} Measurement at VIN = 3.3 V, RL = 1.65 Ω, IOUT = 2 A

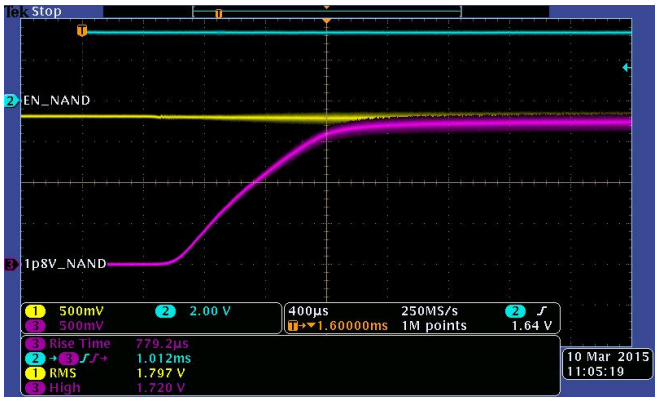


Figure 62. TPS22964C t_R, t_{ON} Measurement at VIN = 1.8 V, RL = 0.72 Ω, IOUT = 2.5 A

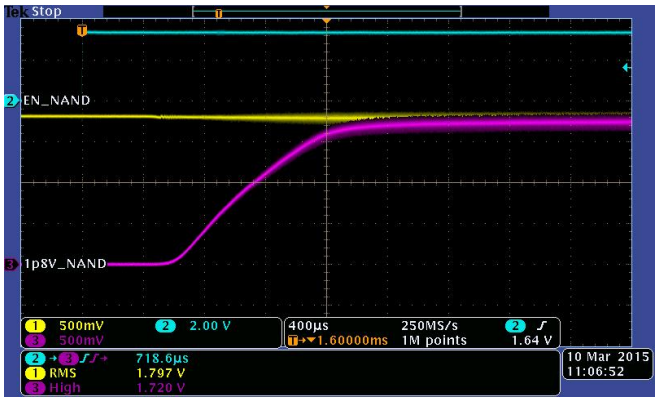


Figure 63. TPS22964C t_D Measurement at VIN = 1.8 V, RL = 0.72 Ω, IOUT = 2.5 A

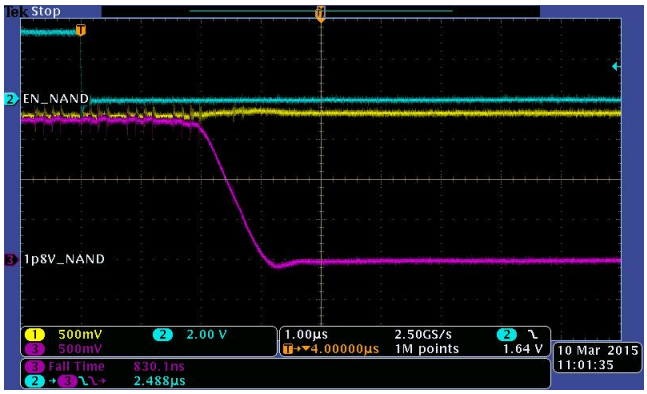


Figure 64. TPS22964C t_F, t_{OFF} Measurement at VIN = 1.8 V, RL = 0.72 Ω, IOUT = 2.5 A

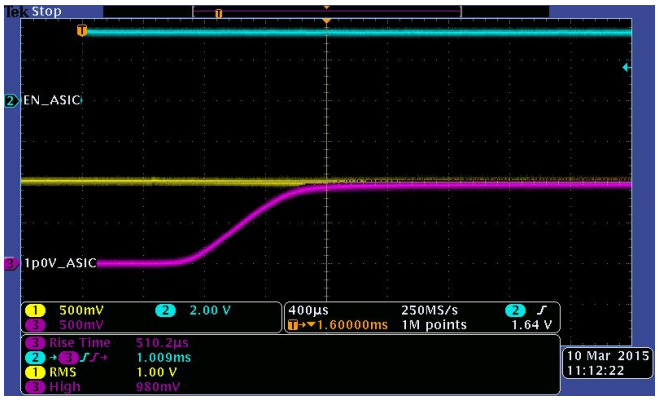


Figure 65. TPS22920 t_R, t_{ON} Measurement at VIN = 1 V, RL = 0.33 Ω, IOUT = 3 A

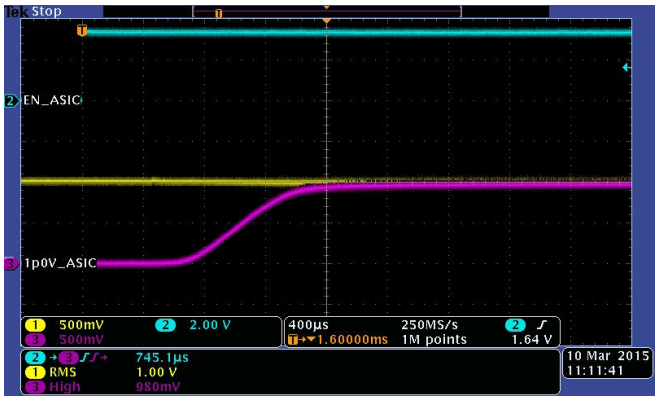


Figure 66. TPS22920 t_D Measurement at VIN = 1 V, RL = 0.33 Ω, IOUT = 3 A

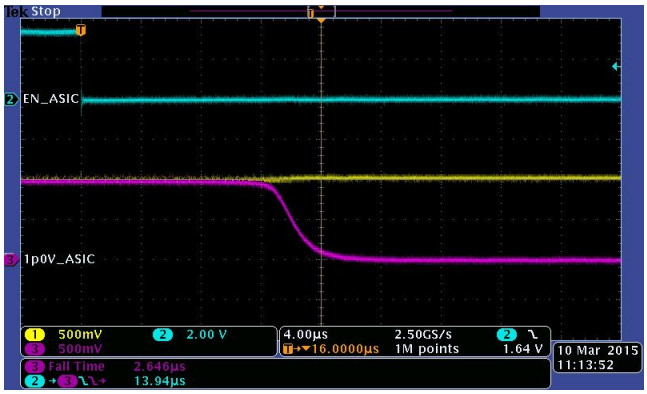


Figure 67. TPS22920 t_F, t_{OFF} Measurement at VIN = 1 V, RL = 0.33 Ω, IOUT = 3 A

7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-00399.

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00399.

7.3 Layout Prints

To download the layer plots, see the design files at TIDA-00399.

7.4 PCB Layout Recommendations

- Input and output voltage traces to load switches should be as wide as possible to minimize series resistance and inductance for high-current applications.
- Devices that require tight tolerance on CT capacitance should use a capacitor with C0G dielectric and minimal copper around the CT capacitor. Copper layers around the CT net can result in additional parasitic capacitance on the order of 100 s of femtofarads (fF) to 10 s of picofarads (pF).
- Devices with an exposed thermal pad should have vias to another layer for thermal relief during high-current operation
- Input and output voltage terminals should be bypassed to ground with a low equivalent series resistance (ESR) capacitor. The recommended dielectric is X5R or X7R depending on the application. A 10:1 ratio is recommended for input to output capacitance on all load switches. Each capacitor should be placed as close as possible to its corresponding terminal.
- Step-down converters should be located close to their point-of-load (PoL) to minimize loss and maximize efficiency.

7.5 Altium Project

To download the Altium project files, see the design files at TIDA-00399.

7.6 Gerber Files

To download the Gerber files, see the design files at TIDA-00399.

7.7 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00399.

7.8 Software Files

To download the software files, see the design files at TIDA-00399.

8 Glossary

AON— "Always On", used to describe a rail that provides low-current standby power. Contrasts with switched rails that provide the necessary current for standard operation.

ASIC— Application-Specific Integrated Circuit. A device designed for a specific purpose, not for general use. In this application, the ASIC refers to a NAND memory management device.

Brownout— A condition where the supply voltage falls below its typical operating value. Brownouts can cause unintentional behavior in circuits and impair system functionality.

GPIO— General purpose input / output, typically used for low-speed digital control. Other functions can be present on GPIO pins as well depending on the platform.

Inrush Current—Current that occurs during turn-on due to load capacitance. Can cause supply voltage sag and brownout. Can be reduced by reducing load capacitance or voltage rise time.

M.2— Formerly NGFF, "Next Generation Form Factor", M.2 is a replacement for the mSATA standard that uses the PCI Express Mini Card physical layout. The M.2 interface is suited for use in SSDs in tablets and ultrabooks, owing to its small size and advanced features.

NAND— "Not AND", a common type of non-volatile flash memory used in solid-state drives.

SSD— Solid-State Drive, an alternative to spinning hard disk drives that store data in non-volatile flash memory.

UVLO— Undervoltage lock-out, the voltage at which a device disables due to the input voltage being too low.

9 References

1. *Load Switches: What Are They, Why Do You Need Them And How Do You Choose The Right One?* (SLVA652)
2. *Choosing an Appropriate Pull-up/Pull-down Resistor for Open Drain Outputs* (SLVA485)
3. *High-efficiency, low-ripple DCS-Control™ offers seamless PWM/power-save transitions*, (SLYT531)
4. Texas Instruments, *Five steps to a great PCB layout for a step-down converter* (SLYT614)
5. Texas Instruments, Solid State Drive (SSD): Enterprise
6. Texas Instruments, Solid State Drive (SSD): Client

10 About the Author

BRIAN LACKEY is a Validation Engineer at Texas Instruments, where he is responsible for validating load switches from the TPS229xx family. Brian earned his Bachelor of Science in Electrical Engineering (BSEE) from Rose-Hulman Institute of Technology in Terre Haute, IN.

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