# TI Designs
# *Low Cost, Small Solution Size Power Management Reference Design for CC3200 SimpleLink™ Wi-Fi®*

**TEXAS INSTRUMENTS**

## TI Designs

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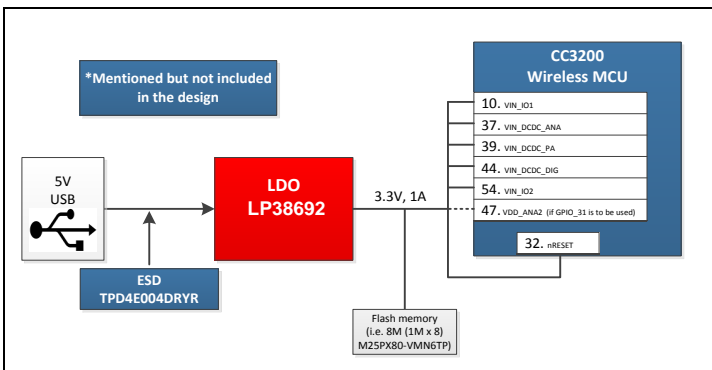
## Design Resources

| | |
|---|---|
| TIDA-00534 | Design Online Folder |
| LP38692 | Product Online Folder |
| TPD4E004 | Product Online Folder |
| CC3200 | Product Online Folder |

| TI E2E™ Community | Ask The Analog Experts |
|---|---|
| | WEBENCH® Design Center |

## Block Diagram



## Design Features

- Power management solution for noise sensitive systems with wireless capabilities.
- Provides 3.3V rectify and clean voltage supply from a 5V power rail (i.e. battery, USB connector, Power over coaxial).
- Low current to ground during load standby (50µA typical).
- 50dbs input ripple rejection at 100 kHz noise frequency and maximum load current.
- Great load transient response. Better than 5% output voltage transient from 1mA to 250 mA load current change.
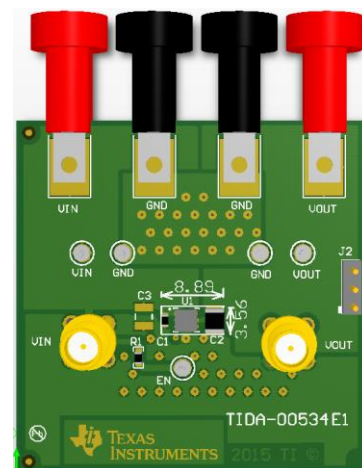- Small foot print; area smaller than 31.7 mm$^2$

## Applications

Some of the possible end equipment's are:

- **Consumer Electronics:**
  - Alarm Systems
  - USB wireless adapter
  - Speakers, headsets, sound-bars
  - Home Appliances
- **Industrial:**
  - Noise sensitive Wi-Fi based sensors.
  - Gas Detection
  - Scales
  - Barcode scanners

## Board Image
TIDA-00534 power solution test Board

# 1   Design Description

The Internet of Things (IoT) has revolutionized the way we interact and operate gadgets, remote sensors, tools, etc. TI has greatly contributed to IoT with the development of CC3200 the first Wi-Fi certified Single chip microcontroller unit built in Wi-Fi Connectivity. This wireless MCU is a robust system on chip (SoC) that could simplify the design and improve time to market.

Equally important are the power management solutions that TI offers which simplify the application design and provide an easy power solution. TIDA-00534 mentions design considerations that must be taken into account when providing powering to the CC3200, but its main focused is to provide guideline and test data of a cost effective and small size power solution that can be used to power the main 3.3V power rails of the CC3200 or other noise sensitive device from a 5V power source (i.e. battery, USB connector, power over coaxial cable, etc.).

**Notice** This design only provides test data and design files for the power section, it does not include the complete system with the CC3200, for details about the CC3200 analog/digital pin connections and application implementations please refer to CC3200 Data Sheet SWAS032F

## 1.1   Design features and benefits

**Low noise**

This design uses a low dropout linear regulator which has a great noise filtering capability over conducted ripple which could be generated by the normal operation of switching circuits. Large discontinuous currents are generated by the power switches turn on and off. In a buck topology, large discontinuous currents are present at the input. The voltage ripple, created by those discontinuous currents, can couple into the rest of the system and cause EMI issues.

**Fold-back Current Limiting**

This feature reduces the amount of the output current the part can deliver as the output voltage is reduced. The amount of load current is dependent on the differential voltage between VIN and $V_{OUT}$. When the input output delta voltage is reduced below 4 V, load current is limited to about 1500 mA.

**ESD protection**

When the TPD4E004 is included in the design the overall system will have an electro static discharge protection up to 15kV pick voltage.

**Enable (EN)**

By pulling the EN pin low in the LP38692 the quiescent current or ground current will be reduced to virtually zero. This will be a great feature in the case that the system has a supervisory microcontroller that can control the EN pin within the low and high limits.

**Fast power up**

With 5V $V_{IN}$ the output will typically takes 150µs from the moment the input voltage goes high to the moment the output voltage reaches 95% of the nominal 3.3V output voltage.

**Input Ripple Rejection**

The high input voltage ripple rejection will act as a line cleaner in from 10Hz to 10 MHz

**Remote sense**

The LP38692 (WSON package only) output sense pin allows remote sensing at the load which eliminates the error in output voltage due to voltage drops caused by the resistance in the traces between the regulator and the load. This pin must be tied to $V_{OUT}$

**Small foot print**

The LP387692 comes in a tiny WSON package with dimensions and only requires two small compensation components: input and output capacitor.
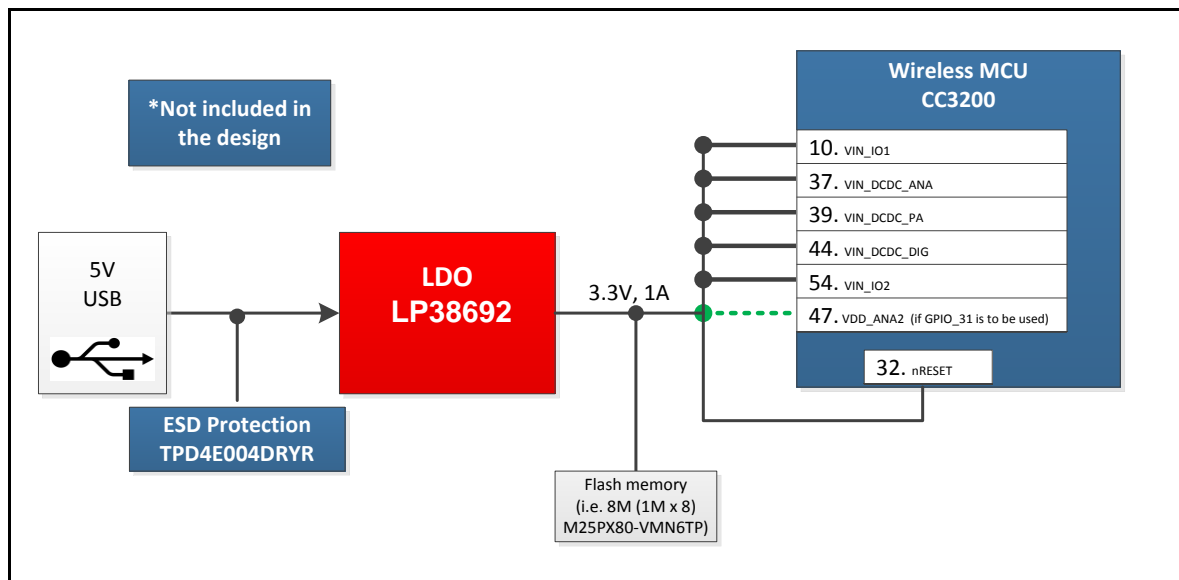
## 2    Block diagram



**Figure 1 Functional Block Diagram**

As mentioned in previous section the main focus of this document is to provide test data and design parameters to provide clean power to the wireless MCU CC3200 using the LP38692 linear regulator. The blocks in blue means that some design parameters of those devices are mentioned in this document, however they are not designed in the system.

The green dotted line connected to the pin 47 in the CC3200 block represents an optional connection only required when the GPIO_31 needs to be used.

## 3   Component Selection

TIDA-00534 mentions the following devices:

LP38692: 1A Low Dropout CMOS Linear Regulators, Stable with Ceramic Output Capacitors
CC3200: CC3200 SimpleLink™ Wi-Fi® and Internet-of-Things solution, a Single-Chip Wireless MCU
TPD4E004: (recommended ESD protection) 4-Channel ESD Protection Array for High-Speed Data Interfaces

## 3.1   LP38692 Low Dropout Regulator

The LP38692 low-dropout CMOS linear regulators provide tight output tolerance (2.5% typical), extremely low dropout voltage, and excellent AC performance utilizing ultra-low ESR ceramic output capacitors.

Part highlights

- The low thermal resistance of the ultra-small WSON package (3mm by 3mm), SOT-223, and TO-252 packages allow the full operating current to be used even in high ambient temperature environments.
- The use of a PMOS power transistor means that no DC base drive current is required to bias it allowing ground pin current to remain below 100 µA regardless of load current, input voltage, or operating temperature.
- The LP38692 can achieve virtually zero quiescent current when the Enable pin is pulled low.
- Remote voltage sense feature to compensate for voltage drop on due to high resistance in the PCB traces.
- This Device does not require feedforward capacitor saving board space and BOM cost.
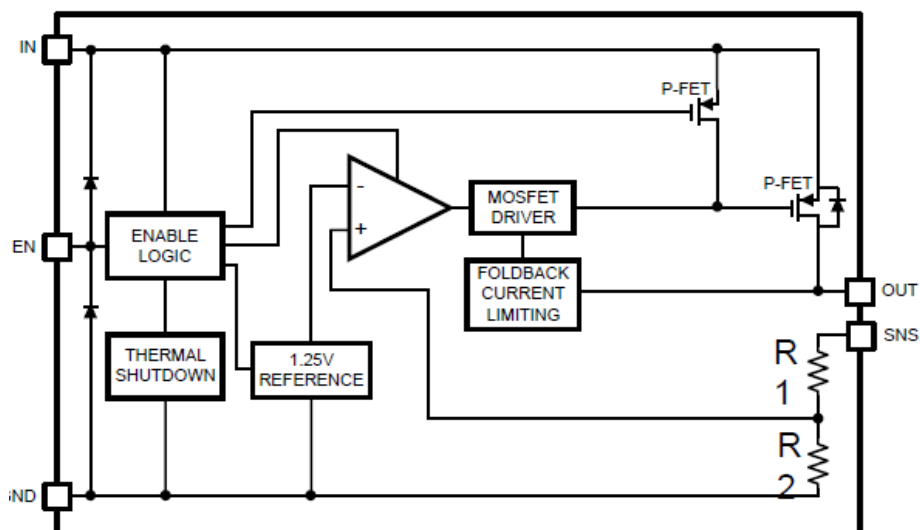


**Figure 2 LP38692 Block Diagram**

## 3.2 CC3200 SimpleLink™ Wi-Fi® and Internet-of-Things solution, a Single-Chip Wireless MCU

CC3200 is the Industry's first Wi-Fi CERTIFIED single-chip microcontroller unit (MCU) with built-in Wi-Fi connectivity. Created for the Internet of Things (IoT), the Simple Link CC3200 device is a wireless MCU that integrates a high-performance ARM Cortex-M4 MCU, allowing customers to develop an entire application with a single IC. With on-chip Wi-Fi, Internet, and robust security protocols, no prior Wi-Fi experience is required for faster development. The CC3200 device is a complete platform solution including software, sample applications, tools, user and programming guides, reference designs, and the TI E2E™ support community. The device is available in a QFN package that is easy to layout.

The applications MCU subsystem contains an industry-standard ARM Cortex-M4 core running at 80 MHz The device includes a wide variety of peripherals, including a fast parallel camera interface, I2S, SD/MMC, UART, SPI, I$^2$C, and four-channel ADC. The CC3200 family includes flexible embedded RAM for code and data and ROM with external serial flash boot loader and peripheral drivers.
The Wi-Fi network processor subsystem features a Wi-Fi Internet-on-a-Chip and contains an additional dedicated ARM MCU that completely offloads the applications MCU. This subsystem includes an 802.11 b/g/n radio, baseband, and MAC with a powerful crypto engine for fast, secure Internet connections with 256-bit encryption. The CC3200 device supports Station, Access Point, and Wi-Fi Direct modes. The device also supports WPA2 personal and enterprise security and WPS 2.0. The Wi-Fi Internet-on-a-chip includes embedded TCP/IP and TLS/SSL stacks, HTTP server, and multiple Internet protocols.

The power-management subsystem includes integrated DC-DC converters supporting a wide range of supply voltages. This subsystem enables low-power consumption modes, such as the hibernate with RTC mode requiring less than 4 µA of current.
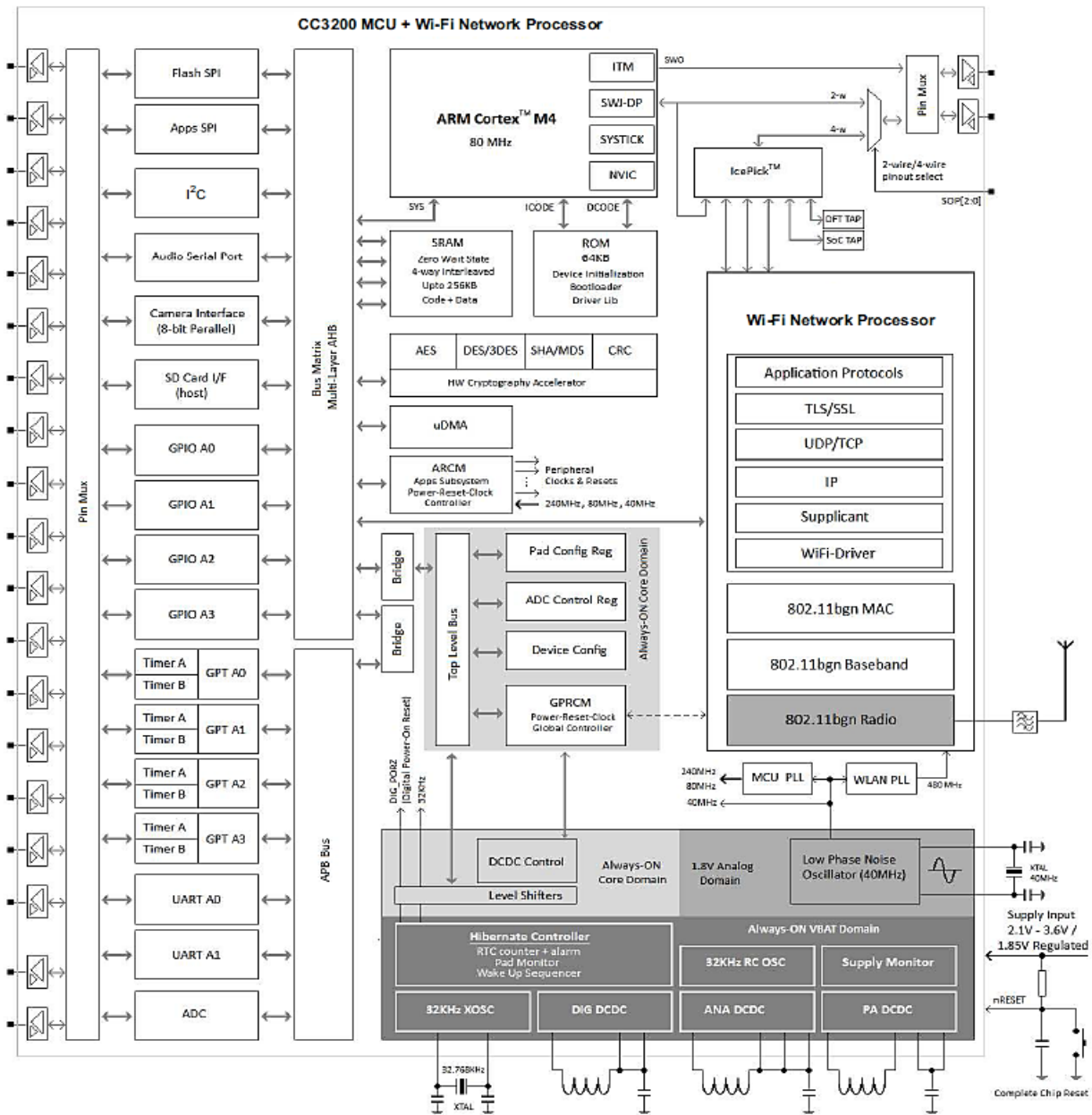
**Figure 3 CC3200 Block Diagram**

## 3.3 TPD4E004 ESD protection

The TPD4E004 is a quad-ESD structure designed for USB, Ethernet, and other high-speed applications. The TPD4E004 has a low-capacitance ±15-kV ESD-protection diode array designed to protect sensitive electronics attached to communication lines. Each channel consists of a pair of diodes that steers ESD current pulses to $V_{CC}$ or GND.

Typically the linear regulators and CC3200 have a 2K (HBM) protection, but by implementing this additional safety feature the system will be protected against higher ESD pulses up to ±15-kV Human-Body Model (HBM), ±8-kV Contact Discharge, and ±12-kV Air-Gap Discharge, as specified in IEC 61000-4-2. This device has a 1.6-pF capacitance per channel, making it ideal for use in high-speed data IO interfaces.

Other benefit of using TPD4E004 over a discrete solution is the ultra-small SON package with dimensions of 1mm by 1.45mm.

EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.

## 4    CC3200 Power Supply Considerations

### 4.1    5V or USB Power Supply for CC3200

The intended used of this power design is to regulate 5V or USB power supply to 3.3V in order to provide stable voltage to the five power pins 10-VIN_IO1, 37-VIN_DCDC_ANA, 39-VIN_DCDC_PA, 44-VIN_DCDC_DIG, and 54-VIN_IO2 of the CC3200.

By using this scheme the CC3200 will utilize the integrated power management subsystem to generate the required voltages to operate the device and the CC3200 will support wide-voltage operations from 2.1 to 3.6 V source.

#### 4.1.1    CC3200 Current Requirements

The current demand of the CC3200 at $3.3V_{IN}$ can reach 450mA during calibration and around 307 mA during transmit (TX). The power source must be able to supply at least 500 mA.

#### 4.1.2    CC3200 Input Supply voltage

The minimum input voltage of the CC3200 in wide input voltage configuration is 2.1V. If a serial flash memory is powered from the same power rail as the CC3200 the input voltage of the voltage requirement of the flash memory must be taken into account, generally the s-flash has a minimum operating range of 2.3V.

Also if the input voltage drops below the minimum 2.1V the CC3200 can fall into a brown-out. For this reasons the input supply voltage must be between 2.6V and 3.6V. If the nominal input voltage is 3.3V the ripple voltage must be lower than ±300mV to avoid exceeding the maximum input voltage.

The supply voltage must not exceed the minimum and maximum voltage limits under a load transient condition of 500 mA at 5µS rising time. In the same way when a line transient occurs the output voltage should not exceed the minimum and maximum voltage limits.

### 4.1.3   CC3200 Brownout and Blackout Voltage levels

The device enters in a brown-out condition whenever the input dips below 2.1V. It is essential to understand the voltage limits that might cause the device to run into a brownout or blackout.

**Table 1 Brownout and Blackout Threshold**

| CONDITION | VOLTAGE LEVEL | UNIT |
|---|---|---|
| $V_{BROWNOUT}$ | 2.1 | V |
| $V_{BLACKOUT}$ | 1.67 | V |

In a brownout condition all the section of the devices shutdown except of the hibernate module. In the other hand during a blackout event the hardware resets. For this reason the voltage regulator must have good transient regulation to avoid a reset and loose of information.
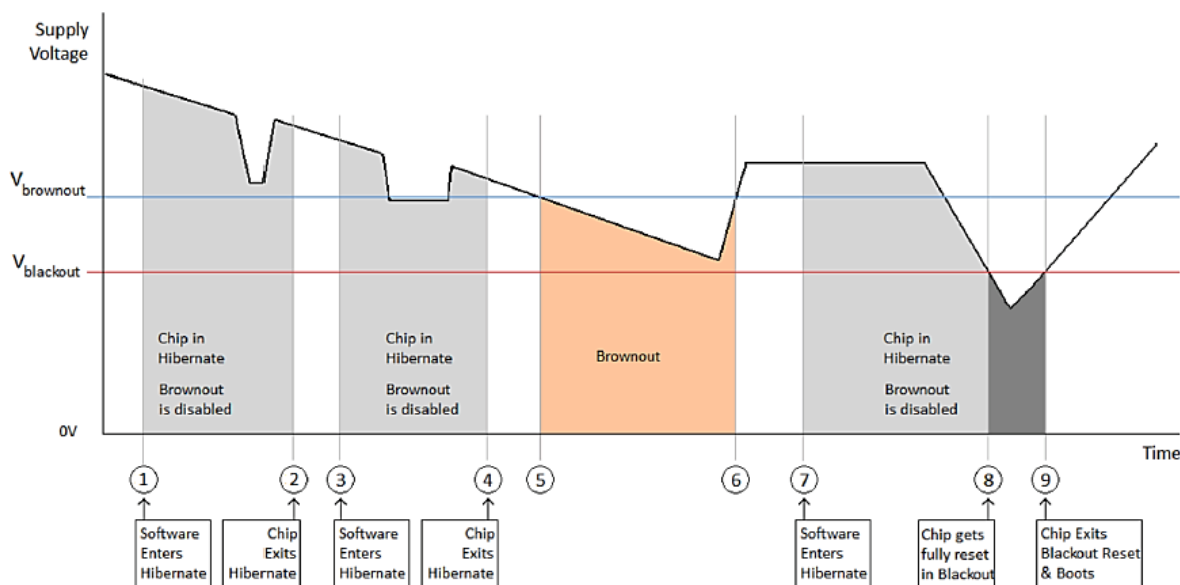


**Figure 4 CC3200 brownout Blackout level**
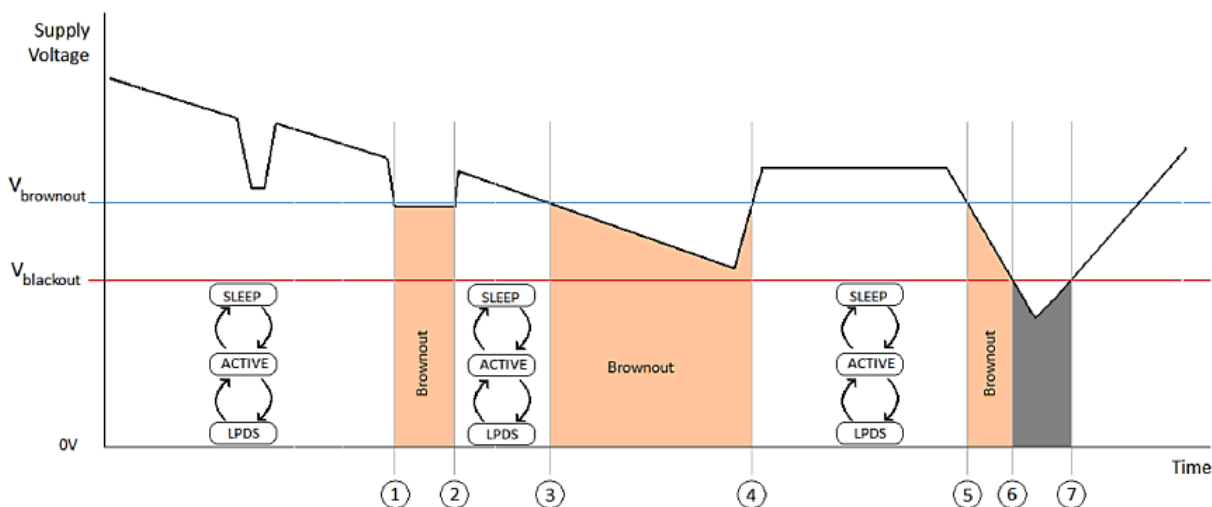


**Figure 5 CC3200 brownout and blackout level (second part)**

### 4.1.4   Devices interfacing with the CC3200

If an external device drives a positive voltage to the signal pads and the CC3200 device is not powered, DC current is drawn from the other device. If the drive strength of the external device is adequate, an unintentional wakeup and boot of the CC3200 device can occur. To prevent current draw, TI recommends any one of the following:

• All devices interfaced to the CC3200 device must be powered from the same power rail as the chip.
• Use level-shifters between the device and any external devices fed from other independent rails.
• The nRESET pin of the CC3200 device must be held low until the VBAT supply to the device is driven and stable.

## 4.2   Power Supply Sequencing

For proper operation of the CC3200 device, perform the recommended power-up sequencing as follows:
1.   Tie VBAT (pins 37, 39, 44) and VIO (pins 54 and 10) together on the board.
2.   Hold the RESET pin low while the supplies are ramping up. TI recommends using a simple RC circuit (100K || 0.1 µF, RC = 10 ms).
3.   Supply setting time requirement is typical 3ms.
4.   For an external RTC clock, ensure that the clock is stable before pulling RESET pin high.

## 4.3   Power subsystem

The CC3200 power-management subsystem contains DC-DC converters to accommodate the differing voltage or current requirements of the system.

• Digital DC-DC – Input: VBAT wide voltage (2.1 to 3.6 V)
• ANA1 DC-DC – Input: VBAT wide voltage (2.1 to 3.6 V)
• PA DC-DC – Input: VBAT wide voltage (2.1 to 3.6 V)
• VIO is Always Tied with VBAT

For a detail chart of CC3200 current demand and analog and digital pin connections and additional requirements please refer to the CC3200 Datasheet SWAS032F

# 5  LP38692 Design considerations

## 5.1  Capacitor Selection

The LP38690 and LP38692 are designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (temperature types Z5U, Y5V or X7R/X5R) with ESR between 5 mΩ to 500 mΩ is suitable in the LP38692 application circuit.

In this case we evaluated the LP38692 with 100µF output capacitor, because of better transient and PSRR, Also two 47µF can be used to achieve similar performance. However this device works fine with 1µF. Performance graphs with various capacitor configurations can be obtained from the datasheet SNVS322L

## 5.2  Efficiency

The 3.3 linear regulator mentioned in this design operates at an efficiency of 66% and a DC-DC would have provided an efficiency of 80% to 85% at full load. Since most of the time the CC3200 is under sleep mode the efficiency the DC/DC buck regulator would be a lot lower so there would not be a great benefit of utilizing a switching regulator.

## 5.3  PCB Trace Voltage Drop

It is crucial to determine the minimum trace width needed for the expected maximum current to avoid voltage drop due to a trace ohmic resistance.
For example if the total system current is 900mA, the thickness of the trace is 1 oz. and the length of the trace is about 2 inches the width of the trace should be at least 27 mils for internal layer and 10.5 mils for external layer.
The trace width can be calculated using the following equations:
First calculate the area

$$Area^2[mils] = \left(\frac{Current\ A}{k \times (temp_{RISE} C^o)^b}\right)^{\frac{1}{c}}$$
( 1 )

Then using the area calculates the minimum trace width.

$$Width[mils] = \frac{Area^2}{Thickness[oz] \times 1.378[\frac{mils}{oz}]}$$
( 2 )

**Note**:  Temp$_{RISE}$ = Temperature rise means the trace temperature increase when current flow thought the trace. This spec is based on the type of PWB material used.
For IPC-2221 internal layers: k = 0.024, b = 0.44, c = 0.725
For IPC-2221 external layers: k = 0.048, b = 0.44, c = 0.725

## 5.4   Thermal Performance for LP38692 in WSON package

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

Specifications for Equations 3 and Equation 4
- WSON package Junction-to-ambient thermal resistance $R_{\theta JA}$ = 50.6°C/W
  - The $R_{\theta JA}$ value is based on EIA/JESD51-7 standard test board
- $T_{A\_MAX}$ = Maximum ambient temperature
- $T_{J\_MAX}$ = Maximum Junction temperature 125°C
- $V_{IN\_MAX}$ = Maximum input voltage = 5V+5% = 5.25V
- $V_{OUT\_MIN}$ = Minimum output voltage = 3.3V
- $I_{LOAD\_MAX}$ = Maximum output current = 500mA
- $I_{GND}$ = Typical quiescent current = 50µA

The maximum allowable power dissipation for the device in a given package can be calculated using Equation 3

$$P_{DMAX} = (V_{INMAX} - V_{OUTMIN}) \times I_{LOADMAX} = 0.975\,w \qquad (3)$$

The Equation 4 can be used to calculate the maximum theoretical ambient temperature of operation

$$T_{A\_MAX} = -(R_{\theta JA} \times P_{DMAX}) + T_{J\_MAX} = -(50.6 \times 0.975w) + 125°C = 75.6°C \qquad (4)$$

The computed $T_{A\_MAX}$ with equation 4 can be consider as the worst case scenario, because a system board rarely approximates the test JEDEC board used to determine $R_{\theta JA}$. The PCB board layout strongly influences the thermal dissipation of the device; the following guidelines should be used to improve thermal dissipation.

- Use large and multi-layer PCB boards (at least 4 layers, 3"x3", 2oz/1oz/1oz/2oz).
- Use thermal vias connecting the DAP landing pattern on the top layer, inter GND, and bottom GND layer in both DAP landing pattern and ground plane.
- Make the thermal vias near the periphery of the exposed DAP if the maximum number of vias is not applicable.
- Use 0.33 mm diameter of vias if possible, especially for packages with small exposed pad, which may reduce $R_{\theta JA}$ about 15~25%.
- Generate as large a GND plane as allowable on the top and bottom layers, especially right near the package.
- Connect the top GND pattern with the DAP landing pattern underneath the package.
- Gather the same functional pins together in die design, such as for GND, $P_{IN}$, $P_{OUT}$ in the power device. This will allow maximizing the Cu area right near the package by eliminating the needs for isolating each lead pattern on the PCB.
- Make the traces as long as possible so that a better thermal conductivity near the package is achieved.

For more detail information about how to design an optimized board for best thermal resistance please refer to application report "AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Packages" (SNVA183B)

## 5.5   Low power Shutdown Mode

To save power, the LP38692 has an Enable pin (EN) which allows an external control signal to turn the regulator output On and Off. The Enable On/Off threshold has no hysteresis. The voltage signal must rise and fall cleanly, and promptly, through the ON and OFF voltage thresholds.

At 5 $V_{IN}$ the EN pin voltage must be higher than 3V to ensure that the device is fully enabled under all operating conditions. The EN pin voltage must be lower than 400 mV to ensure that the device is fully disabled.

The Enable pin has no internal pull-up or pull-down to establish a default condition and, as a result, this pin must be terminated either actively or passively. If the Enable pin is driven from a source that actively pulls high and low, the drive voltage should not be allowed to go below ground potential or higher than $V_{IN}$. If the application does not require the Enable function, the pin should be connected directly to the IN pin.

# 6   Test Setup

## 6.1   Getting Started Hardware

The power solutions mentioned in this design was tested as a separate power module. The output voltage were tested and verified to meet the power specs of the CC3200 SimpleLink™.

As a functionality test the TIDA-00534 board can be tested by powering the CC3200 Launchpad, first remove the USB connector and then connect J2 connector on the TIDA-00534 board to Pin J20 in the CC3200 Launchpad.
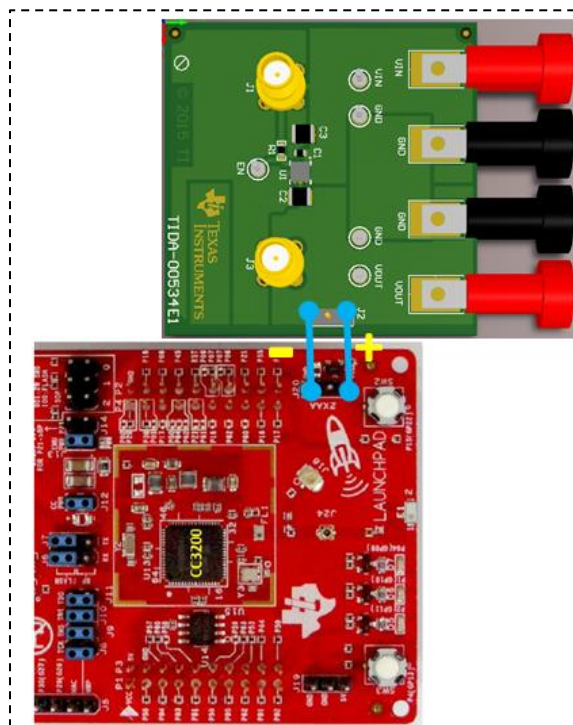


**Figure 6 TIDA-00534 connection to CC3200 Launchpad**

## 6.2   Getting Started Firmware

The functionality of the power solution mentioned in this document was verified by powering the CC3200 Launchpad and following the steps to launch the project 1. For firmware and steps to launch the project 1 of the Launchpad please refer to CC3200 User's guide (swru376b).

For CC3200 hardware connections please refer to CC3200 SimpleLink™ Wi-Fi® hardware user's guide (swru372b).

## 6.3   Test equipment

The following table shows the test equipment used in the upcoming sections.

**Table 2 Test Equipment**

| TEST EQUIPMENT | PART NUMBER |
|---|---|
| Oscilloscope | Agilent MSO7034B |
| Linear voltage supply | Agilent E3631A |
| Function generator | Agilent 33220A |

# 7 Test Data

## 7.1 Power Supply Ripple Rejection

The output voltage ripple rejection ratio was calculated by comparing the regulated output voltage ripple to the input voltage ripple of 1V over a frequency range of 10Hz to 1MHz.

**Table 3 Test Parameters**

| PARAMETER | VALUE |
| --- | --- |
| DC Input Voltage | 5 V |
| AC Input Voltage | 1 V |
| Sweep frequency | 10Hz to 1MHz |
| Output Voltage | 3.3 V |
| $C_{OUT}$ | 100 µF |
| $C_{IN}$ | 10 µF |
| Load current | Variable |
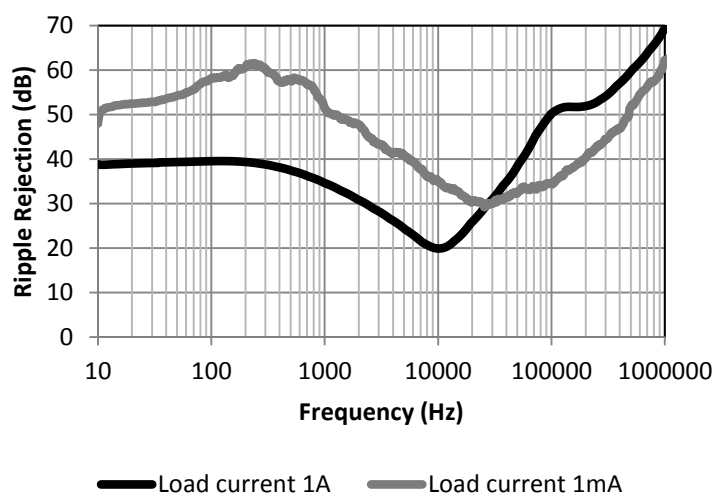


**Figure 7 Power Supply Ripple Rejection**

## 7.2 Quiescent current

The quiescent or ground current was obtained by measuring the current at the ground pin
The typical quiescent current of the LP38692 is 50µA at room temperature with a load current range of 1µA to 1A.

## 7.3 Noise density test

Output noise voltage is the root mean square (RMS) output noise voltage over a given range of frequencies (10 Hz to 100 kHz) under the conditions of a constant output current and a ripple-free input voltage.

The graph below shows the output noise generated, which is ultra-low comparing it with other LDOs.
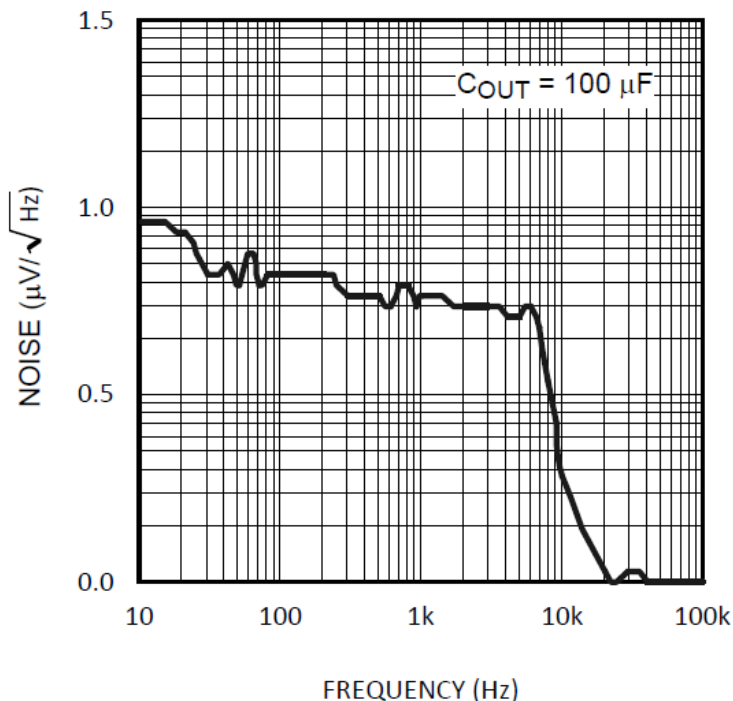


**Figure 8 Noise Density Over Frequency**

## 7.4 Power-up time

When the CC3200 is being power-up from zero  time requires that the power supply is settle before the reset pin is pulled high to initiate the hardware and firmware power-up sequencing.

The graph below shows that the LP38692 has a quick power up time. It takes about 120 µs  to reach 95% of the maximum regulated output voltage
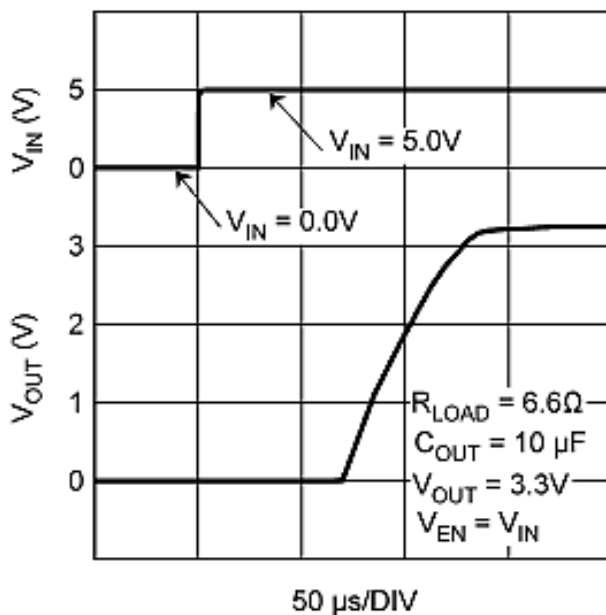


**Figure 9 $V_{OUT}$ VS $V_{IN}$ (Power-UP)**

## 7.5 Output voltage load regulation test

Output voltage load transient regulation is defined as the change in output voltage from nominal value as the load current increases

To simulate the CC3200 current demands an adjustable load was used at the output of the LP38692 with a digital switch to regulate the time the current takes to reach 500mA, the current step was set to 5 µs rising time. A current probe was used to sense the magnetic field around the current carrying conductor to estimate the current
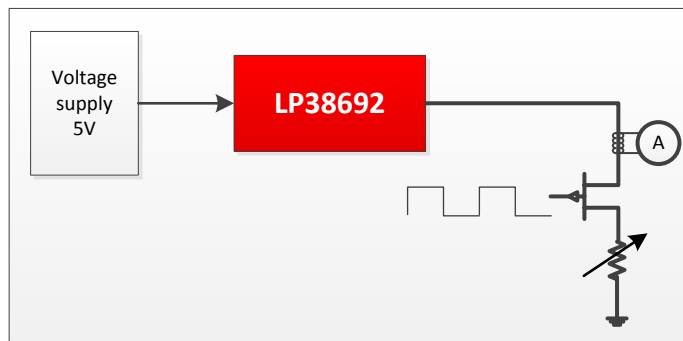


**Figure 10 Load transient test setup**

**Table 4 Test Parameters**

| PARAMETER | VALUE |
|-----------|-------|
| Input Voltage | 5 V |
| Output Voltage | 3.3 V |
| $C_{OUT}$ | 100 µF |
| $C_{IN}$ | 10 µF |
| Load current | Variable |

Figure 11 shows the output voltage transients when the load increased from 1mA to 500mA in 5µs, the output voltage had a transitory drop of 155mV then after 80µs the output voltage becomes stable at 3.27V
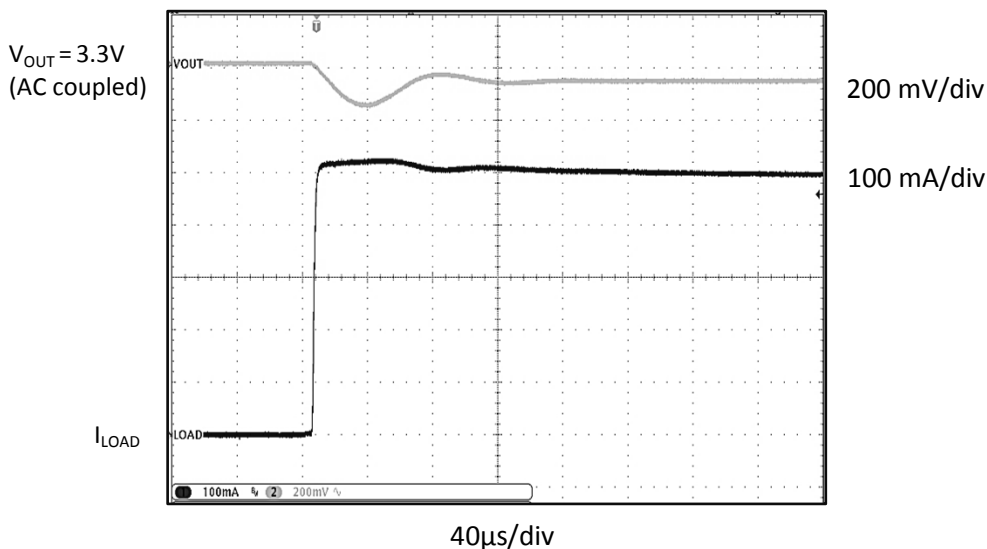


**Figure 11 Load transient from 1mA to 500mA**

Figure 12 shows the output voltage transients when the load increased from 1mA to 100mA in 5µs, the output voltage had transitory change of 20mV and reached steady state after 40µs
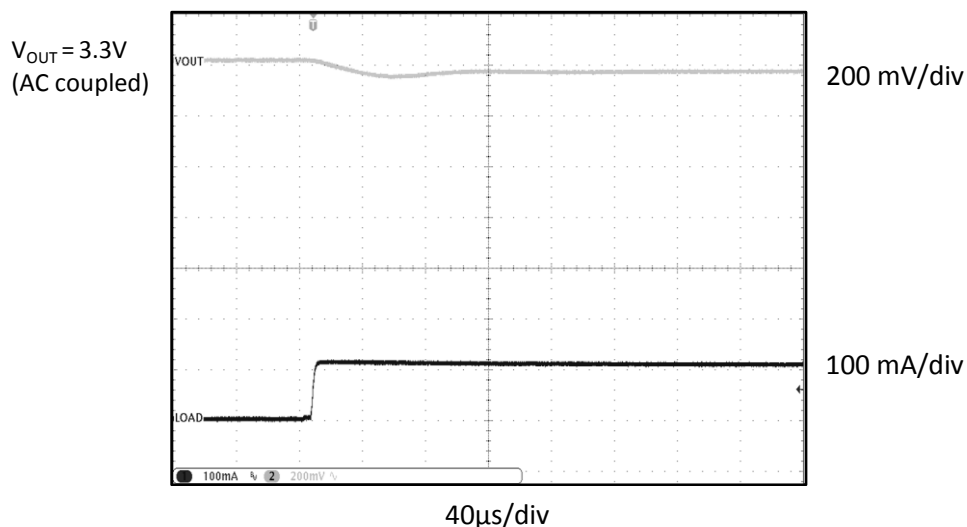


**Figure 12 Load transient from 1mA to 100mA**

### 7.5.1  Load regulation vs temperature

From the graph below we can conclude that at room temperature (25$^O$C) over the full range of operating voltages the LP38692 typically has a change of -1.8% over 1A.

As an example if the device is operating at room temperature with an output voltage of 3.3V and experience $I_{LOAD}$ delta of 500mA the output voltage could drop -0.015% 3.3V.
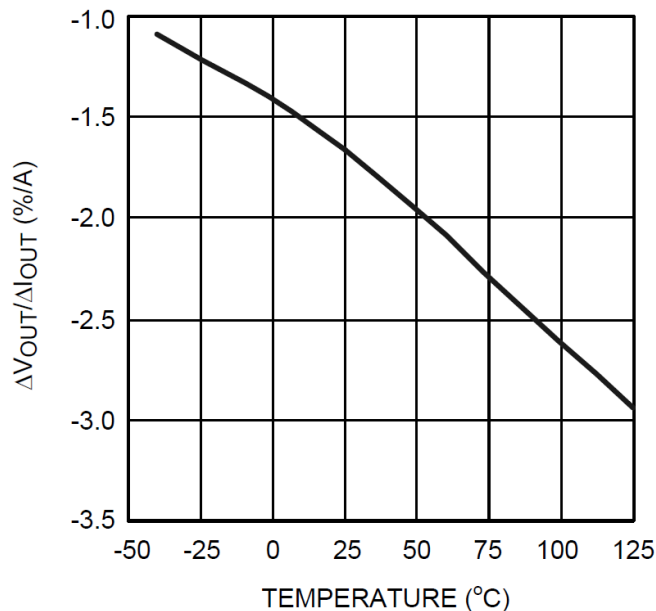


**Figure 13 Load Transient Vs Temperature**

## 7.6 Output voltage line regulation test

Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.

The line transient test measures the transient response of the voltage powering the CC3200 when the input voltage drastically drifts form nominal value.
Figure 14 shows the line transient test setup.
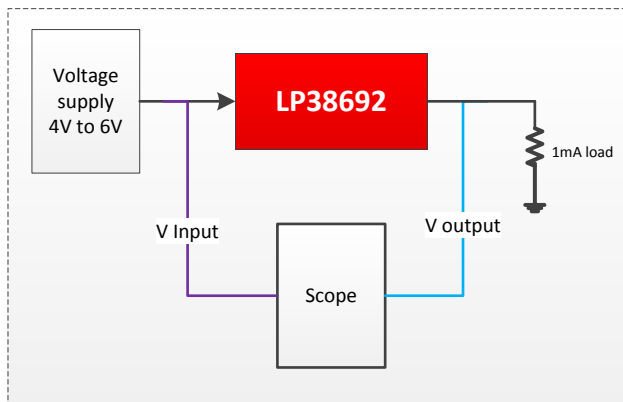


**Figure 14 Line Transient Test Setup**

| PARAMETER | VALUE |
|---|---|
| Input Voltage | Variable 4V to 6V |
| Output Voltage | 3.3V |
| $C_{IN}=C_{OUT}$ | 100µF |
| Load current | 1mA |

**Figure 15 Line Transient Test Parameters**

Figure 16 shows how the regulated 3.3V output (green trace) stays steady under abrupt changes in the input voltage, the steps of the input voltage (Blue trace) are one voltage increment from 4V to 6V and then in decrement steps of the same sizes.



100 ms/Div
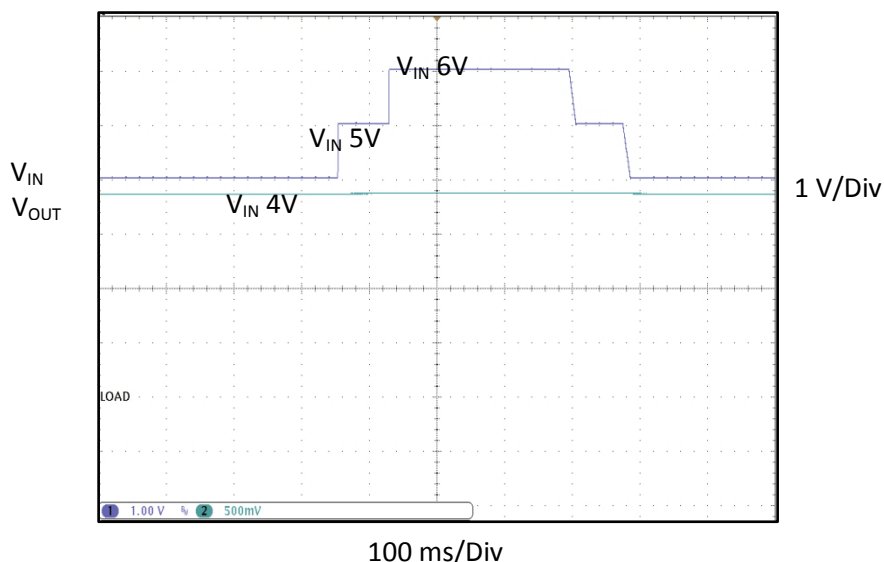
**Figure 16 Line Transient from 4V to 6V**

### 7.6.1    Line regulation vs temperature

From the graph below we can conclude that at room temperature ($25C^O$) over the full range of operating voltages the LP38692 typically has a change of 0.03% over 1V.

As an example if the device is operating at room temperature with an output voltage of 3.3V and experience a $V_{IN}$ delta of 500mV the output voltage could change -0.015% of 3.3V.
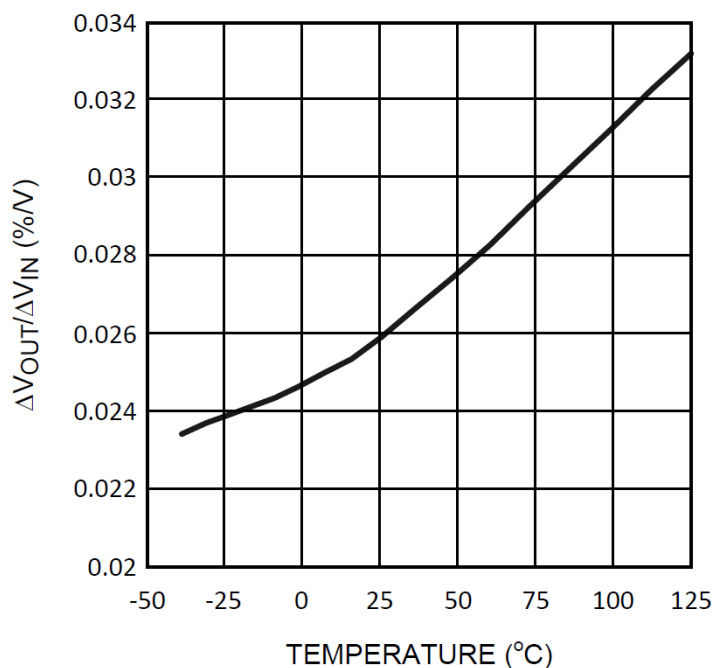


**Figure 17 Line regulation vs temperature**

## 7.7   CC3200 TX Packet current

To measure the active power during transmit follow the folowing steps.

1. Remove the 3V3 jumper (J12).
2. Attach a jumper wire between J12 so that it can be used with a current probe. (For the current probe, coil the wire around the sensor multiple times for good sensitivity, and degauss the probe before taking a measurement).
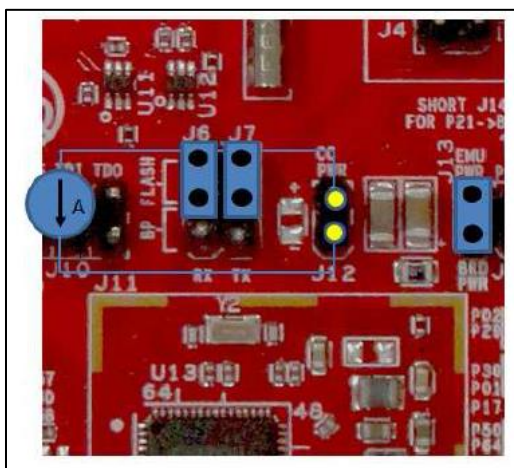


**Figure 18 Jumpers and Measurement Connection**

The following figure shows the TX current waveform. In this case the pick maximum current is about 307mA.
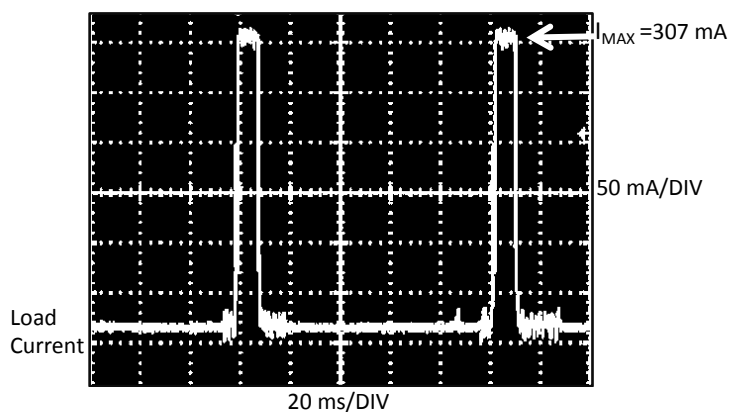


**Figure 19 CC3200 Active Current Waveform Capture**

For more detail information about additional techniques to measure the transmit and sleep mode current of the CC3200 please refer to CC3200 Wiki Page

# 8    Design Files and Layout Guidelines

## 8.1    Layout guidelines

Best performance is achieved by placing $C_{IN}$ and $C_{OUT}$ on the same side of the PCB and as close as is practical to the package. The ground connections for $C_{IN}$ and $C_{OUT}$ should be back to LP38692 GND pin using as wide, and as short, a copper trace as is practical.

Connections using long trace lengths, narrow trace widths, and/or connections through vias should be avoided. These add parasitic inductances and resistance that results in inferior performance especially during transient conditions.

A Ground Plane, either on the opposite side of a two-layer PCB, or embedded in a multi-layer PCB, is strongly recommended. This Ground Plane serves two purposes:

1. Provides a circuit reference plane to assure accuracy, and
2. Provides a thermal plane to remove heat from the LP38690 or LP38692 WSON package through thermal vias under the package DAP.

The input current is split between two IN pins, 1 and 6. The two IN pins must be connected together to ensure that the device can meet all specifications at the rated current.

The thermal dissipation of the WSON package is directly related to the printed circuit board construction and the amount of additional copper area connected to the DAP.

The DAP (exposed pad) on the bottom of the WSON package is connected to the die substrate with a conductive die attach adhesive. The DAP has no direct electrical (wire) connection to any of the pins. There is a parasitic PN junction between the die substrate and the device ground. As such, it is strongly recommend that the DAP be connected directly to the ground at device lead 2 (such as GND). Alternately, but not recommended, the DAP may be left floating (that is, no electrical connection). The DAP must not be connected to any potential other than ground.

Solid polygon for V$_{IN}$ and V$_{OUT}$ to avoid IV drop

Large ground plane on the top and bottom layers for thermal dissipation, and 20mil via stitching for low thermal resistance

C$_{IN}$ and C$_{OUT}$ close to input/output pin with a single point to ground
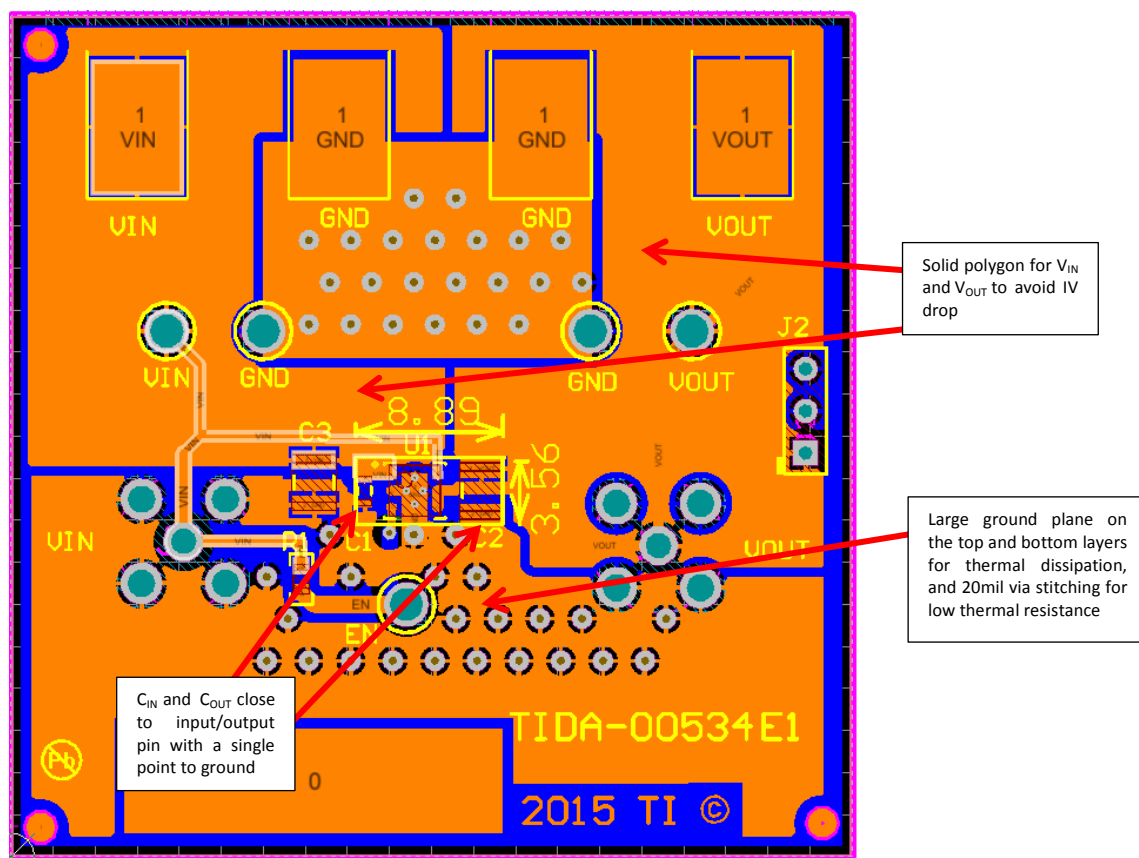
**Figure 20 Layout Guidelines**

## 8.2 Schematics

To download the Schematics, see the design files at http://www.ti.com/tool/TIDA-00534

## 8.3 Bill of Materials

To download the Bill of Materials, see the design files at http://www.ti.com/tool/TIDA-00534

## 8.4 Gerber files

To download the Gerber files, see the design files at http://www.ti.com/tool/TIDA-00534

# 9 References

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10. Resistance for Exposed Packages, SNVA183B, 2013

# 10 Glossary

TI Glossary: SLYZ022 This glossary lists and explains terms, acronyms, and definitions.

# 11 About the Author

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# IMPORTANT NOTICE FOR TI REFERENCE DESIGNS