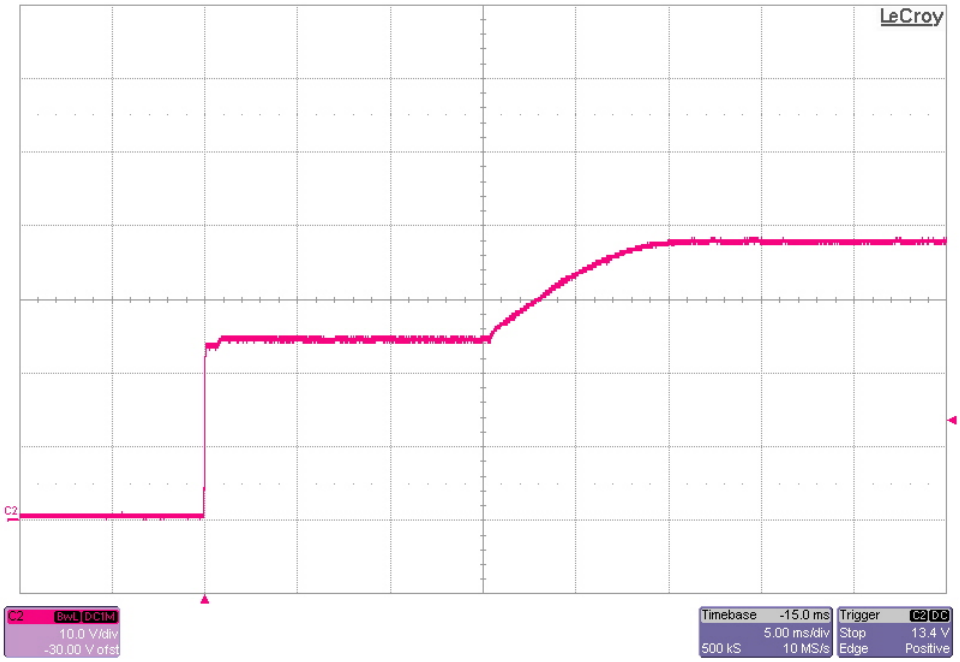
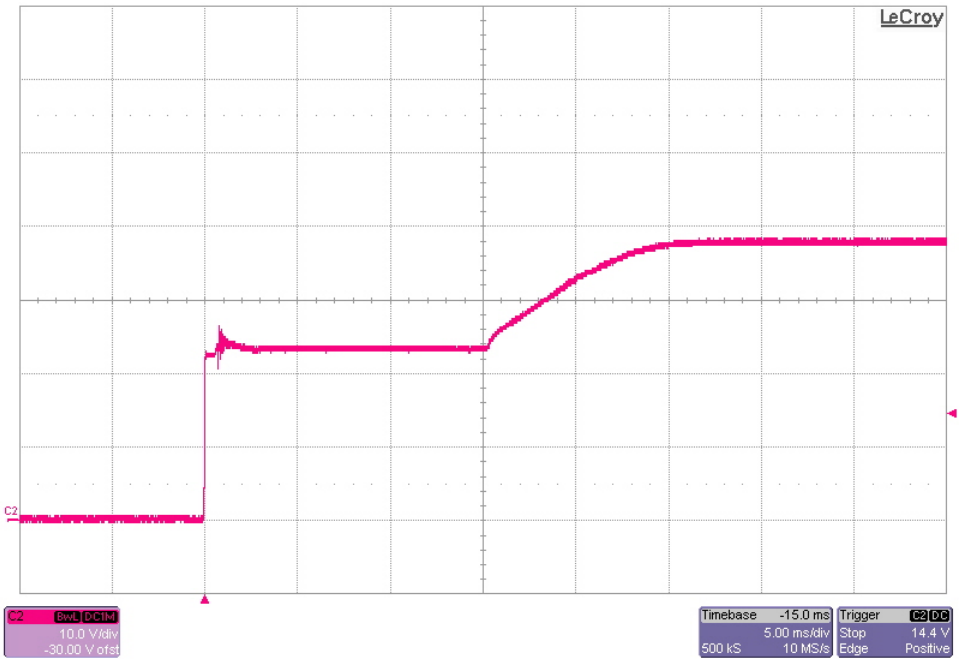
1 Startup

The photo below shows the output voltage startup waveform after the application of 24V in. The 38V output was loaded to 0A. (10V/DIV, 5mS/DIV)

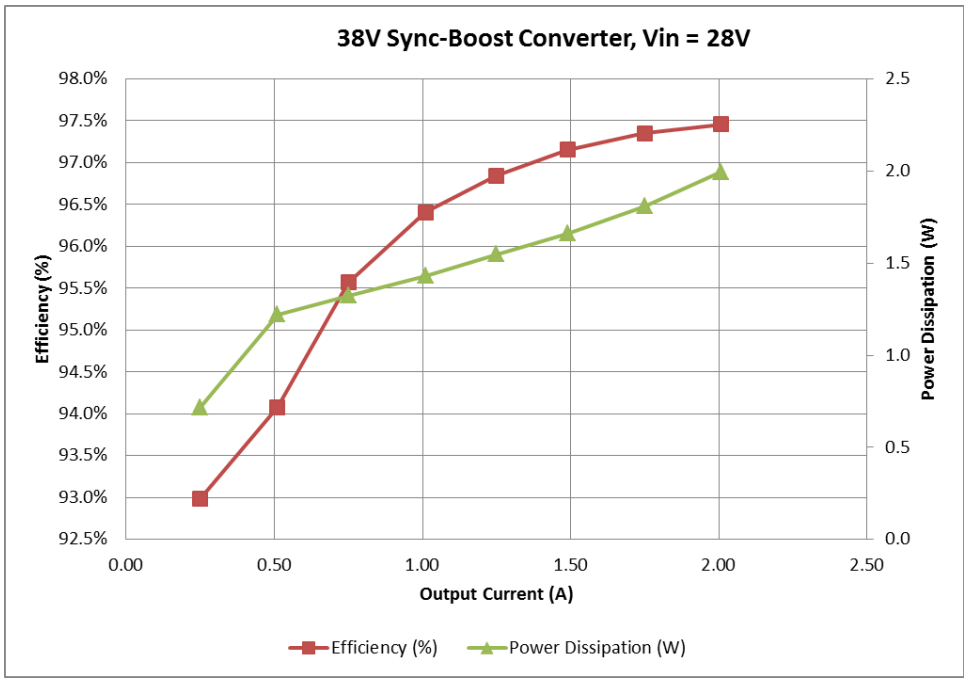


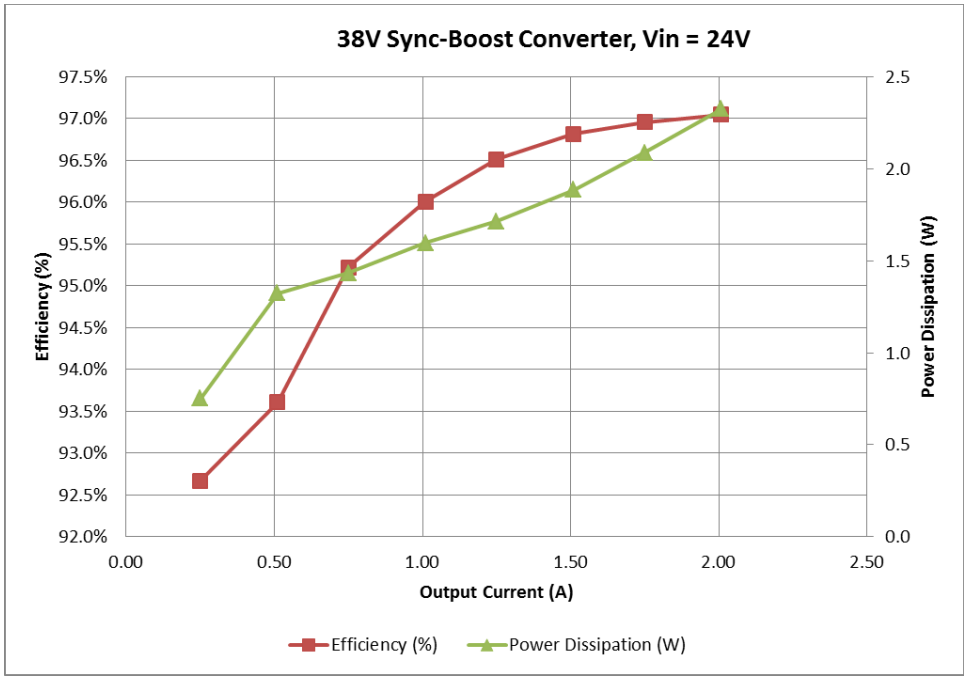
The photo below shows the output voltage startup waveform after the application of 24V in. The 38V output was loaded to 2A. (2V/DIV, 5mS/DIV)

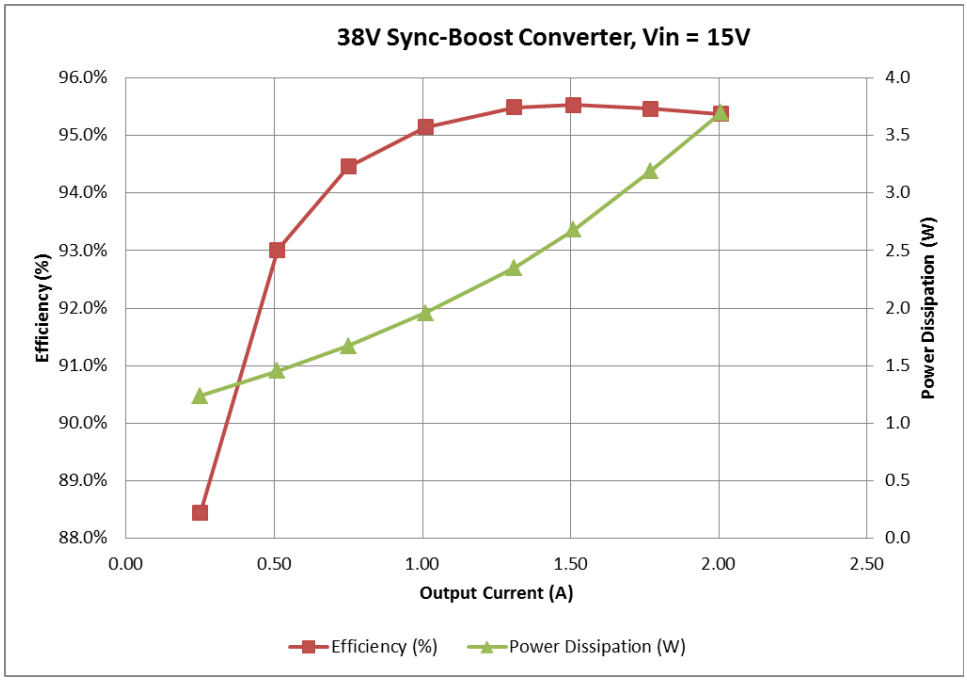


2 Efficiency

The 38V sync boost converter efficiency is shown below.

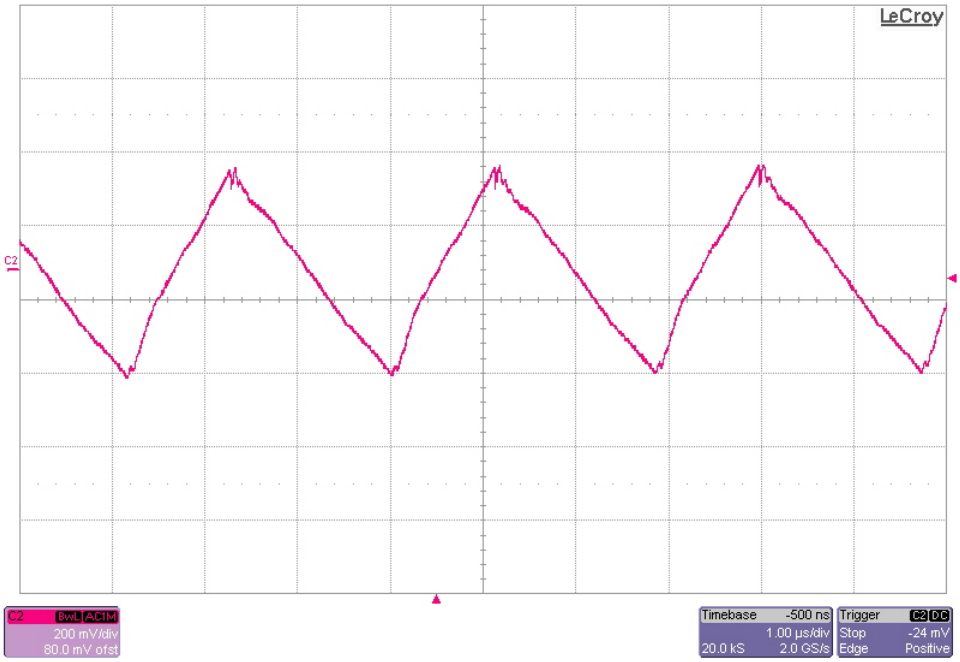




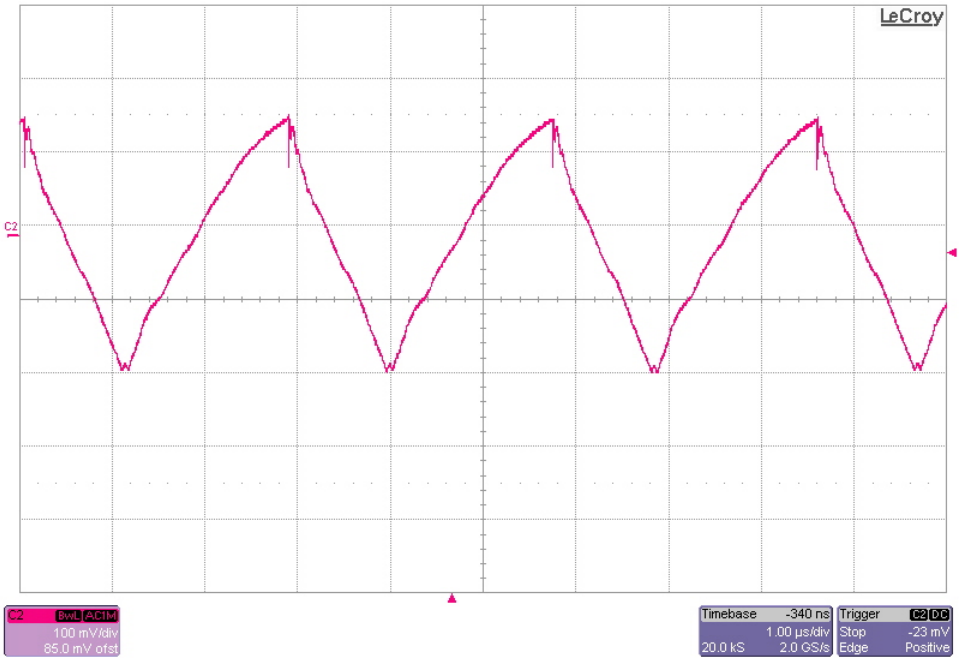

38V Sync-Boost Converter, Vin = 15V
96.0%
95.0%
94.0%
93.0%
92.0%
91.0%
90.0%
89.0%
88.0%
Efficiency (%)
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
Power Dissipation (W)
0.00
0.50
1.00
1.50
2.00
2.50
Output Current (A)
Efficiency (%)
Power Dissipation (W)

3 Output Ripple Voltage

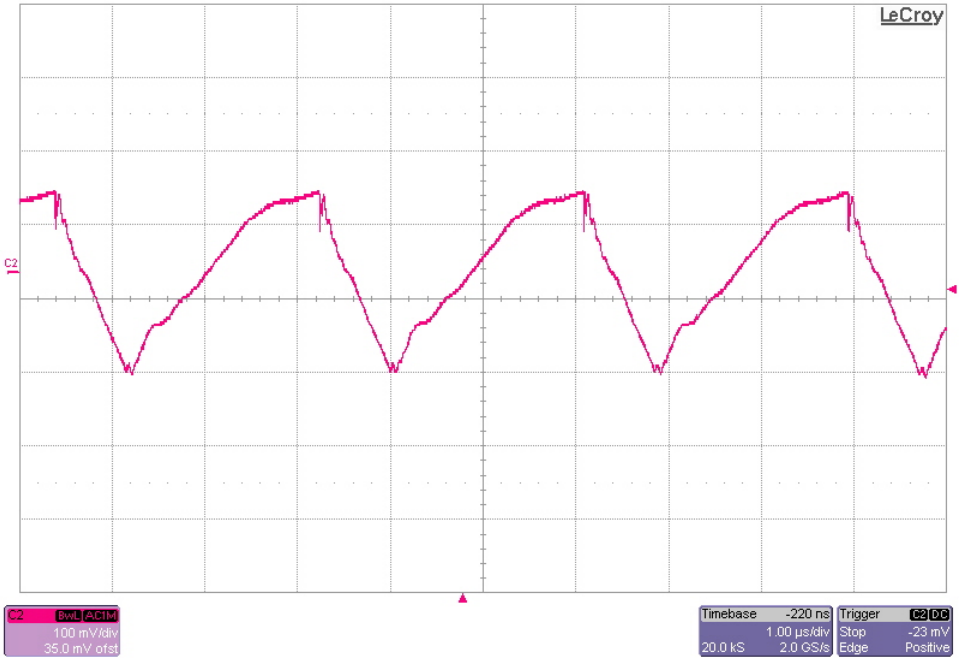
The 38V output ripple voltage is shown in the figure below. The image was taken with the output loaded to 2A. The input voltage is set to 15V. (200mV/DIV, 1uS/DIV)



The 38V output ripple voltage is shown in the figure below. The image was taken with the output loaded to 2A. The input voltage is set to 24V. (100mV/DIV, 1uS/DIV)

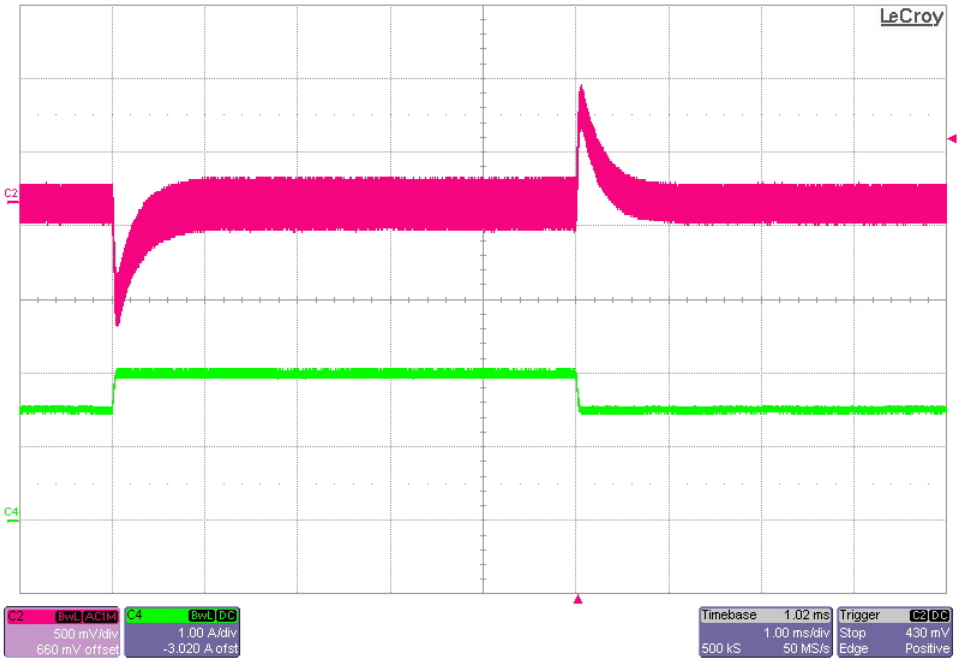


The 38V output ripple voltage is shown in the figure below. The image was taken with the output loaded to 2A. The input voltage is set to 28V. (100mV/DIV, 1uS/DIV)

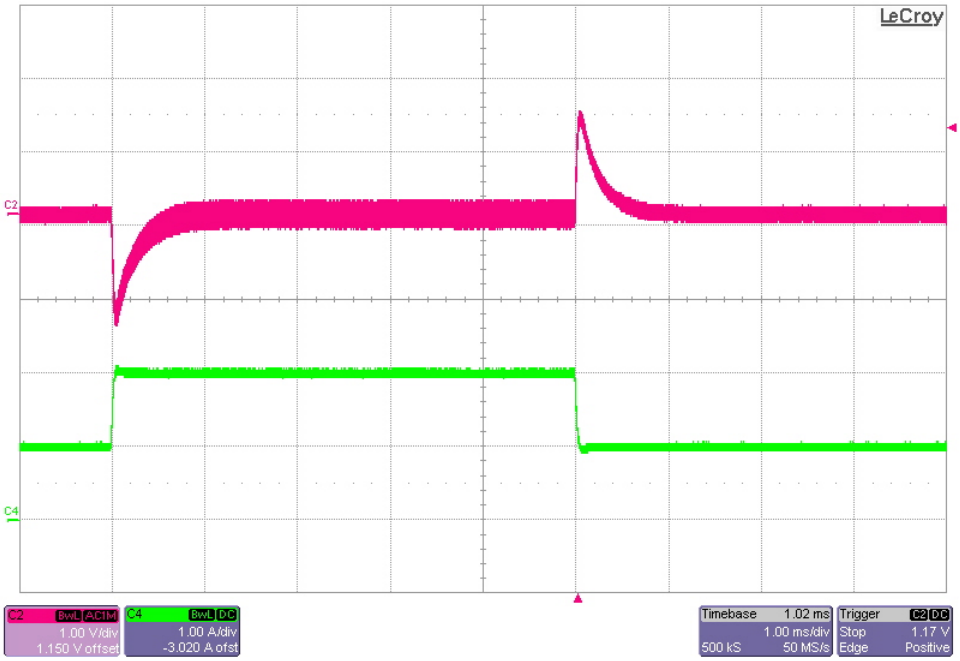


4 Load Transients

The photo below shows the output voltage (ac coupled) when the load current is stepped between 1.5A and 2A. Vin = 24V. (500mV/DIV, 1A/DIV, 1mS/DIV)

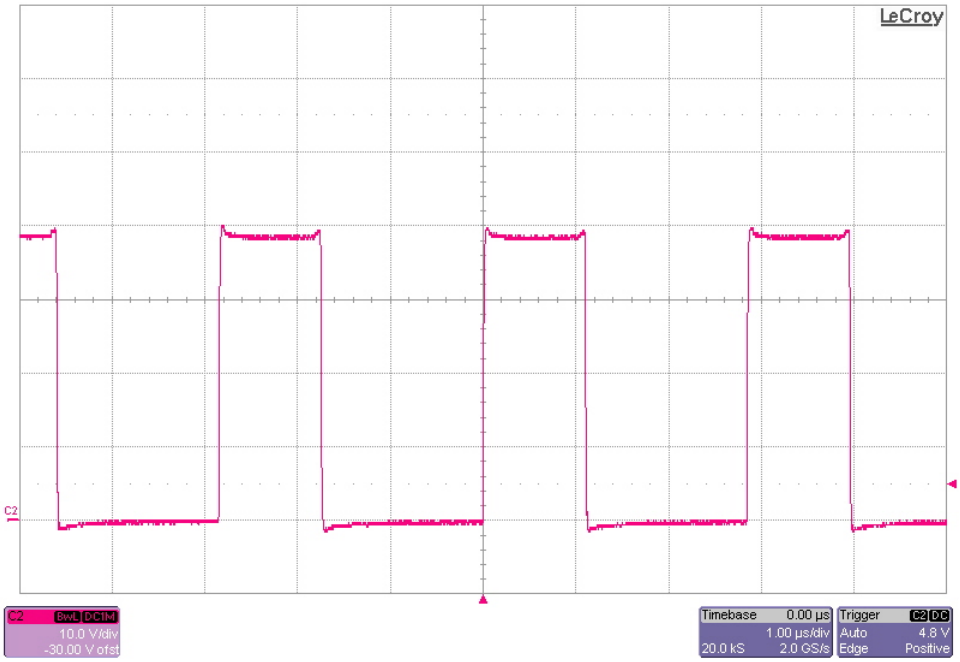


The photo below shows the output voltage (ac coupled) when the load current is stepped between 1A and 2A. Vin = 24V. (1V/DIV, 1A/DIV, 1mS/DIV)

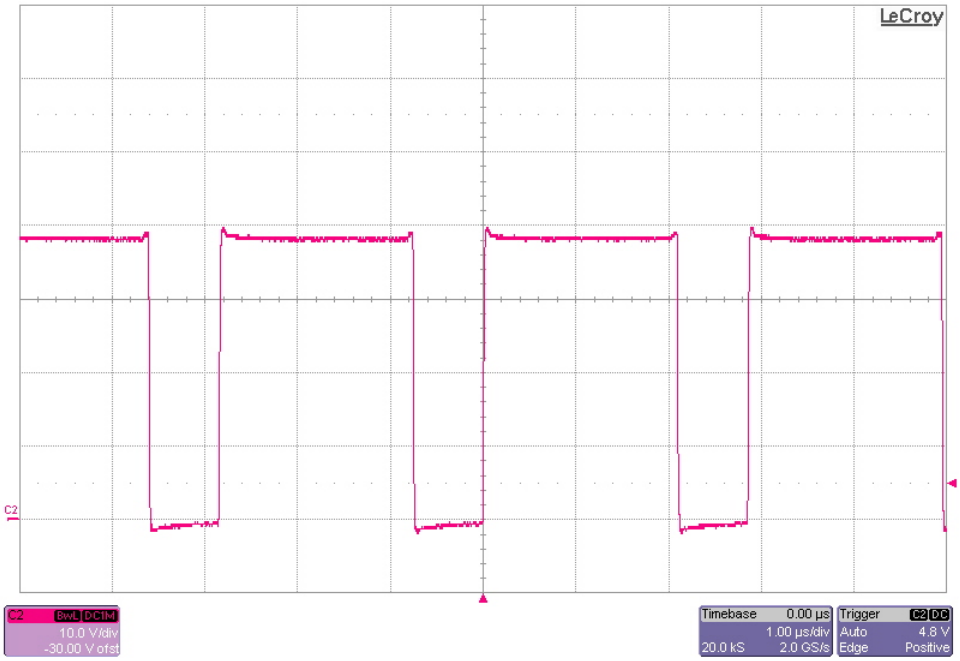


5 Switch Node Waveforms

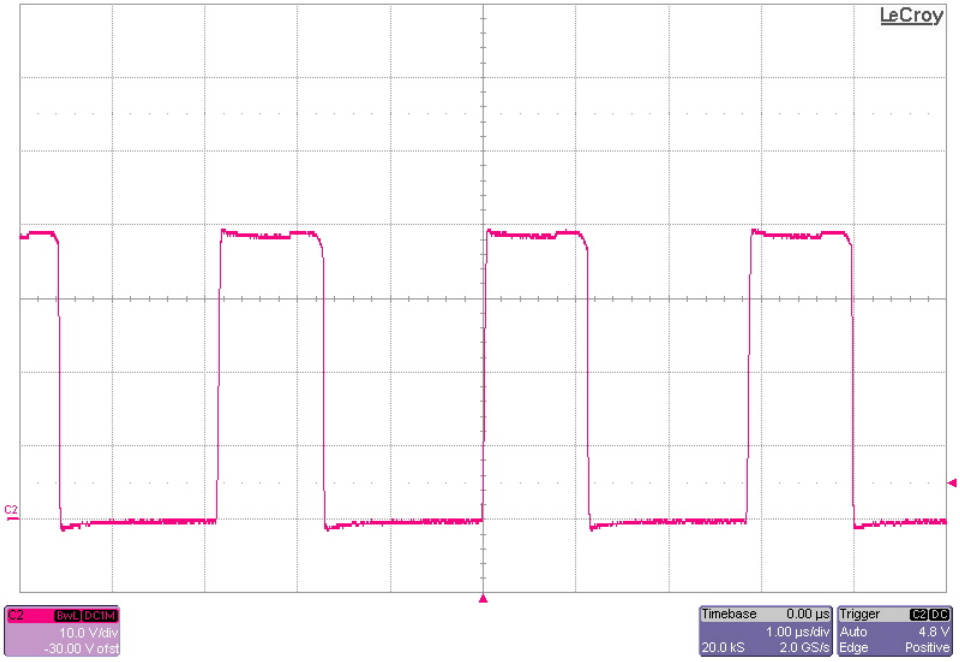
The photo below shows the FET switching voltage. The input voltage is 15V and the output is loaded to 2A. (10V/DIV, 1uS/DIV)



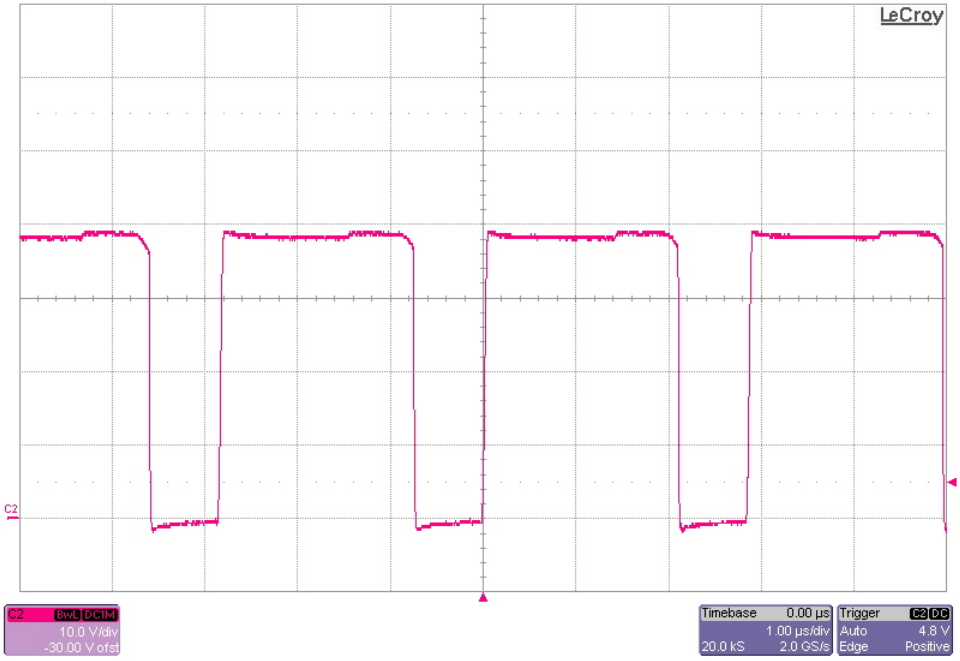
The photo below shows the FET switching voltage. The input voltage is 28V and the output is loaded to 2A. (10V/DIV, 1uS/DIV)



The photo below shows the FET switching voltage. The input voltage is 15V and the output is loaded to 0.17A. The converter is just starting DCM operation. (10V/DIV, 1uS/DIV)



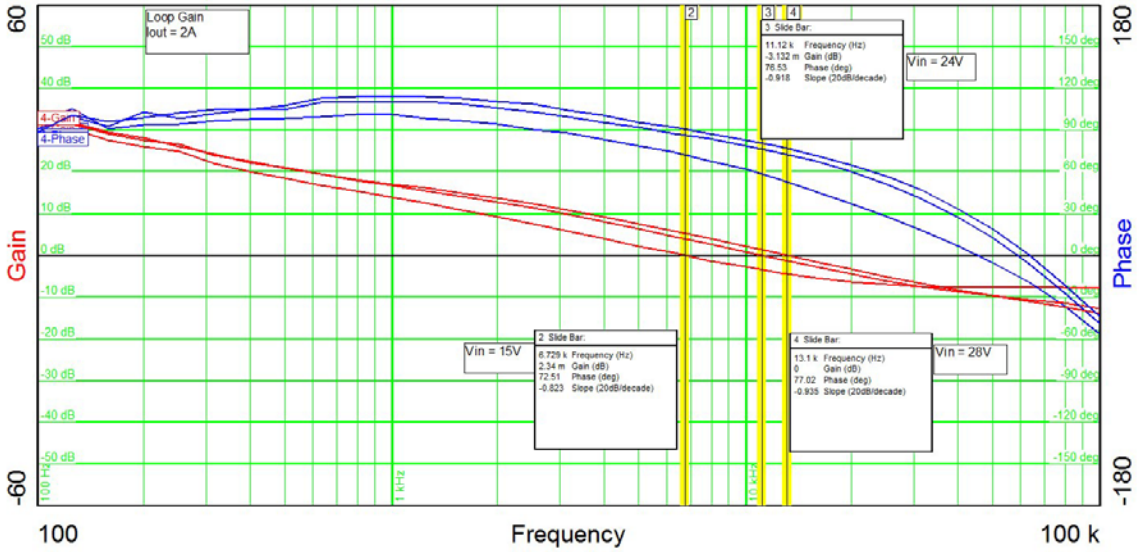
The photo below shows the FET switching voltage. The input voltage is 28V and the output is loaded to 0.29A. The converter is just starting DCM operation. (10V/DIV, 1uS/DIV)



6 Control Loop Gain / Stability

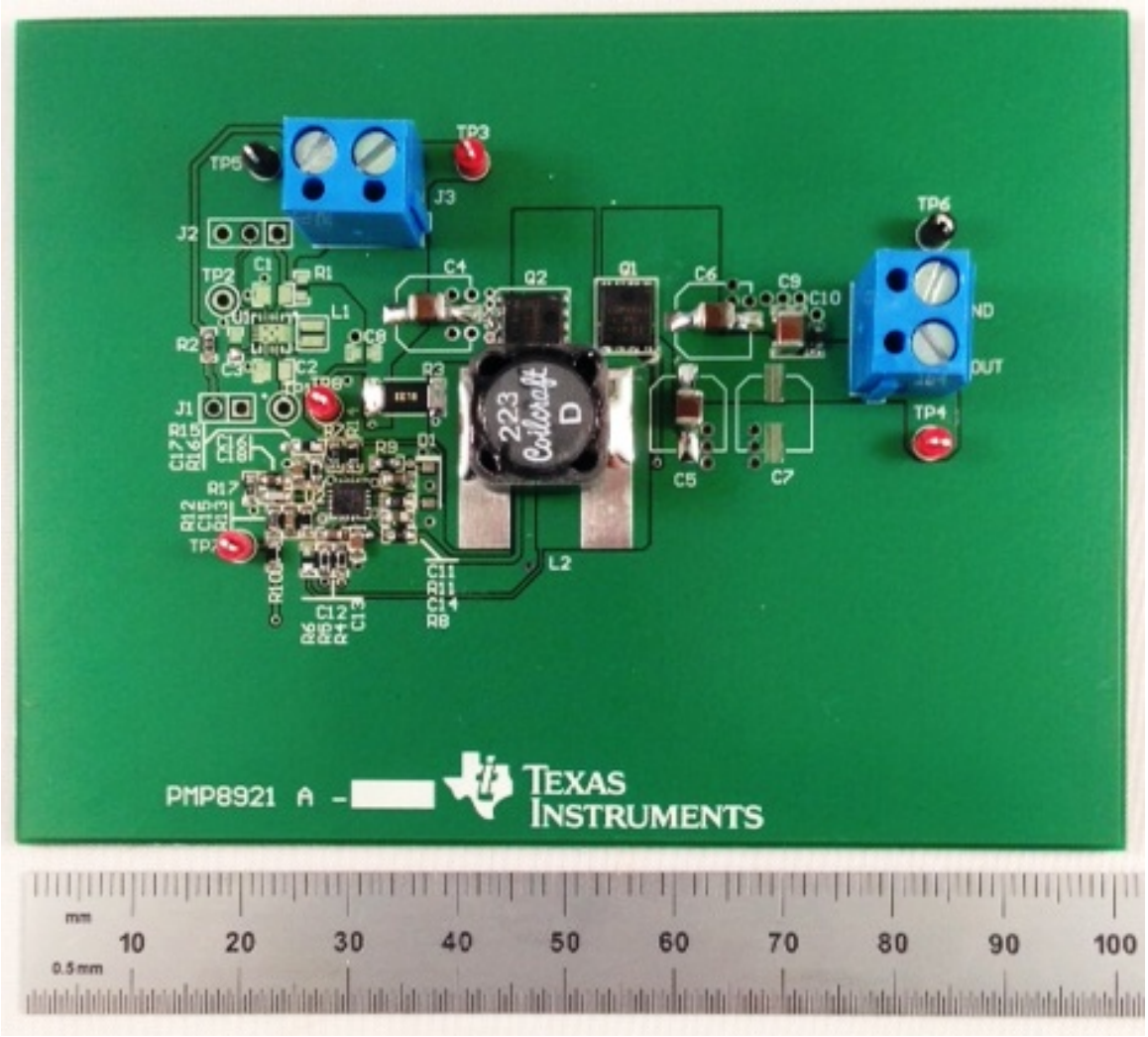
The plot below shows the loop gain and phase margin at 15V, 24V and 28V with the output loaded to 2A.

Vin = 15V	Band Width = 6.73KHz,	Phase Margin = 73 degrees
Vin = 24V	Band Width = 11.1KHz,	Phase Margin = 77 degrees
Vin = 28V	Band Width = 13.1KHz,	Phase Margin = 77 degrees



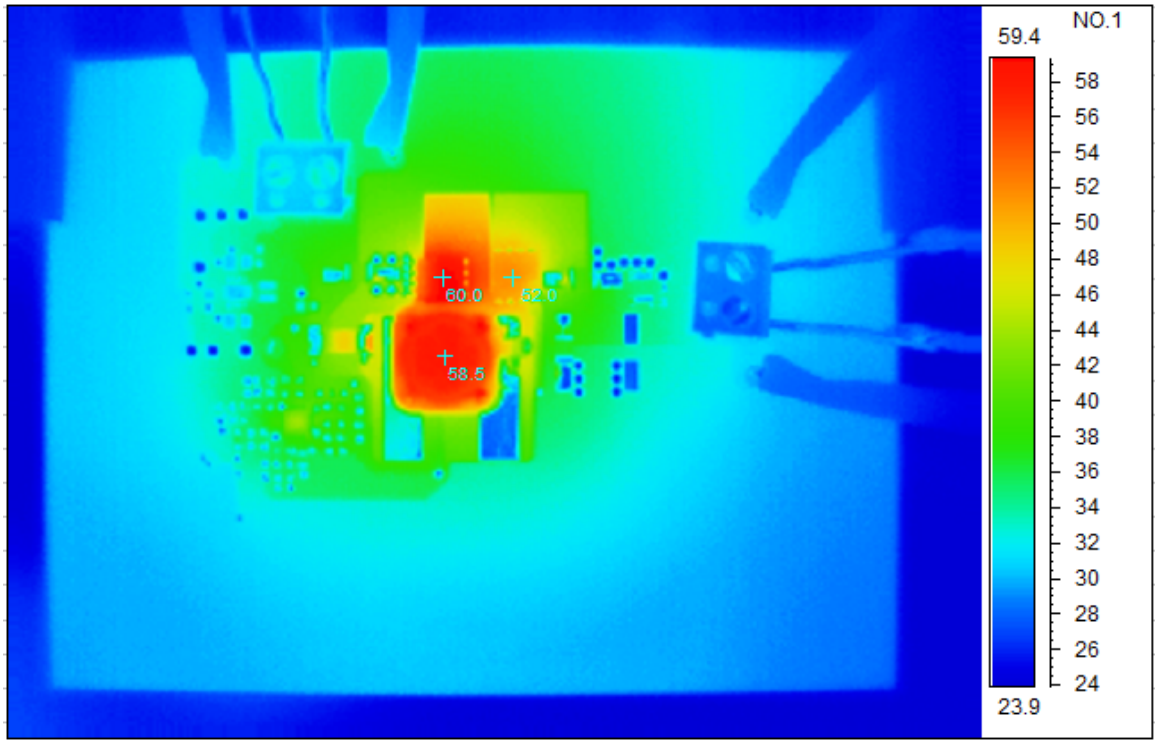
7 Photo

The photo below shows the PMP10324 REVB assy built on the PMP8921 REVA PWB.



8 Thermal Image

A thermal image is shown below operating at 24V input and 2A output (room temp and no airflow).



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