TI Designs

1-W Isolated Power Supply With Planar Transformer Reference Design

TI Designs

The TIDA-00688 is an ultra-thin profile, 1-W output isolated power supply. The design has a height of only 2.2 mm on each side of the PCB and fits even in very small, space-constrained applications. The thin profile is achieved by using a planar transformer that is integrated into the PCB. The TIDA-00688 has three isolated outputs (15 V, –15 V, 5 V) and targets all kind of modules in the PLC, DCS, and PAC area that need a very thin and small, yet isolated, power supply.

Design Resources

TIDA-00688	Design Folder
TIDA-00237	Tools Folder
TIDA-00129	Tools Folder
LM5017	Product Folder
TPS62175	Product Folder
TPS7A4901	Product Folder
TPS7A3001	Product Folder

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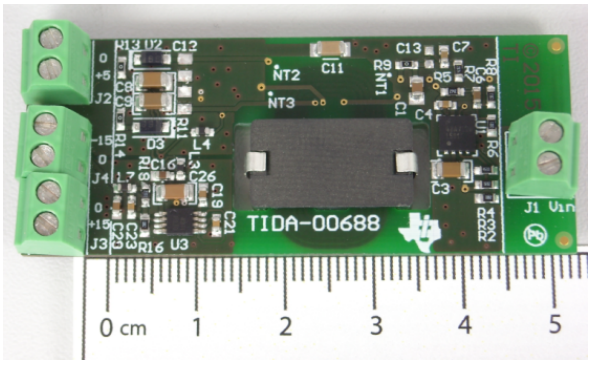
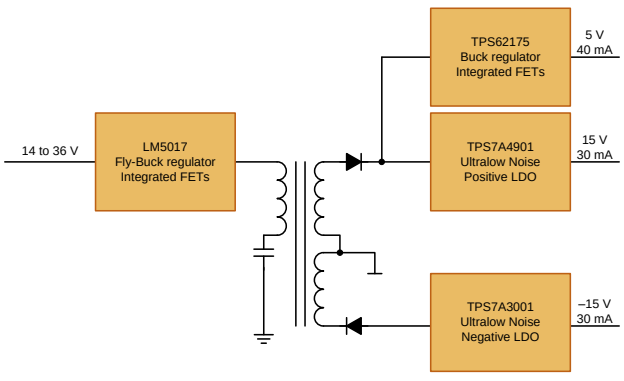
Design Features

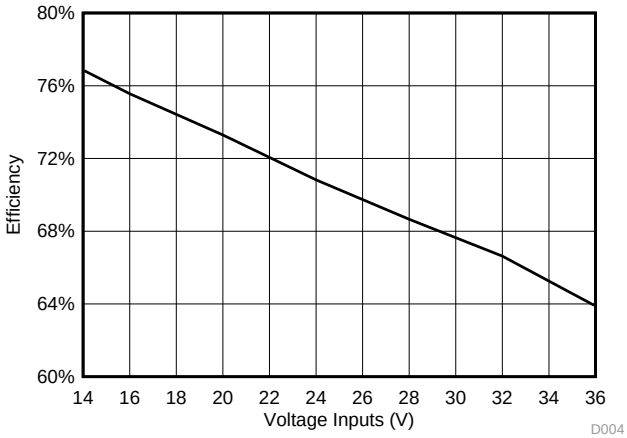
- Integrated Planar Transformer
- Wide Input Voltage Range: 14 to 36 V (24 V_{NOM})
- Three Isolated Outputs:
  - 15 V_{ISO}, 30 mA Ultralow Noise
  - –15 V_{ISO} 30 mA Ultralow-Noise
  - 5 V_{ISO}, 40 mA
- Ultrathin Profile Of Only 2.2 mm

Featured Applications

- PLC, DCS, and PAC:
  - Analog Input Module
  - Analog Output Module
  - Transducer Module
  - Special Function Module







1 Key System Specifications

Table 1. Key System Specifications

SYMBOL	PARAMETER	CONDITIONS	SPECIFICATION			UNIT
			MIN	TYP	MAX	
V_{IN}	Input voltage	Normal operation	14	24	36	V
I_Q	Quiescent current	No output load	—	9	15	mA
V_{J2}	Output voltage connector J2	Normal operation	4.9	5	5.1	V
V_{J3}	Output voltage connector J3	Normal operation	14.8	15	15.2	V
V_{J4}	Output voltage connector J4	Normal operation	–14.8	–15	–15.2	V
I_{J2}	Output current	$V_{IN} > V_{IN(min)}$	0	—	40	mA
I_{J3}	Output current	$V_{IN} > V_{IN(min)}$	0	—	30	mA
I_{J4}	Output current	$V_{IN} > V_{IN(min)}$	0	—	30	mA
P_{OUT}	Output power		0	—	1.1	W
h	Efficiency	V_{IN} = 14 V, $I_{OUT,GES}$ = 106 mA	—	76.9	—	%
		V_{IN} = 24 V, $I_{OUT,GES}$ = 10 mA	—	73.3	—	%
		V_{IN} = 36 V, $I_{OUT,GES}$ = 106 mA	—	52.6	—	%
H1	Component height above PCB		—	—	2.2	mm
H2	Component height below PCB		—	—	2.2	mm
A_A	Active area size		—	—	25.4 × 43.8	mm^2

2 System Description

A programmable logic controller (PLC) is a key component in factory automation. The PLC monitors input and output (I/O) modules in real-time and controls the process according to the requirements. Thanks to flexible I/O modules, PLCs can adapt to many different process requirements. The analog I/O modules, local or remote, acquire process data and set outputs to actuate the process. Figure 1 exhibits an analog input module with emphasize on the power block.

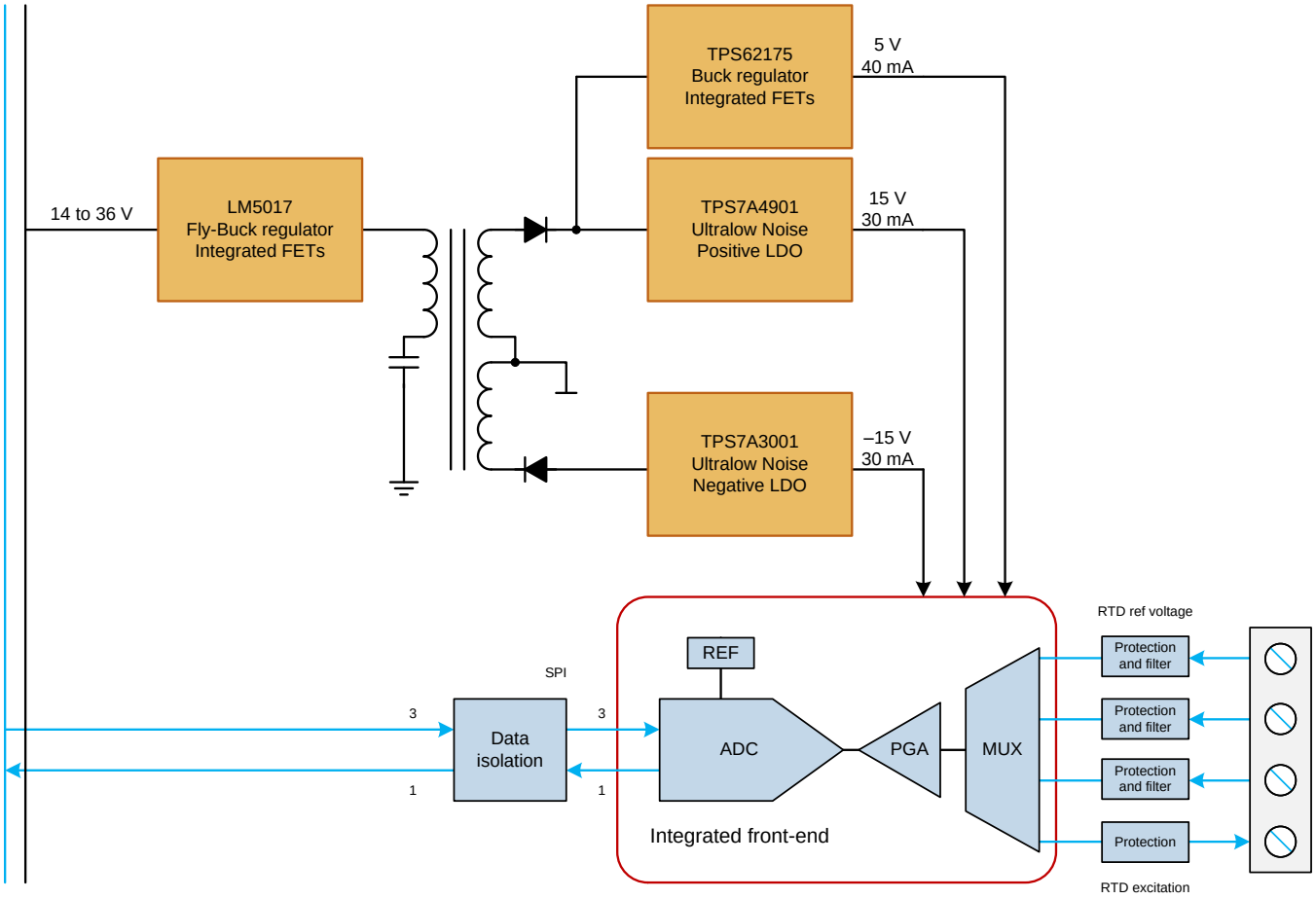


Figure 1. Block Diagram of Analog Input Module

Analog input modules represent about 10% of all PLC I/O modules, and analog output modules represent about 5%. Typical outputs are 4- to 20-mA current loop or ±10-V analog. The analog I/O modules use analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) to convert analog process signals to digital values or vice versa in the output module. A proper data conversion requires an ADC or DAC and potentially an amplifier stage to drive, level shift, filter or impedance match the data converter to the input or output signal.

To ensure the expected performance from the data converter and the amplifier stage, a dedicated low-noise isolated power supply solution is required. In addition to low-noise isolated power, the form factor of the solution plays an important role. Small form factors give users more flexibility and the chance to use their solution even in small, space-constrained areas.

The TIDA-00688 does not only satisfy the need for low-noise isolated power, but comes in a very thin form factor. This is achieved by using a planar transformer instead of a surface mount transformer for the power isolation. Figure 6 shows the block diagram of the design.

3 System Design Theory

For a 1-W isolated power supply with a wide input voltage range, no optocoupler feedback, and low number of external components, the Fly-Buck™ topology is superior to a flyback design. This topology also allows design flexibility for a primary non-isolated power supply. For a high-end post regulation, LDOs with high PSRR ensure a clean power supply for analog circuits. The 5-V rail is derived from the 18-V transformer output using a high efficiency buck regulator. The Fly-Buck is implemented using an LM5017. This part fulfils the Fly-Buck requirements while allowing a small circuit footprint at a low BOM cost. Figure 2 shows the architecture of the LM5017.

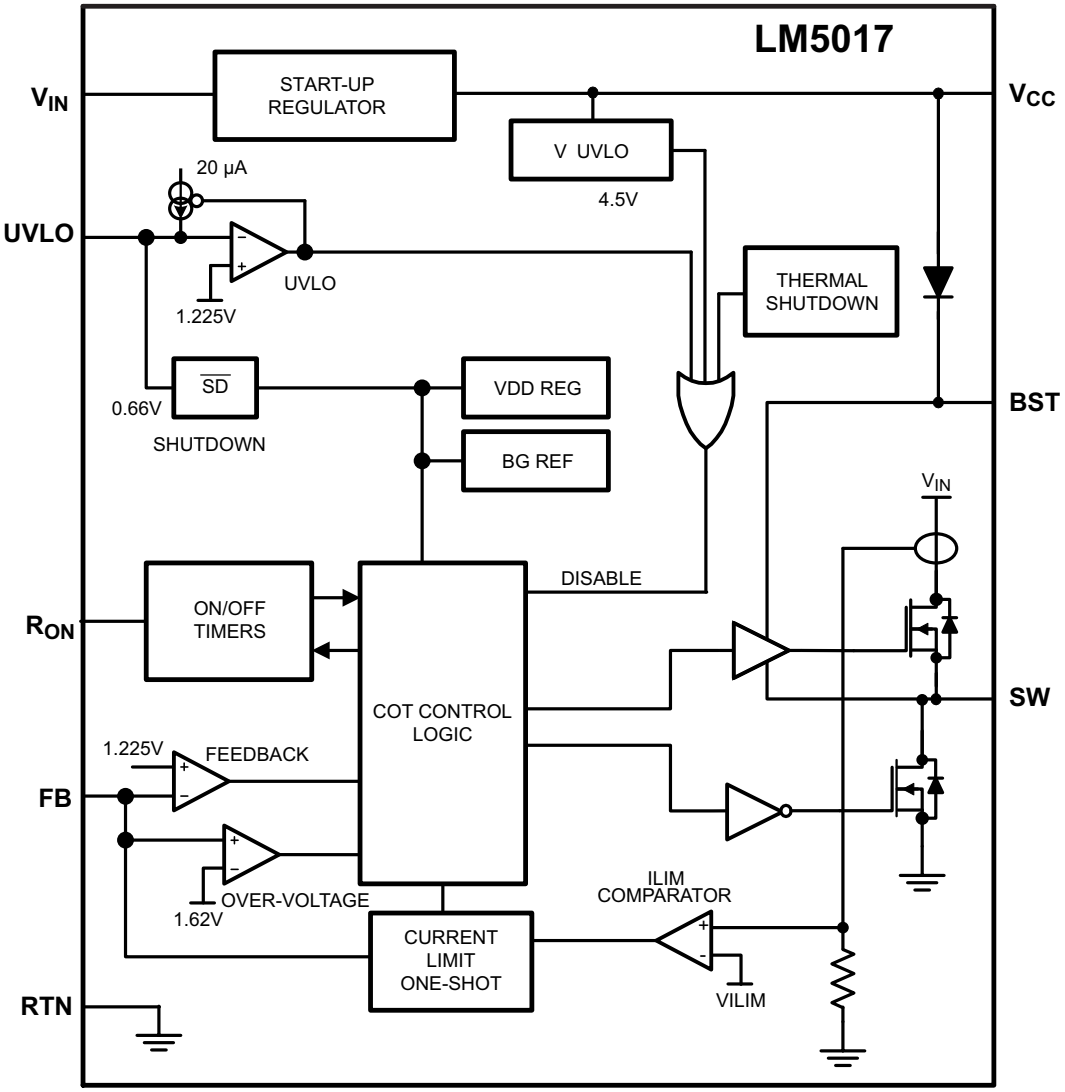


Figure 2. LM5017 Architecture

The TIDA-00688 is based on the TIDA-00237 but reduces height further down to 2.2 mm (1.6-mm PCB thickness) on each PCB side. This is achieved by replacing the surface mount transformer with a planar transformer. The magnetic core of a planar transformer consists out of two parts. First, an E-shaped ferrite (E-core) is put into three holes inside the PCB. Then, a planar ferrite is put from the other side onto the legs of the E-core and fixed to it. In a planar transformer, the windings are placed in the same layer and wired around the middle leg of the magnetic core like a spiral. To increase the inductance of those coils, it is possible to use several layers. However, to keep PCB manufacturing cost down, the TIDA-00688 only uses a four-layer design: one primary side layer, two secondary side layers, and one interconnection layer. The design process of the transformer is explained further in Section 3.2.

3.1 Primary-Side Output Voltage V_{C1}

The primary-side voltage V_{C1} depends on multiple factors. As a rule of thumb, the duty cycle should be below 50%. Otherwise, the transfer time for the energy required to maintain the minimum secondary voltage at maximum current is too short. Short energy transfer times lead to larger peak currents, inferior load regulation performance, and larger voltage drops across the rectifier diodes D2 and D3 on the secondary side as well as across the synchronous rectifier inside the LM5017.

The TIDA-00688 is rated for an input voltage range of 14 to 36 V. According to Equation 1, a maximum duty cycle D of 50% corresponds to a primary side voltage V_{C1} of 7 V.

$$D = \frac{V_{C1}}{V_{IN}}$$

$$\rightarrow V_{C1} = D \times V_{IN} = 0.5 \times 14\ V = 7\ V \quad (1)$$

For an output voltage of 18 V on the secondary side, a turn ratio of 1:2.6 is needed. However, a turn ratio of 1:2.6 leads to high peak currents in the MOSFETs of the LM5017. Instead, with a turn ratio of 1:2, it is possible to keep the peak currents below the specified limits of the LM5017. In conclusion, V_{C1} is regulated to 9 V, which results in a maximum duty cycle of 62%. At this duty cycle, the design is still working stable.

The LM5017 uses a constant on-time (COT) control scheme to control its switching behavior. The COT works as follows. The on time is controlled by an on timer. The off time is defined by the time the feedback voltage drops below the reference voltage. This means the off time is terminated when the lower end of the output ripple voltage matches the reference voltage of the LM5017.

Note that the voltage ripple at C1 is highest for lowest input voltages. This is because the duty cycle is also higher for lower input voltages, as shown in Equation 1. A longer duty cycle means that the high-side FET of the LM5017 is turned on longer, too. As a result, the voltage ripple at C1 is higher, too. However, the average voltage across C1 is lower for lower input voltages.

3.2 Transformer Design

For the transformer design, several things need to be considered: size and space constraints on the PCB, the operating frequency of the LM5017, the maximum allowable magnetic flux inside the magnetic core, the current ripple, DC losses of the PCB coils, and general DC losses occurring in every part.

Table 2 shows the calculation of the minimum primary side voltage of the transformer. Some margin is required for load regulation and general DC losses on top of the minimum required voltage of 8.7 V at C1. In conclusion, setting the primary side voltage to 9 V is sufficient and complies well with the consideration in Section 3.1.

Table 2. Primary-Side Voltage Calculation

PARAMETER	CONDITION	VALUE
VJ3/J4	Full load	15.000 V
LDO (U2, U3) drop-out voltage	30 mA, 125°C	0.180 V
Diode D2 and D3 drop-out voltage	260 mA (average forward current)	0.550 V
Transformer T1, secondary winding loss	1.46 Ω, 260 mA (average forward current)	0.380 V
Required transformer T1, secondary winding voltage		**16.110 V**
Required transformer T1, primary voltage	Winding ration 1:2	8.055 V
Transformer T1, primary winding loss	0.282 Ω, 500 mA (average forward current)	0.141 V
U1 synchronous switch loss	1 Ω, 500 mA (average forward current)	0.500 V
Required voltage at C1		**8.696 V**
$V_{IN,MIN}$ duty cycle	V_{IN} = 14 V	62.11%
$V_{IN,MAX}$ duty cycle	V_{MAX} = 36 V	24.16%

First, the magnetic core must be selected. To achieve low core losses, this design uses a ferrite E core made out of N87 material. As a tradeoff between the needed space for the planar transformer and a small board outline, the following E core is chosen: http://en.tdk.eu/inf/80/db/fer_13/elp_18.pdf. The dimensions of the E core are 18 × 10 × 6 mm. This size enables a very thin solution with only a 6-mm overall height. Later, the E core is put through the PCB itself, which is about 1.6-mm thick. Hence, the final solution has a height of only 2.2 mm, depending on the exact position of the E core, on each side of the PCB.

Figure 3 shows the hysteresis (magnetic flux density B versus magnetic field strength H) of the material. Figure 4 zooms into the relevant part of the B-H curve for this design. These figures show that for higher temperatures the upper and lower limits of the hysteresis become smaller, which means that the maximum acceptable change ΔB becomes smaller as well. Pay attention to the magnetic field strength H in the transformer. However, this section shows that the maximum magnetic field strength is expected to always stay below 10 A/m. Therefore, the important area of the B-H curve is in the range where H is between ±10 A/m. *One goal of the design is that it can be operated at up to 85°C. Because of its big volume, it is assumed that the ferrite does not heat up more than 15°C during operation.* So, to prevent core saturation at core temperatures up to 100°C, ΔB must be below 150 mT.

The TIDA-00688 is rated for input voltages from 14 to 36V and operates at 200 kHz. The non-isolated output voltage of the Fly-Buck is regulated to 9 V. The selected core has an effective core area Ae of 39.3 mm^2. According to Equation 2, this results in a minimum number of six turns for the primary coil.

$$t_{on,max} = \frac{9\ V}{36\ V} \times (200\ kHz)^{-1} = 1.25\ \mu s$$

$$N_{pr,min} = \frac{V_{tr} \times t_{on,max}}{A_e \times \Delta B} = \frac{(36\ V - 9\ V) \times 1.25\ \mu s}{39.3\ mm^2 \times 150\ mT} = 5.73 \quad (2)$$

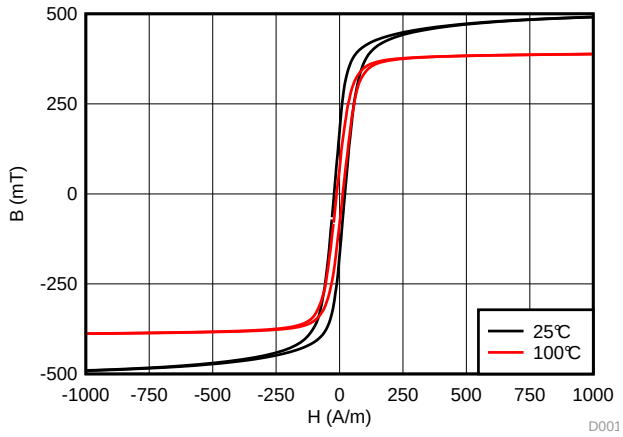


Figure 3. Hysteresis of N87 Material

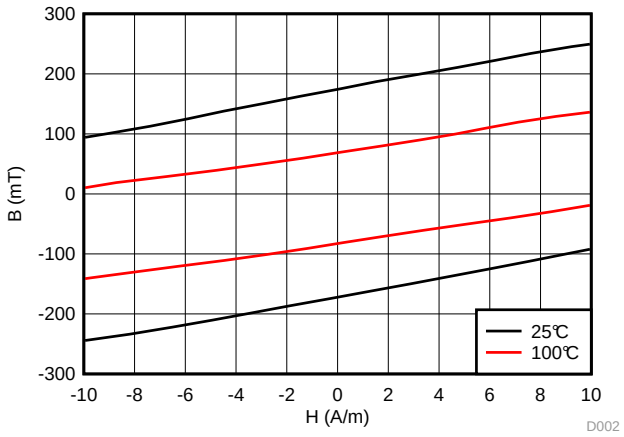


Figure 4. Zoom into Hysteresis of N87 Material

3.2.1 Primary Coil

Standard PCB fabrication requires a minimum distance of 0.15 mm between two traces. For better isolation, leave some distance between the trace and the magnetic core. Furthermore, at one side of the coil, vias are needed to route from the inside to the outside of the coil. These vias are placed 2 mm away from the magnetic core.

To keep these distances and also to keep the DC resistance of the coil as low as possible a trace width of 0.5 mm is chosen. This leaves a distance of around 0.62 mm between the outer or inner winding and the magnetic core. The resulting coil has a length of 0.29 m and an inductance of 110 µH.

Equation 3 calculates the skin depth δ for a defined frequency. At an operating frequency of 200 kHz, the skin depth is 0.146 mm. Because the thickness of the PCB trace is only 0.035 mm, the skin effect can be neglected.

$$\delta = \sqrt{\frac{2\rho_{Cu}}{2\pi f \mu_{Cu}\mu_o}} = \sqrt{\frac{2 \times 1.7 \times 10^{-8}\,\text{m}\Omega}{2\pi \times 200\,\text{kHz} \times 1 \times 4\pi \times 10^{-7}\,\frac{\text{H}}{\text{m}}}} = 0.147\,\text{mm} \tag{3}$$

The DC resistance of the coil can be calculated with Equation 4.

$$R = \rho_{Cu} \times \frac{l}{A} = 1.7 \times 10^{-8}\,\text{m}\Omega \times \frac{0.29\,\text{m}}{0.035\,\text{mm} \times 0.5\,\text{mm}} = 282\,\text{m}\Omega \tag{4}$$

The resulting current ripple is calculated to 307 mA using Equation 5.

$$\Delta I = \frac{V_{pr} \times t_{on,max}}{L_{pr}} = \frac{(36\,\text{V} - 9\,\text{V}) \times 1.25\,\mu\text{s}}{110\,\mu\text{H}} = 307\,\text{mA} \tag{5}$$

To estimate the DC current on the primary side under full load condition, assume the following inputs, slightly higher voltage outputs, and a perfect transformer with no losses:
Output 1: 18 V, 30 mA + 40 mA
Output 2: -18 V, 30 mA

$$V_{IN} \times I_{IN} = V_{OUT} \times I_{OUT}$$

$$\rightarrow I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN}} = \frac{18\,\text{V} \times 70\,\text{mA} + |-18\,\text{V}| \times 30\,\text{mA}}{9\text{V}} = 200\,\text{mA} \tag{6}$$

With the calculated DC current on the primary side, the length of the coil, and Equation 7, the maximum magnetic field strength H is calculated to 4.14 A/m.

$$H = \frac{N \times I}{l} = \frac{6 \times \left(200 + \frac{307}{2}\right)\text{mA}}{0.29\,\text{m}} = 4.14\,\frac{\text{A}}{\text{m}} \tag{7}$$

Taking into account the ripple of around 307 mA, the maximum magnetic field strength is calculated to 7.31 A/m. Therefore, assume that the maximum magnetic field strength always stays below ±10 A/m.

3.2.2 Secondary Coil

To get to the desired output voltage of ±18 V on the secondary side, two coils each with a winding ratio of about 1:2, compared to the primary coil, are needed. Therefore, the coils need 12 windings each. Ground potential of the secondary side is set at the connection point between the two coils. Figure 5 shows the layer setup of the secondary side.

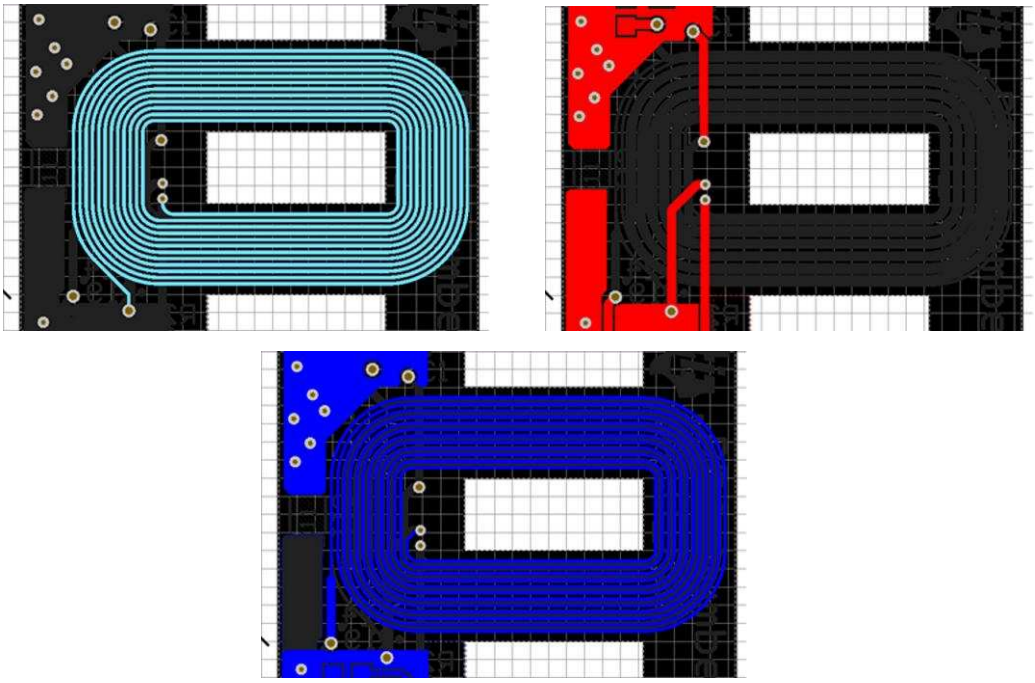


Figure 5. Secondary Side Setup (Secondary Coil 1, Secondary GND (Lower Part), Secondary Coil 2)

Again, to stay within standard fabrication limits and to find a good trade-off between trace width and DC resistance, a trace width of 0.2 mm and a distance of 0.15 mm between the traces are selected. This leaves a distance of around 0.475 mm between the outer and inner winding and the magnetic core. Like for the primary coil, necessary vias for routing are placed 2 mm away from the magnetic core.

The resulting secondary coils have a length of 0.6 m each. As before, the skin effect can be neglected. Again, using Equation 4 the DC resistance of each secondary coil is calculated to 1.46 Ω.

3.3 Operating Switching Frequency

An operating frequency of 200 kHz is chosen. This frequency enables to stay within the limits for ΔB and sets an acceptable current ripple. Furthermore, this frequency complies with the operating recommendation of the selected magnetic core.

The selected frequency sets the minimum energy transfer time for the transformer to 1.25 µs. The switching frequency is set with resistor R4.

$$f_{SW} = \frac{V_{C1}}{10^{-10} \times R4}$$

$$R4 = \frac{9\ V}{10^{-10} \times 200\ kHz} = 450\ k\Omega \quad (8)$$

The next closest standard resistor value is 453 kΩ.

3.4 Output Ripple Configuration

As mentioned in Section 3.1, the LM5017 uses a COT control scheme where the on-time is controlled with a timer. The off-time is terminated when the feedback voltage falls below the reference voltage. For stable operation, it is necessary that during off time the feedback voltage decreases monotonically in phase with the inductor current. To ensure the correct ripple injection in the regulation loop, three different schemes are possible. This design follows scheme type 3 of *AN-2292 Designing an Isolated Buck (Fly-Buck) Converter* [3] with some modifications required to support the large input voltage range and low input voltage.

4 Block Diagram

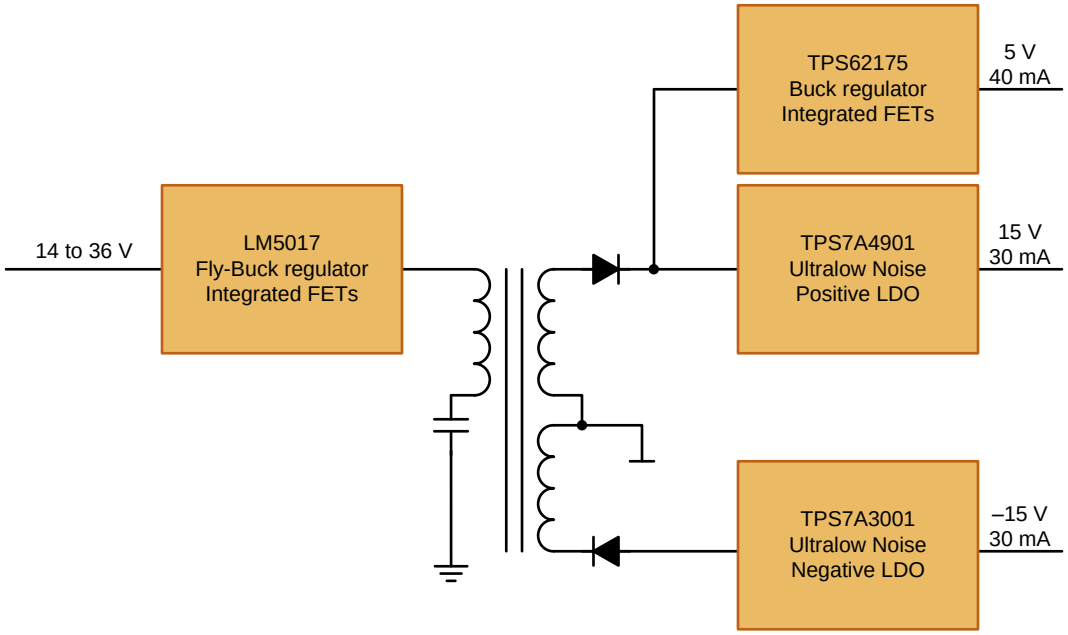


Figure 6. TIDA-00688 Block Diagram

4.1 Highlighted Products

The TIDA-00688 provides isolated analog and digital supply voltages for PLC analog I/O modules. For the analog section of the modules, the TIDA-00688 generates ±15 V. These output voltages are highly accurate and have minimal noise. The additional 5-V supply can be used as digital components like data converters, microcontrollers, or other isolated devices. To avoid the need for a third transformer secondary winding, this voltage is created from the 15-V rail using a high efficiency DC/DC converter.

4.1.1 LM5017

The LM5017 is a 100-V, 600-mA synchronous step-down regulator with integrated high-side and low-side MOSFETs. The COT control scheme employed in the LM5017 requires no loop compensation, provides excellent transient response, and enables very high step-down ratios. The on-time varies inversely with the input voltage resulting in nearly constant frequency over the input voltage range. A high-voltage startup regulator provides bias power for internal operation of the IC and for integrated gate drivers. A peak current limit circuit protects against overload conditions. The under voltage lockout (UVLO) circuit allows the input under voltage threshold and hysteresis to be independently programmed. Other protection features include thermal shutdown and bias supply undervoltage lockout (VCC UVLO).

4.1.2 TPS7A4901

The TPS7A4901 is a positive, high-voltage (36 V), ultralow-noise (15.4 μV_{RMS}, 72-dB PSRR) linear regulator capable of sourcing a load of 150 mA. This linear regulator includes a capacitor-programmable soft-start function that allows for delaying the output voltage generation until the power source is operating stable. Other features available include built-in current limit and thermal shutdown protection to safeguard the device and system during fault conditions. The TPS7A4901 is designed using bipolar technology and is ideal for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This design makes the device an excellent choice to power operational amplifiers, ADCs, DACs, and other high-performance analog circuitry. In addition, the TPS7A4901 is suitable for post DC/DC converter regulation. By filtering out the output voltage ripple inherent to DC/DC switching conversion, maximum system performance is provided in sensitive instrumentation, test and measurement, audio, and RF applications.

4.1.3 TPS7A3001

The TPS7A3001 complements the TPS7A4901 described in Section 4.1.2. It is a negative, high-voltage (–36 V), ultralow-noise (15.1 μV_{RMS}, 72-dB PSRR) linear regulator capable of sourcing a maximum load of 200 mA. The feature list of the TPS3001 is a 1:1 equivalent to the one of the TPS7A4901.

4.1.4 TPS62175

The TPS62175 is a high-efficiency synchronous step-down DC-DC converter, based on the DCS-Control topology, with a wide operating range of input voltage from 4.75 to 28 V providing up to a 500-mA output current. The TPS62175 automatically enters a power save mode at light loads, to maintain high efficiency across the whole load range. As well, it features a sleep mode to supply applications with advanced power save modes like ultralow-power microcontrollers. The Power Good output may be used for power sequencing or power-on reset. The device features a typical quiescent current of 22 µA in normal mode and 4.8 µA in sleep mode. In sleep mode, the efficiency at very low load currents can be increased by as much as 20%. In shutdown mode, the shutdown current is less than 2 µA and the output is actively discharged.

5 Getting Started Hardware

The design can be operated out of the box. Load resistors with a power rating of at least 500 mW can be connected directly to the output terminals. To perform a maximum power test, connect 470-Ω resistors to the 15-V (J3) and –15-V (J4) outputs and a 120-Ω resistor to the 5-V output (J2). Currents I_{J3} and I_{J4} will settle to 32 mA, and I_{J2} to 42 mA.

6 Test Results

The design is tested for an input voltage range of 14 ($V_{IN,MIN}$) to 36 V ($V_{IN,MAX}$). This section presents the test results and scope shots for load regulation, system efficiency, startup and shutdown sequence, switch node switching, and voltage ripple at C1.

6.1 Load Regulation

For the load regulation test, several different output current setups are tested. The tested output currents for the ±15-V outputs are 0 mA, 3 mA, 12 mA, and 32 mA. The tested output currents for the 5-V output are 0 mA, 4 mA, 14 mA, and 42 mA. The test results are listed in Table 3.

The test results show that the output voltage changes only 30 mV for the 15-V output and only 20 mV for the –15-V and 5-V outputs over the complete load range from overall 0 mA up to 104 mA. It is also shown that it has no effect if one output channel is supplying more current than the two others.

Table 3. Load Regulation

V_{IN}	mA			V		
	I_J3	I_J4	I_J2	V_J3	V_J4	V_J2
14 V	0	0	0	15.03	–15.00	5.10
24 V	0	0	0	15.03	–15.00	5.10
36 V	0	0	0	15.03	–15.00	5.10
14 V	3	0	0	15.02	–15.00	5.10
	0	3	0	15.03	–14.99	5.10
	0	0	4	15.03	–15.00	5.01
	3	3	4	15.02	–14.99	5.01
	12	0	0	15.01	–15.00	5.10
	0	12	0	15.03	–14.99	5.10
	0	0	14	15.03	–15.00	5.09
	12	12	14	15.01	–14.99	5.09
	32	0	0	15.01	–15.00	5.10
	0	32	0	15.03	–14.98	5.10
	0	0	42	15.03	–15.00	5.08
	32	32	42	15.00	–14.98	5.08
24 V	3	0	0	15.02	–15.00	5.10
	0	3	0	15.03	–14.99	5.10
	0	0	4	15.03	–15.00	5.10
	3	3	4	15.02	–14.99	5.10
	12	0	0	15.01	–15.00	5.10
	0	12	0	15.03	–14.99	5.10
	0	0	14	15.03	–15.00	5.09
	12	12	14	15.01	–14.99	5.09
	32	0	0	15.01	–15.00	5.10
	0	32	0	15.03	–14.98	5.10
	0	0	42	15.03	–15.00	5.08
	32	32	42	15.00	–14.98	5.08

Table 3. Load Regulation (continued)

V_{IN}	mA			V		
	I_J3	I_J4	I_J2	V_J3	V_J4	V_J2
36 V	3	0	0	15.02	–15.00	5.10
	0	3	0	15.03	–14.99	5.10
	0	0	4	15.03	–15.00	5.10
	3	3	4	15.02	–14.99	5.10
	12	0	0	15.01	–15.00	5.10
	0	12	0	15.03	–14.99	5.10
	0	0	14	15.03	–15.00	5.09
	12	12	14	15.01	–14.99	5.09
	32	0	0	15.01	–15.00	5.10
	0	32	0	15.03	–14.98	5.10
	0	0	42	15.03	–15.00	5.08
	32	32	42	15.00	–14.98	5.08

6.2 Design Efficiency

The efficiency of the design is tested for three different output currents. For a 10-mA overall output current, the output of the ±15-V channel is 3 mA and the output of the 5-V channel is 4 mA. For a 38-mA overall output current, the output of the ±15-V channel is 12 mA and the output of the 5-V channel is 14 mA. For a 106-mA overall output current, the output of the ±15-V channel is 32 mA and the output of the 5-V channel is 42 mA. The measurement results are shown in Figure 7. Efficiency is highest for lowest input voltages because for lower input voltages, the average voltage across capacitor C1 is lower as well. This results in a lower voltage on the secondary side of the transformer and therefore a lower voltage drop and less energy dissipation across the LDOs U2 and U3. The design works best for highest output currents. The peak efficiency is measured to 76.9% at V_{IN} = 14 V and I_{OUT} = 106 mA.

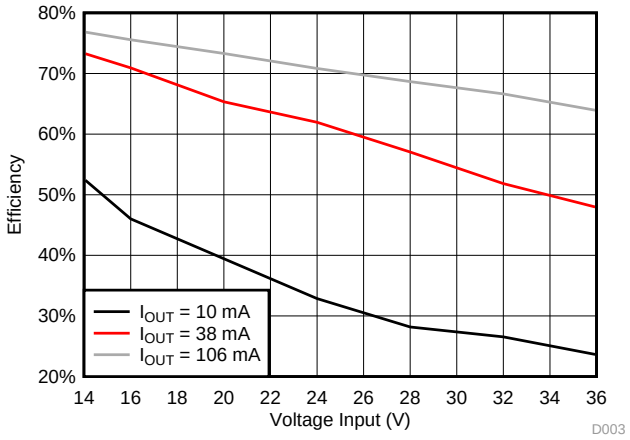


Figure 7. TIDA-00688 Efficiency Results

6.3 Startup and Shutdown Sequence

Figure 8 and Figure 9 show the startup and shutdown sequences for the 12-V, 24-V, and 36-V input voltages. The 12-V input voltage is tested to showcase what is happening if the input voltage drops below the specified 14 V. With just the 12-V input voltage, the design starts working without any problems. However, the output of the ±15-V channels are slightly too low for the LDO's minimum drop voltage to be regulated. Therefore, the design should only be operated within 14- to 36-V input voltage. The UVLO is set to 12 V with resistors R2 and R3.

The startup time goes from 18 ms for the 12-V input voltage down to 12 ms for the 36-V input voltage. For all sequences, as soon as the supply voltage of the LM5017 reaches 12 V, the LM5017 starts operating and the three secondary outputs are enabled. The output of the TPS62175 is enabled in about 1 ms. The regulated LDO outputs take about 10 ms until they reach their final output voltage.

The shutdown sequences look very similar to each other. As soon as the input voltage falls below 12 V, the LM5017 stops working and the secondary outputs are disabled. Then, the outputs caps are discharged.

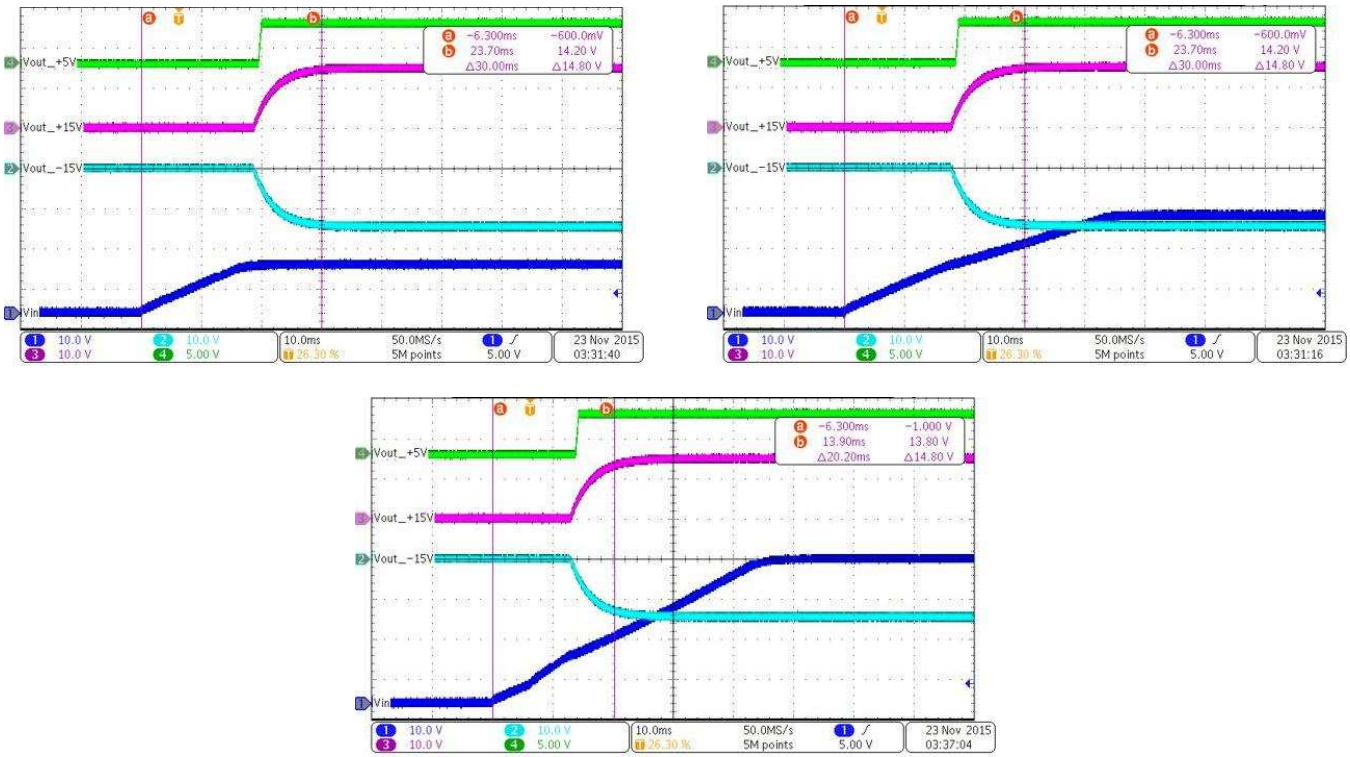


Figure 8. Startup Sequences for V_{IN} = 12 V, 24 V, 36 V

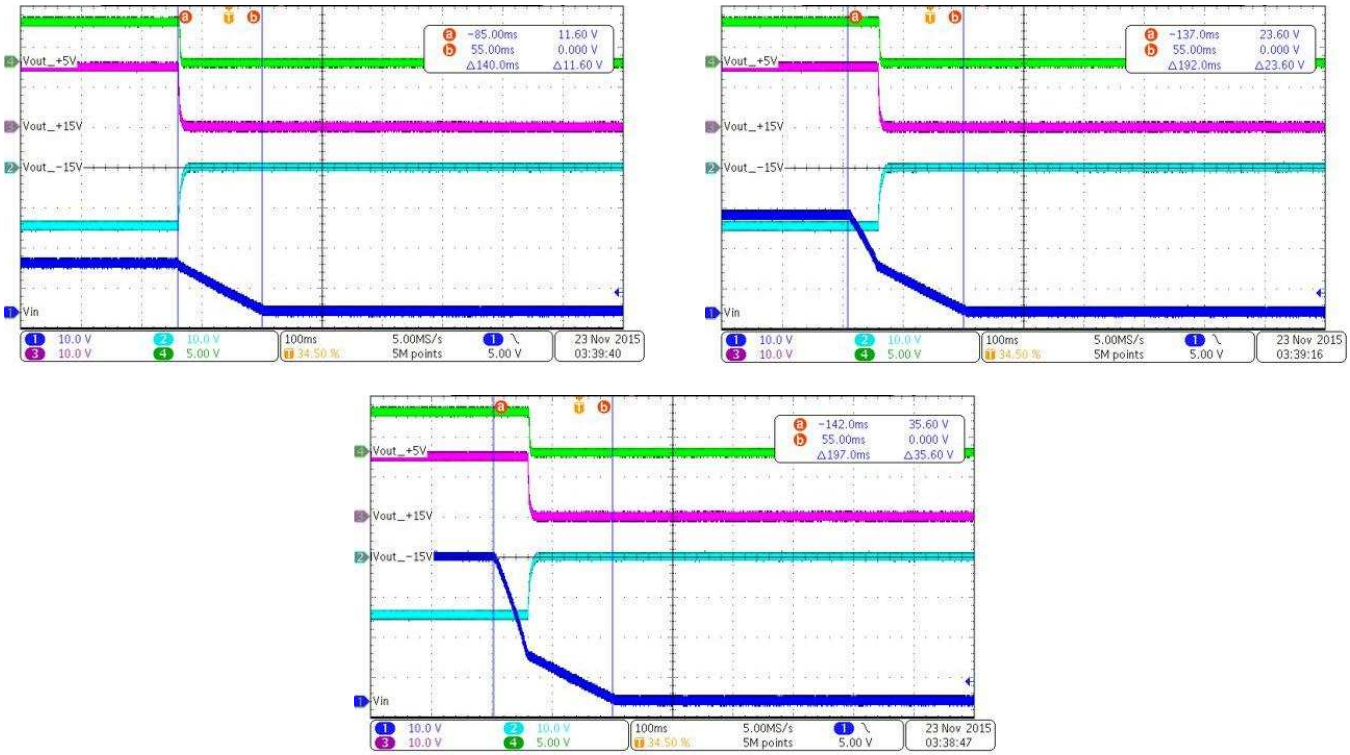


Figure 9. Shutdown Sequences for V_{IN} = 12 V, 24 V, 36 V

6.4 Switch Node

Figure 10 shows the switching behavior of the LM5017 for input voltages of 12, 24, and 36 V, which is that the duty cycle is higher for lower input voltages. As a result of the COT switching behavior of the LM5017, the switching frequency differs with the input voltage as well.

The duty cycle goes from 73% for 12-V input voltage down to 33% for 36-V input voltage.

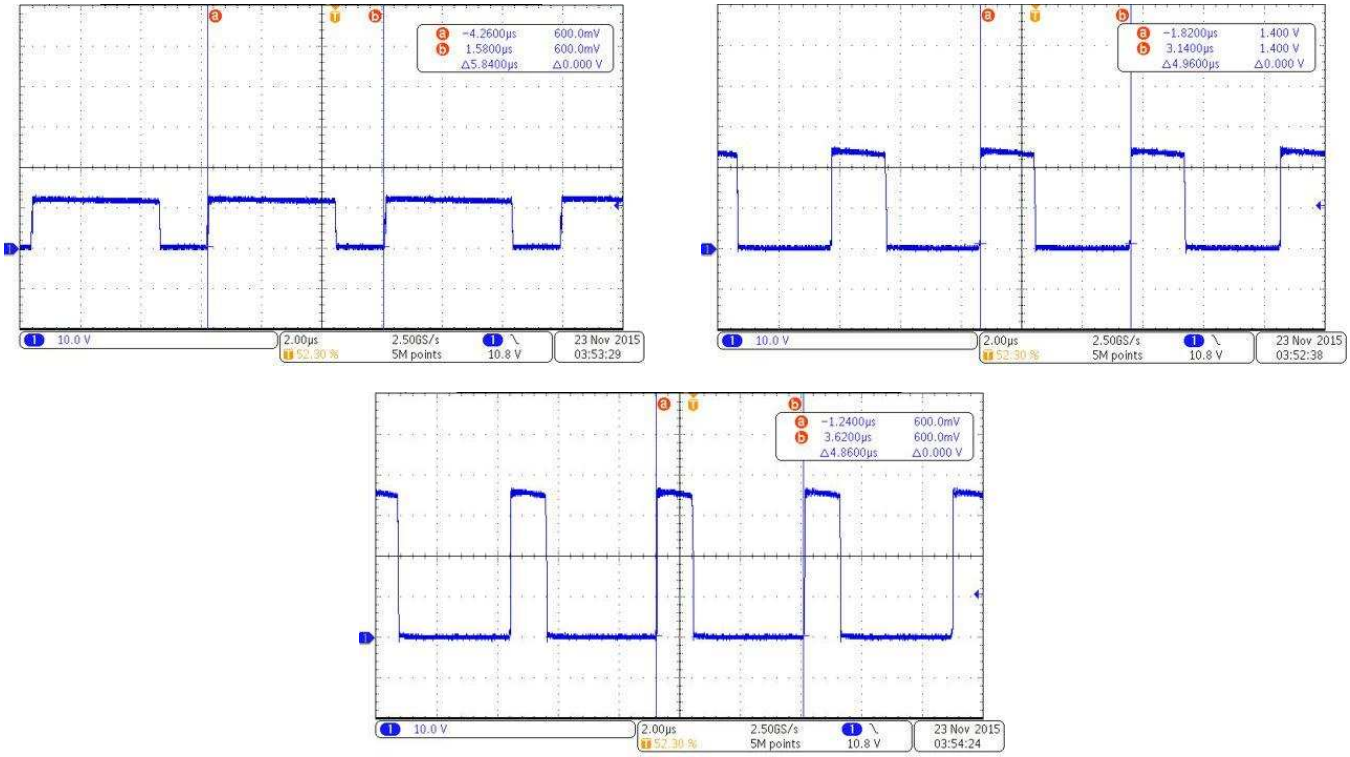


Figure 10. Switching of LM5017 for V_{IN} = 12 V, 24 V, 36 V

6.5 Thermal Measurement

Figure 11 shows thermal pictures of the board for different input voltages under full load condition. The pictures were captured with a FLUKE Ti40FT at 25°C room temperature. The images show that the ferrite stays cool for the complete input voltage range. In the case of V_{IN} = 36 V, the maximum temperature on the board is at the LM5017, which reaches 48°C. The circuit is designed for temperatures of up to 125°C. Therefore, the board can be operated at ambient temperatures of up to 85°C.

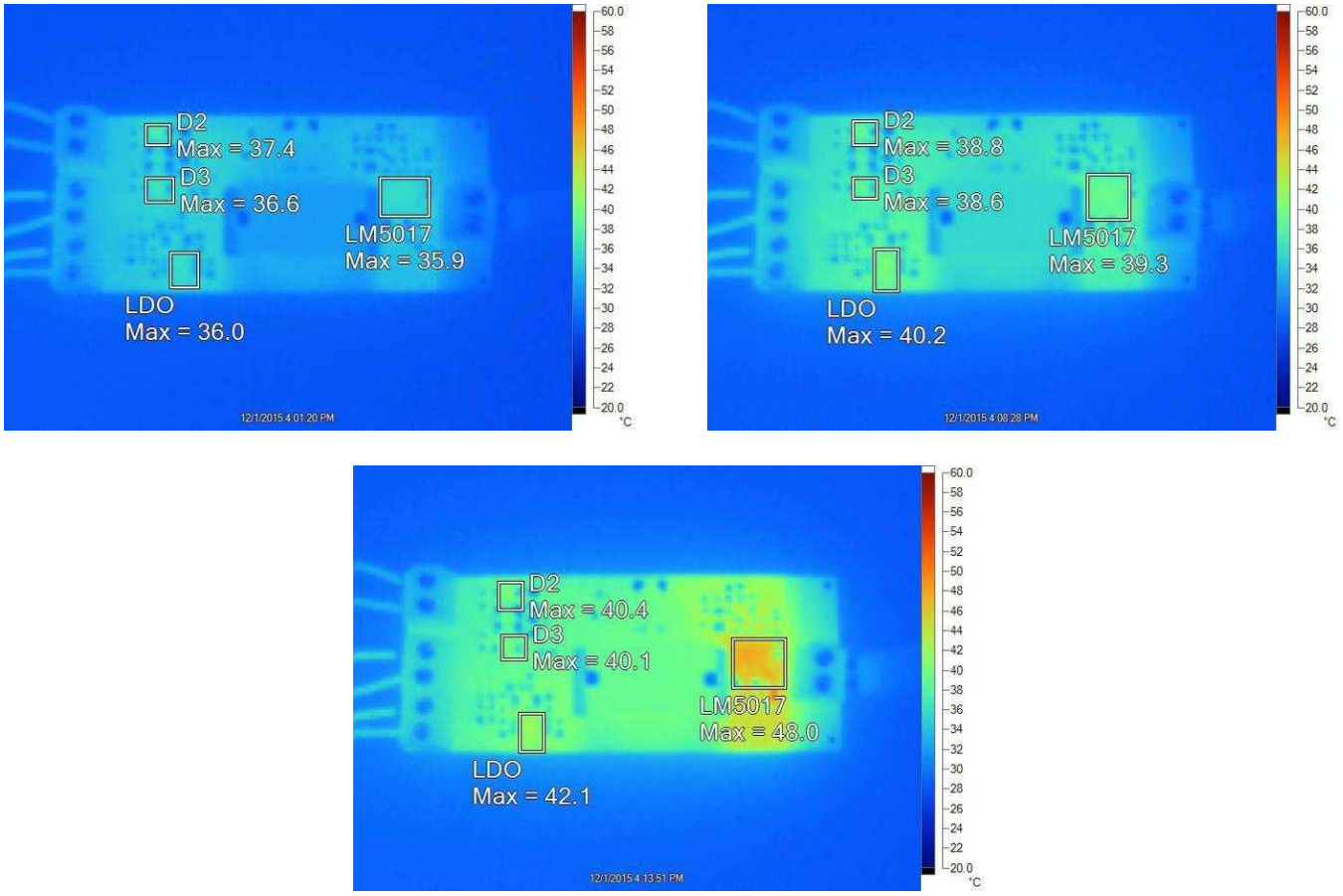


Figure 11. Thermal Pictures of TIDA-00688 for V_{IN} = 12 V, 24 V, 36 V

7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-00688.

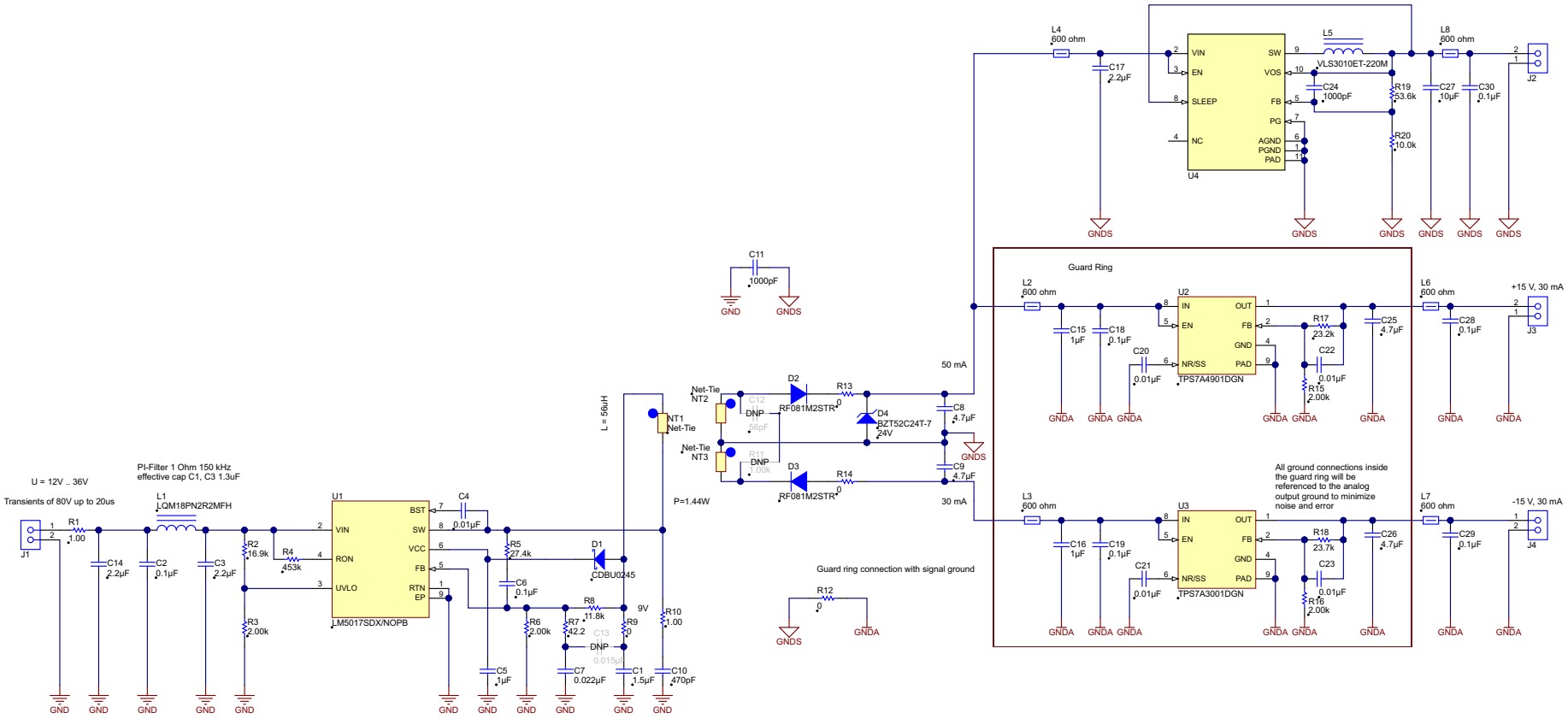


Figure 12. 1-W Isolated Power Supply With Planar Transformer Schematic

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00688.

Table 4. TIDA-00688 BOM

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
1	!PCB	1		TIDA-00688	Any	Printed Circuit Board	
2	C1	1	1.5uF	GRM21BR71E155KA88L	MuRata	CAP, CERM, 1.5 µF, 25 V, +/- 10%, X7R, 0805	0805
3	C2, C18, C19, C28, C29, C30	6	0.1uF	C1608X7R1H104K	TDK	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0603	0603
4	C3, C14	2	2.2uF	UMK316B7225KD-T	Taiyo Yuden	CAP, CERM, 2.2 µF, 50 V, +/- 10%, X7R, 1206	1206
5	C4, C20, C21, C22, C23	5	0.01uF	C0603C103J5RACTU	Kemet	CAP, CERM, 0.01 µF, 50 V, +/- 5%, X7R, 0603	0603
6	C5	1	1uF	GRM188R71E105KA12D	MuRata	CAP, CERM, 1 µF, 25 V, +/- 10%, X7R, 0603	0603
7	C6	1	0.1uF	GCM188R71H104KA57D	MuRata	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0603	0603
8	C7	1	0.022uF	GRM188R71H223KA01D	MuRata	CAP, CERM, 0.022 µF, 50 V, +/- 10%, X7R, 0603	0603
9	C8, C9	2	4.7uF	GRM31CR71E475KA88L	MuRata	CAP, CERM, 4.7 µF, 25 V, +/- 10%, X7R, 1206	1206
10	C10	1	470pF	C0603C471K5RACTU	Kemet	CAP, CERM, 470 pF, 50 V, +/- 10%, X7R, 0603	0603
11	C11	1	1000pF	202R18W102KV4E	Johanson Technology	CAP, CERM, 1000 pF, 2000 V, +/- 10%, X7R, 1206_190	1206_190
12	C15, C16	2	1uF	C0603C105K3RACTU	Kemet	CAP, CERM, 1 µF, 25 V, +/- 10%, X7R, 0603	0603
13	C17	1	2.2uF	C2012X7R1V225K085AC	TDK	CAP, CERM, 2.2 µF, 35 V, +/- 10%, X7R, 0805	0805
14	C24	1	1000pF	GRM188R71E102KA01D	MuRata	CAP, CERM, 1000 pF, 25 V, +/- 10%, X7R, 0603	0603
15	C25, C26	2	4.7uF	C3216X7R1E475K085AB	TDK	CAP, CERM, 4.7 µF, 25 V, +/- 10%, X7R, 1206	1206
16	C27	1	10uF	C3216X7R1A106M085AC	TDK	CAP, CERM, 10 µF, 10 V, +/- 20%, X7R, 1206	1206
17	D1	1	45V	CDBU0245	Comchip Technology	Diode, Schottky, 45 V, 0.2 A, SOD-523F	SOD-523F
18	D2, D3	2	200V	RF081M2STR	Rohm	Diode, Fast Rectifier, 200 V, 0.8 A, SOD-123	SOD-123

Table 4. TIDA-00688 BOM (continued)

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
19	D4	1	24V	BZT52C24T-7	Diodes Inc.	Diode, Zener, 24 V, 300 mW, SOD-523	SOD-523
20	FID1, FID2, FID3	3		N/A	N/A	Fiducial mark. There is nothing to buy or mount.	N/A
21	H1, H4	2		B66284F2204X	TDK	CLAMP ELP 18X4X10 I 18X2X10	
22	H2	1	2.9 uH	B66283PX187	TDK	FERRITE CORE ELP 2.9UH N87	
23	H3	1	2.6uH	B66283GX187	TDK	Ferrite Core, ELP, 2.6uH, N87	
24	J1, J2, J3, J4	4	2x1	1751248	Phoenix Contact	Conn Term Block, 2POS, 3.5mm, TH	11x8.5x7.3mm
25	L1	1	2.2uH	LQM18PN2R2MFH	MuRata	Inductor, Ferrite, 2.2 µH, 0.35 A, 0.38 ohm, SMD	0603
26	L2, L3, L4, L6, L7, L8	6	600 ohm	BLM18KG601SN1D	MuRata	Ferrite Bead, 600 ohm @ 100 MHz, 1.3 A, 0603	0603
27	L5	1	22uH	VLS3010ET-220M	TDK	Inductor, Shielded, Ferrite, 22 µH, 0.38 A, 0.9 ohm, SMD	Inductor, 3x1x3mm
28	R1, R10	2	1.00	CRCW06031R00FKEA	Vishay-Dale	RES, 1.00, 1%, 0.1 W, 0603	0603
29	R2	1	16.9k	CRCW060316K9FKEA	Vishay-Dale	RES, 16.9 k, 1%, 0.1 W, 0603	0603
30	R3, R6, R15, R16	4	2.00k	CRCW06032K00FKEA	Vishay-Dale	RES, 2.00 k, 1%, 0.1 W, 0603	0603
31	R4	1	453k	CRCW0603453KFKEA	Vishay-Dale	RES, 453 k, 1%, 0.1 W, 0603	0603
32	R5	1	27.4k	CRCW060327K4FKEA	Vishay-Dale	RES, 27.4 k, 1%, 0.1 W, 0603	0603
33	R7	1	42.2	CRCW060342R2FKEA	Vishay-Dale	RES, 42.2, 1%, 0.1 W, 0603	0603
34	R8	1	11.8k	CRCW060311K8FKEA	Vishay-Dale	RES, 11.8 k, 1%, 0.1 W, 0603	0603
35	R9, R13, R14	3	0	ERJ-3GEY0R00V	Panasonic	RES, 0, 5%, 0.1 W, 0603	0603
36	R12	1	0	CRCW06030000Z0EA	Vishay-Dale	RES, 0, 5%, 0.1 W, 0603	0603
37	R17	1	23.2k	CRCW060323K2FKEA	Vishay-Dale	RES, 23.2 k, 1%, 0.1 W, 0603	0603
38	R18	1	23.7k	CRCW060323K7FKEA	Vishay-Dale	RES, 23.7 k, 1%, 0.1 W, 0603	0603
39	R19	1	53.6k	CRCW060353K6FKEA	Vishay-Dale	RES, 53.6 k, 1%, 0.1 W, 0603	0603
40	R20	1	10.0k	CRCW060310K0FKEA	Vishay-Dale	RES, 10.0 k, 1%, 0.1 W, 0603	0603
41	U1	1		LM5017SDX/NOPB	Texas Instruments	100V, 600mA Constant On-Time Synchronous Buck Regulator, NGU0008B	NGU0008B
42	U2	1		TPS7A4901DGN	Texas Instruments	+36V, +150mA, Ultralow-Noise, Positive LINEAR REGULATOR, DGN0008D	DGN0008D

Table 4. TIDA-00688 BOM (continued)

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
43	U3	1		TPS7A3001DGN	Texas Instruments	-36V, -200mA, Ultralow-Noise, High PSRR, Adjustable -1.18 to -33 V Output, Negative Linear Regulator, 8-pin MSOP (DGN), -40 to 125 degC, Green (RoHS & no Sb/Br)	DGN0008D
44	U4	1		TPS62175DQCR	Texas Instruments	28V, 0.5A Step-Down Converter with Sleep Mode, DQC0010A	DQC0010A
45	C12	0	56pF	GRM21A5C2E560JW01D	MuRata	CAP, CERM, 56 pF, 250 V, +/- 5%, C0G/NP0, 0805	0805
46	C13	0	0.015uF	GRM188R71H153KA01D	MuRata	CAP, CERM, 0.015 µF, 50 V, +/- 10%, X7R, 0603	0603
47	R11	0	1.00k	CRCW08051K00FKEA	Vishay-Dale	RES, 1.00 k, 1%, 0.125 W, 0805	0805

7.3 PCB Layout Recommendations

The PCB layout is driven by two requirements: First, a small form-factor, and second, usability in the industrial environment, meaning working at ambient temperatures of up to 85°C, low EMI, and low noise.

To achieve a small form factor, place all components very near to each other while keeping design and placement rules in mind. To keep tracks also short, distribute components on both sides of the PCB. To keep cost low, only use 0603-sized or larger components in the design.

To get the planar transformer onto the board, use a four-layer design. Both sides of the board have a GND plane with 35-µm copper. As a result, every IC on the board has enough copper around it to distribute heat, and the design can be operated at ambient temperatures of up to 85°C. The secondary analog section of the board also has guard rings on the top and bottom layers to reduce EMI and noise.

Figure 13 shows the path of the current for one switching cycle. During toff, current follows the dashed path from capacitor C1 on the left into the planar transformer (not shown), then through the switching node and the low-side FET of the LM5017 to GND, and back to C1. Also during toff, C1 serves as a local power supply.

During ton, current follows the dotted path from capacitor C3 on the right through the high-side FET of the LM5017 into the planar transformer (not shown) to capacitor C1 and back to C3. Also during ton, C3 serves as a local power supply.

To keep the current path short and switching noise low, place C1 and C3 close to the LM5017. Figure 13 shows an exemplary layout where these requirements are fulfilled.

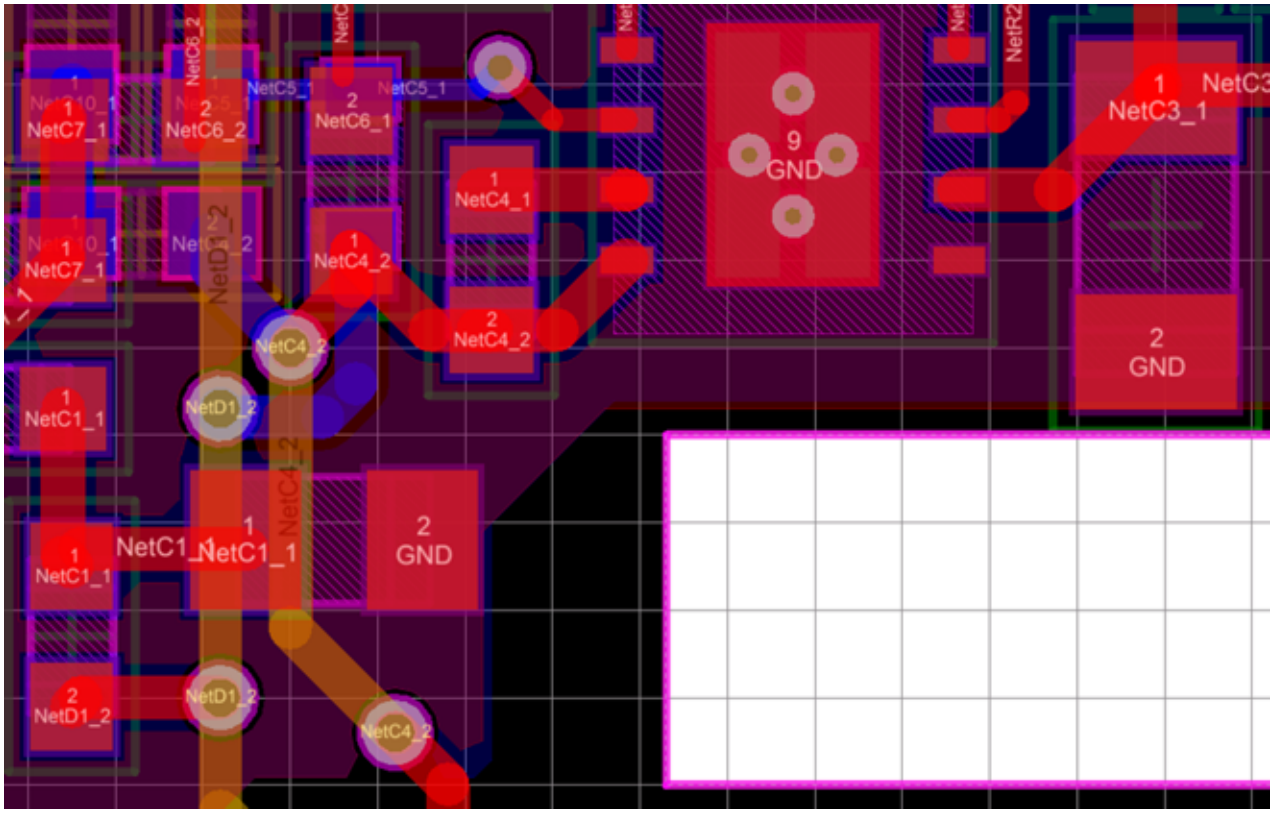


Figure 13. Layout Recommendation LM5017

Figure 14 shows the critical parts of the layout for the secondary side. To provide good filtering of the unregulated voltage, keep the current loops shown by ellipses G8 and G9 as small as possible. The rectified and filtered supply is guided through a strong ground reference to the guard rings of the analog section. They enter the ring through EMI filter ferrites into a filter capacitor. The layout inside the guard ring is then only critical in terms of heat distribution. A symmetric layout on top and bottom layers for positive and negative analog supplies make it easy to achieve cooling on the top and bottom layers.

The guard ring and the ground plane of the switching side are separated as indicated with line G5. The only connection is the 0-Ω resistor R12 to GND potential of both the positive and negative supply voltages. Keep the analog and digital supply separated if possible. Furthermore, the analog section is referenced to its ground output, thus eliminating switching noise all together.

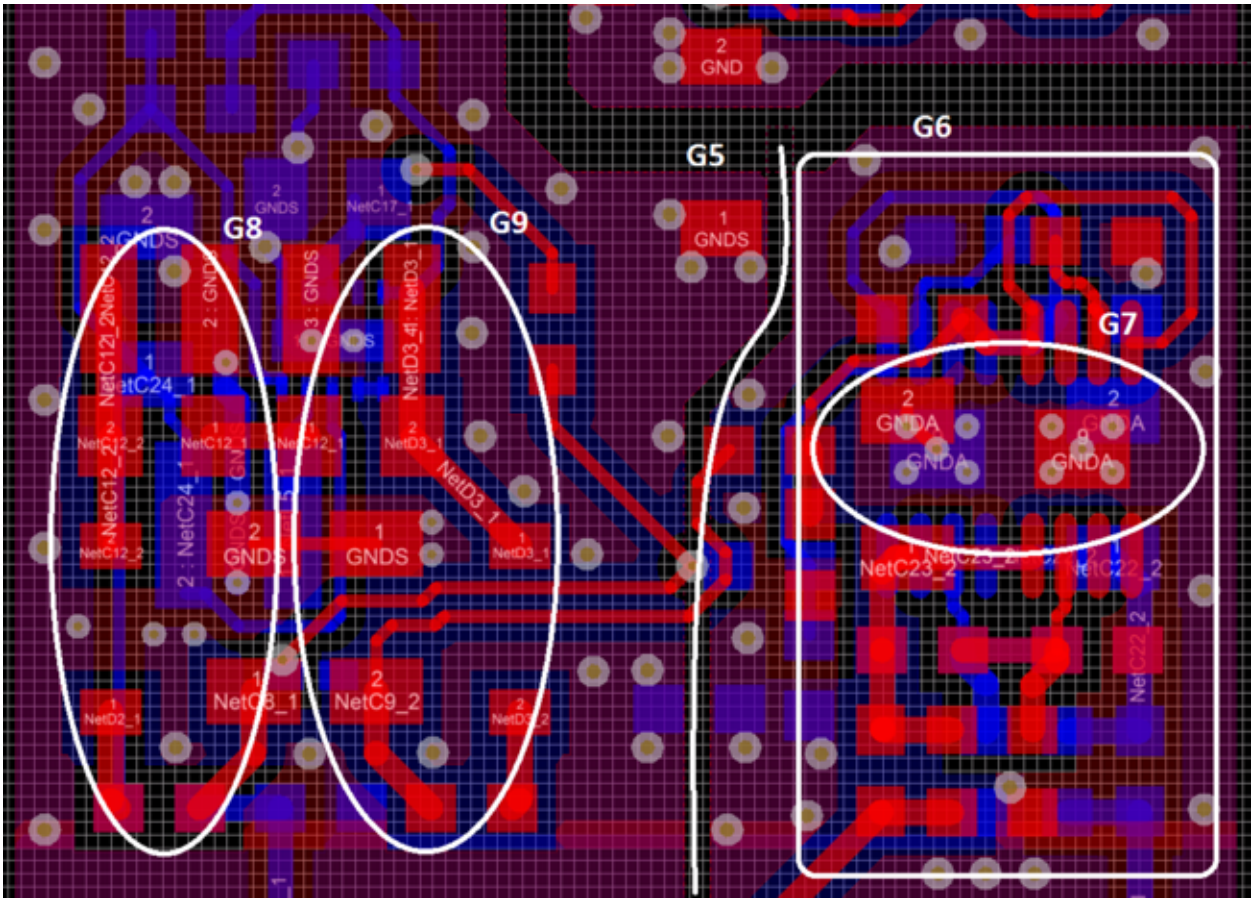


Figure 14. Layout Recommendation Secondary Side

7.3.1 Layer Plots

To download the layer plots, see the design files at TIDA-00688.

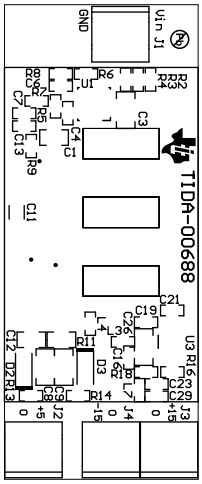


Figure 15. Top Overlay

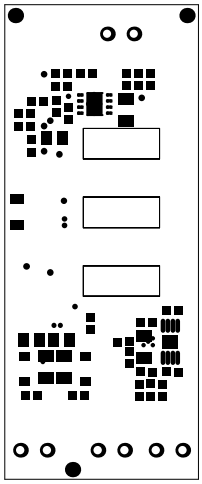


Figure 16. Top Solder Mask

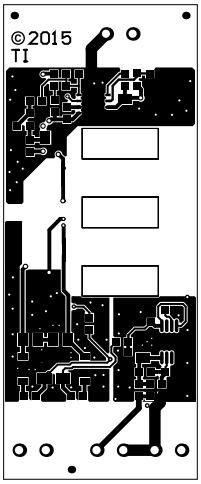


Figure 17. Top Layer

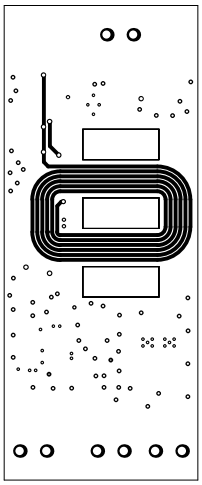


Figure 18. Mid Layer 1

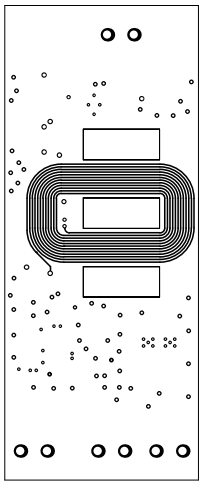


Figure 19. Mid Layer 2

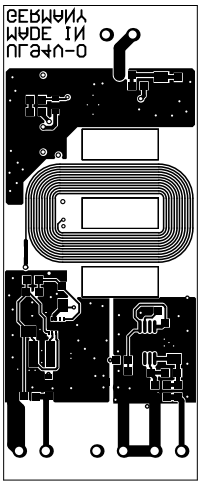


Figure 20. Bottom Layer

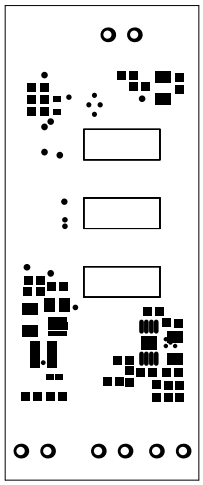


Figure 21. Bottom Solder Mask

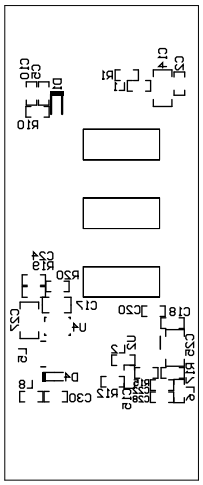


Figure 22. Bottom Overlay

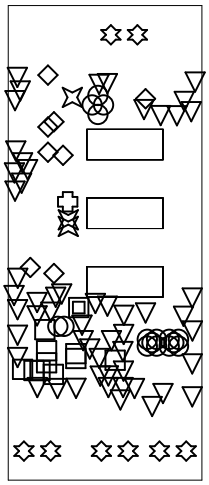


Figure 23. Drill Drawing

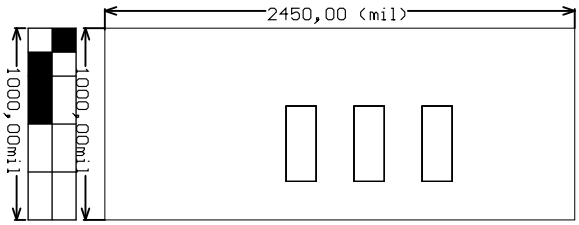


Figure 24. Board Dimensions

7.4 Altium Project

To download the Altium project files, see the design files at TIDA-00688.

7.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00688.

7.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00688.

8 References

1. Texas Instruments, *1-W Small Form Factor Power Supply with Isolated Dual Output for PLC I/O Modules*, TIDA-00129 Design Guide (TIDU263)
2. Texas Instruments, *Ultra-Thin, Small Footprint 1-W, 12- to 36-V Isolated Power Supply With ±15 V and 5 V for Analog PLC Modules*, TIDA-00237 Design Guide (TIDU855)
3. Texas Instruments, *AN-2292 Designing an Isolated Buck (Fly-Buck) Converter*, Fly-Buck Application Note (SNVA674)

9 About the Authors

TOBIAS PUETZ is a systems engineer in the Texas Instruments Factory Automation and Control team, where he is working on PLC modules. Tobias brings to this role his expertise in different sensing technologies, power design, and wireless charging as well as software design. Tobias earned his master's degree in electrical engineering and information technology at the Karlsruhe Institute of Technology (KIT), Germany in 2014.

INGOLF FRANK is a systems engineer in the Texas Instruments Factory Automation and Control team, focusing on PLC I/O modules. Ingolf works across multiple product families and technologies to leverage the best solutions possible for system level application design. Ingolf earned his electrical engineering degree (Dipl. Ing. (FH)) in the field of information technology at the University of Applied Sciences Bielefeld, Germany in 1991.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265