TI Designs
Multi-Band RF Sampling Receiver Solution

TEXAS INSTRUMENTS

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The RF sampling receiver captures signals directly in the radio frequency (RF) band. In a multi-band application, the desired signals do not have a very wide band, but they are spaced far apart within the spectrum. The ADC32RF80 is a dual-channel, 14-bit, 3-GSPS RF sampling telecom receiver. The 3-dB input bandwidth is 3 GHz, and it captures signals up to 4 GHz. The device includes two digital down converters (DDC) per channel. The DDC offers decimation values from 8 to 32 and includes a 16-bit numerically controlled oscillator to move the captured signal down to digital baseband. With the high sampling rate of the ADC32RF80, the device captures a large swatch of the RF spectrum, which contains signals in multiple bands and potentially undesired interferers. The DDC independently mixes the desired bands to digital baseband. Decimation reduces the output data rate to a lower level and provides digital filtering around the desired band to eliminate interference and to improve signal-to-noise ratio (SNR) performance. This feature is critical for high-end telecommunication receivers that require high dynamic range.

Design Resources

|	
TIDA-01163	Design Folder
ADC32RF80EVM	Tool Folder
ADC32RF80	Product Folder
LMX2582	Product Folder
LMK04828	Product Folder

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Design Features

- 3-GSPS RF Sampling Receiver Solution
- Low Noise, High Dynamic Range RF Sampling Receiver Solution
- Programmable Decimation from 8 to 32
- Dual Digital Down-Converter With Independent Numerically Controlled Oscillators

Featured Applications

- Wireless Base Station Multi-Band or Multi-Mode Receiver
- Multi-carrier GSM Receiver
- Digital Pre-Distortion Feedback Receiver
- Telecommunications Receiver
- Carrier Aggregation Receiver
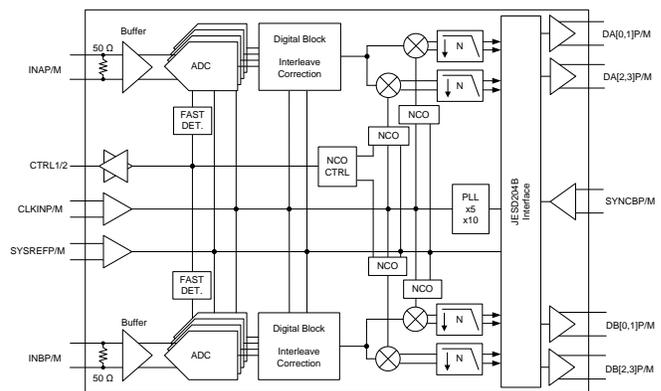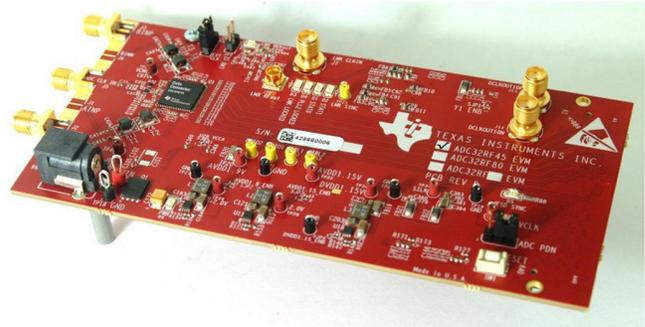
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1 System Description

This reference design implements an RF sampling receiver capable of capturing signals in multiple bands. In a wideband RF sampling implementation, the analog-to-digital converter (ADC) sampling rate dictates the maximum bandwidth captured. When dealing with multiple bands, the useful information is located within their respective bands. The spectrum outside of those bands does not contain useful information. In fact, it may contain unwanted interference that needs to be filtered out. This reference design showcases the ADC32RF80 telecom receiver, which includes two digital down converters (DDC) per channel. Each DDC includes decimation filters and a numerically controlled oscillator (NCO) to extract the useful signal in separate bands.

1.1 ADC32RF80

The ADC32RF80 is a dual-channel telecom receiver. It includes a 14-bit, 3-GSPS ADC with built-in decimation. It has a 3-dB input bandwidth of 3 GHz and is usable up to 4 GHz. The ADC32RF80 employs two DDCs per channel. Each DDC incorporates decimation from 8 to 32 and an independent 16-bit NCO to support multi-band applications.

The ADC32RF80 supports the JESD204B serial interface with data rates up to 12.0 Gbps using up to four lanes per ADC. The device input is buffered with an on-chip 50-Ω differential termination.

1.2 LMK04828

The LMK04828 is a dual-PLL jitter cleaner and clock generator. An onboard 122.88-MHz VCXO provides the reference frequency. This can be locked to an external 10-MHz reference if desired. The LMK04828 supplies the JESD204B SYSREF clocks to the ADC and FPGA and passes the 122.88-MHz reference signal to the LMX2582 for its reference.

1.3 LMX2582

The LMX2582 is a wideband RF synthesizer with a range from 20 to 5500 MHz. It has extremely low-phase noise performance, which is critical for RF sampling ADCs. The phase noise at a 3-GHz output at 1-MHz offset is –140 dBc/Hz. This performance rivals that of bench test equipment. The LMX2582 receives its reference frequency of 122.88 MHz from the LMK04828. The LMX2582 is programmed to 2949.12 MHz and its output feeds the ADC32RF80 clock input.

2 Block Diagram

The block diagram of the ADC32RF80 EVM reference design is shown in Figure 1.
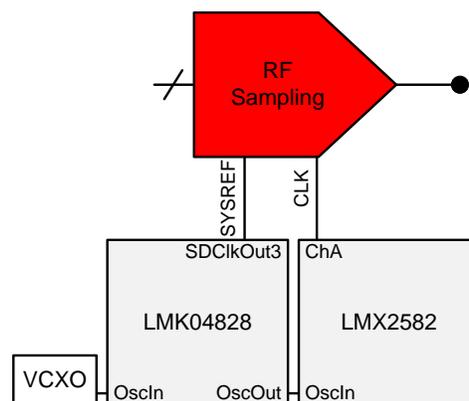
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Figure 1. ADC32RF80 EVM Block Diagram

3 Test Setup

3.1 Test Configuration

The ADC32RF80 EVM connects to the TSW14J56 EVM capture card as seen in Figure 2. The TSW14J56 interfaces with HSDC Pro software for analyzing the captured patterns.
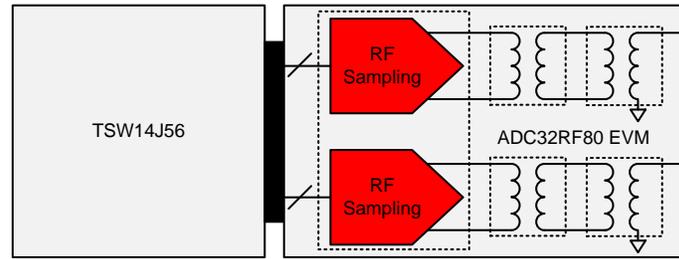

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Figure 2. ADC32RF80 EVM Test Setup

3.2 Input Test Signal

The input test signal is shown in Figure 3. The signal has one 20-MHz LTE carrier centered at 1950 MHz, which is the center of the UMTS receive band. There is a second 20-MHz LTE carrier centered at 2650 MHz. A third signal is centered at 2300 MHz. This signal represents an unwanted interferer that has similar power levels to the desired signals.
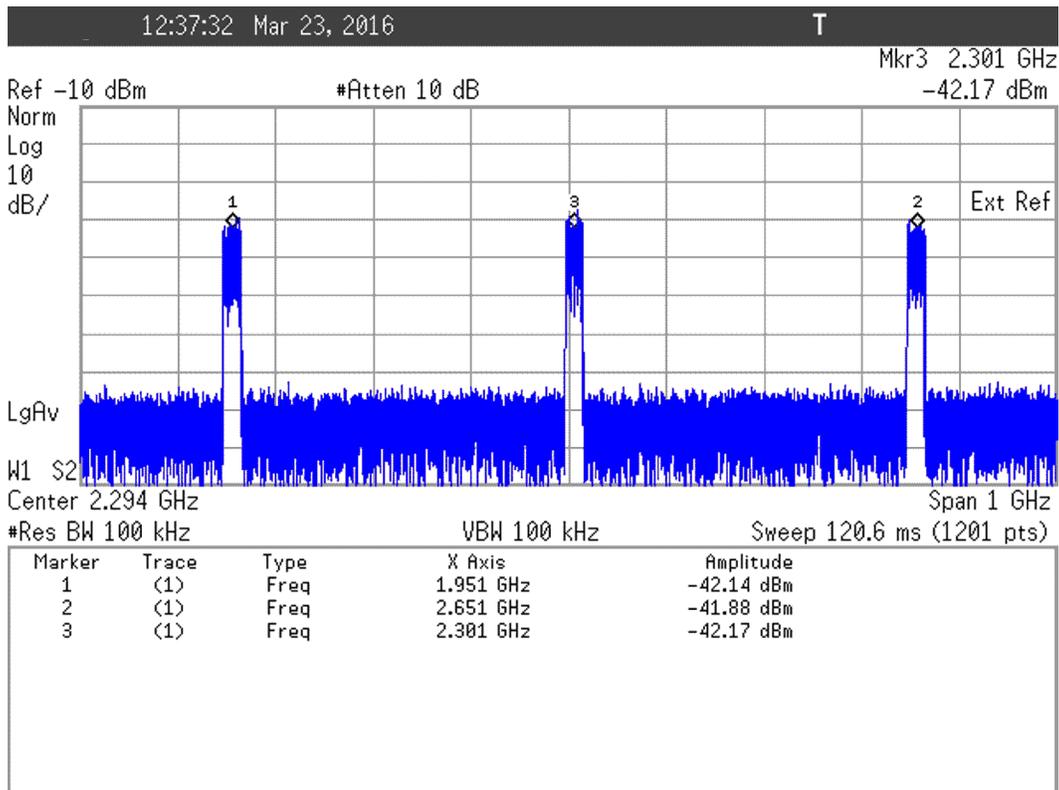
Figure 3. Multi-Band Input Signal With Interferer

3.3 ADC32RF80 EVM GUI Setup

The ADC32RF80 EVM is set in a decimate-by-16 mode. The clock rate is 2949.12 MHz. The output data rate is 184.32 MHz (2949.12 / 16). The complex output Nyquist rate is 184.32 MHz, which is plenty wide for a 20-MHz LTE carrier.

The LMK04828 is programmed to a clock rate of 2949.12 MHz to support the necessary SYSREF signals to the ADC32RF80. The LMX2582 is also programmed to an output frequency of 2949.12 MHz for the ADC clock. The ADC32RF80 uses the configuration file "ADC32RF80_16xIQ_lmfs8821" to load the registers for decimate-by-16 in a complex output.

Each NCO is set to mix the RF input signal down to the digital baseband. One NCO is set to 1950-MHz and the other is set to 2650 MHz. Note the ADC32RF80 only has a 16-bit NCO; hence, the exact desired frequency values are not achievable. For these tests, the closest achievable frequencies were used. Figure 4 illustrates the DDC tab of the ADC32RFxx GUI software where the user sets the decimation and NCO frequencies.
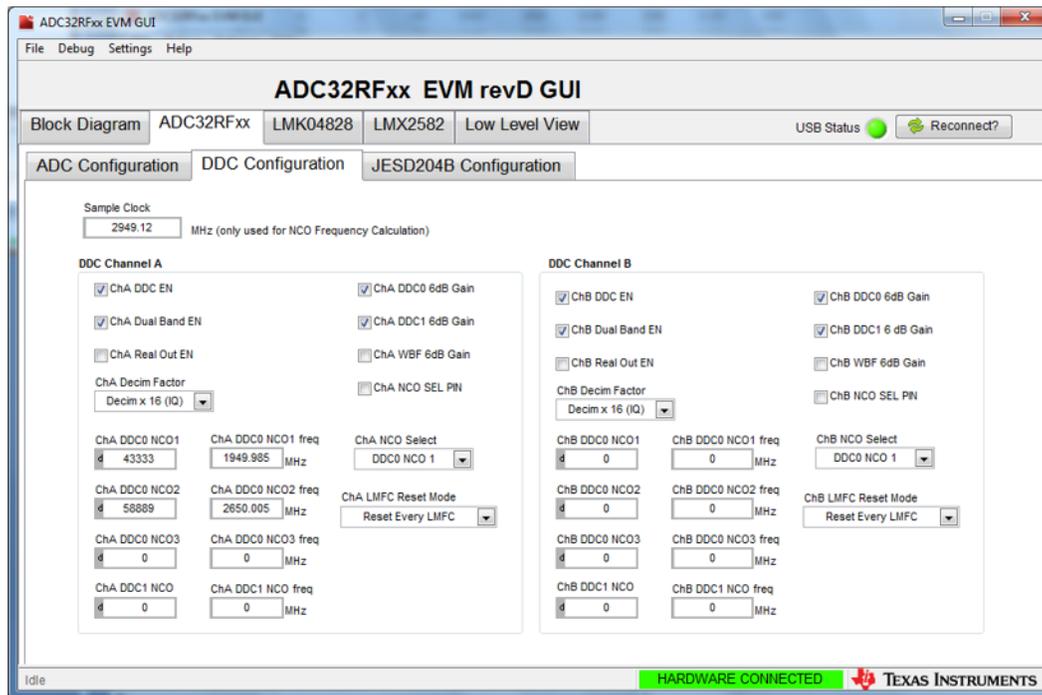
Figure 4. ADC32RFxx DDC Setup Tab

3.4 HSDC Pro Setup

The HSDC Pro software interfaces with the TSW14J56 to capture and analyze the digital data from the ADC32RF80. Set the ini file to "ADC32RF80_LMF_8821" to match the ADC serialized output configuration. Since the DDC is activated, the normal ADC calculations must be modified for the digital mixing function. The gear selector next to the ADC Output Data Rate box brings up a pop-up window to input the NCO and decimation parameters. Figure 5 shows the parameter setting for each carrier. The clock rate is set to 2.94912 GHz. The ADC input frequency is set to 2.65 GHz and 1.95 GHz, respectively. The NCO is set to the same value of the NCO setting in the ADC32RFxx software. Notice the actual number is not exact because of the resolution limitation of the 16-bit NCO. The decimation value is set to 16.
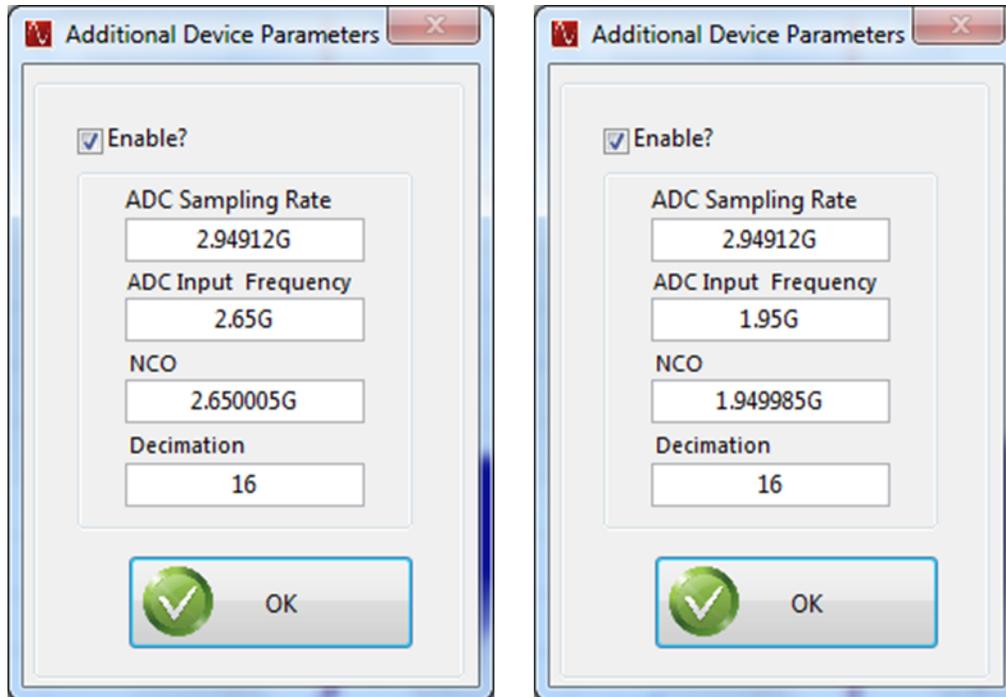
Figure 5. DDC Parameter Setup in HSDC Pro

The ADC32RF80 is a dual-channel device, but because each channel contains two complex (I/Q) down converters, the number of effective converters is eight. This is why the "M" JESD204B parameter, which designates the number of converters, is set to eight. Each carrier resides on a pair (I/Q) of effective channels. In this case, the 1950-MHz carrier is on channel 1 or 2 and the 2.65-GHz carrier is on channel 3 or 4.

4   Measured Performance

The captured patterns in each of the channels are shown in Figure 6. The 20-MHz carrier is down-converted to 0 Hz. The solution has properly captured the signals at the 1950-MHz and 2650-MHz bands. The interferer at 2300 MHz is filtered out. The power of the 1950-MHz carrier is about –30 dBFS; the power of the 2650-MHz carrier is about –35 dBFS. The difference is power level between the carriers is due partly by the roll-off of the source power and partly by the bandwidth roll-off of the ADC32RF80 input due to higher frequencies.

Notice the noise floor rolls off at the band edges. This is due to the decimation filter. The decimation filters limit usable output bandwidth to about 90% of the total available. In this example, the decimate by 16 supports a maximum signal bandwidth of about 165 MHz. The noise floor for each capture is less than –110 dBFs. Part of the noise floor contribution comes from broadband noise in the source. The decimation filter limits the out-of-band noise from folding back within the captured spectrum, so there is an improvement in overall signal-to-noise ratio (SNR). With higher decimation values, the noise contribution decreases as does the bandwidth capability.
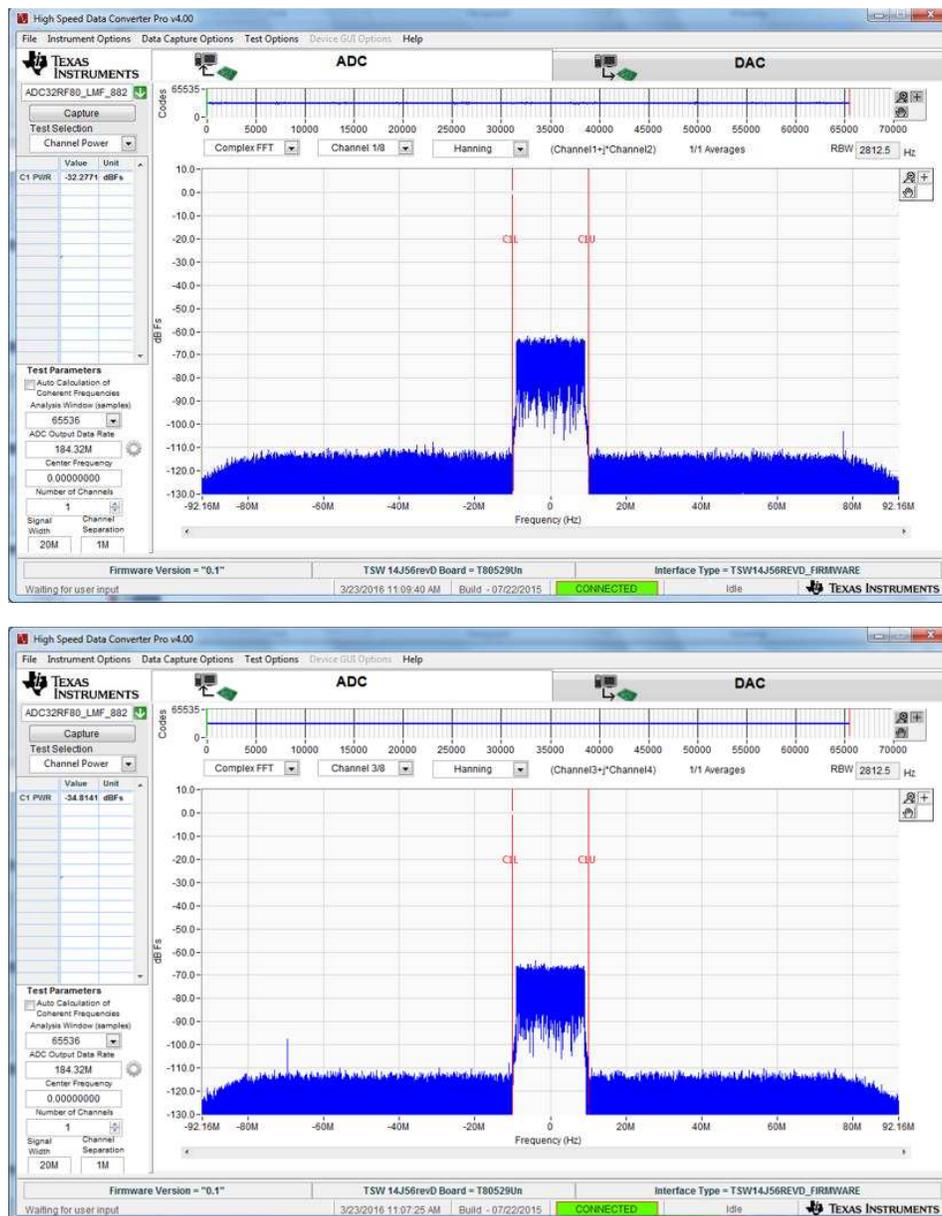
Figure 6. DDC Outputs From 1950-MHz and 2650-MHz Bands

5 Conclusion

The ADC32RF80 operates with multi-band signals. It is effective at capturing desired signals from separate bands and filtering out unwanted interference in other parts of the spectrum. With the decimation filtering, the noise bandwidth is reduced without impacting signal level. This improves SNR performance by a factor of: 10log(Decimation). The DDC allows lower output data rate, band filtering, and improved SNR.

6 Design Files

6.1 Schematics

To download the schematics, see the design files at TIDA-01163.

6.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01163.

6.3 PCB Design Files

To download the PCB design files, see the design files at TIDA-01163.

7 Software Files

To download the software files, see the design files at TIDA-01163.

8 About the Author

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