TI Designs

Data Concentrator Reference Design for Smaller AMI Networks Reduces Infrastructure Cost

Description

This design implements a lightweight powerline communication (PLC) data concentrator (DC) solution integrated with an Ethernet repeater feature. A power grid network is static, which means that once the end nodes are installed the number of nodes to be supported by a DC is fixed. Electric utilities often have many feeder lines with a small number of end consumers. It is not cost-effective to install a high-performance DC solution capable of supporting a large number of end nodes for these feeders. This design offers a low-cost PLC DC solution to support smaller networks with an Ethernet repeater (or edge router) feature to interconnect the local PLC network to an Ethernet-based backbone network so that a control center can control the PLC end-nodes directly.

Resources

TIDM-MINI-DC	Design Folder
TM4C1294NCPDT	Product Folder
TMS320F28375S	Product Folder
AFE032	Product Folder
EK-TM4C1294XL	Tools Folder
TIDM-SOMPLC-FCC	Tools Folder
TI-PLC-G3-FCC-SN	Tools Folder

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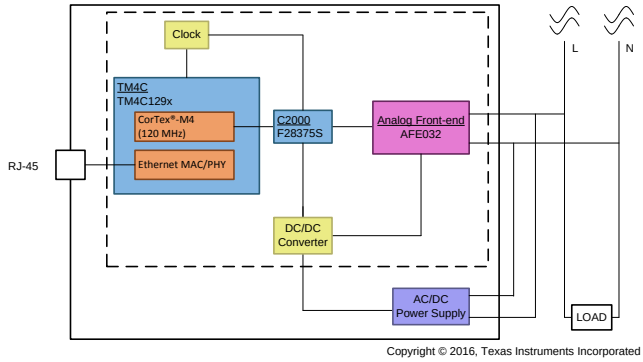
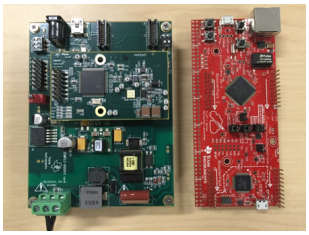
Features

- Supports a Network up to 32 Nodes With Lightweight Data Concentrator Solution Using Same Platform as PLC Service Nodes
- Extends Network Coverage With PLC and Ethernet Repeater (or Edge Router) Feature Interconnecting Ethernet and PLC Networks
- TM4C1294 is Single-Chip Microcontroller (MCU) Device Integrated with Ethernet MAC and PHY
- Supports Both CENELEC-A and FCC Frequency Bands With Mini-DC Solution Based on TMS320F28375S and AFE032

Applications

- Ethernet Repeater
- Data Concentrator
- Power Line Communications





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1 System Overview

1.1 System Description

This design provides a low-cost power line communication (PLC) data concentrator (DC) solution integrated with Ethernet repeater feature. This design is built on top of the existing TI PLC solution capable of running as mini-DC supporting a small number (up to 32 nodes) of PLC end nodes. By virtue of TM4C1294 MCU integrated with Ethernet MAC and PHY (10 and 100 Mbps), this design covers PLC and Ethernet repeater feature, an essential technology in the gateway design in smart grid networks, which allows interconnection between the local PLC network to an Ethernet-based backbone network so that the system operator control center in the backbone network can control and monitor PLC end nodes directly. Another advantage is improved network coverage by using Ethernet communication across transformers at distribution substations or other locations in the smart grid. Transitioning PLC data onto an Ethernet network can also help in high-rise building environments where there is often significant background noise, interference, and attenuation on the PLC networks.

Figure 1 shows the system architecture. The ARM® Cortex®-M4 processor in the TM4C1294 MCU is the core running the Ethernet and PLC repeater application as well as the communication drivers for the Ethernet and PLC. For the system design, the TM4C1294 MCU connects to the C2000 PLC MCU through universal asynchronous receiver/transmitter (UART). The PLC MCU is loaded with the G3-PLC stacks. The PLC communication driver in the Cortex-M4 configures the G3-PLC stacks as mini-DC. The Ethernet and PLC repeater application is running on top of Ethernet and PLC communication drivers, and the primary task is to convert frame formats before transmitting over each network and interconnecting PLC and Ethernet networks by forwarding incoming frames from one network to the another network.

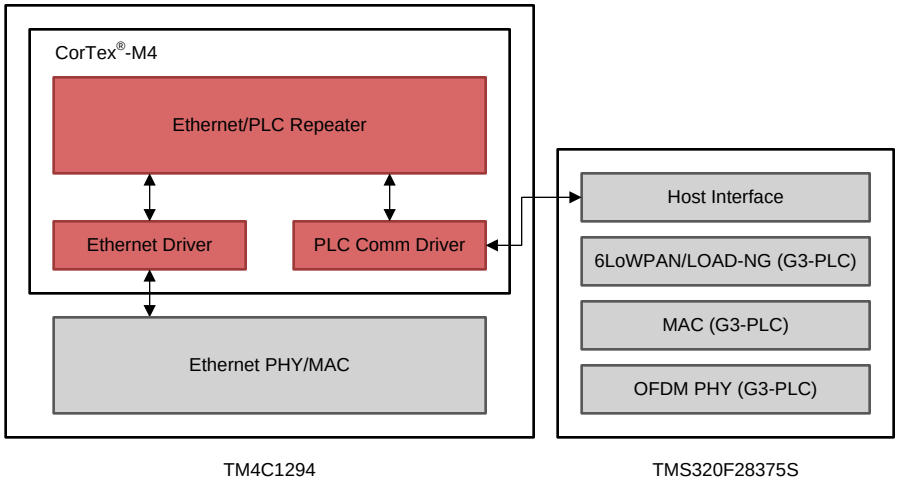

Figure 1. System Architecture

1.2 Block Diagram

Figure 2 shows the block diagram. The primary devices for this design are the TM4C1294NCPDT (or TM4C1294KCPDT with smaller flash of 512KB), TMS320F28375S, and AFE032. The TM4C1294x includes ARM Cortex-M4 used for applications and Ethernet and PLC drivers. The TMS320F28375S with AFE032 (PLC analog front-end) is for PLC. The AC-DC power supply unit (PSU) subsystem is not covered in this TI Design but is a key subsystem for end products, which will be discussed in Section 1.3.4.

For this design, these devices were chosen due to:

- The TM4C1294x integrates 10- and 100-MB Ethernet MAC+PHY with a powerful 120-MHz 32-bit ARM Cortex-M4F MCU and sufficient peripheral options.
- The TMS320F28375S provides optimized PLC OFDM performance with VCU-II and allows programmable flexible PLC design upgradable to different PLC solutions without hardware modification. Additionally, this device can support both CENELEC-A and FCC bands.

- AFE032 analog front-end to provide high reliability in PLC applications by monolithic integrated circuit with thermal and overcurrent protection, and to support frequency bands up to 500 kHz.

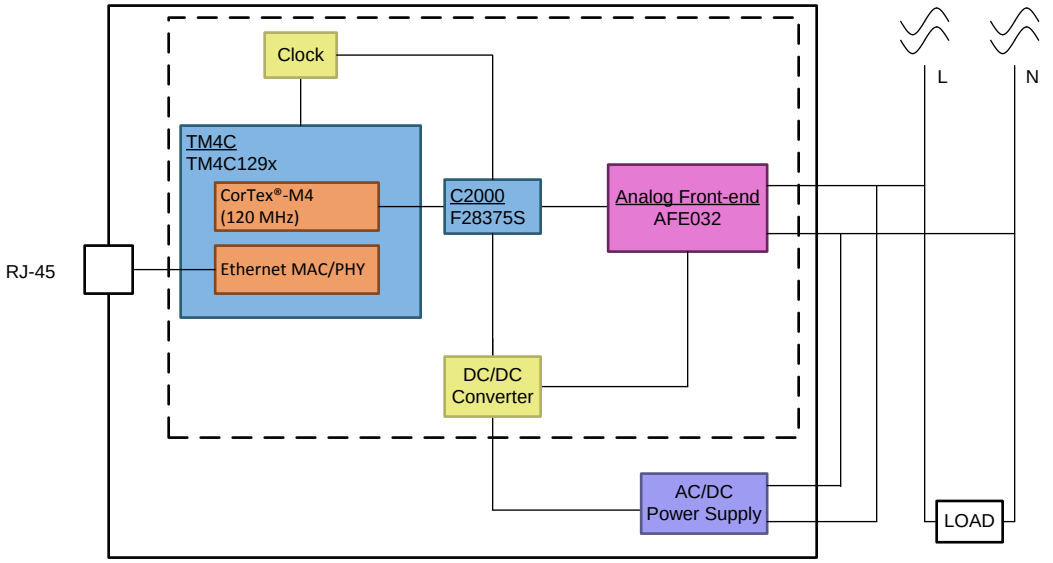

Figure 2. Block Diagram

1.3 Highlighted Products

1.3.1 TM4C1294x

Tiva™ ARM® C-Series MCUs integrate a large variety of rich communication features to enable a new class of highly connected designs with the ability to allow critical, real-time control between performance and power. The MCUs feature integrated communication peripherals along with other high-performance analog and digital functions to offer a strong foundation for many different target uses, spanning from human machine interface to networked system management controllers.

In addition, Tiva ARM C-Series MCUs offer the advantages of ARM's widely available development tools, system-on-chip (SoC) infrastructure, and a large user community. Additionally, these MCUs use ARM's Thumb®-compatible Thumb-2 instruction set to reduce memory requirements, which also lowers the cost. Finally, the TM4C1294NCPDT MCU is code-compatible to all members of the extensive Tiva C-Series, which provides flexibility to fit precise requirements. Figure 3 shows a high-level block diagram of the TM4C1294NCPDT MCU.

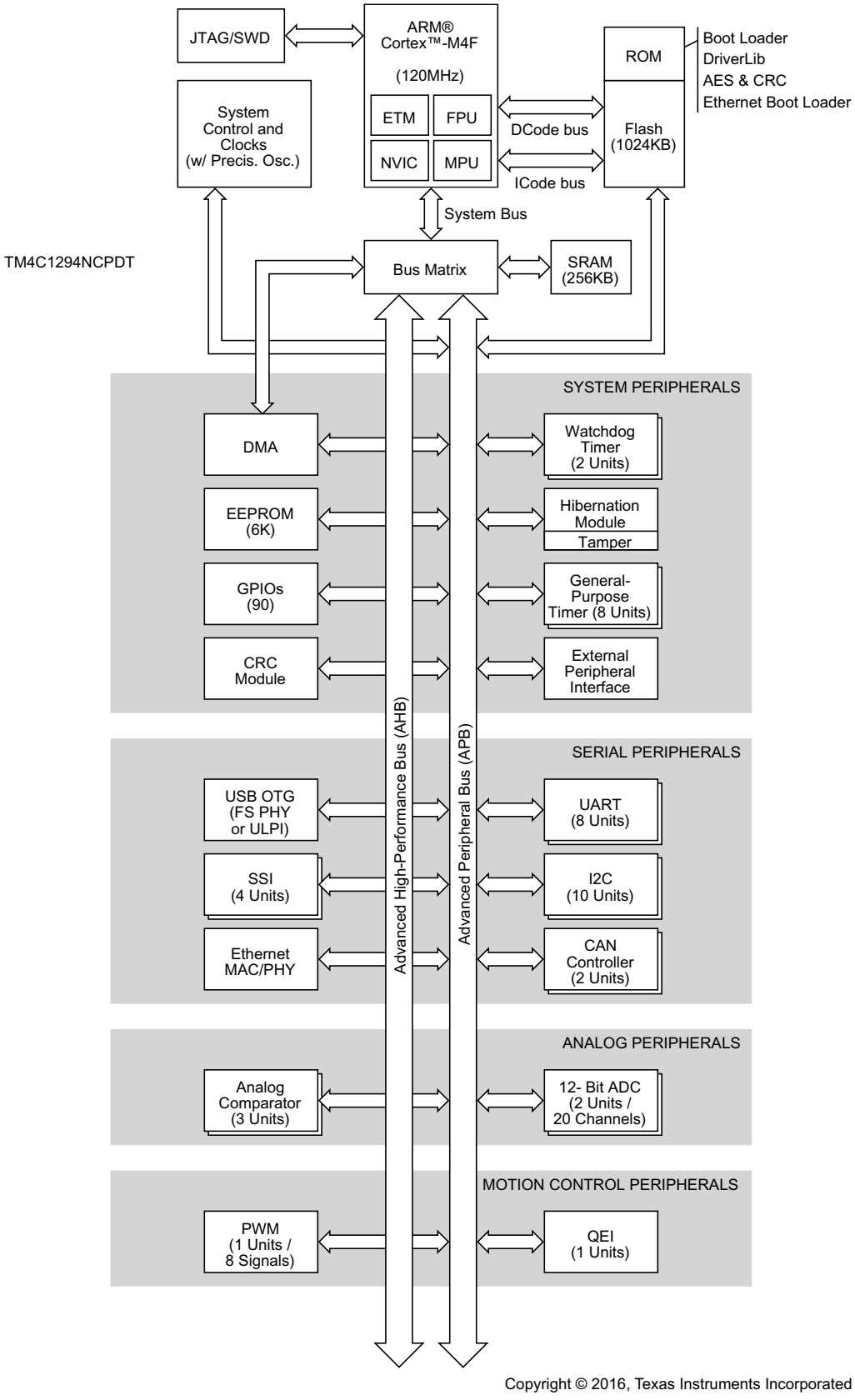

Figure 3. TM4C1294NCPDT MCU High-Level Block Diagram

1.3.1.1 ARM® Cortex®-M4F Processor

The ARM Cortex-M4F processor is built on a high-performance processor core with a three-stage pipeline Harvard architecture, which makes it ideal for demanding embedded applications. The processor delivers exceptional power efficiency through an efficient instruction set and extensively optimized design, which provides high-end processing hardware including IEEE754-compliant single-precision floating-point computation, a range of single-cycle and SIMD multiplication and multiply-with-accumulate capabilities, saturating arithmetic, and dedicated hardware division. To facilitate the design of cost-sensitive devices, the Cortex-M4F processor implements tightly coupled system components that reduce processor area while significantly improving interrupt handling and system debug capabilities. The Cortex-M4F processor implements a version of the Thumb instruction set based on Thumb-2 technology, which ensures high code density and reduced program memory requirements. The Cortex-M4F instruction set provides the exceptional performance expected of a modern 32-bit architecture, with the high-code density of 8-bit and 16-bit MCUs. The Cortex-M4F processor closely integrates a nested interrupt controller (NVIC), to deliver industry-leading interrupt performance. The TM4C1294NCPDT NVIC includes a non-maskable interrupt (NMI) and provides eight interrupt priority levels. The tight integration of the processor core and NVIC provides fast execution of interrupt service routines (ISRs), dramatically reducing interrupt latency. The hardware stacking of registers and the ability to suspend load-multiple and store-multiple operations further reduce interrupt latency. Interrupt handlers do not require any assembler stubs which remove code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another. To optimize low-power designs, the NVIC integrates with the sleep modes, including deep-sleep mode, which enables the entire device to be rapidly powered down.

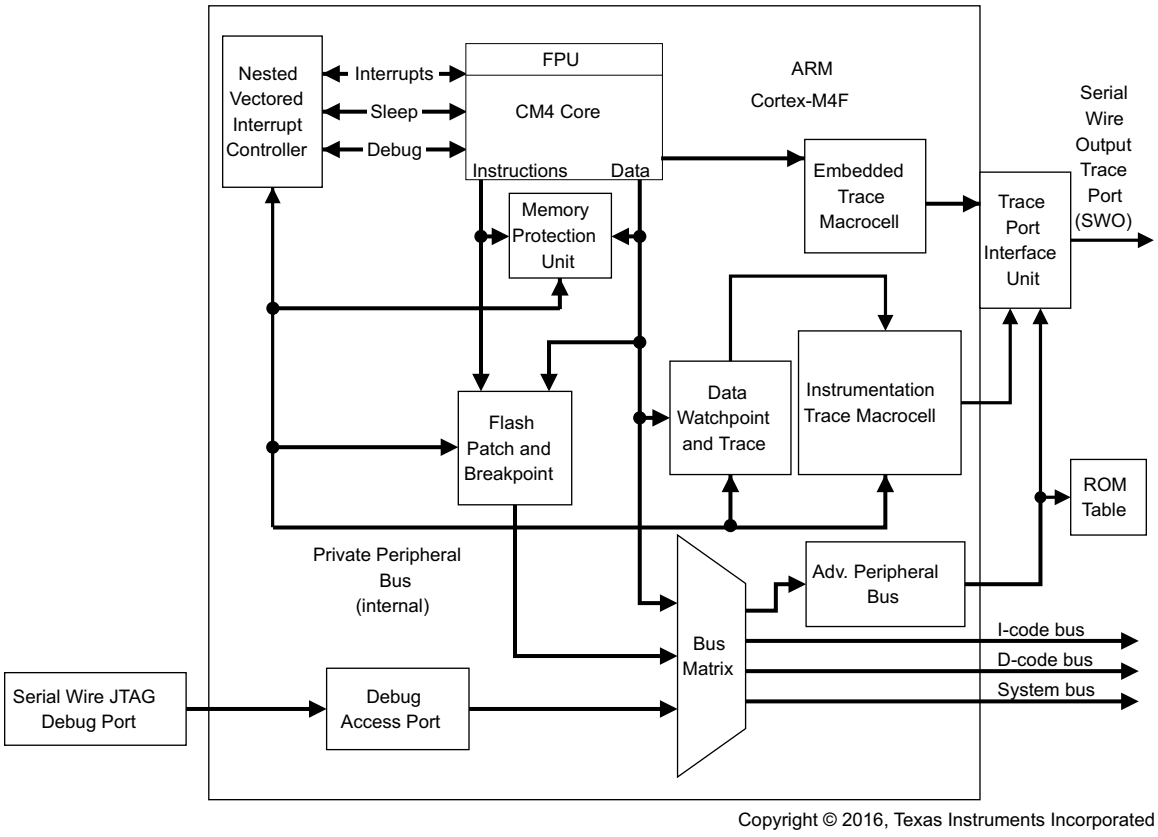

Figure 4. CPU Block Diagram

1.3.1.2 Ethernet Controller

Figure 5 shows the block diagram of the Ethernet MAC with an integrated PHY interface.

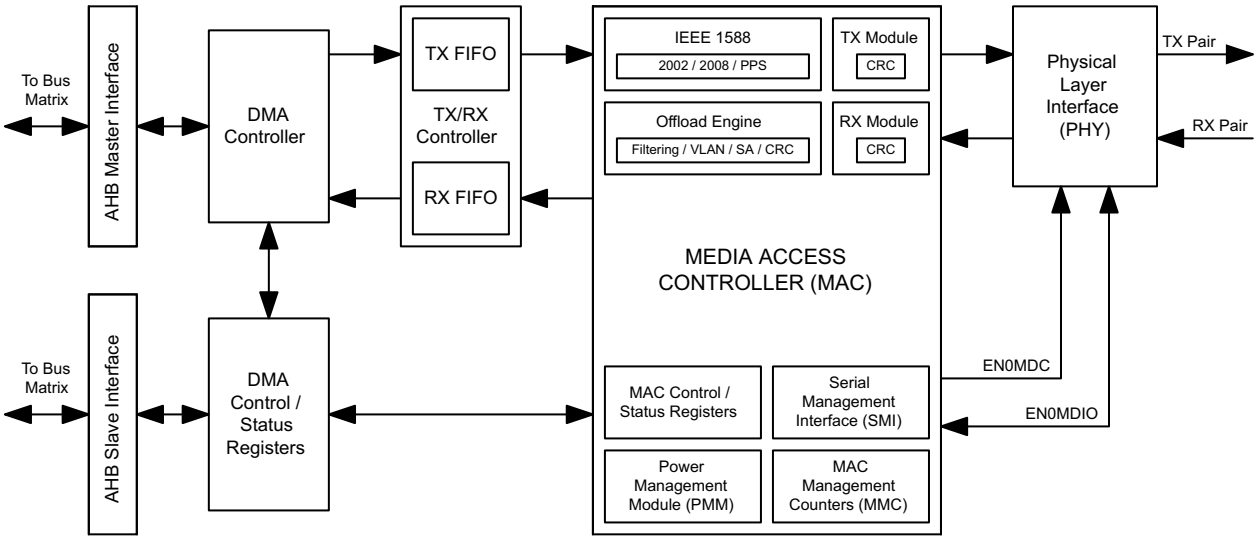

Figure 5. Ethernet MAC With Integrated PHY Interface

1.3.2 TMS320F28375S

The Delfino™ TMS320F2837xS is a powerful 32-bit floating-point MCU designed for advanced closed-loop control applications such as industrial drives and servo motor control, solar inverters and converters, digital power, transportation, and power line communications. Complete development packages for digital power and industrial drives are available as part of the powerSUITE and DesignDRIVE initiatives.

The real-time control subsystem is based on TI's 32-bit C28x floating-point CPU, which provides 200 MHz of signal processing performance. The C28x CPU is further boosted by the new TMU accelerator, which enables fast execution of algorithms with trigonometric operations common in transforms and torque loop calculations, and the VCU accelerator, which reduces the time for complex math operations common in encoded applications.

The F2837xS MCU family features a CLA real-time control coprocessor. The CLA is an independent 32-bit floating-point processor that runs at the same speed as the main CPU. The CLA responds to peripheral triggers and executes code concurrently with the main C28x CPU. This parallel-processing capability can effectively double the computational performance of a real-time control system. By using the CLA to service time-critical functions, the main C28x CPU is free to perform other tasks, such as communications and diagnostics.

The TMS320F2837xS supports up to 1MB (512KW) of onboard flash memory with error correction code (ECC) and up to 164KB (82KW) of SRAM. Two 128-bit secure zones are also available on the CPU for code protection.

Performance analog and control peripherals are also integrated on the F2837xS MCU to further enable system consolidation. Four independent 16-bit ADCs provide precise and efficient management of multiple analog signals, which ultimately boosts system throughput. The new sigma-delta filter module (SDFM) works in conjunction with the sigma-delta modulator to enable isolated current shunt measurements. The comparator subsystem (CMPSS) with windowed comparators allows for protection of power stages when current limit conditions are exceeded or not met. Other analog and control peripherals include DACs, PWMs, eCAPs, eQEPs, and other peripherals.

Peripherals such as EMIFs, CAN modules (ISO11898-1 and CAN 2.0B-compliant), and a new uPP interface extend the connectivity of the F2837xS. The uPP interface is a new feature of the C2000™ MCUs and supports high-speed parallel connection to field programmable gate arrays (FPGAs) or other processors with similar uPP interfaces. Lastly, a USB 2.0 port with MAC and PHY lets users easily add universal serial bus (USB) connectivity to their application. Figure 6 shows the CPU system and associated peripherals.

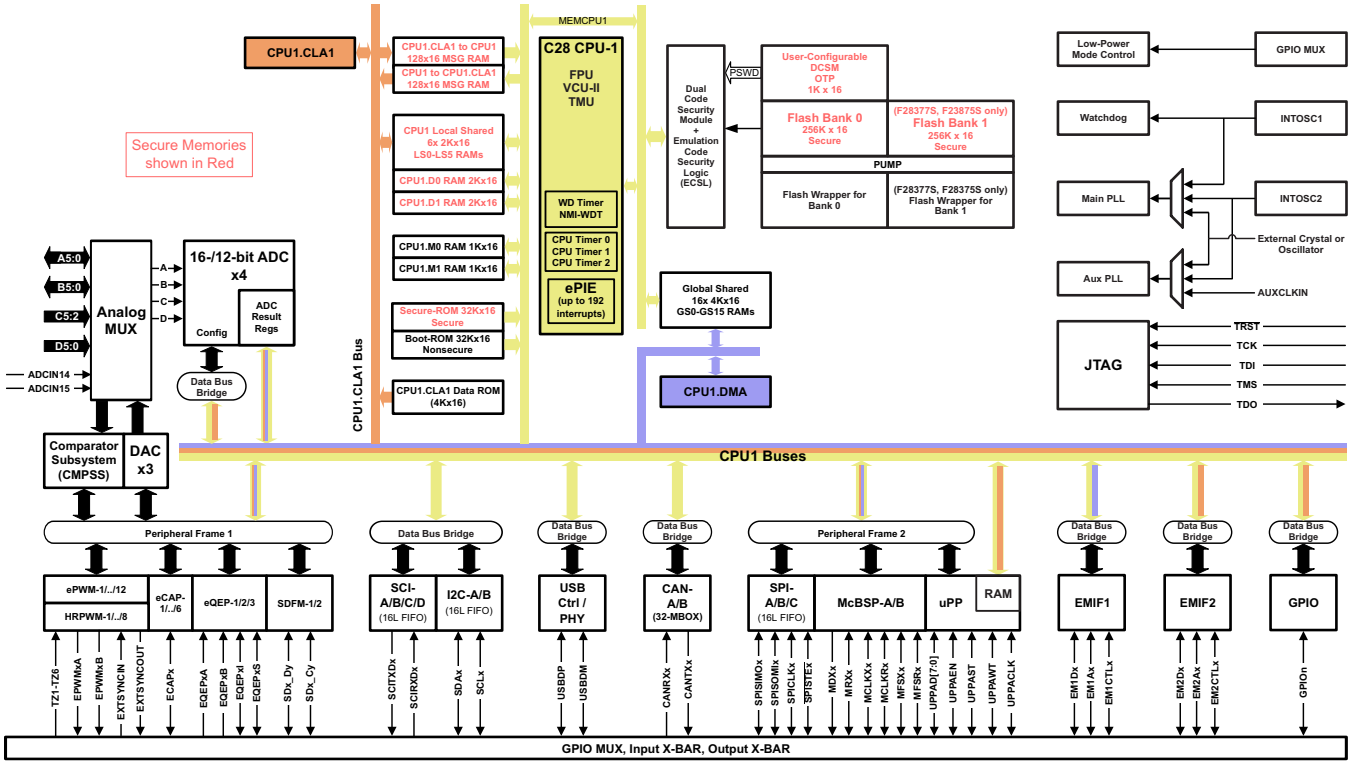

Figure 6. Functional Block Diagram

1.3.3 AFE032

The AFE032 is a low-cost, integrated, power-line communications (PLC), and analog front end (AFE) device capable of transformer-coupled connections to the power-line while under the control of a digital signal processor (DSP) or MCU. This device is ideal for driving high-current, low-impedance lines up to 1.9 A into reactive loads.

The integrated receiver is able to detect signals down to 10 μV_{RMS} (G3-FCC mode) and is capable of a wide range of gain options to adapt to varying input-signal conditions. The monolithic integrated circuit provides high reliability in demanding power-line communication applications. The AFE032 transmit power amplifier operates from a single supply in the range of 7 to 24 V. At typical load current (I_{OUT} = 1.5 A_{PEAK}), a wide output swing provides a 12-V_{PP} capability with a nominal 15-V supply.

The device is internally-protected against overtemperature and short-circuit conditions. The device also provides a selectable current limit. An interrupt output is provided, which indicates current limit, thermal limit, and undervoltage. A shutdown pin is also available, which can quickly place the overcurrent protection device into the lowest-power state. Each functional block can be enabled or disabled to optimize power dissipation through the serial peripheral interface (SPI).

The AFE032 is housed in a thermally-enhanced, surface-mount PowerPAD™ QFN-48 package. Operation is specified over the extended industrial junction temperature range of –40°C to 125°C. Figure 7 shows the functional block diagram.

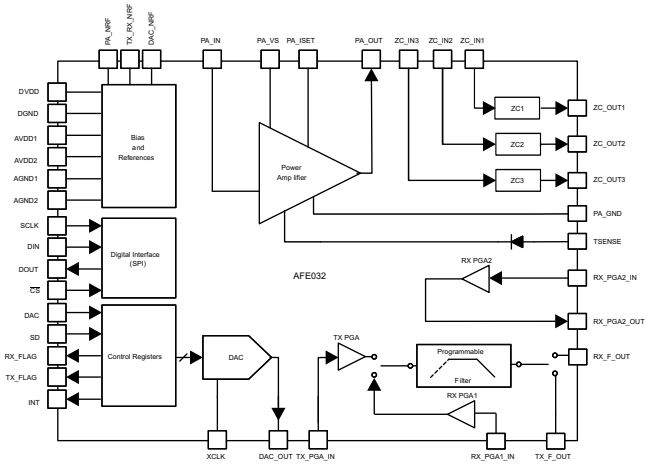

Figure 7. AFE032 Functional Block Diagram

1.3.4 AC-DC Power Supply Unit (PMP7146)

The PMP7146 reference power supply design is to convert AC to DC power to feed to digital devices on end-product design. The PMP7146 design offers various DC output power options and, depending on the power levels applicable to the end-product, the AC-DC power supply design can be easily modified. Additionally, this design considers PLC performance in terms of the operating frequency for the switching parts of the power supply that should not fall into the PLC frequency bands, the main filter design of the PSU that should not attenuate the PLC signal, and sufficient power supply to the PLC modem in low-impedance condition.

The key ICs composed of the PSU design are the LM5021-2, TPS54040, TPS76933, and TPS62260. The details of the power supply unit (PSU) design such as the BOM, design files, and test results can be found in the PMP7146 reference design.

2 System Design Theory

Several considerations were taken into account when defining this design with the main focus on all of the followings:

- Low system design cost with mini-DC feature support
- To support mini-DC features over universal PLC frequency bands (CENELEC-A and FCC)

2.1 System Cost

This design targets at support mini-DC feature in small networks with lower cost compared to the high-performance DC reference design (TIDEP0006). The TM4C1294x ARM Cortex-M4F MCU integrated with Ethernet MAC and PHY reduces the total bill of materials (BOM) cost because it does not require Ethernet PHY, external flash, memory, and power management IC. The TM4C1294NCPDT is the MCU used for this design but depending on end-product flash requirement, the system cost can be lower by selecting pin-to-pin compatible TM4C1294KCPDT (with 512-KB flash and 256-KB SRAM). In addition, the TM4C1294x MCU supports enough external interfaces, which makes easy to extend the design to support additional communications, sensors and so on.

2.2 Mini-DC Features Support

The TMS320F28375S is the MCU that supports mini-DC feature over CENELEC-A and FCC frequency bands. The PLC firmware loaded on the MCU can be configured to run as mini-DC. The AFE032 is an analog front-end for PLC that supports up to 500 kHz frequency bands, which is required to support FCC frequency band.

3 Getting Started Hardware and Software

3.1 Hardware

The TIDM-MINI-DC design is built with two standard EVMs: EK-TM4C1294XL (Figure 8) and TIDM-SOMPLC-FCC (Figure 9). To run PLC for this design, plug in the TIDMSOMPLC-FCC SOM module on a PLC docking board. The docking board can be separately obtained by purchasing TMDSPLCKITV4-ARIB or TMDSPLCKITV4-CEN and replacing the SOM with the TIDMSOMPLC-FCC. The TMDSPLCKITV4 is shown in Figure 10.

To run the demonstration described in Section 4 requires having two EK-TM4C1294XL EVMs, two TIDM-SOMPLC-FCC SOMs, and two PLC docking boards. Table 1 summarizes the required EVMs to purchase.

Table 1. EVMs for Demonstration

EVM	QUANTITY	NOTE
EK-TM4C1294XL	2	-
TIDM-SOMPLC-FCC	2	-
TMDSPLCKITV4-ARIB (or TMDSPLCKITV4-CEN)	1	A single kit includes two modems (docking boards)

Figure 8. EK-TM4C1294XL

Figure 9. TIDM-SOMPLC-FCC

Figure 10. TMDSPLCKITV4 EVM

3.1.1 Hardware Configuration

The TIDM-MINI-DC design is based on two standard EVMs. The design requires UART connection between the EK-TM4C1294XL and TMDSPLCKITV4 EVM: UART_TX, UART_RX, and GND, which is for PLC communication between host application and PLC modem. There are multiple UART pin connection options in the EVMs but Figure 11 shows a working example. The M3:P2-12 (PLC_SCIA_TX) pin is connected to X1-12 (UART RX) in the EK-TM4C1294XL EVM, and M3:P2-14 (PLC_SCIA_RX) to X1-14 (UART TX) in the EK-TM4C1294XL EVM. One of the GND pins on J2 in TMDSPLCKITV4 EVM, shown in Figure 11, is connected to TP14 in EK-TM4C1294XL.

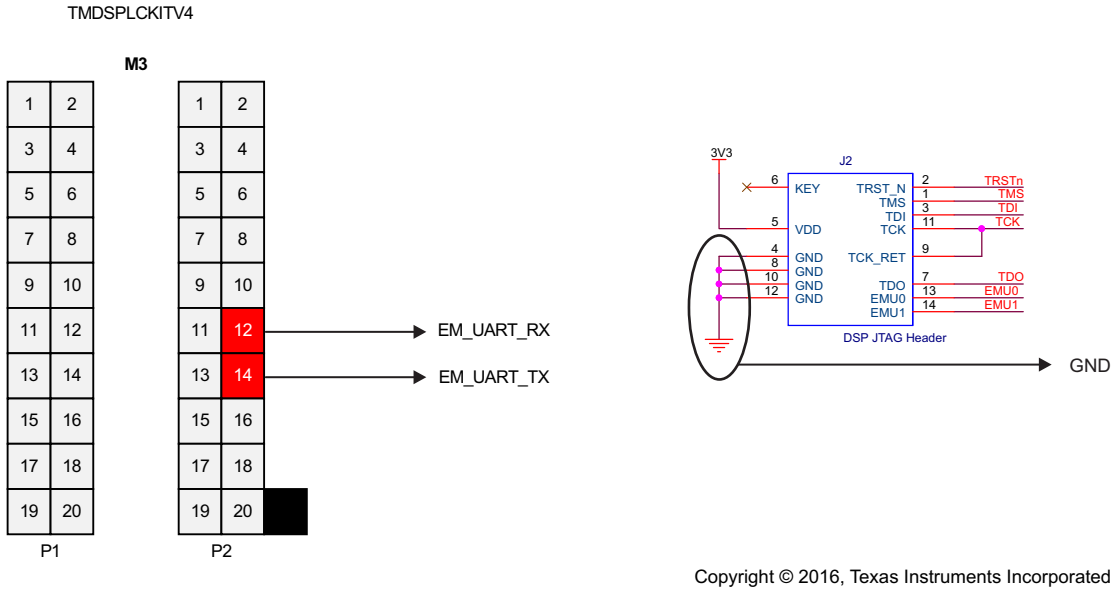

Figure 11. Working Example: UART Connection Between TMDSPLCKITV4 and EK-TM4C1294XL

As shown in Figure 12, additional configuration change is SW2 position to OFF. Turning off the SW2 blocks UART communication with the mini-USB port in TMDSPLCKITV4. Thus, it allows the TMDSPLCKITV4 EVM to have the UART connection to the external devices through the M3 module (shown in Figure 11) only.

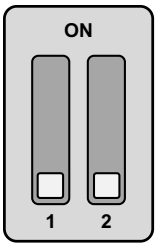

Figure 12. SW2 Position in TMDSPLCKITV4 EVM

3.2 Software

This TI design provides a Code Composer Studio™ (CCS) software example (*TI_Mini_Data_Concentrator_Example*) including Ethernet repeater application, Ethernet driver, and PLC host driver. This section covers details of the example software architecture and is followed by how to build and flash the CCS project.

The prerequisite to build the software example is to install CCS v6.1.2 (or above) with the software update (select *Help → Check for Updates* in the CCS top menu) and TivaC TI-RTOS v2.16.0.08 (TI-RTOS-MCU). The TI-RTOS version to be installed can be checked in the RTSC menu (right click on the example CCS project and then property → *General*) as shown in Figure 13. Once installed, the TI-RTOS for TivaC examples can be found by selecting *View → Resource Explorer*. The *Mini_Data_Concentrator_Example* CCS project was built upon the reference examples of *uartecho_EK_TM4C1294XL* (under *UART examples*) and *udpEchoIPv6_EK_TM4C1294XL* CCS projects (under *Ethernet examples*) in the directory of the EK-TM4C1294XL evaluation kit. Figure 14 shows snapshot of the example projects on CCS.

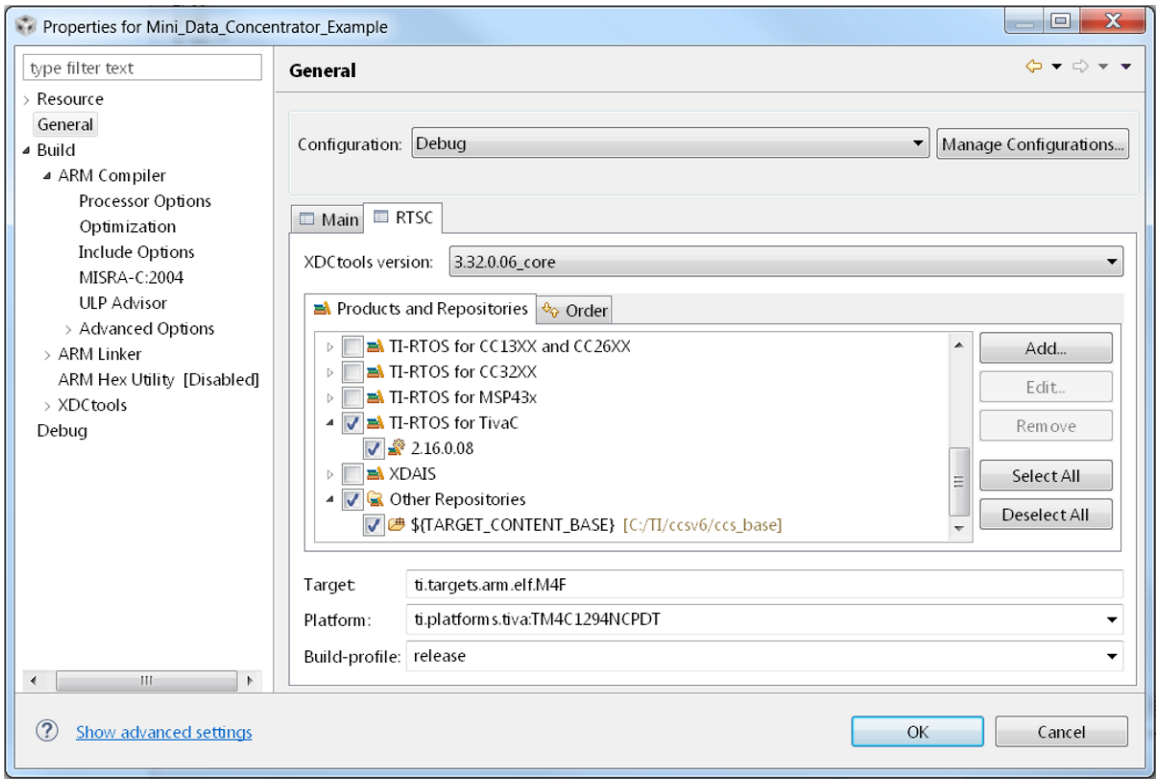

Figure 13. CCS™ Property for Mini_Data_Concentrator_Example

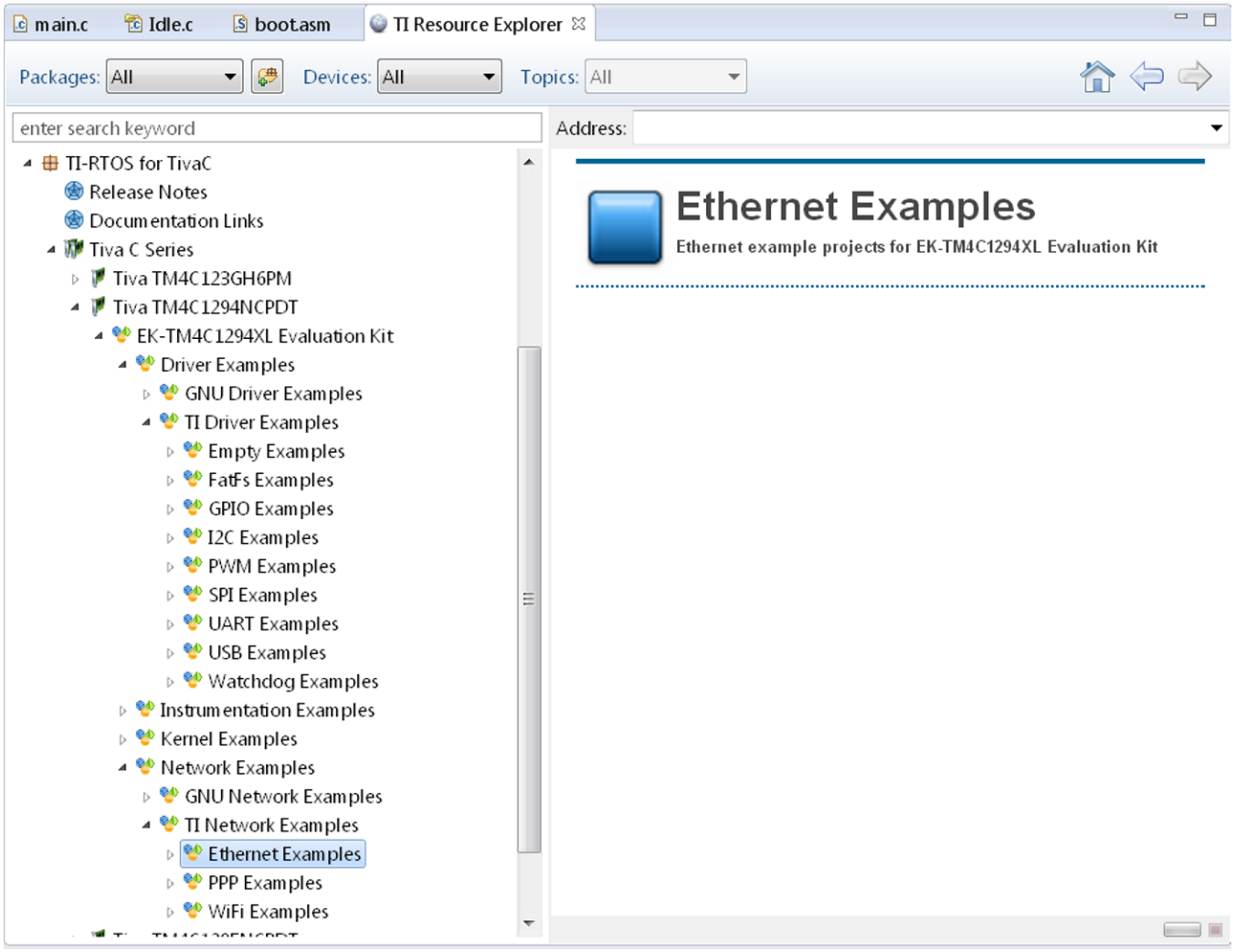

Figure 14. Ethernet Example Project in CCS™ TI Resource Explorer

3.2.1 The Mini_Data_Concentrator Example

The CCS project provided acts as a working example that can be baseline software for end-product development. Note that the example software does not consider optimizing software in terms of performance, code size, and memory usage.

The example runs based on TI-RTOS in the ARM Cortex-M4 core. For PLC, the host driver is built to work with the G3-PLC system in the F28375S DSP. The default configuration is FCC frequency band, TMR (*Tonemap Request*) enabled, and the TX level of 0x20 (maximum). The Ethernet driver reuses most of the network interface management unit (NIMU) and the network developer's kit (NDK) software embedded in the TI-RTOS Ethernet examples but activates Ethernet MAC and PHY stacks only to enable Ethernet and PLC repeater. The default Ethernet PHY configuration is full-duplex at 10 Mbps.

The example project contains two CCS build configurations of *Debug* and *Debug_Test_Server*. The discussion in this Section is mostly for the Debug configuration mode. The example project with *Debug_Test_Server* was created to emulate an Ethernet control center for demonstration purpose only. The details will be discussed in Section 3.2.1.6.

The PLC configuration is set in the *init_plcHanlder()* in *g3_plc.c*. The configuration includes G3-PLC long address, PAN ID, short address, G3-PLC TX and RX parameters, and pre-defined IPv6 and UDP header information. The default FCC frequency band can be switched to CENELEC-A band by changing the variable of *plcHandle.g3ToneMaskSelection* from *TONEMASK_FCC_FULL_BAND* to *TONEMASK_CENELEC_A_36*.

The maximum number of nodes supported by the *Mini_Data_Concentrator_Example* is configured to 32 in *g3_plc.h*. This number of nodes can be also modified to a bigger number if the G3-PLC mini-DC is capable of supporting more nodes. The example project implements the Ethernet repeater application that forwards PLC data through the Ethernet link or vice versa. The overall software architecture consists of five tasks: *uartRxTask*, *PLCStateMachineTask*, *emacTxTask*, *EMAC_handlePackets* (SWI), and *PLCTxTask*.

3.2.1.1 uartRxTask

The *uartRXTask* processes PLC messages received from the PLC modem. The task waits for six-byte PLC message header that contains host message type, payload length, and header CRC. If the CRC passes, the task extracts remaining bytes including payload CRC, payload subheader, and payload. If the payload CRC passes and the message is not application data then the task passes the message to the *PLCStateMachineTask* to update PLC state machine. If the received message is application data, this task copies the data in a static buffer and then signals to *emacTxTask* through the *EmacTxMbox* (mailbox) to forward the data to the Ethernet link.

3.2.1.2 PLCStateMachineTask

The *PLCStateMachineTask* maintains G3-PLC mini-DC state machine. When powered on, the *PLCStateMachine* task initializes G3-PLC modem through host message exchanges with the pre-defined configuration and then starts a G3-PLC network as mini-DC with the predefined PAN ID. Once all steps are complete, the task changes the state machine to NORMAL state, which is ready to send and receive application data. Additionally, this task maintains G3-PLC node entries joined to the network. This example covers basic message sequences to configure C2000 G3-PLC modem and to maintain the G3-PLC node entries.

3.2.1.3 emacTxTask

The *emacTxTask* waits for a mailbox message of *SEND_EMAC_DATA*. Once the task receives the mailbox message from the *uartRxTask*, it prefixes the Ethernet MAC header (source and destination MAC address and the type field of IPv6) to the application data and then sends the frame through the Ethernet link.

3.2.1.4 PLCTxTask

The *PLCTxTask* waits for mailbox messages of *SEND_PLC_DATA* and *RETX_PLC_DATA*. If the task receives a message, it sends the data over UART to the PLC modem for PLC transmissions and then copies the data into *PLC_HoldQueue* for retransmission in case transmission errors occur. The *RETX_PLC_DATA* message can be received when the transmission fails due to PLC communication errors or the task does not receive confirmation message till timeout. When retransmission happens, the task simply re-sends the data in the *PLC_HoldQueue* through the UART.

3.2.1.5 EMAC_handlePackets

EMAC_handlePackets is a SWI task. The primary task is to parse and forward the received Ethernet MAC frames. The first step is to check if the received Ethernet frame is valid by checking the Ethernet MAC header and frame size. If it passes and the PLC state is NORMAL, the SWI task copies the data into the *PLCTxBuffer*, conveys the information to *PLCTxTask* through the mailbox post, and then removes the received frame.

3.2.1.6 Ethernet Test Server Project

The test server project can be built with build configuration of *Debug_Test_Server* in the *Mini_Data_Concentrator_Example* CCS project as shown in Figure 15.

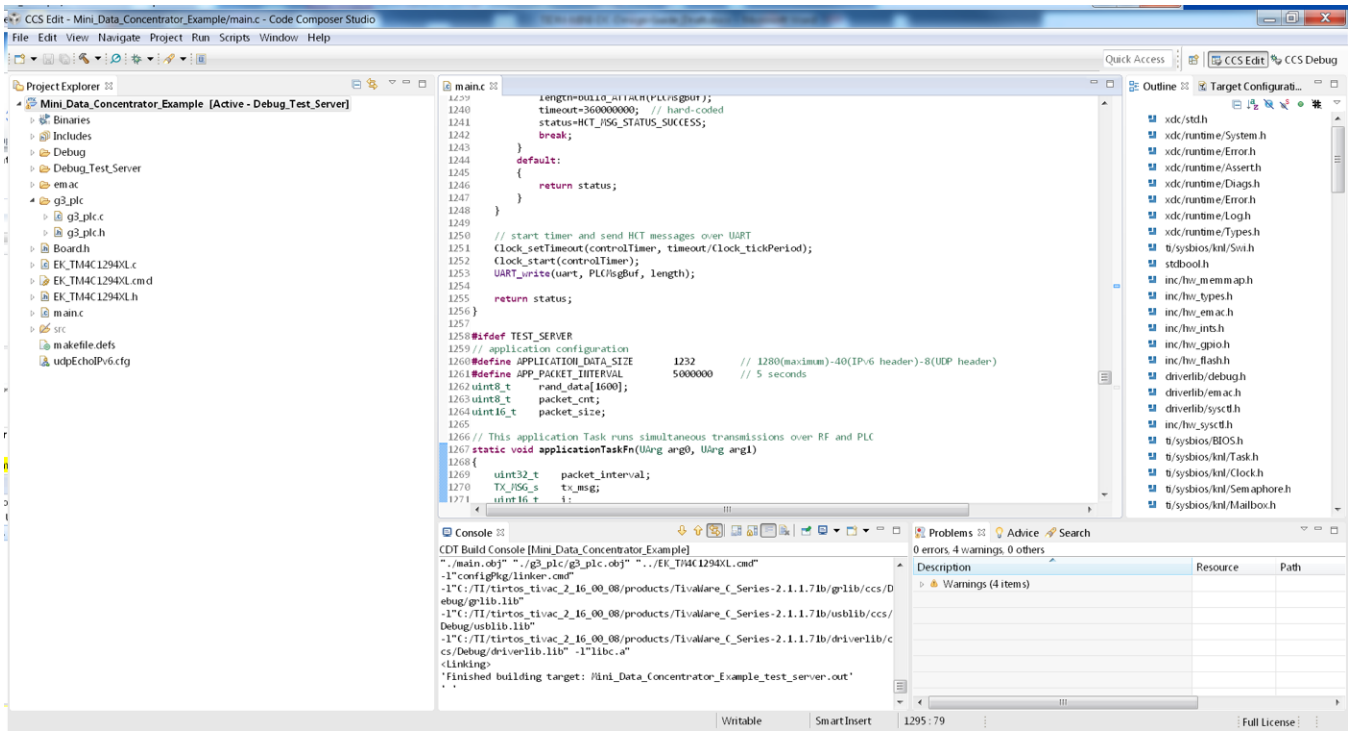

Figure 15. Debug_Test_Server CCS™ Configuration

The test server sends Ethernet frames to the mini-DC every five seconds and processes the received data from the mini-DC Ethernet link. The test server starts to send a 10-B IPv6 packet and increases the packet size by one every transmission. The maximum packet size is 1280 B (including IPv6 and UDP headers). If the packet size reaches the destination at the maximum size, it returns to the minimum size of 10 B. The IPv6 destination and source address is fixed. This example is provided to evaluate mini-DC functionality.

3.2.1.7 LED Configuration

The example project configures two LEDs (D1 and D2). Table 2 summarizes the LED number mapping to the specific software behavior for mini-DC and test server examples.

Table 2. LED Mapping

LED NUMBER	BEHAVIOR MAPPING TO SOFTWARE ACTIVITY	
	MINI-DC (ETHERNET REPEATER)	TEST SERVER (DEMONSTRATION ONLY)
D1	PLC TX/RX, EMAC TX/RX	EMAC TX
D2	ON when PLC state becomes NORMAL	EMAC RX

3.2.2 Building Mini_Data_Concentrator_Example Project using CCS™

The example project is built with CCS IDE v6.1.2 (or above). The CCS project can be opened by importing the CCS project files under the directory of *mini_Data_Concentrator_Example* from the example installation directory. Then configure the project with the build configuration of Debug. The screen capture is shown in Figure 16. Once built successfully, the binary file (*Mini_Data_Concentrator_Example.out*) will be generated under the directory of *Debug/*.

For the test server binary, the build and flash instruction is the same as previously described but with a different binary file (*Mini_Data_Concentrator_Example_test_server.out*) in the directory of *Debug_Test_Server/*.

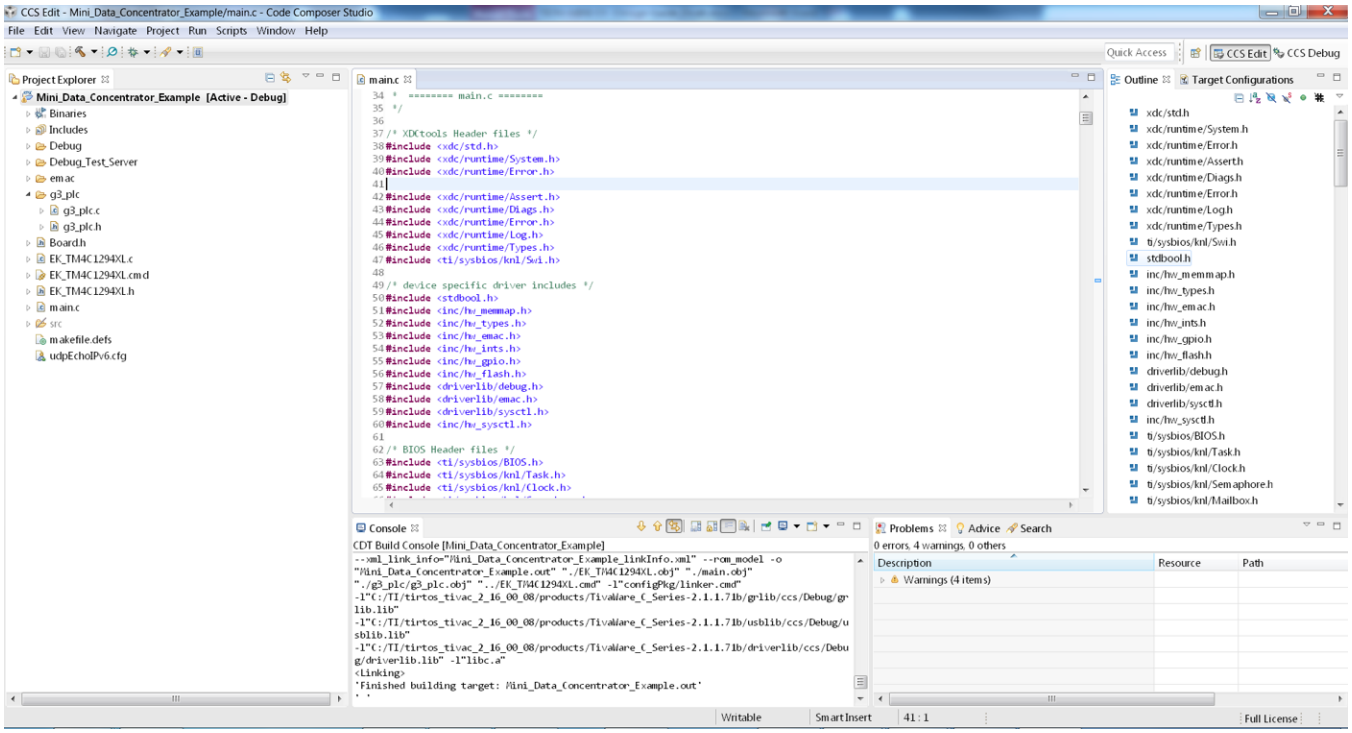

Figure 16. Mini_Data_Concentrator_Example CCS™ Project

3.2.3 Flashing Binaries using CCS™

This section covers step-by-step procedure to flash the example binary to the EK-TM4C1294XL EVM and the PLC binary on PLC FCC SOM module.

3.2.3.1 Flashing Mini_Data_Concentrator_Example Binary

This section covers how to flash the *Mini_Data_Concentrator_Example.out* binary on the TM4C1294NCPDT device using CCS.

1. Connect the USB cable to the EK-TM4C1294XL.
2. Select *View* → *Target Configurations* and create a new target configuration as shown in Figure 17.

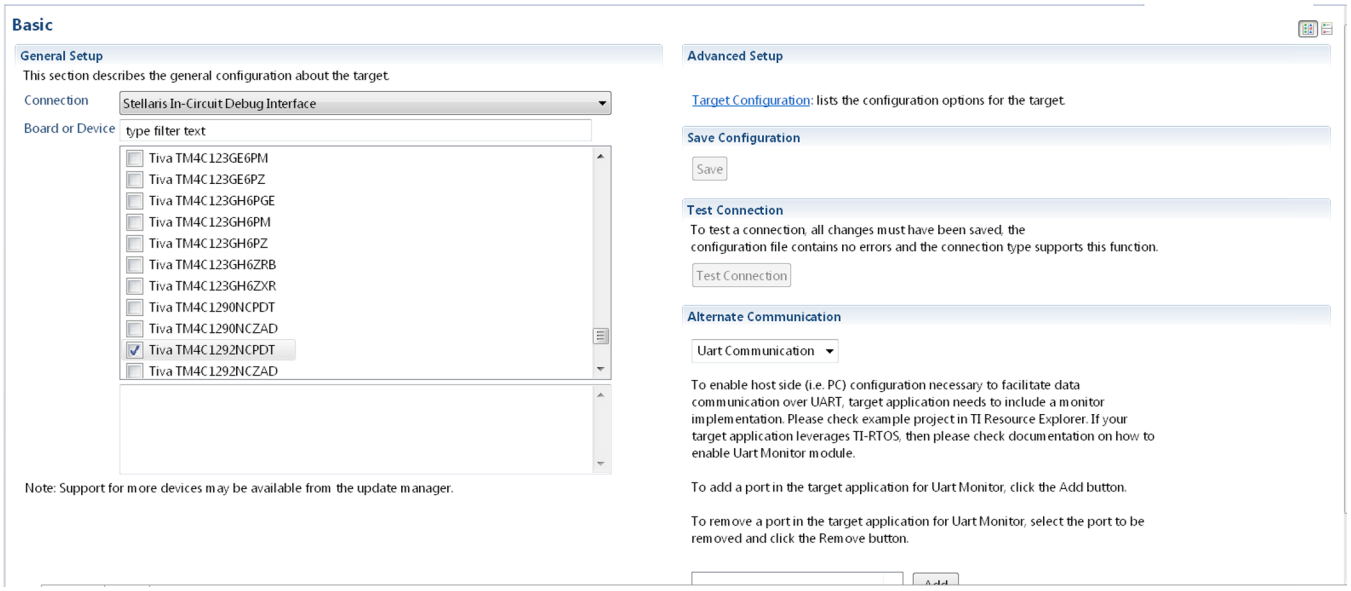

Figure 17. Target Configuration for EK-TM4C1294XL

3. Launch the target configuration and connect to the *CORTEX_M4_0* core shown in Figure 18.

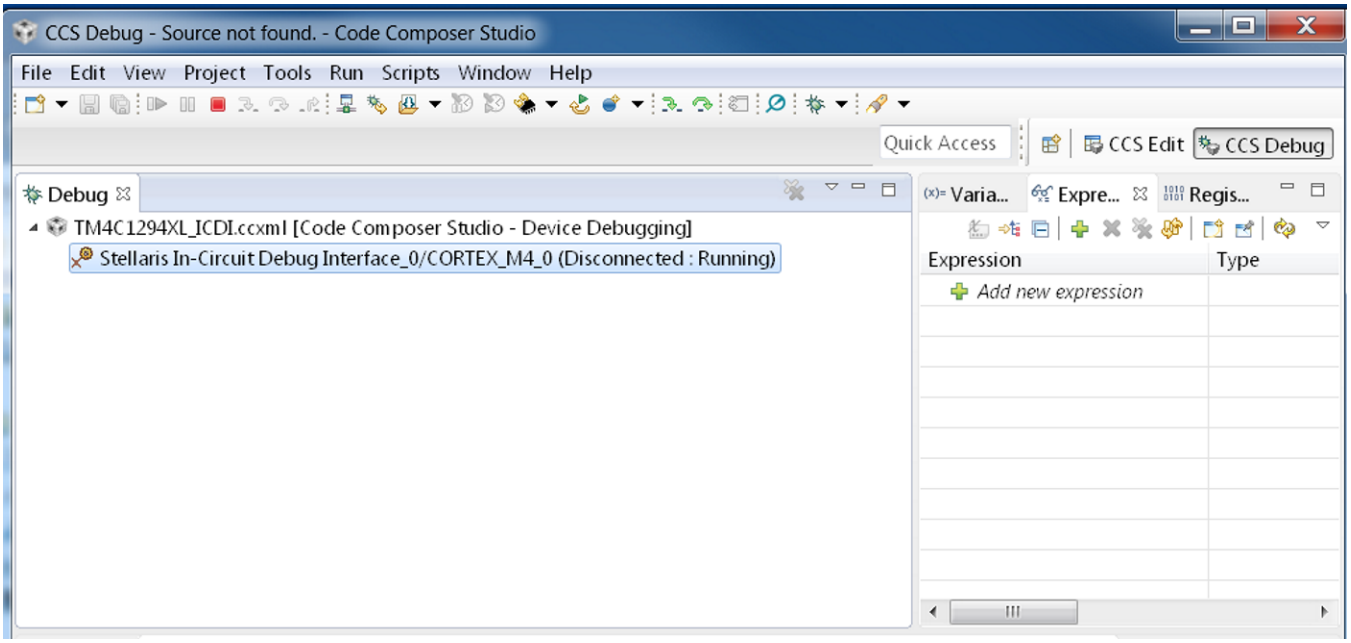

Figure 18. CCS™ Debug Window for EK-TM4C1294XL

4. Select *Run → Load → Load Program* and flash *Mini_Data_Concentrator_Example.out* binary.

3.2.3.2 Flashing PLC Binary to TMS320F28375S

Step-by-step procedures are found in Section 7.1 in the power line communication TI Design (TIDU812). The latest G3-PLC FCC software can be obtained from TI-PLC-G3-FCC-SN.

4 Testing and Results

The goal of mini data concentrator example testing is to validate the PLC and Ethernet repeater function implemented in the software. This is verified with three-node set-up: one G3-PLC service node, one Ethernet and PLC repeater, and one test server capable of Ethernet communication only.

4.1 Test Setup

Table 3 and Table 4 summarize required EVMs for the mini-DC testing and the required tools and software to run the mini-DC testing, respectively.

Table 3.

EVM	QUANTITY	NOTE
EK-TM4C1294XL	2	http://www.ti.com/tool/EK-TM4C1294XL
TIDM-SOMPLC-FCC	2	http://www.ti.com/tool/TIDM-SOMPLC-FCC
TMDSPLCKITV4-ARIB* (or TMDSPLCKITV4-CEN)	1	http://www.ti.com/tool/TMDSPLCKITV4-ARIB http://www.ti.com/tool/TMDSPLCKITV4-CEN
* A single kit includes two modems. For the testing, only docking boards are needed with the TIDM-SOMPLC-FCC module.		

Table 4. Tools for Mini Data Concentrator Test Setup

Device	EVM	UART WIRING	FLASH FIRMWARE	GUI TOOL
G3-PLC service node	TMDSPLCKITV4-ARIB +TIDM-SOMPLC-FCC	No	Yes (G3-PLC binary)	Yes (zero-configuration GUI[1])
Mini-DC (with Ethernet repeater)	TMDSPLCKITV4-ARIB +TIDM-SOMPLC-FCC +EK-TM4C1294XL	Yes (Section 3.1.1)	Yes (mini-DC binary[2])	No (standalone mode)
Ethernet test server	EK-TM4C1294XL	No	Yes (test server[3] binary)	No (standalone mode)
[1] Zero-configuration GUI is used to run G3-PLC service node. The G3-PLC software package (TI-PLC-G3-FCC-SN) will install the GUI automatically.				
[2] The pre- built mini-DC binary (*Mini_Data_Concentrator_Example.out*) can be found in the Debug/ under *Mini_Data_Concentrator_Example* install directory. Flashing instruction is given in Section 3.2.3.1.				
[3] The pre- built Test Server binary (*Mini_Data_Concentrator_Example_test_server.out*) can be found in the *Debug_Test_Server/* under *Mini_Data_Concentrator_Example* install directory. Flashing instruction is given in Section 3.2.3.1.				

4.2 Test Overview

Figure 19 shows the three-node test set-up. The PLC service node runs with zero-configuration GUI tool. The mini-DC and test server nodes run as standalone mode.

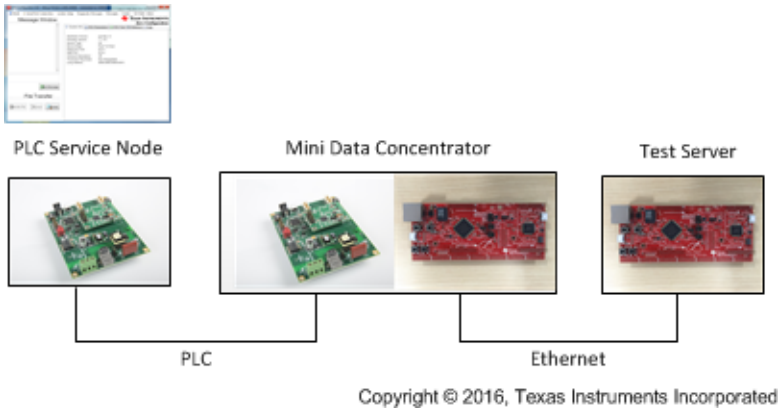

Figure 19. Mini-DC Test Setup

Once all nodes power on and the GUI starts for the PLC service node, the G3-PLC service node starts to join to the mini-DC. Once the service node joins to the mini-DC, it is ready to send and receive Ethernet and PLC data. Figure 20 shows the data flow for the testing.

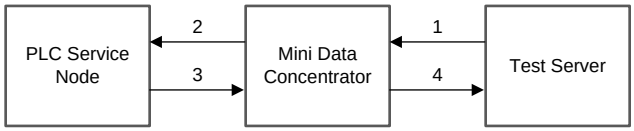

Figure 20. Data Flow for Mini-DC Test

In step one, the test server sends UDP and IPv6 data through the Ethernet link. In step two, the mini-DC receives the data and then passes the data to the PLC service node through the PLC link after removing the Ethernet header from the data. In step three, the PLC service node sends the received data back to mini-DC through the PLC link. In step four, the mini-DC sends the received data to test server through the Ethernet link after the prefix Ethernet header to the received data.

4.2.1 Test Procedure

This section covers step-by-step procedure to run the mini-DC testing.

1. Turn on the PLC and TM4C1294 EVMs for the mini-DC. When the TM4C1294 EVM configures the PLC EVM as mini-DC successfully, LED1 will be turned ON.
2. Start PLC service node with GUI tool and wait until joining to the mini-DC. See Section 4.2.2.
3. Turn on the test server and the data reception will be shown on the zero-configuration GUI as shown in Figure 26.

4.2.2 PLC Service Node Setup

This section covers how to run the G3-PLC service node with the GUI tool.

1. Connect the PLC service node to the computer and open intermediate GUI.
2. Set a unique long address by using *Set System Config* and configure *Host/Diag Ports* to *SCI-A*.

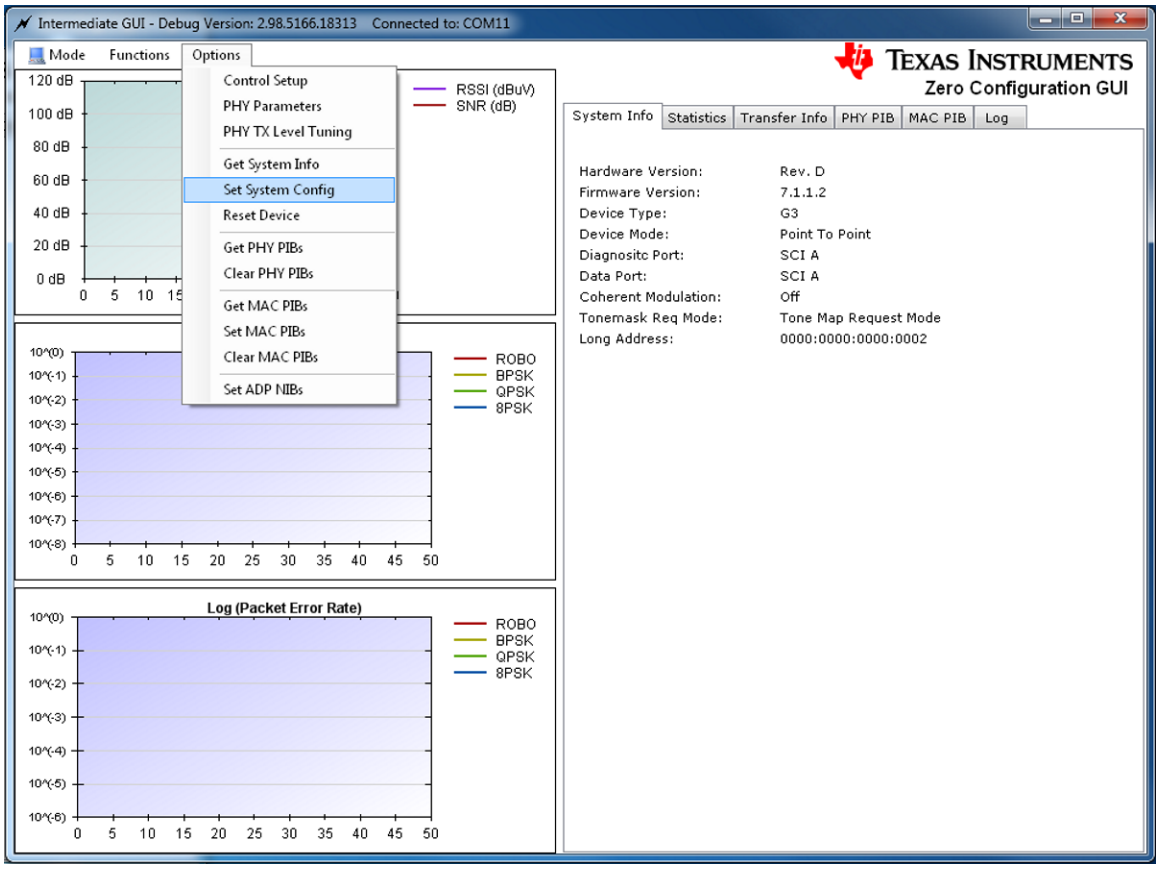

Figure 21. Set System Configuration

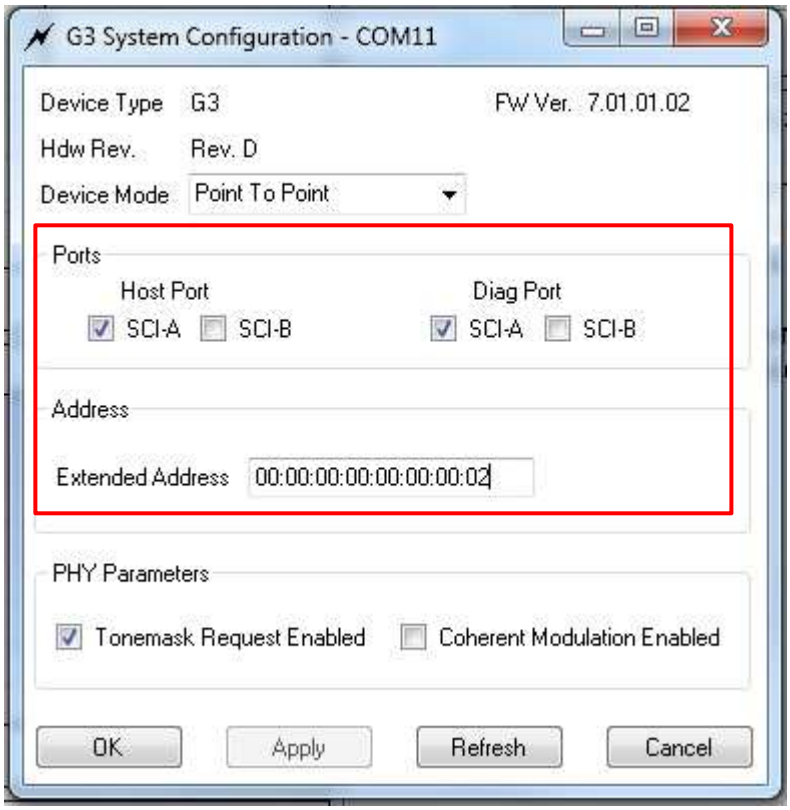

Figure 22. G3-PLC System Configuration

3. Start a device as G3-PLC service node by selecting *Functions* → *Start Service Node*.

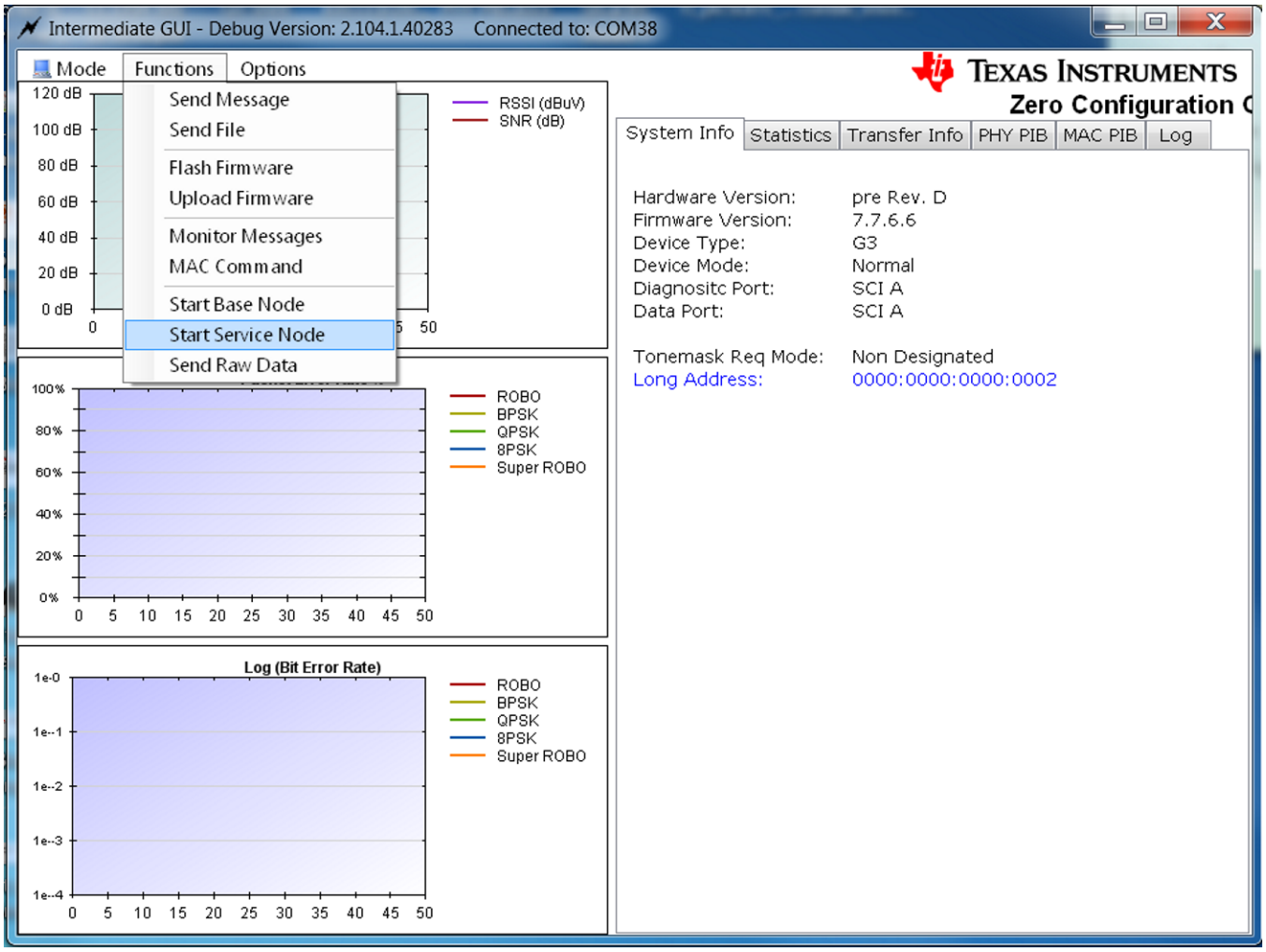

Figure 23. Start Service Node

4. In the pop-up window of G3 Service Node, click *Start*.

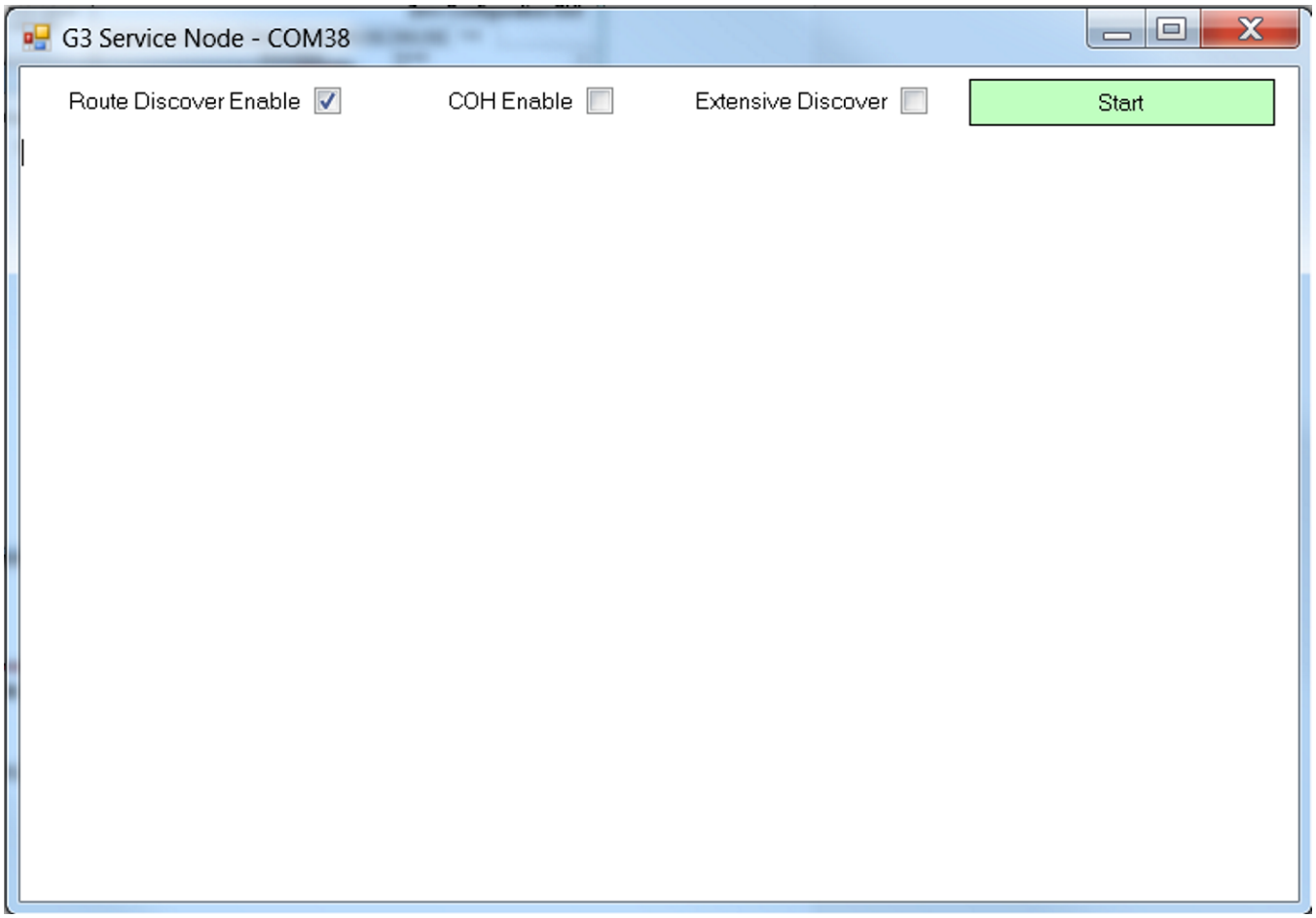

Figure 24. G3-PLC Service Node Window

5. When the G3-PLC service node is joined, the information on the window will display. If the service node is joined with the short address other than 0x0001, power-cycle the mini-DC (both the PLC EVM and the EK-TM4C1294XL EVM) and then start joining process again with the G3-PLC service node.

NOTE: For the demonstration the service node should be assigned to the short address of 0x0001 because the test server always uses the fixed IPv6 destination address with postfix of 0x0001.

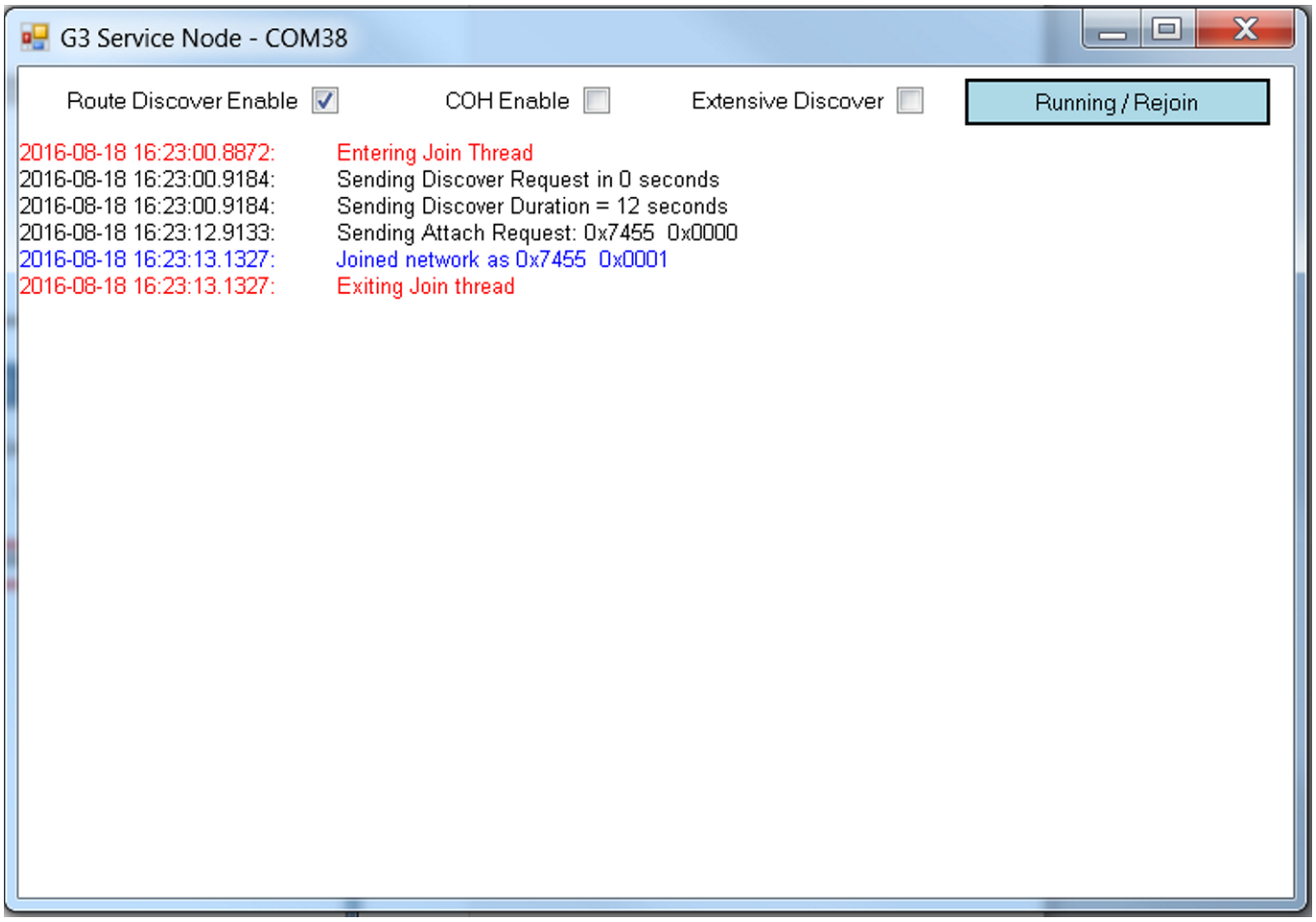

Figure 25. G3-PLC Network Join Completed

4.2.3 Test Results

This section shows mini-DC test results to verify Ethernet and PLC repeater functionality. Figure 26 shows the test results. For the testing, the test server starts to transmit data with the packet size of 10 B. The packet interval is set to five seconds. The packet size increases by 1 B every transmission till reaching at the maximum size of 1280 B which is limited by G3-PLC maximum data size. The test result shows that the mini-DC forwards the data received from the test server to the G3-PLC service node without any drops. Additionally, the test server increases the packet size only when the test server receives the echo-back data from the PLC service node. No duplicated data size (shown in Figure 26) shows that the mini-DC is functional for the forward path from the G3-PLC service node to the test server. This result is because the test server receives all the packets echoed back from the G3-PLC service node.

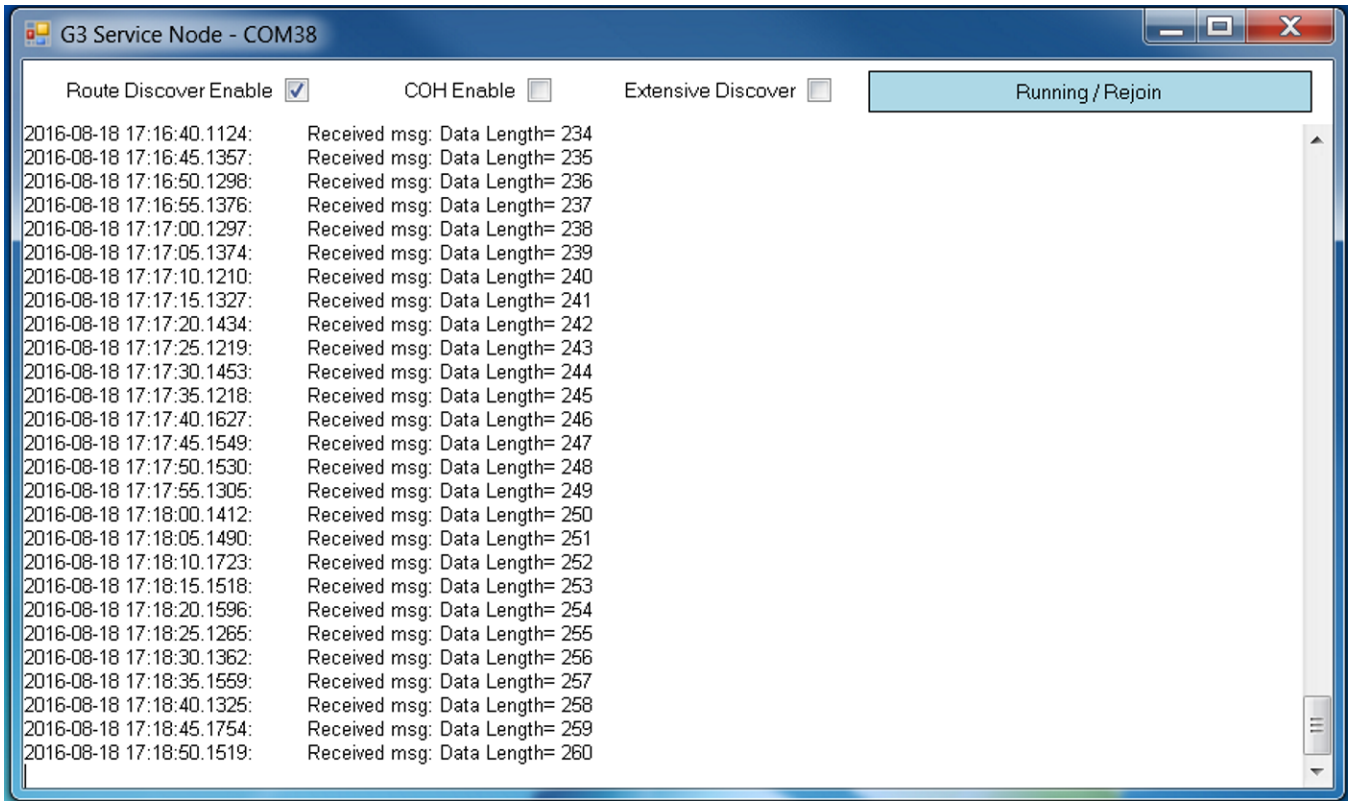

Figure 26. Mini-DC Test Result

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDM-MINI-DC.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDM-MINI-DC.

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDM-MINI-DC.

5.4 Altium Project

To download the Altium project files, see the design files at TIDM-MINI-DC.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDM-MINI-DC.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDM-MINI-DC.

6 Software Files

To download the software files, see the design files at TIDM-MINI-DC.

7 References

1. Texas Instruments, *Tiva™ TM4C1294NCPDT Microcontroller,*, Data Sheet (TM4C1294NCPDT)
2. Texas Instruments, *TMS320F2837Xs Delfino™ Microcontrollers*, Data Sheet (SPRS881)
3. Texas Instruments, *Powerline Communications Analog Front-End*, Data Sheet (SBOS669)
4. Texas Instruments, *3-ph E-Meter Input Voltage: 2 and 3 phase; output: 16.5V@300mApk, 12V@500mA, 3.3V@100mApk, 1.9V@15*, Tools Folder (PMP7146)
5. Texas Instruments, *System on Module for G3 Power Line Communication (FCC Frequency Band)*, TI Design (TIDU812)

8 About the Author (Optional)

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