TI Designs

20-Bit, 1-MSPS Isolated Data Acquisition Reference Design Optimizing Jitter for Maximum SNR and Sample Rate

Description

The TIDA-01035 is a 20-bit, 1-MSPS isolated analog input data acquisition reference design demonstrating how to resolve and optimize performance challenges typical of digitally isolated data acquisition systems. This TI Design:

- Significantly improves high frequency AC signal chain performance (SNR and THD) by effectively mitigating ADC sample clock jitter across isolation boundary
- Maximizes sample rate by eliminating or minimizing propagation delay introduced by a digital isolator
- Provides option to evaluate performance with and without jitter mitigation technique with jumper
- Includes detailed timing analysis detailing the isolator's additive jitter impact on data throughput

Resources

TIDA-01035	Design Folder
ADS8900B, REF5050, THS4551	Product Folder
ISO7840, ISO7842, ISO1541, SN6501	Product Folder
LMZ14203, TPS7A4700, TPS70918	Product Folder
OPA376, LMK61E2	Product Folder
SN65LVDS4RSET, SN7AUP1G80	Product Folder
SN74AHC1G04	Product Folder
ADS8900B EVM-PDK	Associated Design

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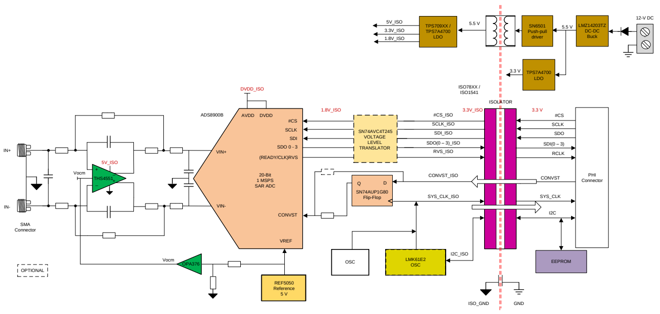
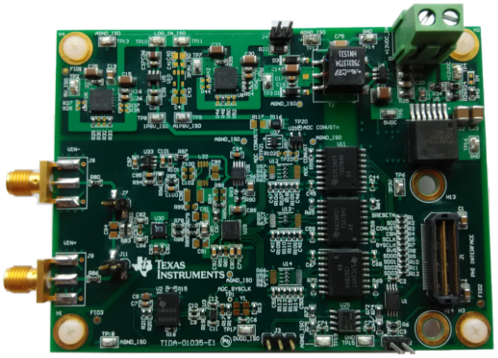


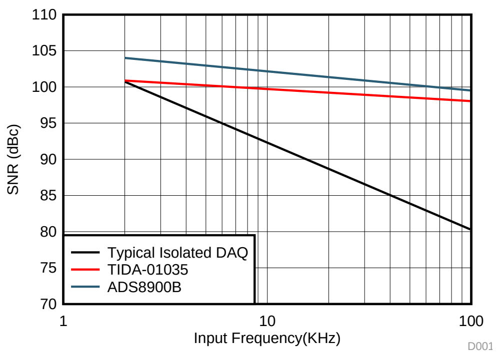
Features

- Isolated 20-Bit, 1-MSPS, Single-Channel Differential Input Data Acquisition (DAQ) System
- Jitter Mitigation Technique Realizes More Than 18-dB System-Level SNR Improvement for High-Frequency Input Signals (100-kHz Fin, 1 MSPS)
- Reduced Logic (on Isolated ADC Side) Eliminates Need for Higher Power and Complex PLL Solutions
- Achieves 1-MSPS Sampling Rate While Preserving Low SPI CLK Rates With the ADS8900B ADC's Innovative multiSPI™ and ADC Master or Source-Synchronous Mode Digital Interfaces
- Includes Theory, Calculations, Component Selection, PCB Design and Measurement Results

Applications

- Modular DAQ Systems
- Lab Instrumentation and Field Instrumentation
- Design Validation and Verification
- Remote Process Monitoring and Control





1 System Overview

Data acquisition (DAQ) systems are found in numerous applications from simple temperature monitoring to high-end process and control. DAQs are primarily used to measure real-world analog electrical or physical properties (voltage, current, temperature, pressure, vibration, and so on), apply the appropriate signal conditioning (amplification and filtering), and digitize the signal so it can be further processed by the host processor or computer. The electronics that support and interface with the physical transducer, amplifier, and analog-to-digital converter (ADC) are often referred to as the analog input DAQ module and are the focus of this reference design. Figure 1 illustrates an analog input module and how the DAQ is integrated within the system. Find more details in Section 2 of the TIDA-00732 design guide.

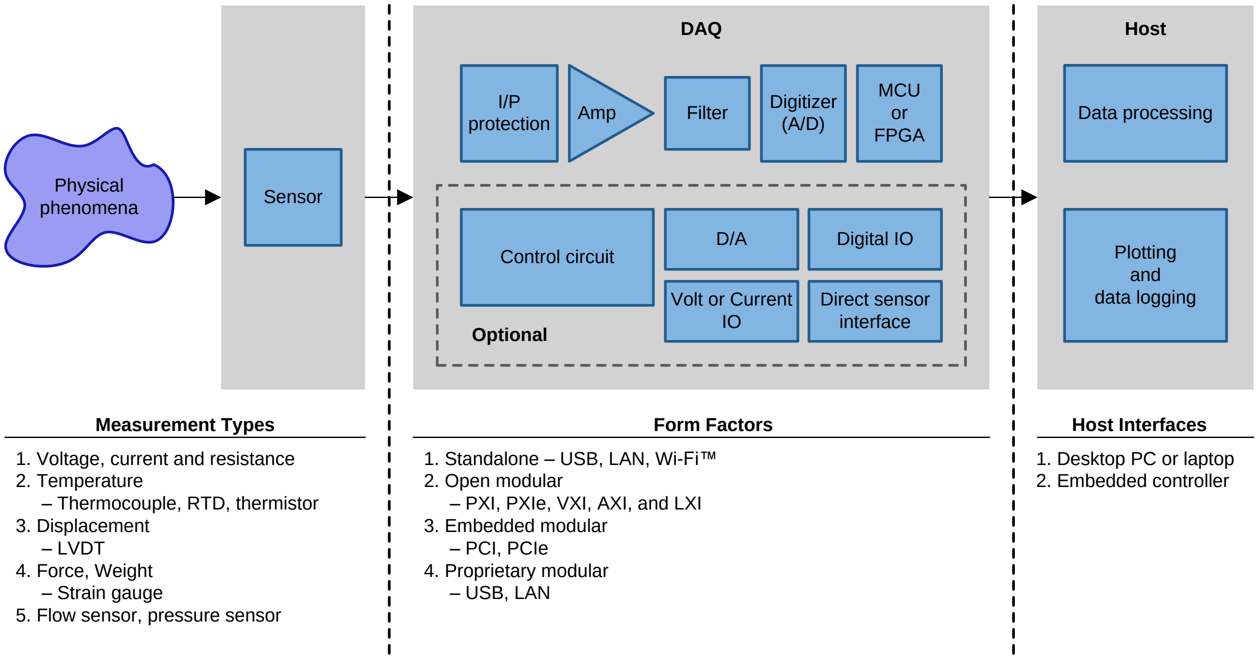


Figure 1. Generic DAQ System Block Diagram

The environmental and performance requirements of many DAQ end-equipment applications require galvanic isolation in order to break ground loops and improve measurement accuracy. Harsh environments often require the transducer to be electrically isolated from the system controller to enable measurements at higher voltages while preventing the threat of electrical shock. Furthermore, the electrical isolation can also improve noise immunity, especially between input channels, enhancing the signal-to-noise ratio (SNR) of the data channel.

Depending on the system requirements, isolation can be achieved through the analog domain (before ADC) or digital domain (after ADC). Signal chain metrics such as dynamic range, system bandwidth (BW), SNR, and power all play a role in determining which is the best solution; however, due to ADC dynamic range constraints, cost, and complexity, digital isolation is often the preferred solution. Because each digital line requires isolation, minimizing the number of digital lines with serial peripheral interface (SPI) communication while maximizing the data rate is a system design challenge presented by digitalized isolated input DAQs. Furthermore, the isolation boundary presents non-ideal signal transfer, limiting data rate due to propagation delay and adding nondeterministic signal jitter making system timing challenging.

In this comprehensive reference design, the designer is shown how to mitigate the challenges presented by the isolated propagation delay and jitter while optimizing signal chain SNR performance.

1.1 System Description

This design guide focuses on maximizing the signal integrity characteristics of an isolated analog input module as illustrated in Figure 2, which outlines the input protection, analog front end (AFE), digital isolation, isolated power, non-isolated power, and host processor functions of the DAQ. The input signal from the measuring sensor is received by the DAQ input connector. Many systems will require input protection, which must be selected to provide the necessary protection without impacting signal integrity. Due to the normally small signal being detected and the associated noisy environment, the AFE consists of a scaling or programmable gain amplifier (PGA) followed by an anti-aliasing, noise limiting, low pass filter (LPF), which is paired with the appropriate ADC driver prior to digitization. The ADC converts the time varying analog input to either a serial or parallel binary bit stream, which is then passed across the digital isolation barrier to the embedded host controller (MCU or FPGA). Depending on the application, the ADC may contain the necessary reference and/or the associated buffer integrated as part of the ADC. Furthermore, portions or the entire AFE may also be integrated as a single device for specific applications, but this can also limit flexibility.

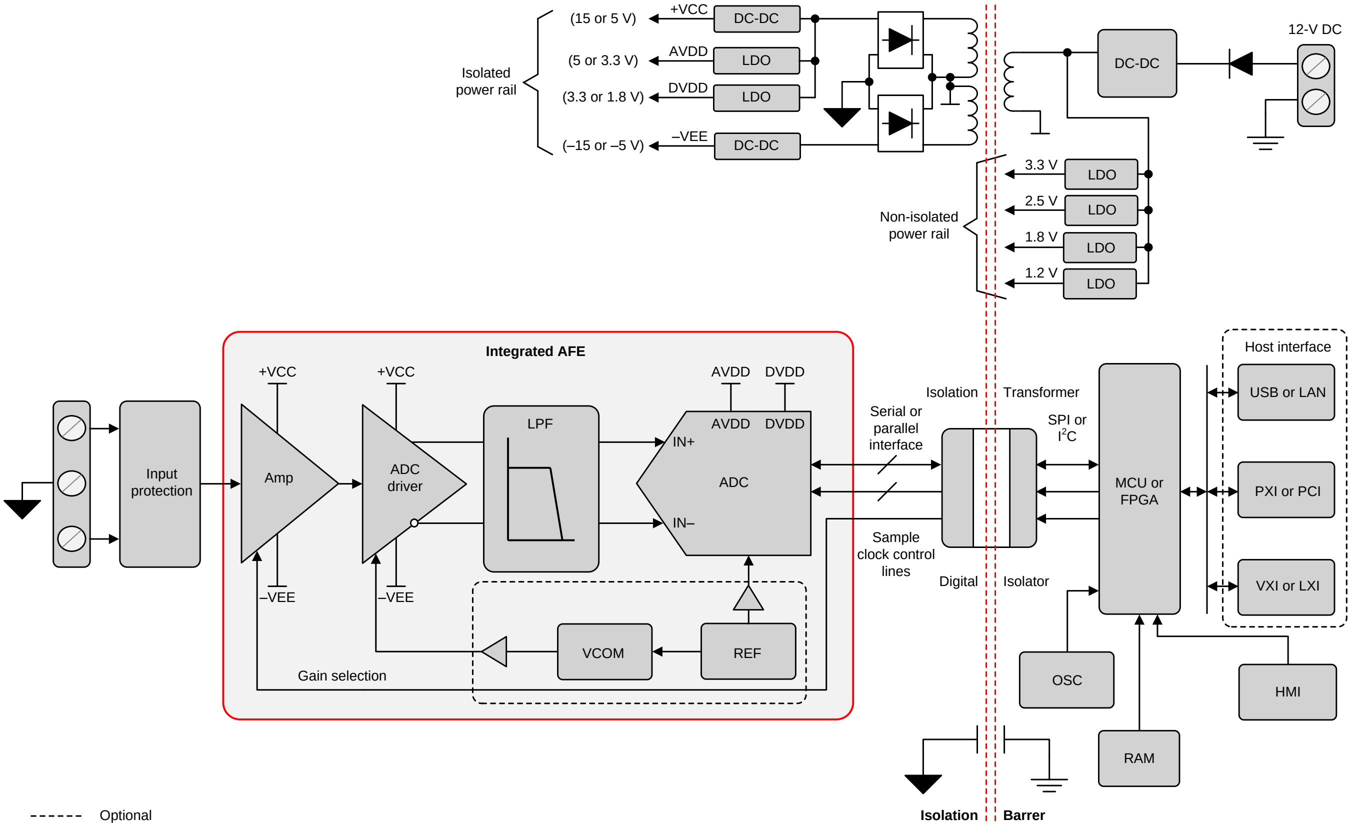


Figure 2. Isolated Analog Input DAQ Reference Diagram

In this example, the host or embedded controller interfaces with the ADC through a serial interface (for example, SPI or I^2C) in order to minimize the total number of required isolated channels. The controller will also support one or more interfaces to a central controller with either PXI, PCI, LXI, VXI, or USB protocols. A human machine interface (HMI) with an embedded GUI can also be included for local monitoring, data logging, and accessing. A local oscillator or clock and well as memory will normally be required.

Finally, isolated and non-isolated power DC-DC and LDO solutions are required to power the electronics on both sides of the isolation barrier. Normally, for sensitive analog inputs, both DC-DC and LDO solutions are required in order to maximize system power efficiency and noise immunity.

The following sections detail the timing challenges presented by the isolation barrier in terms of its effect on the ADC's data rate and SNR performance, and the challenges of synchronizing the sample clock with the host clock. When these performance limiting characteristics are understood, solutions using key features of TI's high performance AFE solutions for amplifiers, ADCs, and isolation devices are highlighted along with TI's power solutions for both isolated and non-isolated supplies. Furthermore, a novel design for synchronizing the ADC's sample clock with the host clock is also demonstrated.

For more background information on DAQ challenges and solutions, see the design guides for the TIDA-00732 and TIDA-00164 designs.

1.2 Key System Level Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Number of channels	Single
Input type	Differential
Input range	±5 V fully differential
Input impedance	1 kΩ
Resolution	20 bits
SNR(1)	98 dB at 100-kHz signal input
	101 dB at 2-kHz signal input
	101 dB at 1-kHz signal input
THD(1)	–109 dB at 100-kHz signal input
	–124 dB at 2-kHz signal input
	–125 dB at 1-kHz signal input
Power supply isolation	250-V DC (continuous) basic insulation
	5000-V AC for 1 minute (withstand)
Digital channel isolation	5.7-kV$_{RMS}$ isolation for 1 minute per UL 1577
Operating temperature	0°C to 60°C
Storage temperature	–40°C to 85°C
Connectors	60-pin Samtec high density connector for precision host
	Interface (PHI) module interface
Power	12-V DC, 200 mA
Form factor (L × W)	100 mm × 75 mm

(1) See Table 18 for more details.

1.3 Block Diagram

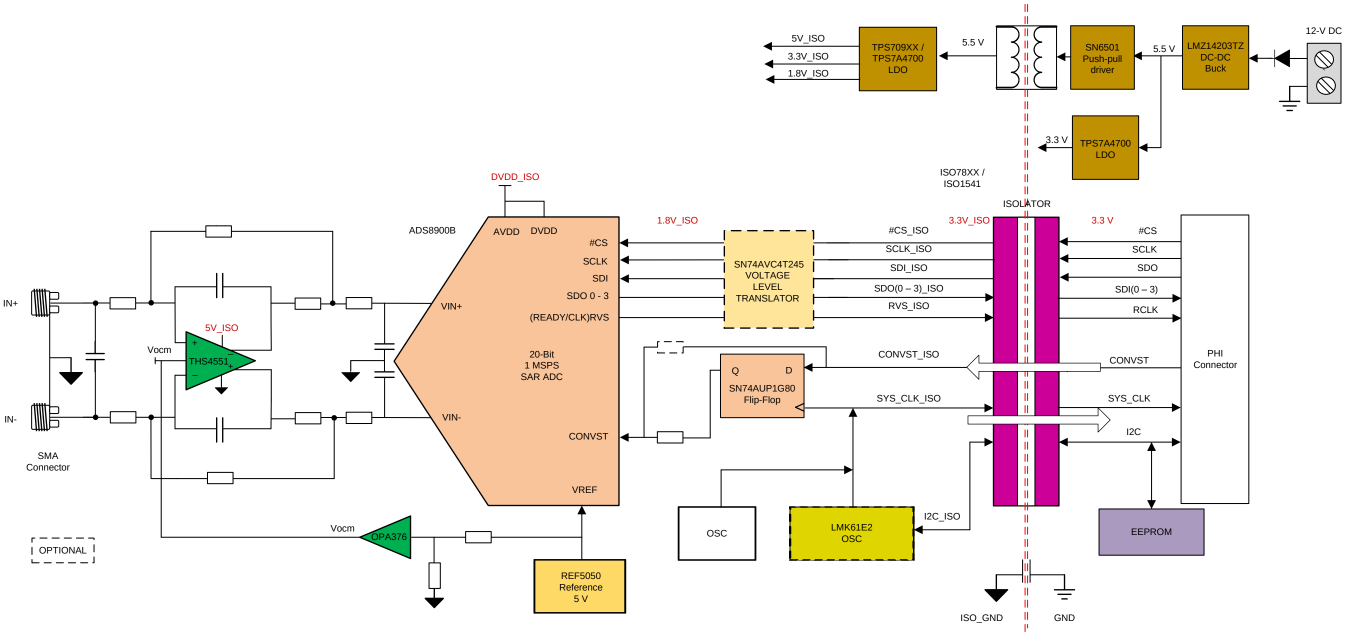


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Figure 3. TIDA-01035 System Block Diagram

1.4 Highlighted Products

The system contains the following highlighted parts, which determine the overall system performance. These parts are grouped into these sub-blocks:

- Analog signal chain
- Clock
- Power

1.4.1 Analog Signal Chain

- *THS4551*: The THS4551 fully differential amplifier offers an easy interface, high precision, and a high-speed differential ADC. To achieve a higher resolution performance (16 to 20 bit), the driving amplifier should have a very low DC error and drift. With the exceptional DC accuracy, low noise, and robust capacitive load driving, this device is well suited for DAQ systems where high precision is required along with the best signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR) through the amplifier and ADC combination.
- *ADS8900B*: The module has a single-channel differential analog input and uses the ADS8900B, 20-bit, 1MSPS SAR ADC with an integrated reference buffer.
- *REF5050*: The onboard reference REF5050 (ultra-low noise, low drift, and high precision) followed by low noise, low temperature drift, and low output impedance buffer provides a 5-V reference to the ADC core.
- *ISO784x* and *ISO1541*: The digital isolation for the host SPI and control signal is achieved using the ISO7840 and ISO7842 digital isolators. The host controller communicates with the LMK61E2-SIAR (ultra-low programmable clock oscillator) through the ISO1541, which isolates the I^{2}C bus.

1.4.2 Clock

The LMK61E2 programmable oscillator has the following features:

- Ultra-low noise, high performance (90 fs RMS jitter at > 100 MHz)
- Frequency tolerance ±50 ppm
- Frequency output 10 MHz to 1 GHz
- I^{2}C interface

1.4.3 Power

Figure 4 illustrates the power supply tree of the TIDA-01035. The TIDA-01035 needs 12-V DC of power to generate the 5.5-V and 3.3-V non-isolated power rails and the 5.2-V, 3.3-V, and 1.8-V isolated power rails.

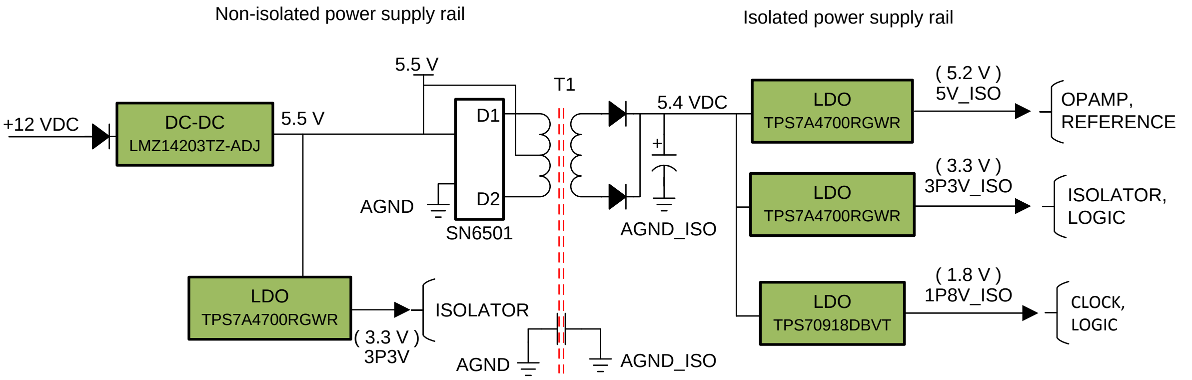


Figure 4. TIDA-01035 Power Supply Block

- *SN6501*: The isolated power supply power is generated using the SN6501, low-noise, low-EMI push-pull transformer driver.
- *DC-DC and LDO*: The power supply rail for both the isolated and non-isolated sections is generated by the DC-DC convertor and LDO, which are shown in Table 2.

Table 2. Power Supply Rail

SERIAL NO	TYPE	PART NO	SUPPLY RAIL
1	DC-DC	LMZ14203	5.5 V
2	LDO	TPSA4700RGWR	5.2 V, 3.3 V
3	LDO	TPS70918DBVT	1.8 V

2 System Design Theory

Galvanic isolation is commonly used by DAQ systems in order to breaks ground loops and thereby improves measurement accuracy and safety. Isolation may be achieved within the analog domain prior to the ADC or in the digital domain, after the ADC. Prior to this publication, digital isolation was the preferred embodied solution for systems requiring medium performance (resolution < 16 bits, sampling rates < 1 MSPS, and BW < 100 kHz). However, for higher resolution, higher speed solutions (> 18 bits, > 1 MSPS, and > 100 kHz), digital isolators will limit signal chain performance, dramatically reducing the DAQ's effective number of bits (ENOB). Digital isolators present two main design challenges:

1. Propagation delay in digital isolator (described in Section 2.1)
2. Additive jitter due to digital isolator (described in Section 2.2)

These challenges and a detailed analysis of their impact with examples are described in the following sections.

2.1 *Isolated DAQ Signal Chain Design—Timing Analysis*

In DAQ systems, isolation in the signal chain breaks ground loops and thereby improves measurement accuracy and safety. Isolation may be achieved within the analog domain prior to the ADC or in the digital domain after the ADC. Digital isolation is preferred when higher sampling rates are required. However, for a higher resolution (>16 bits) and higher speed (>1 MSPS), the propagation delay and jitter of the digital isolator limits the signal chain performance for higher input signal frequencies. The propagation delay reduces the sampling rate of the signal chain. The jitter introduced by the digital isolator degrades the SNR at higher input frequencies.

This design guide describes the performance impact of propagation delay and jitter associated with isolated DAQ systems, explains the theory, calculation, and design, and presents examples.

2.1.1 Effect of Propagation Delay on Sampling Rate

In a typical DAQ system, a serial peripheral interface (SPI) transfers data between the ADC and the host. Figure 5 shows a generic SPI block diagram. The host is generally the SPI master that decides the sampling rate and data transfer rate. In a typical SPI Motorola® protocol, the host sends data at rising edge and receives data on the falling edge within the same clock cycle.

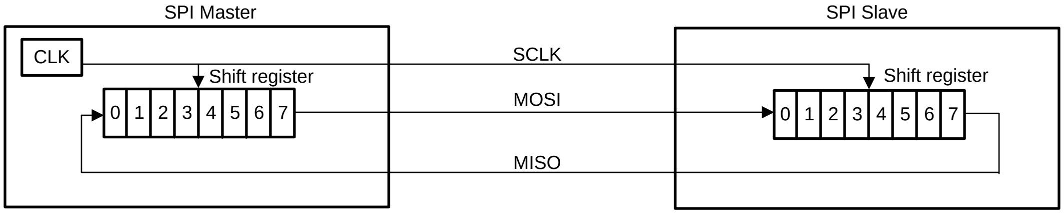


Figure 5. SPI Block Diagram

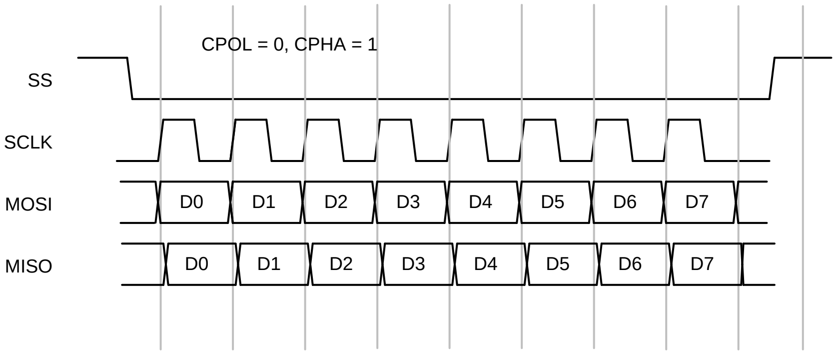


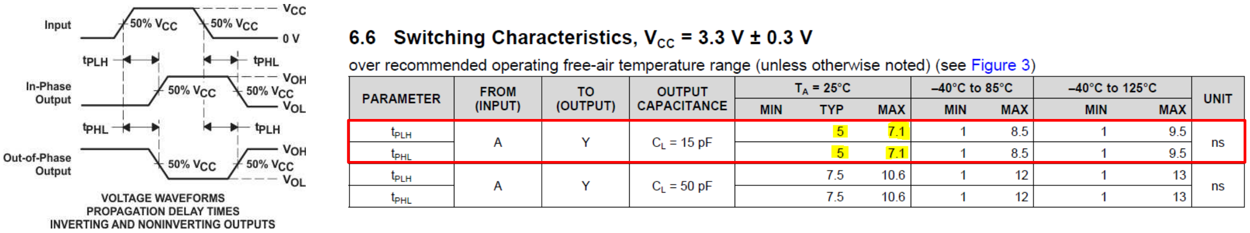
Figure 6. SPI Timing Diagram

As depicted in Figure 6, the host expects the valid data before the clock falling edge. The total round trip propagation delay must be less than half the SCLK period to avoid missing bits. Hence, the theoretical maximum SPI clock can be calculated as:

$$SCLK_{max} = \frac{1}{2 \times t_{pd}} \quad (1)$$

Equation 1 assumes that there is no change in the waveform shape. However, digital signals become analog in nature as they have finite rise-fall times, which result in waveform deformities that cause pulse width distortion (PWD) as they propagate through different digital signal chain elements. The pulse width of the clock or the data line changes due the different threshold voltages and rise-fall times of the digital devices in the path.

Figure 7 shows a datasheet example of propagation delay and PWD that can be found in various devices.



6.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		5	7.1	1	8.5	1	9.5	ns
t_{PHL}					5	7.1	1	8.5	1	9.5	
t_{PLH}	A	Y	C_L = 50 pF		7.5	10.6	1	12	1	13	ns
t_{PHL}					7.5	10.6	1	12	1	13	

Figure 7. Propagation Delay and PWD

A detailed timing analysis is required to calculate the maximum SPI clock rate by considering the SPI propagation delay and PWD.

2.1.2 Non-Isolated DAQ Timing Analysis

The timing analysis of a simple non-isolated DAQ system shown in Figure 8 is first considered. The interface between the ADC and host is an SPI with a level translator. The analysis assumes that in each sampling interval, the ADC acquires a sample, converts it, and sends the serialized data to the host. The said assumption is critical for low latency systems.

The objectives of the timing analysis are:

- Compute the maximum SPI clock rate (serialized data rate).
- Compute the maximum sampling rate of the ADC.

The maximum SPI clock is computed by estimating the total propagation delay and total PWD of the SPI. The ADC sampling rate is calculated from the SPI clock rate and ADC acquisition time. In this example, level translators or buffers are used in between the host and the ADC to make input and output voltage levels compatible and thus will add to the total round trip delay must be considered for timing analysis. Table 3 breaks down all the timing parameters in the ADC-host interface that is considered in this example.

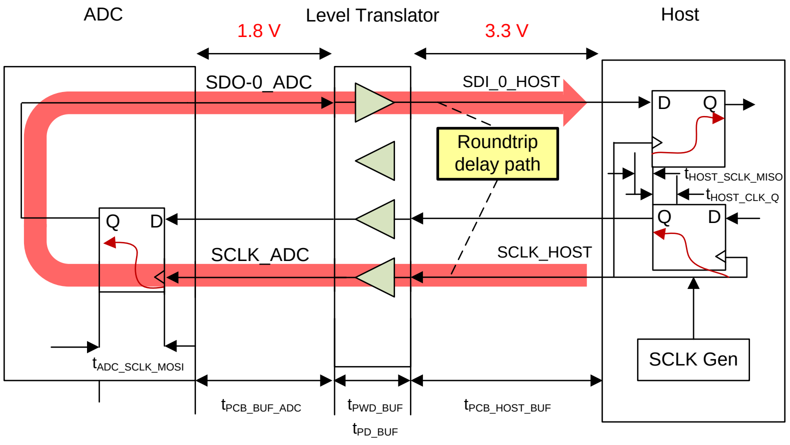


Figure 8. Simple Non-Isolated SPI ADC-Host Interface

Table 3. Timing Parameter

PARAMETER	DESCRIPTION
t_{SCLK_min}	Minimum SCLK period
$t_{PCB\_HOST\_ISO}$	PCB trace delay between host and isolator
$t_{PCB\_HOST\_BUF}$	PCB trace delay between host and buffer
t_{PD_ISO}	Isolator propagation delay
t_{PD_BUF}	Buffer or level translator propagation delay
$t_{PCB\_BUF\_ADC}$	PCB trace delay between buffer and ADC
$t_{PCB\_ADC\_BUF}$	PCB trace delay between ADC and buffer
$t_{PCB\_BUF\_ISO}$	PCB trace delay between buffer and isolator
$t_{PCB\_ISO\_HOST}$	PCB trace delay between isolator and host
t_{SU_HOST}	Setup time of host MISO line
t_{PLHmax}	Maximum propagation delay from low to high
t_{PHLmin}	Minimum propagation delay from high to low
t_{PHLmax}	Maximum propagation delay from high to low
t_{PLHmin}	Minimum propagation delay from low to high
$t_{PWD\_BUF\_max}$	Maximum pulse width distortion of buffer or level translator
$t_{SCLK\_PH\_min}$	Minimum positive clock high period
$t_{PWD\_HOST\_max}$	Maximum host PWD
f_{SCLK_max}	Maximum SCLK frequency
$t_{PD\_HOST\_SCLK}$	Propagation delay of host SCLK at host end
$t_{ADC\_SCLK\_MOSI}$	ADC SCLK to MOSI output delay
$t_{HOST\_SCLK\_MISO}$	Host SCLK to MISO delay
t_{RTPD_max}	Maximum propagation round-trip delay
t_{OD_BUF}	Buffer output delay due impedance mismatch and loading effect of receiver
t_{OD_ISO}	Isolator output delay due impedance mismatch and loading effect of receiver

$$t_{RTPD\_max} = t_{PD\_HOST\_SCLK} + 2 \times t_{PD\_BUF} + t_{ADC\_SCLK\_MISO} + t_{HOST\_SCLK\_MISO} \tag{2}$$

2.1.2.1 Determining Maximum SPI Clock (SCLK)

In a low latency system, the converted data should be made available to the host system with minimum delay. A higher SCLK results in lower latency. The SPI clock should be computed for two cases:

1. SPI clock limited by ADC
2. SPI clock limited by round-trip delay

The minimum of these two cases will be the maximum SPI clock. The following section details the procedure to find the maximum SPI clock for a non-isolated SPI example.

$$\mathrm{SCLK_{max}} = \min\left(\mathrm{SCLK_{max\_adc\_limited,}}\ \mathrm{SCLK_{max\_rtpd\_limited}}\right) \tag{3}$$

2.1.2.2 SPI Clock Limited by ADC

The maximum SPI SCLK is the same as ADC_SCLK. However, the SPI SCLK duty cycle is affected by the PWD of the various digital devices it passes through. As a result, the maximum SPI SCLK limited by the ADC and digital device in the path is computed from $t_{SCLK\_ADC\_max}$ and $t_{PWD\_BUF\_max}$.

The system shown in Figure 8 is used as an example with individual devices as listed in Table 4.

Table 4. Devices Used in Non-Isolated and Isolated Interface Examples

SLNO	DESCRIPTION	DEVICE
1	ADC	ADS8900B
2	LEVEL TRANSLATOR	74AVC4T245
3	ISOLATOR	ISO78xx
5	Flip-flop	SN74AUP1G80
4	PCB TYPE	FR4 - 4layer

Step 1: Estimating the PWD of the Buffer

To find the PWD for the buffer 74AVC4T245, the max and min values of t_{PLH} and t_{PHL} are taken from the 74AVC4T245 datasheet.

$$t_{PWD\_BUF\_max} = \max\left(\left|t_{PLHmax} - t_{PHLmin}\right|, \left|t_{PHLmax} - t_{PLHmin}\right|\right) \tag{4}$$

$$t_{PWD\_BUF\_max} = \left(\left|4.5 - 0.1\right|, \left|4.5 - 0.1\right|\right)$$
$$t_{PWD\_BUF\_max} = 4.4\ \mathrm{ns}$$

Step 2: Calculating the Maximum ADC Clock

$$t_{SCLK\_PH} = t_{SCLK\_PH\_min} + t_{PWD\_BUF\_max} + t_{PWD\_HOST\_max} \tag{5}$$

Table 5. Non-Isolated Interface Timing Parameters

PARAMETER	DELAY (ns)	REMARK
$t_{PWD\_HOST\_max}$	0	—
$t_{PWD\_BUF\_max}$ (t_{PWD_BUF} + t_{OD_BUF})	4.40	No buffer or level translator in the TIDA-01035 round-trip path
$t_{SCLK\_PH\_min}$ (0.45 × $t_{ADC\_CLK\_min}$)	5.99	—
t_{SCLK_PH}	10.39	—

$$f_{SCLK\_max} = \frac{1}{2 \times t_{SCLK\_PH}} = 48.1\,\mathrm{MHz} \tag{6}$$

The maximum SCLK frequency supported by the ADC is 48 MHz.

2.1.2.3 SCLK Limited by Round-Trip Delay and Host SPI

The SCLK limited by round-trip delay is computed by finding the total propagation delay of the path that starts from the host MOSI and back to the host MISO through an ADC, which is marked as "round-trip" in Figure 8.

$$t_{RTPD\_max} = t_{PD\_HOST\_SCLK} + 2 \times t_{PD\_BUF} + t_{ADC\_SCLK\_MISO} + t_{HOST\_SCLK\_MISO} \quad (7)$$

$$t_{RTPD\_max} = 0\text{ ns} + 2 \times 4.5\text{ ns} + 6.5\text{ ns} + 1.2\text{ ns}$$

$$t_{RTPD\_max} = 16.7\text{ ns}$$

$$t_{SCLK\_min} \geq 2 \times t_{RTPD\_max} \quad (8)$$

$$t_{SCLK\_max} = \frac{1}{2 \times 16.7 \times 10^{-9}} \cong 30\text{ MHz} \quad (9)$$

2.1.2.4 Determining Maximum ADC Sample Clock

The maximum ADC sampling clock assumes that in each sampling interval (or conversion cycle), the ADC performs a sample acquisition, conversion, and data transfer. Figure 9 shows a typical ADC timing diagram for one conversion cycle. The acquisition time and conversion time can be found in the ADC's datasheet. The data transfer time can be computed from the bits transferred and the SCLK period. However, acquisition and data transfer can happen at the same time. Hence, the minimum conversion cycle time is:

$$t_{CONVST\_CYCLE\_min} = t_{CONV} + N \times t_{SCLK\_min} \quad (10)$$

For ADS8900B:

- t_{CONV} = 300 ns
- N = 20 for SDO0 only

NOTE: The time requirement for the SCLK cycle varies depends on the resolution of the ADC resolution; see the ADC datasheet for the SPI mode of transfer.

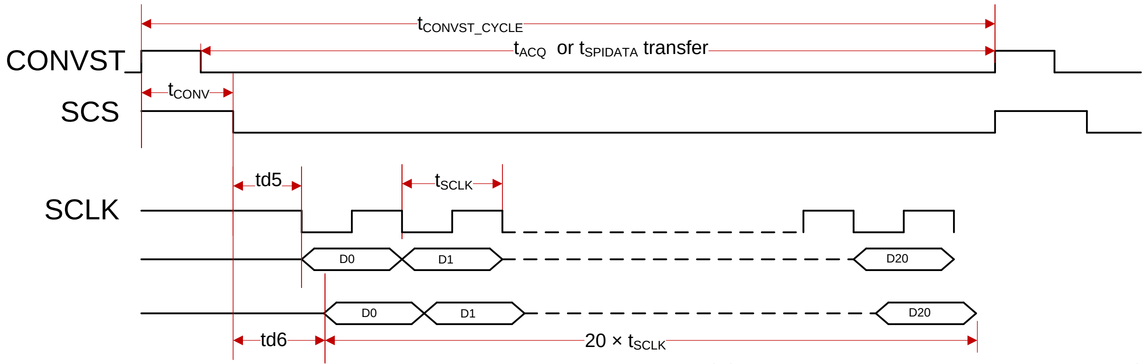


Figure 9. ADS8900B ADC Timing Diagram

Table 6. ADS8900B Timing Parameter

PARAMETER	DESCRIPTION
t_{CONVST_CYCLE}	Time between two consecutive conversion start signal
t_{ACQ}	Acquisition time or SPI data transfer time
t_{CONV}	Conversion time
t_{SCLK}	SPI clock time period
td5	Minimum time required SCS low to SCLK low
td6	Time between SCS low to MISO change

The maximum ADC sampling clock frequency depends on the number of SDO lines and the maximum conversion time for the ADC. Equation 11 shows the relationship between ADC sampling clock frequency and SDO line configuration. Table 7 lists the maximum SCLK frequency ($f_{ADC\_SAMPLECLK\_max}$) for various SDO lines calculated using Equation 11.

$$f_{ADC\_SAMPLECLK\_max} = \left(\frac{1}{\left(N \times \frac{1}{f_{SCLK\_max}} \right) + t_{CONV}} \right) \tag{11}$$

Table 7. SDO Lines versus ADC Sampling Frequency

SDOx	N	$f_{ADC\_SAMPLECLK\_max}$
SDO[0]	20	1 MHz
SDO[0..1]	10	1.6 MHz
SDO[0..3]	5	2.1 MHz

Table 7 shows that a single SDO line is sufficient to achieve a 1-MSPS sampling rate in this non-isolated interface example.

2.1.3 DAQ Timing Analysis With Digital Isolator in Data Path

The isolated DAQ system shown in Figure 10 is typical of such a system and is the subject of the next timing analysis example. The interface between the ADC and host is the SPI with a level translator and a digital isolator. Again, the analysis assumes that in each sampling interval, the ADC acquires the sample, converts it, and sends the serialized data to the host.

The objectives of the timing analysis are:

- Compute the maximum SPI clock rate (serialized data rate)
- Compute the maximum sampling rate of the ADC

As described in previous sections, the maximum SPI clock is computed by estimating the total propagation delay and total PWD of the SPI. The ADC sampling rate is calculated from the SPI clock rate and ADC acquisition time. Figure 10 shows the timing parameter that is considered for this timing analysis example.

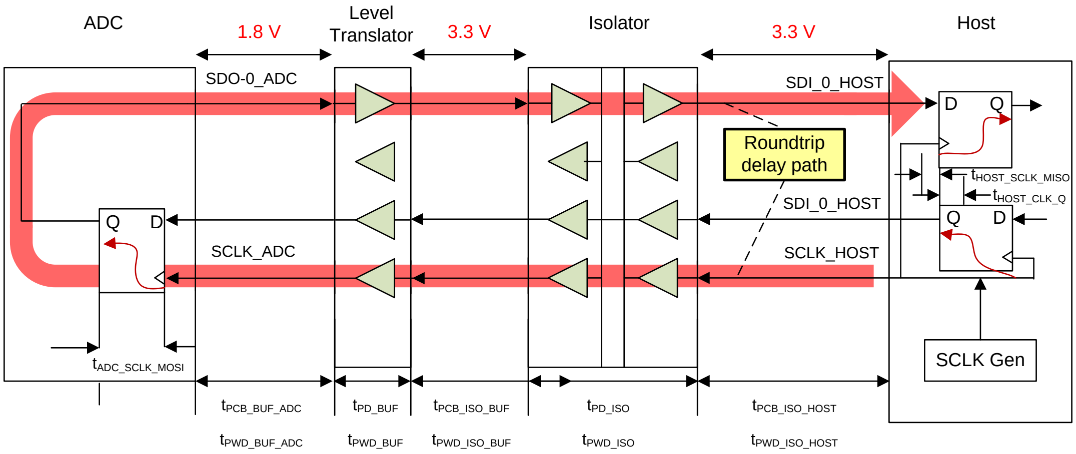


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Figure 10. Isolated SPI ADC-Host Interface

2.1.3.1 Determining Maximum SPI Clock (SCLK)

As described in Section 2.1.2.1, in a low latency system, the converted data must be made available to the host system with minimum delay. Compute the SPI clock for two cases:

1. SPI clock limited by ADC
2. SPI clock limited by round-trip delay

The minimum of these two cases is the maximum SPI clock. Section 2.1.3.2 details the procedure to find the maximum SPI clock for isolated SPI example.

$$f_{SCLK\_max} = \min\left(f_{SCLK\_max\_adc\_limited},\ f_{SCLK\_max\_rtpd\_limited}\right) \tag{12}$$

2.1.3.2 Determining Maximum SCLK Limited by ADC

Computing the maximum SCLK limited by the ADC is similar to the procedure described in Section 2.1.2.2. Table 8 lists the associated timing parameter values taken from respective device datasheets. In this example, assume the level translator is not required and make the corresponding timing values zero.

Table 8. Host to ADC Clock Path Timing

PARAMETER	DELAY (ns)	REMARK
$t_{PWD\_HOST\_max}$	0	Maximum PWD of host driver, typical value in tens of ps for FPGA
$t_{PWD\_BUF\_max}$ (t_{PWD_BUF} + t_{OD_BUF})	0	No buffer or level translator in the TIDA-01035
$t_{PWD\_ISO\_max}$ (t_{PWD_ISO} + t_{OD_ISO})	4.20	PWD of isolator (ISO7840)
$t_{SCLK\_PH\_min}$ (0.45 × 13.33)	5.99	High pulse time for 75-MHz clock with 45% duty cycle
$t_{SK\_BUF\_max}$	0	Buffer skew (no buffer in the TIDA-01035)
$t_{SK\_ISO\_max}$	2.50	Isolator skew
$t_{SCLK\_PH\_ISO}$	12.69	—

$$t_{SCLK\_PH\_ISO} = t_{SCLK\_PH\_min} + t_{PWD\_ISO\_max} + t_{SK\_ISO\_max} + t_{PWD\_BUF\_max} + t_{SK\_BUF\_max} + t_{PWD\_HOST\_max} \tag{13}$$

$$t_{SCLK\_PH\_ISO} = 12.69\ \text{ns}$$

$$f_{SCLK\_max\_adc\_limited} = \frac{1}{2 \times t_{SCLK\_PH\_ISO}} = \frac{1}{2 \times 12.69\ \text{ns}} = 39.4\ \text{MHz} \tag{14}$$

The maximum ADC supported SCLK for isolated system with added isolator in data path is $f_{SCLK\_max\_adc\_limited}$ ≅ 39 MHz

2.1.3.3 SCLK Limited by Round-Trip Delay and Host SPI

The SCLK limited by round-trip delay computation for the isolated DAQ example is similar to the procedure detailed in Section 2.1.2.2. Table 9 lists all the timing parameter values in the round-trip path. The total round-trip delay is given by Equation 15:

$$\begin{aligned} t_{RTPD\_ISO\_max} = {} & t_{PD\_HOST\_SCLK} + t_{PCB\_HOST\_ISO} + 2 \times t_{PD\_ISO} + t_{PCB\_ISO\_BUF} + 2 \times t_{PD\_BUF} \\ & + t_{PCB\_BUF\_ADC} + t_{ADC\_CLK\_MISO} + t_{PCB\_ADC\_BUF} + t_{PCB\_BUF\_ISO} + t_{PCB\_ISO\_HOST} \\ & + t_{HOST\_SCLK\_MISO} \end{aligned} \tag{15}$$

Table 9. Timing Parameters in Isolated SPI Example

PARAMETER	DELAY (ns)	DESCRIPTION
$t_{PD\_HOST\_SCLK}$	0	Propagation delay host SCLK to output
$t_{PCB\_HOST\_ISO}$	1.5	PCB delay between host to Isolator
$t_{PD\_ISO} \times 2$	32.0	Isolator propagation delay
$t_{PCB\_ISO\_BUF}$	0	PCB delay between Isolator to buffer or level translator
$t_{PD\_BUF} \times 2$	0	Buffer or level translator propagation delay
$t_{PCB\_BUF\_ADC}$	0	PCB delay between buffer to ADC
$t_{ADC\_CLK\_MISO}$	6.5	ADC clock to output delay
$t_{PCB\_ADC\_BUF}$	0	PCB delay between ADC to buffer
$t_{PCB\_BUF\_ISO}$	0	PCB delay between buffer to isolator
$t_{PCB\_ISO\_HOST}$	0	PCB delay between isolator to host
$t_{HOST\_SCLK\_MISO}$	1.2	Setup time of host MISO line
$t_{RTPD\_ISO\_max}$	41.2	—

The minimum SCLK period limited by the round-trip delay is:

$$t_{SCLK\_min\_rtpd\_limited} \geq 2 \times t_{RTPD\_ISO\_max}$$

$$f_{SCLK\_max\_rtpd\_limited} = \frac{1}{2 \times 41.2 \times 10^{-9}} \cong 12.1\,\text{MHz} \quad (16)$$

Hence, f_{SCLK_max} = 12 MHz.

The round-trip delay limits the SPI SCLK to 12 MHz; any delay added in the round-trip path further reduces the maximum SCLK.

2.1.3.4 Determining Maximum ADC Sample Clock

The maximum ADC sampling clock rate computation procedure is same as described in Section 2.1.2.4 and Equation 11 is repeated for reference:

$$f_{ADC\_SAMPLECLK\_max} = \left(\frac{1}{t_{CONVST\_CYCLE\_min}} \right) = \left(\frac{1}{t_{CONV} + N \times t_{SCLK\_min}} \right) \quad (17)$$

The ADC sampling clock rate for a different SDO line configuration is calculated using Equation 17 and listed in Table 10.

Table 10. Maximum ADC Clock and SDO Line Configuration

SDOx	N	$f_{ADC\_SAMPLECLK\_max}$
SDO[0]	20	508 kHz
SDO[0..1]	10	1.1 MHz
SDO[0..3]	5	1.4 MHz

These results show the design needs at least two SDO lines to achieve a 1-MSPS sampling rate in this isolated SPI example.

2.1.4 Maximizing Sample Rate With Source-Synchronous Mode

Part of TI's family of high performance SAR ADCs, both the ADS9110 and ADS8900B possess a source-synchronous feature that significantly overcomes the limitation of SCLK reduction due to round-trip propagation delay. The source-synchronous mode provides a clock output (on the RVS pin) synchronized to the output data (SDOx data lines). The host can receive the data with a slave SPI. The maximum ADC sampling clock frequency is determined by selecting the minimum of SCLK limited by ADC and RVS limited by the host.

$$f_{SCLK\_max} = \min\left(f_{SCLK\_max\_adc\_limited}, f_{SCLK\_max\_host\_limited}\right) \tag{18}$$

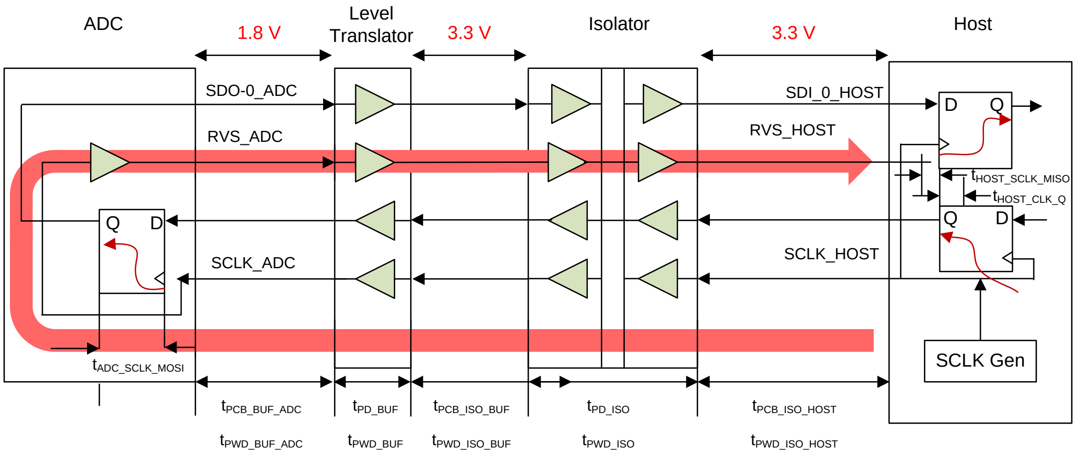

Figure 11. Isolated SPI in Source-Synchronous Mode

2.1.5 Determining Maximum SCLK Limited by ADC and Host

Computing the maximum SCLK limited by the ADC is described in Section 2.1.3.2. A level translator is not required, and corresponding timing values are made zero.

$$f_{SCLK\_max\_adc\_limited} = \frac{1}{2 \times t_{SCLK\_PH\_ISO}} = \frac{1}{2 \text{ x } 12.69 \text{ ns}} \; 39.4 \text{ MHz} \tag{19}$$

Hence, the maximum SCLK limited by ADC is:

$$f_{SCLK\_max\_adc\_limited} \cong 39 \text{ MHz}$$

Similarly, the SCLK limited by the host can be computed as:

$$\begin{aligned} t_{SCLK\_min\_host\_limited} &= t_{RVS\_SCLKPH\_ISO} \\ &= t_{SCLK\_PH\_min} + t_{PWD\_BUF\_max} + t_{SK\_BUF\_max} \\ &+ \; t_{PWD\_ISO\_max} + t_{SK\_ISO\_max} + t_{PWD\_ADC\_max} \end{aligned} \tag{20}$$

Table 11. ADC to Host Clock Path Timing

PARAMETER	DELAY (ns)	REMARK
$t_{SCLK\_PH\_min}$ (0.45 × 2 × 12.69)	11.4	High pulse time for $f_{SCLK\_max\_adc\_limited}$ clock with 45% duty cycle
$t_{PWD\_BUF\_max}$ (t_{PWD_BUF} + t_{OD_BUF})	0	No buffer or level translator in the TIDA-01035
$t_{SK\_BUF\_max}$	0	Buffer skew (no buffer in the TIDA-01035)
$t_{PWD\_ISO\_max}$ (t_{PWD_ISO} + t_{OD_ISO})	4.2	PWD of isolator (ISO7840)
$t_{PWD\_ADC\_max}$	0	Maximum PWD of ADC SDO output lines
$t_{SK\_ISO\_max}$	2.5	Isolator skew
$t_{RVS\_SCLKPH\_ISO}$	18.1	—

$$t_{SCLK\_min\_host\_limited} = 18.1\,\text{ns} \tag{21}$$

$$f_{SCLK\_max\_adc\_limited} = \frac{1}{2 \times t_{SCLK\_min\_host\_limited}} = \frac{1}{2 \times 18.1\,\text{ns}} = 27.6\ \text{MHz} \tag{22}$$

The value of PCB trace delay does not matter if the user can route RVS and SDOx at equal length and keep the differential length to a minimum. The differential length between RVS and SDOx results in a skew and that must be considered to calculate $t_{RVS\_SCLKPH\_ISO}$.

Hence, with f_{SCLK_max} = 27.6 MHz, the maximum ADC sampling rate is computed for different SDOx line configurations and listed in Table 12.

Table 12. Maximum ADC Sample Rate in Source-Synchronous Mode

SDOx	N	$f_{ADC\_SAMPLECLK\_max}$
SDO[0]	20	975 kHz
SDO[0..1]	10	1.5 MHz
SDO[0..3]	5	2.0 MHz

These results show that it possible to achieve a sampling rate of 2 MSPS using source-synchronous mode and a multiSPI configuration.

2.1.6 Concluding Remarks

This design guide provides a comprehensive timing analysis for non-isolated and isolated ADC interfaces. The objective of the timing analysis is to determine the maximum ADC sampling rate and maximum SPI clock to maximize ADC sample rate. The maximum SPI clock ensures minimum latency. Digital isolators have large propagation delays, which limit the maximum SPI clock. Source-synchronous mode and a multiSPI configuration make it possible to achieve a high sampling rate with digital isolators.

2.2 Additive Jitter Due to Digital Isolator

The ADC SNR performance is a function of the sampling clock jitter at a high input signal frequency. The digital isolator's additive jitter to the sample clock limits the signal chain SNR. To the first order, the jitter impact on the SNR can be calculated as:

$$\text{SNR} = -20 \log(2\pi f_{in} \times t_{jitter}) + 10 \log(\text{OSR}) \tag{23}$$

where:

- f_{in} is the input signal frequency
- t_{jitter} is the total jitter of the ADC (internal clock + external clock)
- OSR is the oversampling ratio (only for the sigma-delta ADC)

Figure 12 shows that the SNR impact from jitter increases with the signal frequencies because it results in a larger measurement error. Find more details in the TIDA-00732 design guide, *18-Bit, 2-MSPS Isolated Data Acquisition Reference Design for Maximum SNR and Sampling Rate* (TIDUB85).

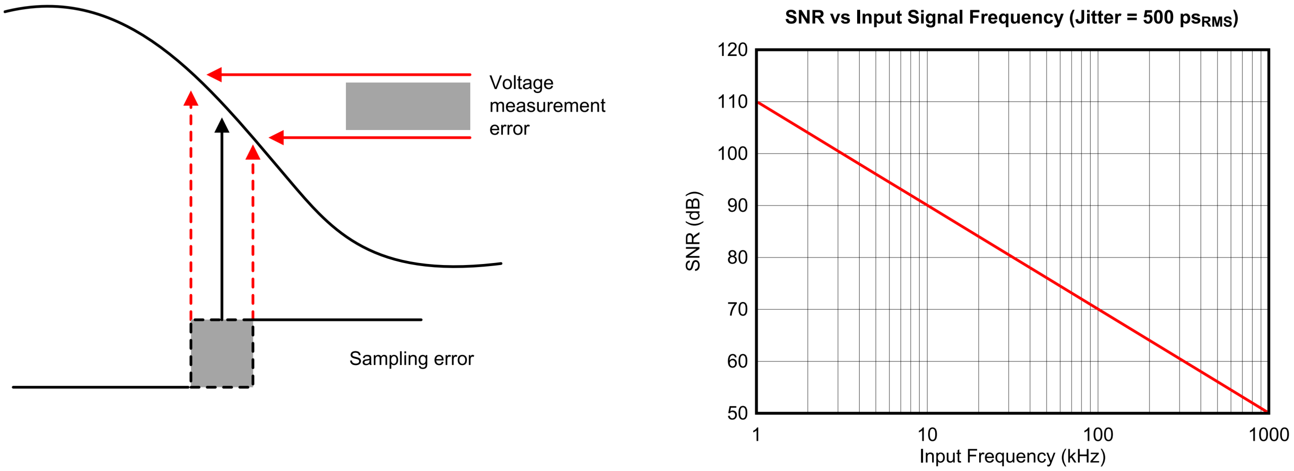

Figure 12. Error Due to Jitter on Sampling Clock

2.3 TIDA-01035 Solution

2.3.1 Compensating for Propagation Delay

The ADS8900B has a multiSPI digital interface that allows the host controller to operate at a slower SPI SCLK and still achieves the required sampling rate. The multiSPI module offers the following options to reduce SCLK speed:

- Option to increase the width of the output data bus: 1, 2, and 4 SDO lines
- ADC mode or source-synchronous mode

The multiSPI option allows the SPI SCLK to be reduced which in turn reduces the impact on the sampling rate of the propagation delay. If the reduced SCLK rate is still above the loopback delay, then use source-synchronous mode.

In ADC mater mode or source-synchronous mode, the SCLK from the host is looped back by the ADC along with the data. The clock and data are synchronous in source-synchronous mode; therefore, the propagation delay of the isolator has no impact on the data rate.

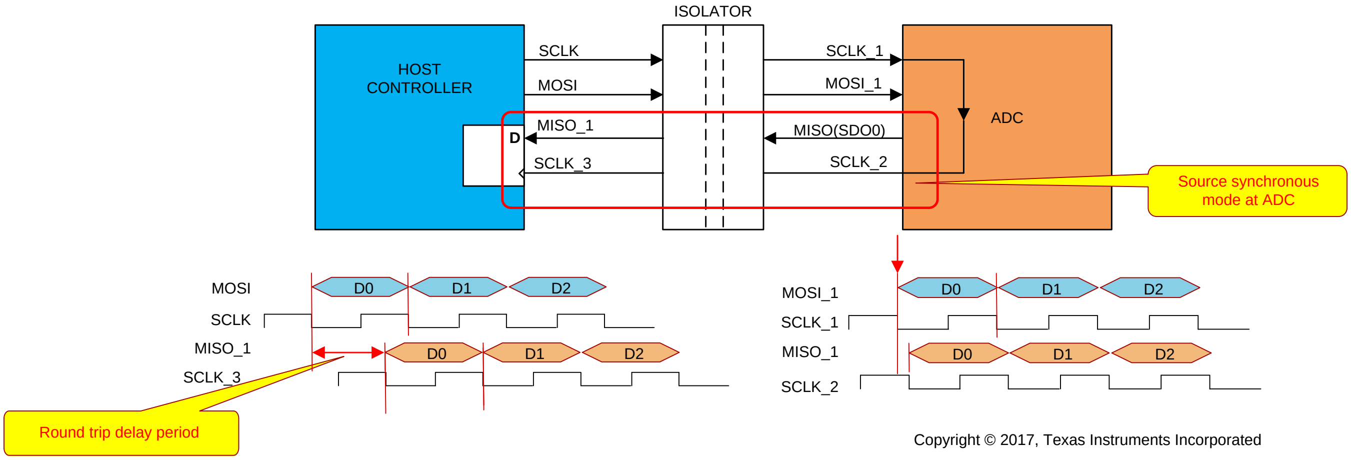

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Figure 13. ADS8900B SPI Source-Synchronous Mode With Host and Slave End Timing Waveform

As illustrated in Figure 13, in ADC-master or source-synchronous mode, the device provides a synchronous output clock (on the RVS pin) along with the output data (on the SDO-x pins). The ADC-master or source-synchronous mode completely eliminates the effect of isolator delays and the clock-to-data delays, which are typically the largest contributors in the overall delay.

2.3.2 Mitigating SNR Degradation Due to Jitter

As per the analysis done in the TIDA-00732 TI Design, the jitter on the conversion clock "CONVST" signal degrades the performance of the ADC SNR at higher input signal frequency and will impact the system performance. Generating a CONVST signal with a low-jitter oscillator will address the issue and mitigate jitter impact and improve SNR performance by almost 12 dB. The solution provided in the TIDA-00732 may not be suitable for the system that host controlled sample clock (CONVST) generation. As a result, this TI Design addresses both digital isolate propagation delay and SNR degradation due additive jitter on the host controlled sample clock.

As shown in Figure 14, the host generated the ADC sample clock CONVST, which is derived from SYS_CLK. A low-jitter SYS_CLK_ISO is generated at local end (ADC side) and passed through isolator and used as host side system clock (SYS_CLK).

The ADC sample clock (CONVST) signal is derived from CONVST_ISO and passed to flip-flop to synchronize with SYS_CLK_ISO before it is connected to the ADC. This helps to mitigate isolator additive jitter on the sampling clock (CONVST). Figure 15 shows the timing diagram jitter mitigation logic implemented in the TIDA-01035.

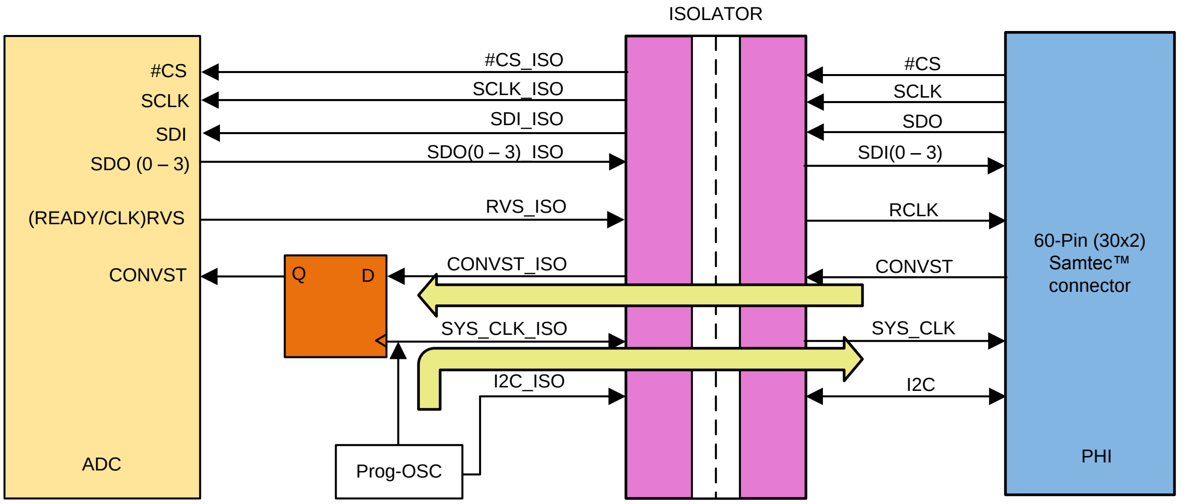

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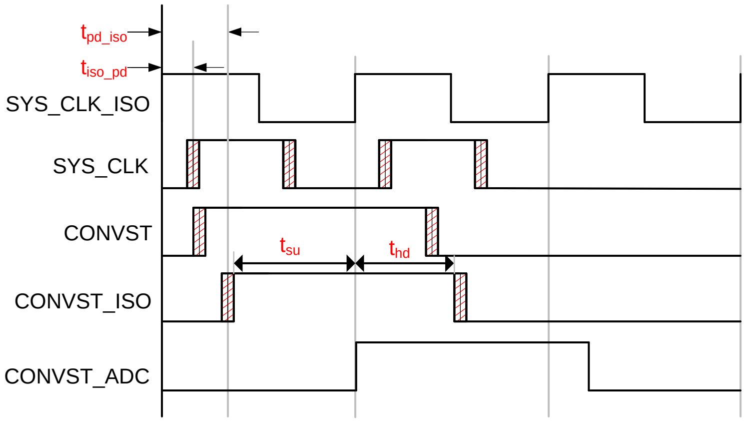
Figure 14. TIDA-01035 Jitter Optimization Technique



t_{rt_pd} = Round-trip propagation delay
t_{iso_pd} = Isolator propagation delay
t_{su} = Setup time available for FF
t_{hd} = Hold time available for FF

Figure 15. TIDA-01035 Timing Diagram

From Figure 15:

- SYS_CLK_ISO: Low jitter system clock on ADC side
- SYS_CLK: Jitter in SYS_CLK after passing through the digital isolator
- CONVST: Host generates CONVST start signal from SYS_CLK with jitter
- CONVST_ISO: More jitter on CONVST_ISO signal after passing through digital isolator
- CONVST_ADC: Jitter in CONVST is minimized after synchronizing with SYS_CLK_ISO on ADC side

2.4 Circuit Design

To optimize the performance of the 20-bit, 1-MSPS DAQ system, the input buffer, anti-aliasing filter, and reference driver must be designed in such a way that the performance is equal to or greater than the ADC performance.

2.4.1 Analog Input Front-End (Input Buffer and Anti-Aliasing Filter)

Figure 16 describes the TIDA-01035's analog front-end, which highlights the differential input filter, high-output drive differential input buffer, and anti-aliasing filter. A high-speed, fully differential amplifier (FDA) with a programmable output common mode is well suited to drive the data converter due to its inherent nature to increase immunity to external common-mode noise and reduce even order harmonics.

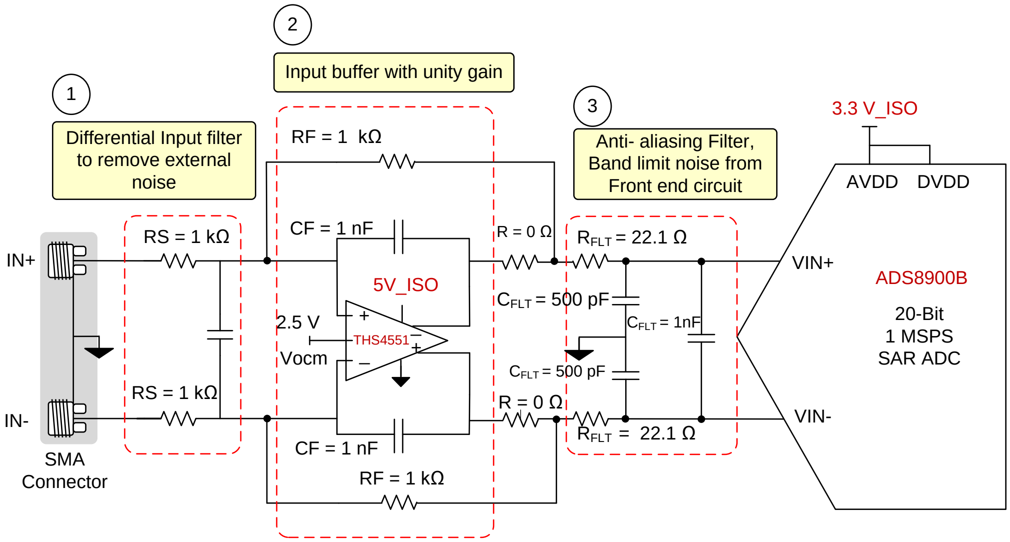


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Figure 16. TIDA-01035 Analog Front End

The TIDA-01035 is designed with the THS4551 FDA configured as an unity gain second-order active low-pass filter, which drives the 20-bit, 1-MSPS ADS8900B SAR ADC at full dynamic range. The transfer function of this filter is determined by Equation 24:

$$\frac{V_{OD}}{V_{IN}} = \frac{RF}{RS} \times \left(\frac{1}{1 + j2\pi f \times RF\, C_F}\right) \times \left(\frac{1}{1 + j2\pi f \times 2 \times R_{FLT} C_{FLT}}\right) \qquad (24)$$

The amplifier gain is determined by the RF and RS ratio and both were chosen to be 1 kΩ, so the FDA is configured as an unity gain buffer. In order to satisfy the design's targeted spec of supporting 100-kHz input signals, the anti-aliasing filter cutoff frequency was designed to be ≅ 4 MHz. The differential mode capacitor added across the filter output helps remove high-frequency differential noise and increase THD performance. Take care to select passive components with minimum voltage and temperature coefficients in order to preserve THD performance for varying input and temperature conditions.

2.4.2 Reference Buffer Circuit

The reference driver circuit, illustrated in Figure 17, generates a voltage of 5-V DC using a single 5.2-V supply. This circuit is suitable to drive the reference of the ADS8900B at higher sampling rates up to 1 MSPS. The reference voltage of 5 V in this TI Design is generated by the high-precision, low-noise REF5050 circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter formed by resistor R90 and capacitor C88.

The R_{BUF_FLT} is R93, and the C_{BUF_FLT} is C96 at the output of the reference driving ADC reference input. The value of R_{BUF_FLT} and C_{BUF_FLT} can be found using Equation 25:

$$C_{BUF\_FLT} = \frac{I_{REF} \times T_{CONV\_MAX} \times 2^N}{V_{REF}} \qquad (25)$$

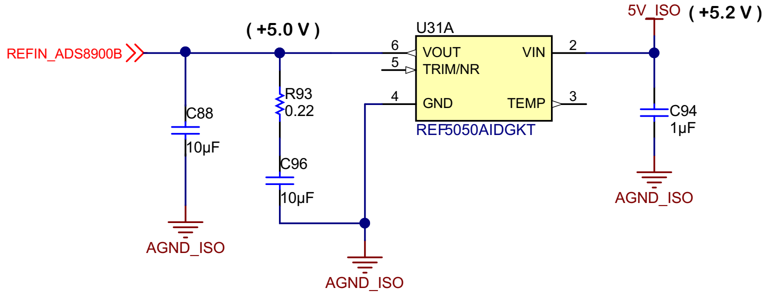


Figure 17. Reference Buffer Circuit

2.4.3 Common-Mode Voltage (VOCM)

The external REF5050 high-precision, ultra-low noise, low drift voltage reference generates both ADC voltage reference and signal input common-mode in order to ensure the complete dynamic range of the ADS8900B is used. The voltage is at a value of 2.5 V (5 V / 2) by using the REF5050 and the OPA376 precision, low-noise amplifier as a buffer, as illustrated in Figure 18.

The FDA common-mode voltage (VOCM) should be at mid-supply to achieve maximum output dynamic range. VOCM is derived from the supply voltage with resistive divider network. The VOCM voltage is buffered using the OPA376 op amp with in the loop compensation method. This configuration has good stability when driving larger capacitive loads.

Resistor R96 is an isolation resistor that is connected in series between the op amp output and the capacitive load to provide isolation and avoid oscillations. Capacitor C95 between the op amp output and the inverting input becomes the dominant AC feedback path at higher frequencies. This configuration allows heavy capacitive loading while keeping the loop stable. The feedback resistor R94 helps to maintain the output DC voltage same as the non-inverting input of the op amp.

Resistor R96 should have a 10% lower value compared to the load resistance. The combination of resistor R95 and capacitor C100 forms a low-pass filter with a cutoff frequency of 159 Hz. This filter will clean the ripple and noise.

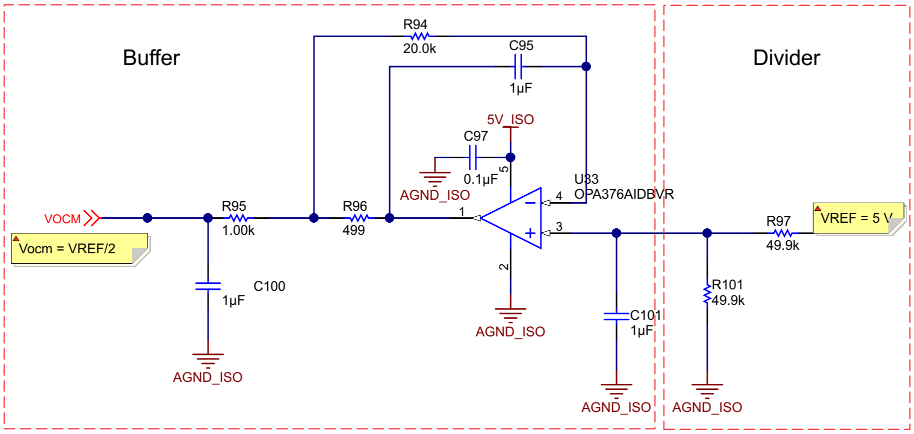


Figure 18. Common-Mode Voltage

2.4.4 Clock Circuit Section

The clock source is an essential component in a signal chain design, specifically when driving the ADC sample clock. Clock jitter directly impacts ADC SNR performance and becomes proportionally greater at higher input signal frequencies. It is important that the jitter from the selected clocking source is significantly less than the jitter introduced by the digital isolator.

This TI Design has two master clock sources that can be used for ADC sample clock generation, jitter cleaner logic, and host interface synchronization. Table 13 shows how to select one of the sources by properly setting indicated resistor jumpers:

- Crystal oscillator (3.3 V, 125 MHz, 50 ppm, low jitter, 1.9-ps jitter)
- LMK61E2: Programmable crystal oscillator (3.3 V, 150 MHz, 90-fs jitter)

Table 13. Master Clock Selection

SERIAL NO	MASTER CLOCK	RESISTOR MOUNTING	REMARKS
1	Crystal oscillator	R14: Populate	3.3 V, 125 MHz, 50 ppm, low jitter, 1.9-ps jitter
		R17: Do not populate	
2	Programmable crystal oscillator (LMK61E2)	R14: Do not populate	3.3 V, 150 MHz, 90-fs jitter (Frequency of oscillator must be programmed to 125 MHz through I^2C interface)
		R17: Populate	

2.4.4.1 Programming LMK61E2

The LMK61E2 programmable crystal oscillator can be program using a USB2ANY programming cable with the CodeLoader4 software programming tool. The setup file of LMK61E2 can be downloaded from the CodeLoader webpage.

Figure 19 shows the hardware setup of the TIDA-01035 with USB2ANY hardware. Table 14 lists the connection definitions.

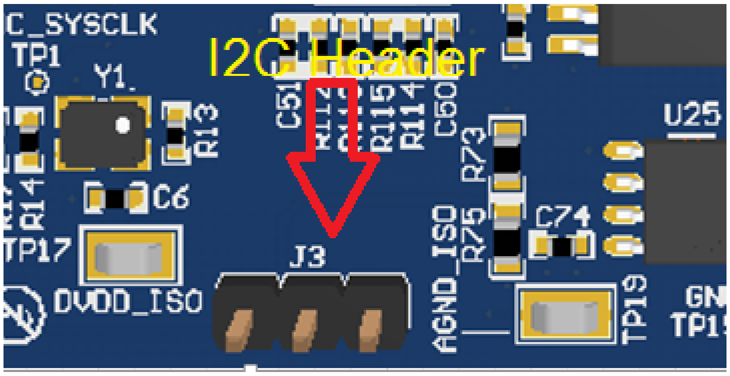


Figure 19. LMK61E2 Programming Setup

Table 14. USB2ANY Connection

SIGNAL NAME	TIDA-01035	USB2ANY
SCL	Pin no 3 / J3	Pin no 2 /J4
SDA	Pin no 2 / J3	Pin no 1 /J4
GND	Pin no 1 / J3	Pin no 5 /J4

Programming Procedure

1. Open the CodeLoader 4 programming tool and select the LMK61E2 device.

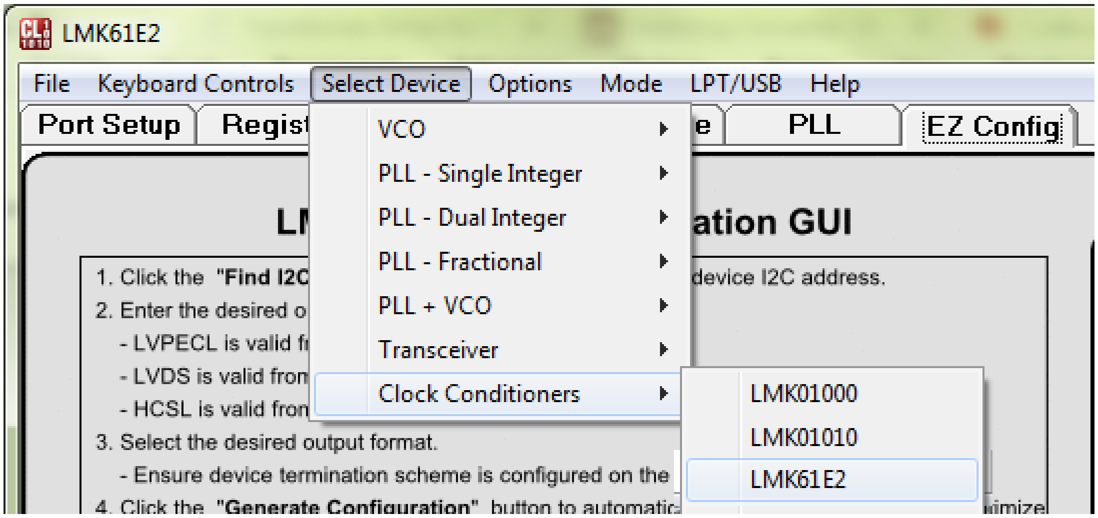
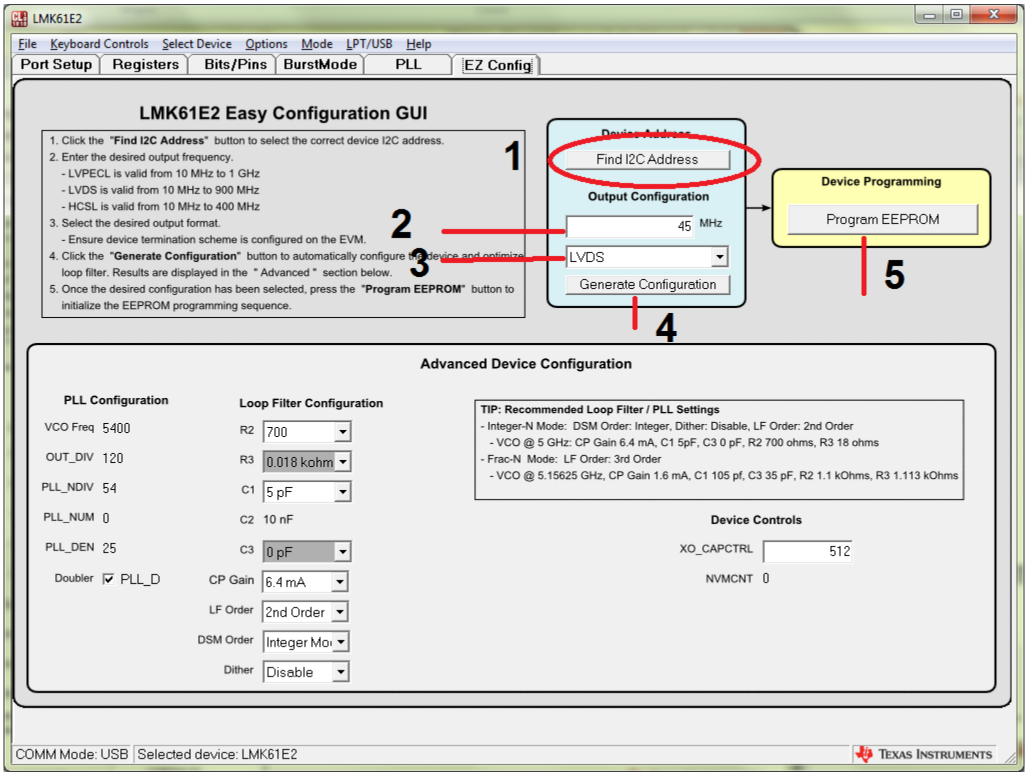


Figure 20. Select Device

2. Go to the EZ Config tab. Under *Output Configuration*, enter "45" for MHz and the output type as "LVDS". Then generate the configuration and click the Program EEPROM button. Figure 21 illustrates these steps (as 1 to 5).



LMK61E2 Easy Configuration GUI

1. Click the **"Find I2C Address"** button to select the correct device I2C address.
2. Enter the desired output frequency.
   - LVPECL is valid from 10 MHz to 1 GHz
   - LVDS is valid from 10 MHz to 900 MHz
   - HCSL is valid from 10 MHz to 400 MHz
3. Select the desired output format.
   - Ensure device termination scheme is configured on the EVM.
4. Click the **"Generate Configuration"** button to automatically configure the device and optimize loop filter. Results are displayed in the " Advanced " section below.
5. Once the desired configuration has been selected, press the **"Program EEPROM"** button to initialize the EEPROM programming sequence.

45 MHz
LVDS

VCO Freq 5400
OUT_DIV 120
PLL_NDIV 54
PLL_NUM 0
PLL_DEN 25
Doubler ☑ PLL_D

R2 700
R3 0.018 kohm
C1 5 pF
C2 10 nF
C3 0 pF
CP Gain 6.4 mA
LF Order 2nd Order
DSM Order Integer Mo
Dither Disable

TIP: Recommended Loop Filter / PLL Settings
- Integer-N Mode: DSM Order: Integer, Dither: Disable, LF Order: 2nd Order
  - VCO @ 5 GHz: CP Gain 6.4 mA, C1 5pF, C3 0 pF, R2 700 ohms, R3 18 ohms
- Frac-N Mode: LF Order: 3rd Order
  - VCO @ 5.15625 GHz, CP Gain 1.6 mA, C1 105 pf, C3 35 pF, R2 1.1 kOhms, R3 1.113 kOhms

XO_CAPCTRL 512
NVMCNT 0

COMM Mode: USB
Selected device: LMK61E2

Figure 21. Steps to Configure LMK61E2 GUI

2.4.5 Isolator Section

The TIDA-00732 uses TI's ISO784x and ISO1541 family of high-performance isolators to provide the required system protection. The ISO784x series supports signaling rates up to 100 Mbps with typically low propagation delay (11 ns) and a wide supply voltage (2.25 to 5.5 V). These isolators are reinforced with very high immunity and a 5.7-kV_{RMS} isolation voltage with very low jitter. The system requires six isolation channels for standard SPI communication and ten isolation channels for multiSPI. The ISO784x isolators are used for SPI and ADC control lines while the ISO1541 bidirectional isolator is used for I^2C isolation.

2.4.6 Power Supply Section

The design requires isolated and non-isolated power rails to various components. The following section details the design procedure for the various power supply rails.

2.4.6.1 DC-DC

The LMZ14203TZ-ADJ simple switcher is capable of accepting 6- to 46-V DC input and deliver a 0.8- to 6-V output with 90% efficiency. The undervoltage lockout is selected at 7.97 V, which helps to enable the LMZ4203TZ-ADJ.

To set 5-V output voltage, the resistor R_{FBT} (R25) and R_{FBB} (R31 + R36) decide the output voltage of the LMZ14203TZ-ADJ. For a 5.6-V output:

$$\frac{R_{FBT}}{R_{FBB}} = \left(\frac{5.6}{0.8}\right) - 1 \tag{26}$$

$$\frac{R_{FBT}}{R_{FBB}} = 6$$

$$R_{FBT} = \frac{5.62\ K}{6} = 932\ \Omega \tag{27}$$

Therefore, R25 = 5.62K , R31 = 931 Ω, and R36 = 1 Ω.

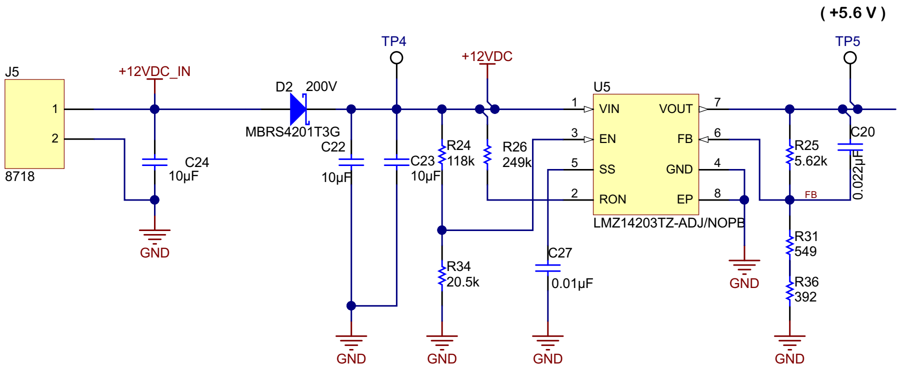


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Figure 22. DC-DC Power Supply

2.4.6.2 LDOs

The TPS7A4700 is a positive voltage (36 V), ultra-low-noise (4 μV_{RMS}) LDO capable of sourcing a 1-A load. The TPS7A470x is designed with bipolar technology primarily for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This feature makes the device ideal for powering op amps, ADCs, DACs, and other high-performance analog circuitry.

The TPS7A4700RGWR has ANY-OUT™ programmable pins to program the desired output voltage. The sum of the internal reference voltage (V_{REF} = 1.4 V) plus the accumulated sum of the respective voltage is assigned to each active pins. The ANY-OUT pins (Pin 8, Pin 1, and Pin 12) are programmed to active low to get 3.3 V at the output.

The TPS709 series of linear regulators are ultra-low quiescent current devices designed for power sensitive applications. A precision band-gap and error amplifier provides 2% accuracy over temperature. The LDO can accept 2.7- to 30-V input voltages and deliver fixed output voltages 1.2 to 6.5 V with a maximum 200-mA output current. The TPS70918DBVT generates 1.8 V from 5-V DC of the LMZ14203TZ-ADJ DC-DC converter.

2.4.6.3 Push-Pull Transformer

The SN6501 is a transformer driver designed for low-cost, small form-factor, isolated DC-DC converters using push-pull topology. The device includes an oscillator that feeds a gate-drive circuit. The gate drive, comprising a frequency divider and a break-before-make (BBM) logic, provides two complementary output signals that alternately turn the two output transistors on and off.

The SN6501 transformer driver is designed for low-power push-pull converters with input and output voltages in the range of 3 to 5.5 V. While converter designs with higher output voltages are possible, take care that higher turns ratios do not lead to primary currents that exceed the SN6501 specified current limits.

The TIDA-01035 uses the recommended transformer inform the SN6501 datasheet. For transformer selection and isolation power supply design, see the SN6501 datasheet. Table 15 shows key parameters of the transformer.

Table 15. Transformer Specification

PARAMETER	VALUE
Voltage, time	11 µs
Turns ratio	1.1:1 ± 2%
Switching frequency	150 kHz min
Di electric	6250 rms, 1 second

3 Getting Started Hardware and Software

3.1 Host Interface

The TIDA-01035 system performance can be evaluated using TI's Precision Host Interface (PHI) controller. PHI is TI's SAR ADC evaluation platform, which supports the entire TI SAR ADC family. By using PHI, the TIDA-01035 easily communicates with the host PC using a USB interface. PHI supports the ADS8900B multiSPI and onboard configuration I^2C EEPROM interface. PHI GUI software can be used to evaluate both AC and DC parameter of the ADS8900B.

For more information on PHI, see the ADS8900BEVM-PDK product page.

3.2 Hardware Functional Block

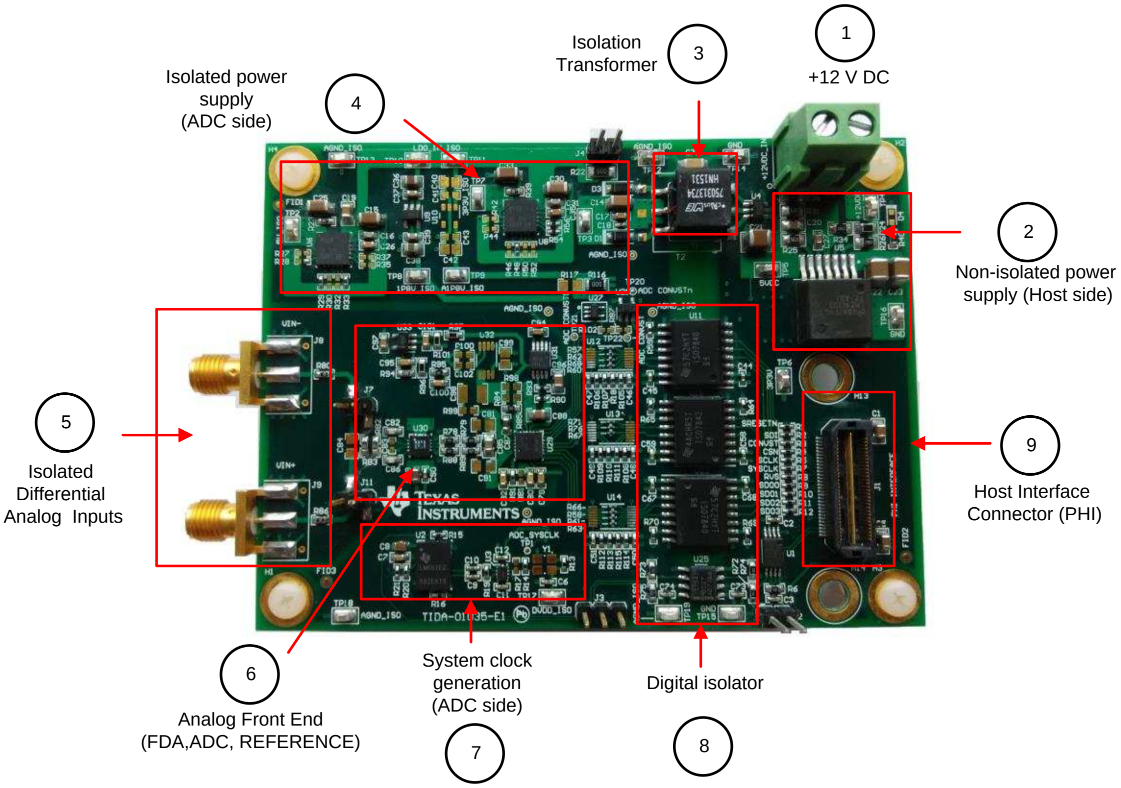


Figure 23. TIDA-01035 Hardware

Figure 23 shows various hardware functional blocks of the TIDA-01035 and function of each block:

1. 12-V DC power supply input connector that accepts 9- to 12-V DC input to power the TIDA-01035
2. Host-side DC-DC buck convertor that generates 5 V from the 12-V input
3. Isolation transformer for power supply isolation and isolated power that is generated with the SN6501 push-pull transformer driver
4. Isolated power supply rails block that generates 5-V, 3.3-V, and 1.8-V power rails
5. Differential analog inputs connector
6. Analog front-end circuits (ADC ADS8900B, THS4551, REF5050)
7. System clock generation
8. Digital isolator for data isolation (SPI and I^2C)
9. PHI interface connector, which uses the TIDA-01035 to communicate with the host PC through USB interface

3.2.1 Operation Mode

The TIDA-01035 hardware had provision to see performance difference of jitter mitigation mode versus normal mode. Figure 24 shows resistor location in the TIDA-01035 hardware, and Table 16 shows the mode of operation and corresponding resistor jumper configuration.

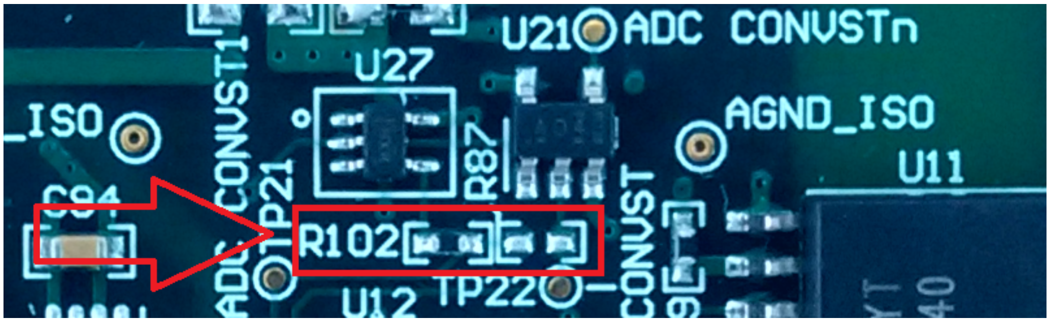


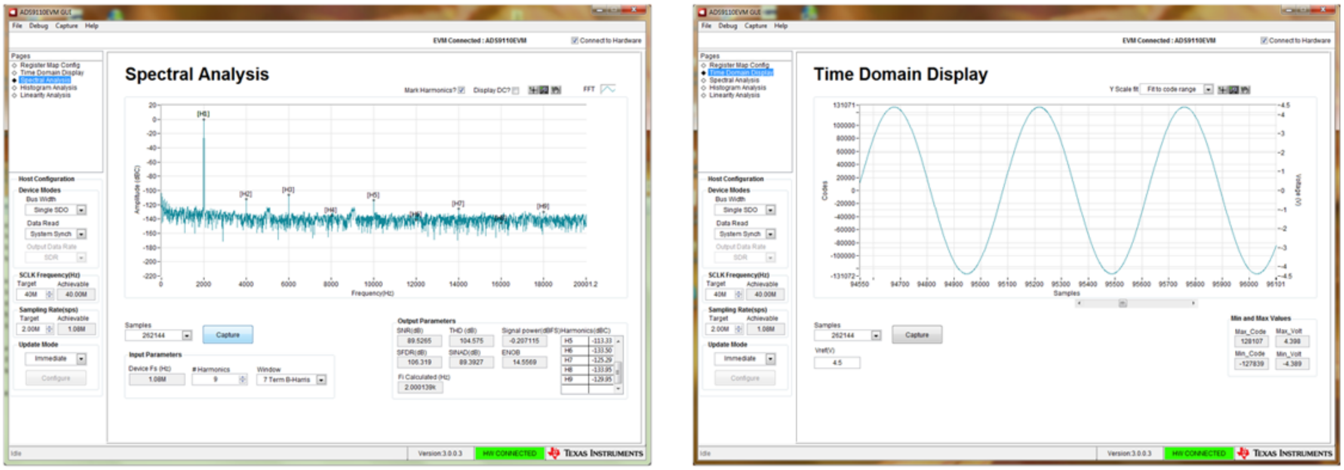
Figure 24. Resistor Jumper

Table 16. Operation Mode Jumper Setting

MODE	RESISTOR SETTING	DESCRIPTION
Normal mode	R87: Populate	CONVST signal is directly connected to the ADC sample clock input (Jitter mitigation logic is bypassed)
	R102: Do not populate	
Jitter mitigation mode	R87: Do not populate	CONVST signal passes through jitter mitigation logic
	R102: Populate	

3.3 Getting Started Application GUI

The PHI GUI software, which is based on the LabVIEW™ platform, validates the TIDA-01035. Figure 25 shows the available test options in the PHI GUI.



Spectral Analysis

EVM Connected : ADS9110EVM

☑ Connect to Hardware

Bus Width: Single SDO
Data Read: System Synch
Output Data Rate: SDR
SCLK Frequency(Hz) Target: 40M Achievable: 40.00M
Sampling Rate(sps) Target: 2.00M Achievable: 1.08M
Update Mode: Immediate

Mark Harmonics? ☑ Display DC? ☐

Samples: 262144

Input Parameters
Device Fs (Hz): 1.08M
Harmonics: 9
Window: 7 Term B-Harris

Output Parameters
SNR(dB): 89.5265
THD (dB): 104.575
Signal power(dBFS): -0.207115
SFDR(dB): 106.319
SINAD(dB): 89.3927
ENOB: 14.5569
Fi Calculated (Hz): 2.000139k

Harmonics(dBC)	
H5	-113.33
H6	-133.50
H7	-125.29
H8	-133.35
H9	-129.95

Time Domain Display

EVM Connected : ADS9110EVM

☑ Connect to Hardware

Y Scale fit: Fit to code range

Samples: 262144
Vref(V): 4.5

Min and Max Values
Max_Code: 128107
Max_Volt: 4.398
Min_Code: -127839
Min_Volt: -4.389

Figure 25. PHI GUI Demonstrate AC Parameter Analysis (Spectral and Time Domain)

The PHI GUI can be used to validate the following system key specifications:

1. Spectral analysis
   - SNR
   - THD
   - SFDR
   - SINAD
   - ENOB
2. Linearity analysis
   - DNL
   - INL
   - Accuracy
3. Histogram analysis
   - Effective resolution

PHI GUI software can be found at http://www.ti.com/product/ADS8900B/toolssoftware.

4 Testing and Results

4.1 Test Setup

Figure 26 shows the TIDA-01035 test setup to validate complete signal chain performance of isolated high-speed, high SNR (20-bit, 1-MSPS) analog input DAQ module.

The test needs to evaluate the performance of the high-speed (1-MSPS) and high-resolution (20-bit) system that is compliant with testing requirements. The setup has a DS360, a standard research systems precision ultra-low distortion waveform generator, which is capable of generating a sine pattern with a signal frequency range of 10 MHz to 200 kHz. The device needs high precision with a very low ripple power supply to power the entire system. This TI Design requires 9- to 12-V DC at 250 mA with high precision and low ripple power. The 12-V DC voltage is generated using the Keithley triple output power supply (2230G). It is capable of generating up to 30 V with 0.03% voltage accuracy and 0.1% current accuracy with simultaneous voltage and current indication.

The data capturing is established using USB 2.0 interface. The testing computer must have one USB port and should support USB 2.0 specification.

Sometimes the signal source may also have noise on top of the signal while generating a sine wave with 100 kHz. To remove this unwanted noise, connect a 100-kHz differential band pass filler in between the signal source and the TIDA-01035 input connector. This will attenuate input noise at a 100-kHz band.

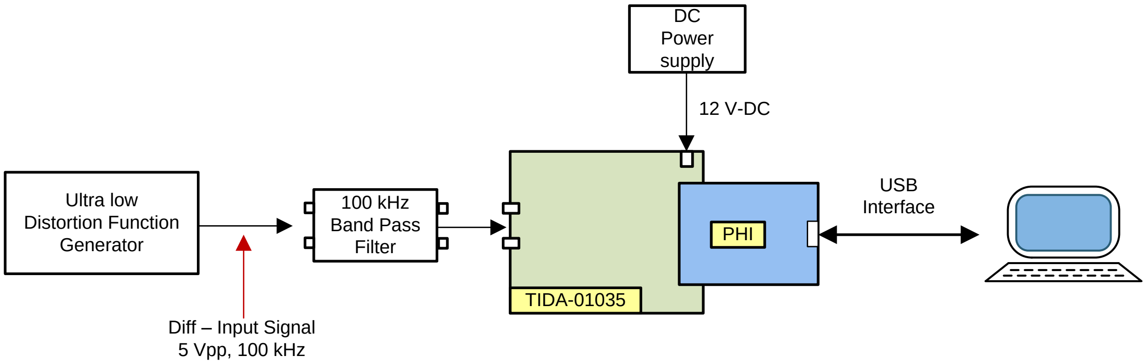


Figure 26. TIDA-01035 Test Setup

Follow these steps to install the PHI GUI software in the host computer before testing:

1. Plug the PHI interface board into the Samtec connector (J1).
2. Configure operation mode using programmable resistor jumper (see Section 3.2.1).
3. Connect 12-V DC of power to the J5 connector. Ensure the positive terminal is connected to the positive input (Pin 2 of J5) and the negative terminal is connected to the negative input (Pin1 of J5).
4. Connect the differential output of the function generator to the differential input terminal (J8 and J9 SMA connector) of the TIDA-01035 board (for a 100-kHz input signal frequency, connect the 100-kHz band pass filter in between signal source and the TIDA-01035 board). Also, make sure both differential signals are balanced and configure as shown in Figure 26.
5. Connect the PHI module to the PC or laptop using micro-USB cable.
6. Switch on the power supply.
7. Switch on the signal source and set the signal source parameter. Then, enable the output.
8. Run the PHI GUI software, go to spectrum analysis tab, and capture the results (SNR, THD, and ENOB) with various input signal frequencies.

Table 17. Signal Source Test Condition

PARAMETER	VALUE
Pattern	Sine
Voltage	7.23 Vpp (adjust to cover full input dynamic range)
Frequency	2 kHz and 100 kHz
Source impedance	600 Ω
Power supply	12-V DC at 250 mA

The test results are taken for both the 2-kHz and 100-kHz input frequencies with and without jitter cleaner mode.

NOTE:

1. While testing with a 100-kHz input signal frequency, a bandpass filter is used in between the signal source and the TIDA-01035 module.
2. The corresponding resistor jumper is populated for with or without jitter mitigation mode (see Section 3.2.1).

4.2 Test Results

Table 18 and Figure 27 show the performance test results for with and without jitter mitigation mode with input signal frequencies of 2 kHz and 100 kHz, respectively. The datasheet SNR performance of the ADS8900B at a 100-kHz input signal is 99 dB. Table 18 shows that the SNR performance of the host generated CONVST (without jitter mitigation mode) is 80.25 dB while CONVST generated at host (with jitter mitigation mode) is 98.03 dB, which is close to the datasheet's specification. This result shows that signal chain performance degraded due to isolator jitter, and the solution provided in the TIDA-01035 gives an improved SNR performance of almost 18 dB.

Also, the serial data rate of SPI can be reduced to 45 MHz by using multiSPI while operating the ADS8900B with a maximum sample rate of 1 MSPS.

Table 18. Performance Test Result

PARAMETER	ADS8900B DATASHEET SPECIFICATION	TIDA-01035	
		WITHOUT JITTER MITIGATION LOGIC	WITH JITTER MITIGATION LOGIC
Fin (kHz) = 2			
SCLK (MHz)	45		
Sample rate (MSPS)	1		
SNR (dB)	104.00	100.72	100.88
THD (dB)	–125.00	–121.62	–127.68
ENOB	17.00	16.43	16.46
Fin (kHz) = 100			
SCLK (MHz)	45		
Sample rate (MSPS)	1		
SNR (dB)	99.50	80.25	98.03
THD (dB)	–110.00	–105.90	–109.97
ENOB	16.20	13.04	15.94

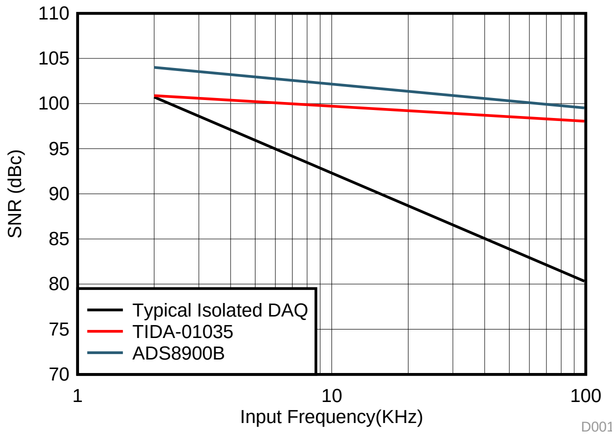
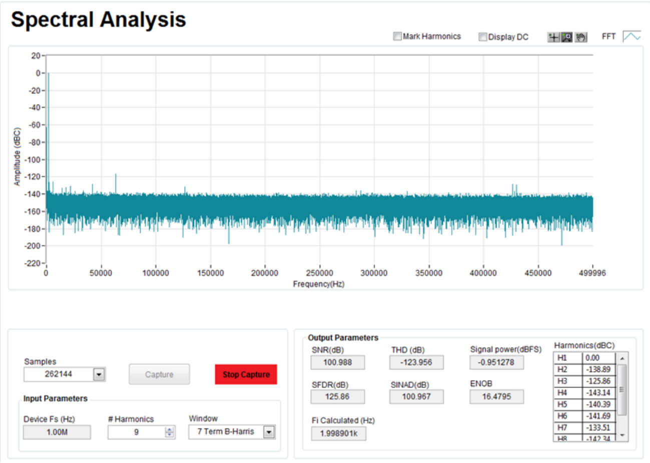


Figure 27. TIDA-01035 SNR Performance Graph



Samples: 262144

Input Parameters

Device Fs (Hz): 1.00M
Harmonics: 9
Window: 7 Term B-Harris

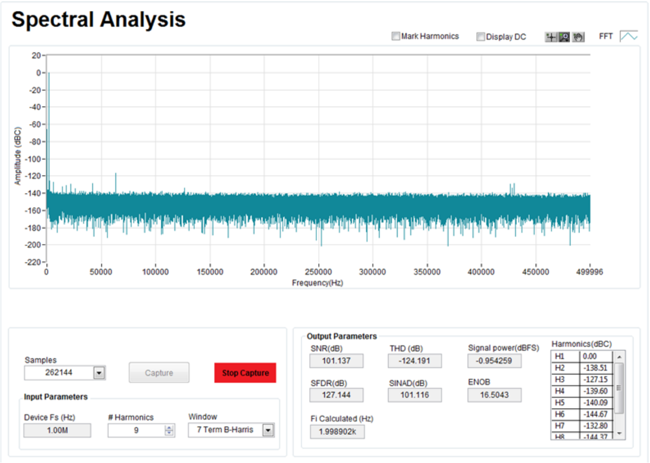
Output Parameters

SNR(dB): 100.988
THD (dB): -123.956
Signal power(dBFS): -0.951278
SFDR(dB): 125.86
SINAD(dB): 100.967
ENOB: 16.4795
Fi Calculated (Hz): 1.998901k

Harmonics(dBC)

H1	0.00
H2	-138.89
H3	-125.86
H4	-143.14
H5	-140.39
H6	-141.69
H7	-133.51
H8	-142.34

Figure 28. 2-kHz Spectrum (Normal Mode)



Samples: 262144

Input Parameters

Device Fs (Hz): 1.00M
Harmonics: 9
Window: 7 Term B-Harris

Output Parameters

SNR(dB): 101.137
THD (dB): -124.191
Signal power(dBFS): -0.954259
SFDR(dB): 127.144
SINAD(dB): 101.116
ENOB: 16.5043
Fi Calculated (Hz): 1.998902k

Harmonics(dBC)

H1	0.00
H2	-138.51
H3	-127.15
H4	-139.60
H5	-140.09
H6	-144.67
H7	-132.80
H8	-144.37

Figure 29. 2-kHz Spectrum (Jitter Mitigation Mode)

Samples: 262144

Input Parameters

Device Fs (Hz): 982.10k
Harmonics: 9
Window: 7 Term B-Harris

Output Parameters

SNR(dB): 80.5967
THD (dB): -108.919
Signal power(dBFS): -1.08298
SFDR(dB): 110.177
SINAD(dB): 80.5903
ENOB: 13.0947
Fi Calculated (Hz): 100.392373k

Harmonics(dBC)

H1	0.00
H2	-123.33
H3	-110.18
H4	-124.56
H5	-124.46
H6	-121.59
H7	-121.61
H8	-125.38

Figure 30. 100-kHz Spectrum (Normal Mode)

Samples: 262144

Input Parameters

Device Fs (Hz): 988.56k
Harmonics: 9
Window: 7 Term B-Harris

Output Parameters

SNR(dB): 98.0325
THD (dB): -109.975
Signal power(dBFS): -1.01446
SFDR(dB): 110.426
SINAD(dB): 97.7633
ENOB: 15.9474
Fi Calculated (Hz): 101.052849k

Harmonics(dBC)

H1	0.00
H2	-129.13
H3	-110.43
H4	-145.95
H5	-124.56
H6	-145.77
H7	-126.96
H8	-143.02

Figure 31. 100-kHz Spectrum (Jitter Mitigation Mode)

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-01035.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01035.

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01035.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-01035.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01035.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01035.

6 Software Files

To download the software files, see the design files at TIDA-01035.

7 Related Documentation

1. Texas Instruments, *Noise Analysis in Operational Amplifier Circuits*, Application Report (SLVA043)
2. Texas Instruments, *Fully-Differential Amplifiers*, Application Report (SLOA054)
3. Texas Instruments, *Chapter 10: Op Amp Noise Theory and Applications*, Excerpted from *Op Amps for Everyone* (SLOA082)
4. Texas Instruments, *18-Bit, 2-MSPS Isolated Data Acquisition Reference Design for Maximum SNR and Sampling Rate*, TIDA-00732 Design Guide (TIDUB85)

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8 About the Authors

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Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2016) to A Revision **Page**

Change	Page
Changed language and images to fit current style guide	1
Changed "REF5045 Reference 4.5 V" to "REF5050 Reference 5 V"	1
Changed "REF5045 Reference 4.5 V" to "REF5050 Reference 5 V"	5

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