TI Designs

Eight-Channel, Isolated, High-Voltage Analog Input Module With ISOW7841 Reference Design

Description

The TIDA-01333 reference design is a high-voltage analog input module with eight channels. Each channel can be used for both voltage and current measurement. The TI Design uses the ADS8681 16-bit analog-to-digital converter (ADC), which can handle input voltages of up to ±12.288 V. This specification makes any preprocessing of standard input voltages in the industrial space unnecessary. In addition, four channels of the design are able to handle common-mode (CM) voltages of up to ±160 V, which eliminates any concern about ground loops or compensation currents flowing between the connected inputs. The TIDA-01333 design is based on TIDA-00764; however, to power and communicate with the isolated side, the TIDA-01333 design uses TI's ISOW7841.

Features

- High Voltage Inputs of up to ±12.288 V
- Voltage and Current Measurement
- Four Channels With CM of up to ±160 V
- –85-dB Crosstalk Rejection for Adjacent Channels
- 100-MΩ Input Impedance
- Surge Transient Immunity According to EN 61000-4-5 Class 2 (±1 kV, 24 A)
- BeagleBone Compatible
- 5-V Isolated Power and Isolated SPI in Single Chip

Applications

- PLC
- Analog Input Modules

Resources

TIDA-01333	Design Folder
ADS8681	Product Folder
OPA192	Product Folder
MUX36S08	Product Folder
TPS55010	Design Folder
SN74AHC594	Product Folder
TS5A23157	Product Folder
ISO7140	Product Folder
ISOW7841	Product Folder
LP2985	Product Folder

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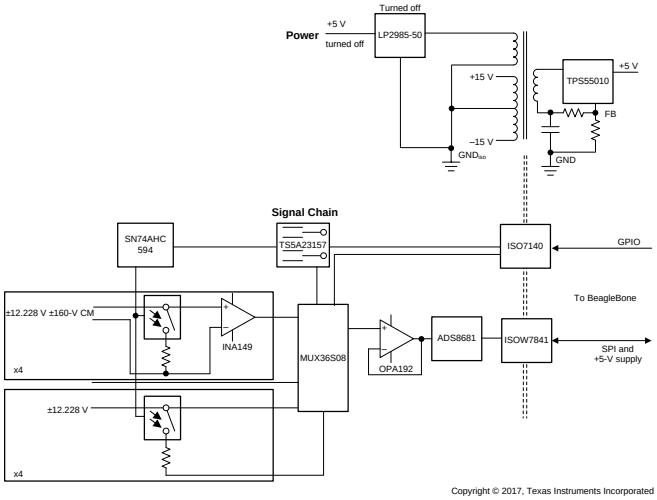

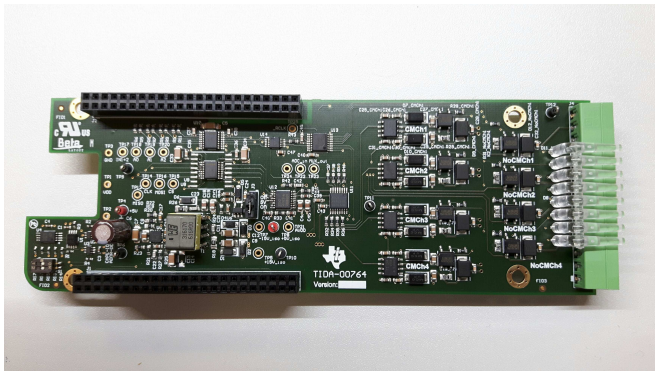

1 System Overview

1.1 System Description

TIDA-01333 is an isolated, eight-channel, high-voltage analog input module that can handle input voltage of up to ±12.288 V without any necessary signal preprocessing. Although the analog-to-digital converter (ADC) ADS8681 used for this design only has one input channel, the overall design contains eight input channels. This number of input channels is achieved by combining the ADS8681 with the MUX36S08 multiplexer (MUX) . Depending on its supply voltages, the MUX36S08 can switch voltages in the range of ±18 V. The maximum input range of the ADS8681 is ±12.288 V, which makes preprocessing of the incoming voltage signals unnecessary.

Four input channels of the design can handle input signals with a common-mode (CM) range of up to ±160 V in respect to the ground potential of the board. For this configuration, an INA149 device is put in front of the MUX inputs for each of the four channels.

Furthermore, every channel of the design can also be used for current measurement in the range of 0 mA to ±20 mA. To switch between voltage and current measurement, the SN74AHC594 serial-in, parallel-out register, can be programmed with two isolated control lines. The eight outputs of the SN74AHC594 device then control one optical switch each. If the switch is turned on, the current flows through a shunt resistor and the voltage drop across the shunt is measured by the ADC. To indicate that a channel has been configured for current measurement, a light emitting diode (LED) turns on for the specific channel. The LEDs are placed at the input connector of the design, so that the channel status can also be seen by the user.

The board is BeagleBone compatible, which means that it can be directly put onto a BeagleBone board. Communication between the AM3359 processor of the BeagleBone and the ADC of the design is possible by using a serial peripheral interface (SPI). SPI communication is isolated from the BeagleBone using the ISOW7841. Further necessary control lines for MUX switching and programming of the SN74AHC594 are isolated from the BeagleBone using an ISO7140 isolator.

The TIDA-01333 design has two isolated power supplies to power the isolated side of the board. A Fly-Buck™ converter topology, built up with a TPS55010 Fly-Buck regulator and a transformer, is used to create the ±15-V rails required for the MUX and the INA149 device. The board offers two options for creating the +5-V supply rail. In the first option, the same transformer used for the ±15-V rails has another separate winding to generate a +5-V rail. This rail can be disabled or enabled with a jumper that turns on or turns off a low-dropout regulator (LDO), which is connected subsequently to the separate the 5-V winding of the transformer. In the second option, the +5-V rail created by the ISOW7841 device can be used. The two options are implemented so that the user can evaluate the two options against each other. The TIDA-01333 design shows a solution using the ISOW7841 device, which is why this reference design does not offer further explanation on the optional creation of the +5-V rail using the transformer. For more details on this option, refer to TIDA-00764 reference design [1].

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATION			DETAILS
	MIN	TYP	MAX	
Supply voltage	4.5 V	5 V	5.5 V	Section 2.1
Power consumption isolated side	—	—	420 mW	
Channels	Eight isolated overall	—	—	Section 2.2
	Four with CM support of ±160 V	—	—	Section 2.2.1
Input voltage	Max. ±12.288 V	—	—	—
Input current	0 mA – 24 mA	—	—	—
Surge transient immunity	EN 61000-4-5 class 2 (±1 kV, 24 A)	—	—	Section 2.2.2
Resolution	16-bit ADC	—	—	Section 2.3
Input ranges	±2.56, ±5.12, ±6.144, ±10.24, ±12.288	—	—	—
	0 V to 5.12 V, 0 V to 6.144 V, 0 V to 10.24 V, 0 V to 12.288 V	—	—	—
Input impedance	100 MΩ	—	—	Section 2.3.2
Crosstalk	–85 dB for adjacent channels	—	—	Section 3.2.5
Channel settling time	52 µs for –12.288 V to 12.288 V	—	—	Section 3.2.6
Operating temperature	-40°C – 85°C	—	—	—
Form factor	158.75 mm x 54.51 mm	—	—	—

1.3 Block Diagram

Figure 1 shows the block diagram of the TIDA-01333 design. This block diagram only shows one out of the four channels with CM capabilities (upper block) and one out of the four channels without CM capabilities (lower block) once because the build of the corresponding channels are identical.

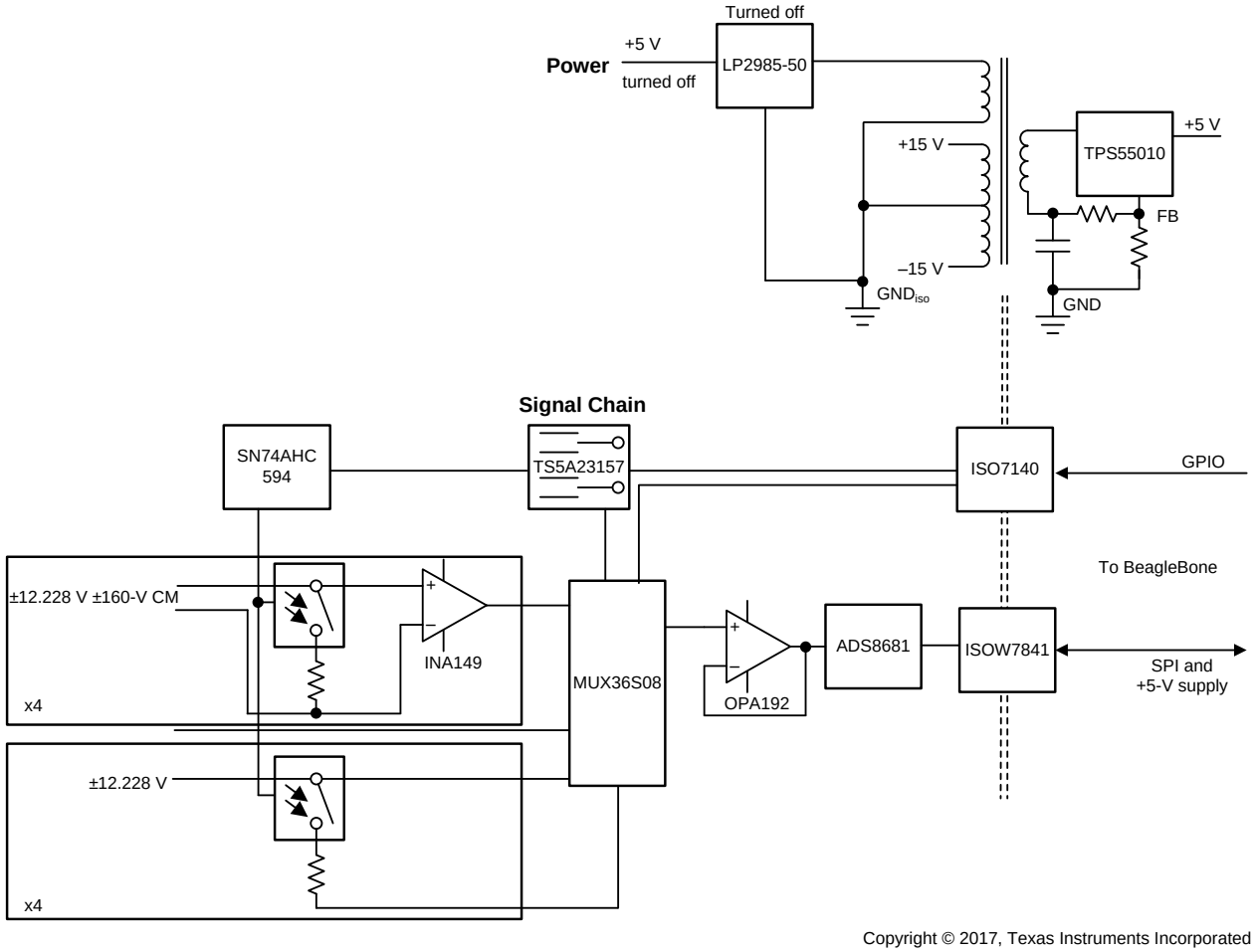

Figure 1. TIDA-01333 Block Diagram

1.4 Highlighted Products

1.4.1 TPS55010

The TPS55010 is a transformer driver designed to provide isolated power (see Table 2). The device operates from 6 V down to 2.95 V. The device uses fixed-frequency current mode control and a half-bridge power stage with primary-side feedback to regulate the output voltage for power levels up to 2 W. The switching frequency is adjustable from 100 kHz to 2000 kHz to allow optimization of solution size, efficiency, and noise. The switching frequency is set with a resistor or is synchronized to an external clock using the RT/CLK pin. To minimize inrush currents, a small capacitor can be connected to the soft-start pin. The EN pin can be used as an enable pin or to increase the undervoltage lockout (UVLO) of the default input from 2.6 V.

Table 2. Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS55010	WQFN (16)	3.00 mm × 3.00 mm

1.4.2 LP2985

The LP2985 family of fixed-output LDOs offers exceptional, cost-effective performance for both portable and non-portable applications (see Table 3). Available in voltages of 1.8 V, 2.5 V, 2.8 V, 2.9 V, 3 V, 3.1 V, 3.3 V, 5 V, and 10 V, the family has an output tolerance of 1% for the A version (1.5% for the non-A version) and is capable of delivering 150-mA continuous load current. Standard regulator features, such as overcurrent and overtemperature protection, are included.

Table 3. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP2985	SOT-23 (5)	2.90 mm x 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the corresponding datasheet.

1.4.3 ISOW7841

The ISOW784x is a family of high-performance, quad-channel reinforced digital isolators with an integrated high-efficiency power converter. The integrated DC-DC converter provides up to 650 mW of isolated power at high efficiency and can be configured for various input and output voltage configurations. Therefore these devices eliminate the requirement for a separate isolated power supply in space-constrained isolated designs.

The ISOW784x family of devices provide high electromagnetic immunity and low emissions while isolating CMOS or LVCMOS digital I/Os. The signal-isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier, whereas, power isolation uses on-chip transformers separated by thin film polymer as insulating material. Various configurations of forward and reverse channels are available. If the input signal is lost, the default output is high for the ISOW784x devices and low for the devices with the F suffix.

Table 4. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISOW7840	SOIC (16)	10.30 mm × 7.50 mm
ISOW7841		
ISOW7842		
ISOW7843		
ISOW784		

(1) For all available packages, see the orderable addendum at the end of the corresponding datasheet.

1.4.4 ISO7140

ISO7140 provides galvanic isolation up to 2500 V_{RMS} for 1 min per UL and 4242 V_{PK} per VDE. ISO7140 is a quad-channel isolator and has four forward channels. The device is capable of a 50-Mbps maximum data rate with 5-V supplies and 40-Mbps maximum data rate with 3.3-V or 2.7-V supplies, with integrated filters on the inputs for noise-prone applications. The suffix F indicates that the default output state is low.

Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. Used with isolated power supplies, the device prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. The device has transistor-transistor logic (TTL) input thresholds and can operate from 2.7-V, 3.3-V, and 5-V supplies. All inputs are 5-V tolerant when supplied from a 2.7-V or 3.3-V supply.

Table 5 lists the device information for the ISO71xx family.

Table 5. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7131CC	SSOP (16)	4.90 mm × 3.90 mm
ISO7140CC		
ISO7140FCC		
ISO7141CC		
ISO7141FCC		

(1) For all available packages, see the orderable addendum at the end of the corresponding datasheet.

1.4.5 INA149

The INA149 is a precision unity-gain difference amplifier with a very-high-input common-mode voltage range. This amplifier is a single, monolithic device that consists of a precision op amp and an integrated thin-film resistor network. The INA149 can accurately measure small differential voltages in the presence of common-mode signals up to ±275 V. The INA149 inputs are protected from momentary common-mode or differential overloads of up to 500 V.

The INA149 can replace isolation amplifiers in many applications where galvanic isolation is not required. This ability can eliminate costly, isolated-input-side power supplies and the associated ripple, noise, and quiescent current. The excellent 0.0005% nonlinearity and 500-kHz bandwidth of the INA149 are superior to those of conventional isolation amplifiers (see Figure 2).

The INA149 is pin-compatible with the INA117 and INA148 type high common-mode voltage amplifiers and offers improved performance over both devices. The INA149 is available in the SOIC-8 package with operation specified over the extended industrial temperature range of –40°C to +125°C.

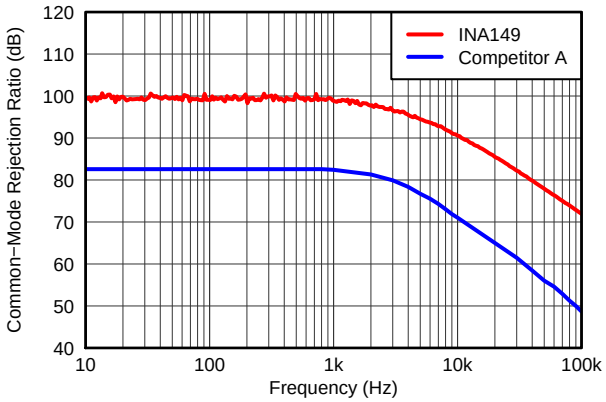

Figure 2. INA149 Common-Mode Rejection Ratio Over Frequency

1.4.6 ADS8681

The ADS8681 is an integrated data acquisition (DAQ) system based on a 16-bit successive approximation (SAR) ADC, which operates at a throughput of 1 MSPS (see Table 6). The device features a high-precision SAR ADC, integrated analog front-end (AFE) input driver circuit, overvoltage protection circuit up to ±20 V, and an on-chip 4.096-V reference with extremely-low temperature drift. Operating on a single 5-V analog supply, the ADS8681 can support true bipolar input ranges of ±12.288 V, ±6.144 V, ±10.24 V, ±5.12 V, and ±2.56 V, as well as unipolar input ranges of 0 V to 12.288 V, 0 V to 10.24 V, 0 V to 6.144 V, and 0 V to 5.12 V. The gain and offset errors for the AFE circuit are accurately trimmed within the specified values for each input range to ensure high DC precision. The input range selection is done by software programming of the device internal registers. The device offers a high resistive input impedance (≥ 1 MΩ) irrespective of the selected input range.

The ADS8681 offers an enhanced SPI-compatible serial interface (multiSPI™ technology) to the digital host and also supports daisy-chaining of multiple devices. The digital supply can operate from 1.65 V to 5.25 V, enabling a direct interface to a wide range of host controllers.

Table 6. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS8681	TSSOP (16)	5.00 mm × 4.40 mm
	WQFN (16)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the corresponding datasheet.

1.4.7 OPA192

The OPA192 is an integrated DAQ system based on a 16-bit successive approximation (SAR) ADC, which operates at a throughput of 1 MSPS (see Table 7). The device features a high-precision SAR ADC, integrated analog front-end (AFE) input driver circuit, overvoltage protection circuit up to ±20 V, and an on-chip 4.096-V reference with extremely-low temperature drift. Operating on a single 5-V analog supply, the OPA192 can support true bipolar input ranges of ±12.288 V, ±6.144 V, ±10.24 V, ±5.12 V, and ±2.56 V, as well as unipolar input ranges of 0 V to 12.288 V, 0 V to 10.24 V, 0 V to 6.144 V, and 0 V to 5.12 V. The gain and offset errors for the AFE circuit are accurately trimmed within the specified values for each input range to ensure high DC precision. The input range selection is done by software programming of the device internal registers. The device offers a high resistive input impedance (≥ 1 MΩ) irrespective of the selected input range.

The OPA192 offers an enhanced SPI-compatible serial interface (multiSPI) to the digital host and also supports daisy-chaining of multiple devices. The digital supply can operate from 1.65 V to 5.25 V, enabling direct interface to a wide range of host controllers.

Table 7. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA192	TSSOP (16)	5.00 mm × 4.40 mm
	WQFN (16)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the corresponding datasheet.

1.4.8 MUX36S08

The MUX36S08 and MUX36D04 (MUX36xxx) are modern complementary metal-oxide semiconductor (CMOS) analog multiplexers (see Table 8). The MUX36S08 offers 8:1 single-ended channels; whereas, the MUX36D04 offers differential 4:1 (8:2) channels. The MUX36S08 and MUX36D04 work equally well with either dual supplies (±5 V to ±18 V) or a single supply (10 V to 36 V). The devices also perform well with symmetric supplies (such as V_{DD} = 12 V, V_{SS} = –12 V), and unsymmetric supplies (such as V_{DD} = 12 V, V_{SS} = –5 V). All digital inputs have TTL-logic compatible thresholds, ensuring both TTL and CMOS logic compatibility when operating in the valid supply voltage range.

The MUX36S08 and MUX36D04 have very low ON and OFF leakage currents, allowing these multiplexers to switch signals from high-input impedance sources with minimal error. A low supply current of 45 µA enables use in portable applications.

Table 8. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
MUX36S08IPW	TSSOP (16)	5.00 mm × 4.40 mm
MUX36D04IPW		

(1) For all available packages, see the package option addendum at the end of the corresponding datasheet.

1.4.9 TS5A23157

The TS5A23157 device is a dual single-pole double-throw (SPDT) analog switch designed to operate from 1.65 V to 5.5 V (see Table 9). This device can handle both digital and analog signals. Signals up to 5.5 V (peak) can be transmitted in either direction.

Table 9. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A23157DGS	VSSOP (10)	3.00 mm × 3.00 mm
TS5A23157RSE	UQFN (10)	2.00 mm × 1.50 mm

(1) For all available packages, see the orderable addendum at the end of the corresponding datasheet.

1.4.10 SN74AHC594

The SNx4AHC594 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register (see Table 10). Separate clocks and direct overriding clear ($\overline{SRCLR}$, $\overline{RCLR}$) inputs are provided on the shift and storage registers. A serial ($Q_{H'}$) output is provided for cascading purposes.

Table 10. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SNx4AHC594	SOIC (16)	9.90 mm × 3.91 mm
	SSOP (16)	6.20 mm × 5.30 mm
	PDIP (16)	19.30 mm × 6.35 mm
	SOP (16)	12.60 mm × 5.30 mm
	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the corresponding datasheet.

2 System Design Theory

2.1 Isolated Power Supply

With the exception of a standard 24-V supply rail, some programmable logic controller (PLC) systems have a 5-V backplane which can be used to power modules. To accommodate this specification, the TIDA-01333 design is also powered from a 5-V supply. Figure 1 shows the power supply of the TIDA-01333, which is used to generate the ±15-V rails. The TIDA-01333 design only requires the upper secondary winding of the transformer.

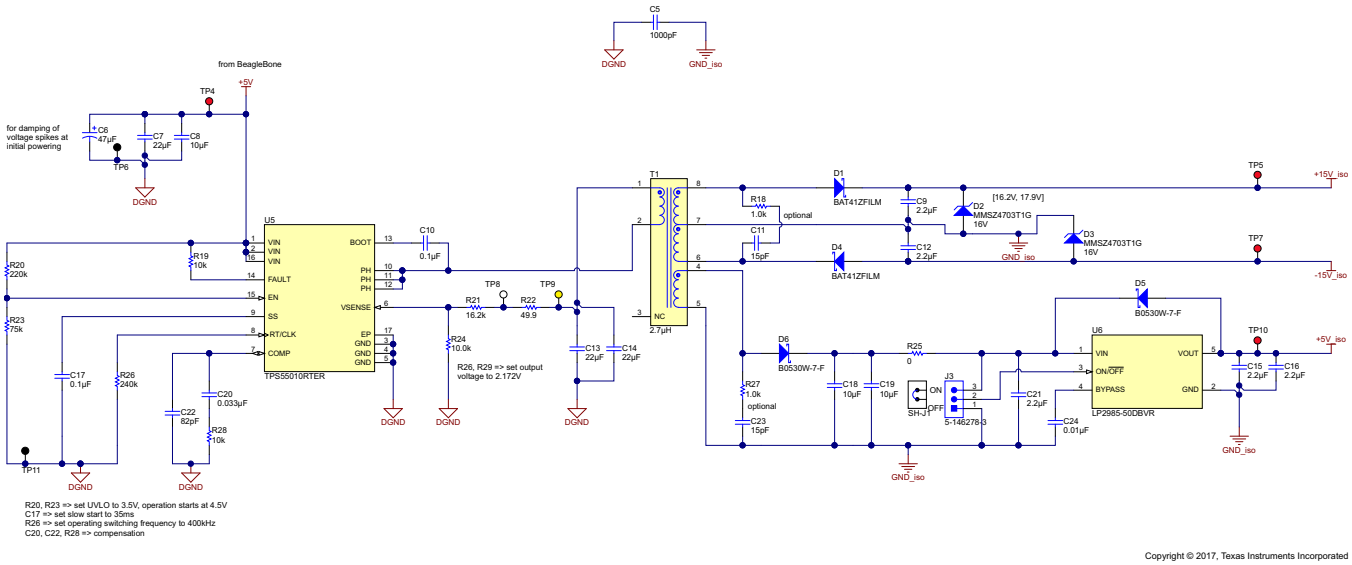

Figure 3. TIDA-01333 Power Supply

TIDA-01333 supports a supply range of 4.5 V to 5.5 V. The board is not protected against input voltages that are higher than this. If protection against input voltage above 5.5 V is required, the user must add a protection circuit to the design.

The expected maximum power consumption on the isolated side of the design is 420 mW (see Table 11). The ISOW7841 can supply up to 500 mW, which is enough to supply all parts on the isolated side even under the worst conditions.

Table 11. TIDA-01333—Power Consumption of Isolated Side

DEVICE	V_{IN}	I_{IN}	NUMBER	P_{IN_SUM}
ADS8681	5 V	10 mA	1	50 mW
ISO7140	5 V	5 mA	1	25 mW
SN74AHC594	5 V	32 mA	1	160 mW
TS5A23157	5 V	1 mA	1	5 mW
MUX36S08	±15 V	1 mA	1	30 mW
OPA192	±15 V	1 mA	1	30 mW
INA149	±15 V	1 mA	4	120 mW
			PARAMETER	**P_{IN_SUM}**
			P_{IN_TOTAL}	420 mW

Figure 4 shows a simplified schematic of a Fly-Buck design. The primary-side voltage V_{PRI} is regulated like in a standard buck converter and given by the duty cycle D.

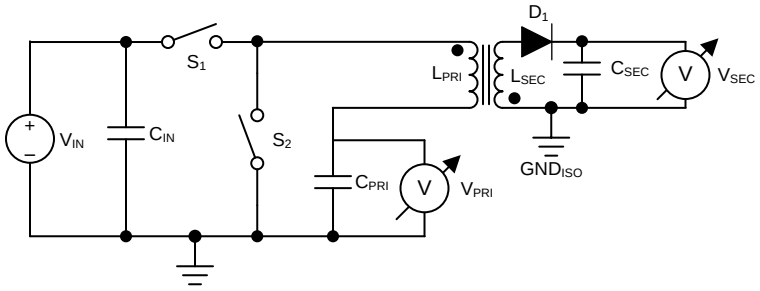

Figure 4. Simplified Schematic of Fly-Buck™ Topology

Equation 1 shows the calculation of the duty cycle D.

$$D = \frac{V_{PRI}}{V_{IN}} = \frac{t_{ON}}{t_{ON} + t_{OFF}} \quad (1)$$

where:

- t_{ON} is the time when switch S_1 is closed and switch S_2 is open
- t_{OFF} is the time when switch S_1 is open and switch S_2 is closed.

The output capacitor C_{OUT} is charged during t_{ON}. Power is transferred to the secondary side during t_{OFF}. For a fixed frequency $f = (t_{ON} + t_{OFF})^{-1}$, which means that for an increasing duty cycle, or longer t_{ON} time, less time is available to transfer power to the secondary side. For this reason, high duty cycles lead to high peak currents on the secondary side. An example of an effect of higher currents is a higher voltage drop across the diode D_1. As a result, the output regulation of the secondary voltage V_{SEC} worsens. Also, the internal switches of the regulator must be able to withstand those peak currents, which is why Fly-Buck duty cycles should be in the range of 40% to 60%. Figure 5 shows the relation between increasing duty cycle D and the ratio of primary current I_{PRI} to secondary current I_{SEC}, assuming a transformer with a turns ratio of N = 1. The figure shows that a duty cycle of 50% I_{PRI} is equal to I_{SEC}; however, a duty cycle of 80% I_{PRI} is already four times higher than I_{sec}. This effect is increased further for systems using a transformer with a turns ratio of $N_{SEC} / N_{PRI} > 1$.

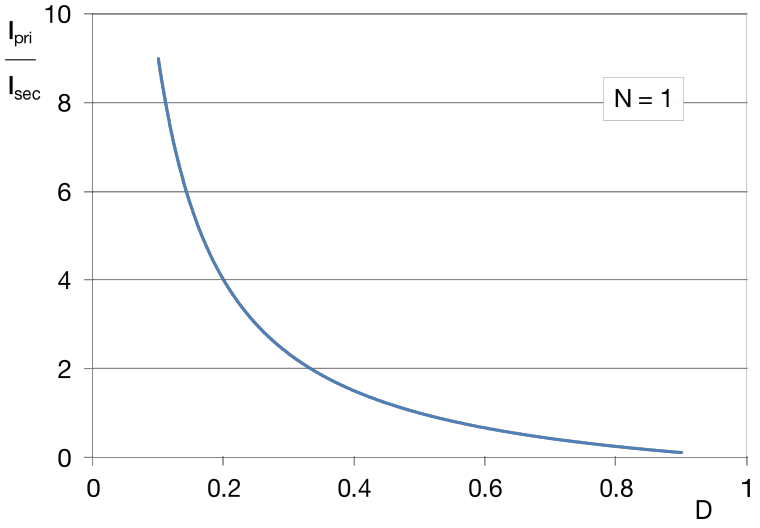

Figure 5. Relation of D to I_{PRI} / I_{SEC} With N = 1

The input range of the design is defined from 4.5 V to 5.5 V. To achieve a reasonable range for the duty cycle D, the primary output voltage is regulated to 2.172 V, which results in a duty cycle from 40% to 48%. The switching frequency is set to 400 kHz, which results in a good ratio of conduction-to-switching losses. Furthermore, the harmonics of 400 kHz (800 kHz, 1.2 MHz, ...) do not interfere with the sampling frequency of 1 MSPS of the ADS8681.

The secondary side requires two output voltages, which are created directly from the transformer: –15 V and +15 V. Therefore, the transformer has a turns ratio of 1:14 for the ±15-V supplies and has a third connection pin after seven turns. When the board is connected, the final output voltages on the secondary side (after the rectification diodes) are around ±15.7 V. This specification provides a safe margin to switch the maximum input signals of ±12.288 V. The supplies of the MUX36S08 and the INA149 devices are rated for a maximum of ±18 V. To ensure that these voltages are not exceeded, two Zener diodes are placed from the respective supply rail to GND.

Higher voltages improve the CM range of the INA149 and the switching speed of the MUX36S08 devices.

2.2 Analog Front End

The TIDA-01333 design realizes its eight input channels by combining the single-channel ADC ADS8681 with the 8:1 MUX MUX36S08. Four of these channels can handle input signals of ±12.288 V plus an additional CM voltage of ±160 V with respect to the isolated GND of the board. The other four channels can handle input voltages of ±12.288 V with respect to the isolated GND. In the following subsections, “CM channel 1-4” refers to the CM channels and “no CM channel 1-4” refers to channels that do not support CM.

Figure 6 shows a schematic of an input channel without CM support and Figure 7 shows an input channel with CM support.

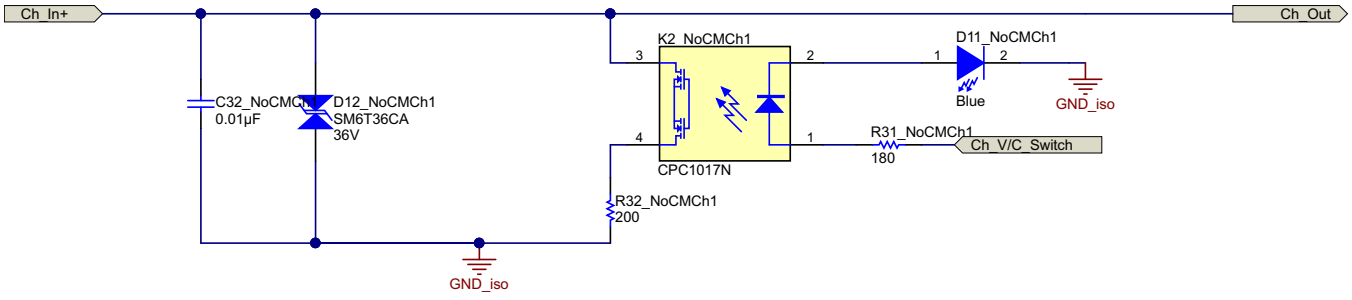

Figure 6. Input Channel Without CM Support

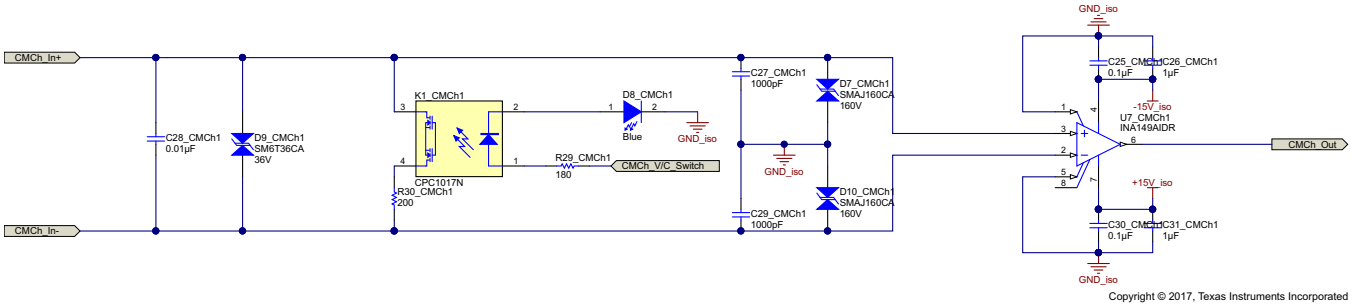

Figure 7. Input Channel With CM Support

2.2.1 Input Channel With CM support

In industrial applications, several sensor outputs are often connected to one multichannel input module. These sensors can be located at different positions, powered from different sources, and suffer from different disturbing sources. All of these effects result in different GND potentials for the different sensors. If all of these sensors are connected to one common ground, large compensation currents would flow between the different GND potentials and may destroy the sensors as a result. To solve this problem, the TIDA-01333 design has four CM input channels (CM channels) which can handle CM voltages of up to ±160 V in respect to the isolated GND of the analog input module.

To handle the different CM voltages, every CM channel uses an INA149 device. Figure 8 shows a block diagram of the device.

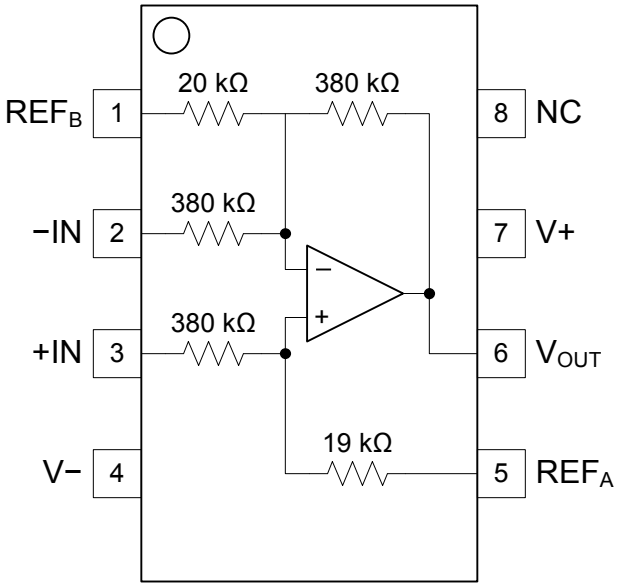

Figure 8. Block Diagram of INA149

The INA149 works like a standard differential amplifier; Equation 2 provides its transfer function:

$$V_{OUT} = (+IN) - (-IN) + 20 \times REF_A - 19 \times REF_B \quad (2)$$

The device has two inputs (+IN) and (–IN) that are connected to the output terminals of the design and one output V_{OUT} that is connected to the MUX input. The INA149 is supplied by the ±15-V rails. Higher supply voltages enable the support of higher CM ranges. For supply voltages of ±16.5 V, the supported CM range goes up to ±300 V; however, the design is only rated for a CM range of ±160 V because of the clamping diodes used in the design: SMA160CA. These diodes have a reverse standoff voltage V_R of 160 V and a maximum breakdown voltage V_{BR} of 197 V. In the worst-case scenario, the clamping voltage V_C of these diodes is 259 V.

Figure 9 shows the curve characteristics of the diodes.

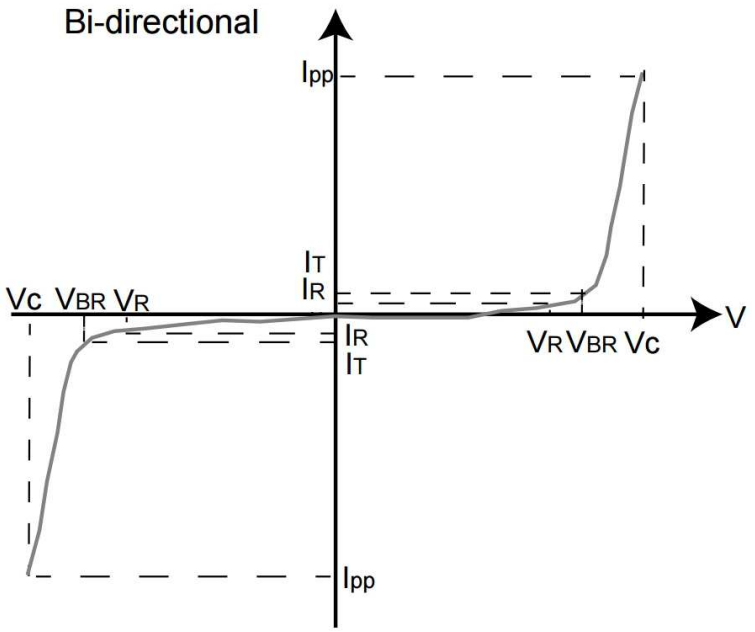

Figure 9. Curve Characteristics of Clamping Diode SMAJ160CA

The output of the device can be referenced to different voltages REF_A and REF_B. In TIDA-01333, the output is only referenced to the isolated GND of the design, which means that $REF_A = REF_B = GND_{ISO}$. In this configuration, the INA149 device acts as a simple unity-gain amplifier; therefore, its output voltage V_{OUT} is calculated by using Equation 3.

$$V_{OUT} = (+IN) - (-IN) + 20 \times GND_{ISO} - 19 \times GND_{ISO} = (+IN) - (-IN) \quad (3)$$

2.2.2 Input Protection

Every MUX input channel is protected against surge events according to EN61000-4-5. The goal is that the board can withstand class-2 surges: ±1 kV with a current of 24 A. To achieve this standard, transient voltage suppression (TVS) diodes with a clamping voltage of 36 V are placed after every channel input. In addition, a capacitor is placed in parallel to the diode so that steep pulses can be suppressed better.

In the case of a surge event, the diode clamps the voltage to 36 V; however, the dynamic resistance R_D) of the TVS diode must be considered, too. The dynamic resistance of the diode is 0.427 Ω. The resulting clamping voltage V_C is calculated using the following Equation 4:

$$V_C = V_{BR} + R_D \times I_{PEAK} = 36\ V + 0.427\ \Omega \times 24\ A = 48.05\ V \quad (4)$$

If the design is intended for use in environments with 125°C ambient temperature, this breakdown voltage can be increased to 50.04 V.

The design uses optocouplers to switch between voltage and current sensing. The optocouplers can withstand voltage differences of up to 60 V between their switch connections, which is why a TVS diode with a higher breakdown voltage must not be selected.

In the case of a surge event, the inputs of the MUX36S08 must be protected, too. The internal electrostatic discharge (ESD) diodes of the MUX start conducting if the input voltage raises more than 0.3 V above or falls more than –0.3 V below the supply voltages. The assumption is that the ESD diodes can handle currents of a maximum 10 mA. To protect the inputs, a 5.11-kΩ resistor is placed in front of every MUX input. In the case of a surge event, this action results in a maximum current of $\frac{(50.04\ V - 0.3\ V - 15\ V)}{5.11 k\Omega} = 6.8\ mA$ flowing through the ESD diodes.

Every diode has a certain leakage current that results in a measurement error. For the following example, assume an input voltage of 12.288 V at an ambient temperature of 85°C. According to the device-specific datasheet, the leakage current of the diode is about 10 nA for a standoff voltage of 30.8 V and an ambient temperature of 85°C. For a 0-mA to 24-mA current signal, the maximum voltage drop across the 200-Ω shunt is 4.8 V. The leaking 10 nA causes a voltage drop of 2 µV across the shunt resistor; however, the corresponding voltage range of the ADC is 0 V to 5.12 V with a resolution of 78.125 µV. This result means that the “missing” voltage drop across the shunt is not measurable by the ADC.

2.2.3 Switching Between Voltage and Current Sensing

Every channel can be used for voltage and current sensing. To ensure isolation, an optocoupler is used to switch between the two modes. After turning on the optocoupler, the current flows through the optocoupler and the connected 200-Ω precision shunt resistor. The resulting voltage drop is measured by the ADC. The resistor is rated for a maximum power of 125 mW. Equation 5 shows that input currents of up to 24 mA can be measured.

$$200\ \Omega \times (0.024\ \text{mA})^2 = 0.1152\ \text{mW} \tag{5}$$

The shunt resistor has a variance 0.02% and a temperature drift of ±25 ppm/°C, which ensures a stable and linear resistor value for the current measurement. However, note that in addition to the voltage drop across the shunt resistor, the optocoupler is also measured. The resistance of the optocoupler varies over temperature and current. To compensate these effects, measure the ambient temperature of the system and calculate these additional voltage drops out in software.

To save cost for isolated signals, all eight optocouplers are controlled by the serial-in parallel-out register SN74AHC594, which is programmed with two isolated data lines. Figure 10 shows the register and how it is connected on the board.

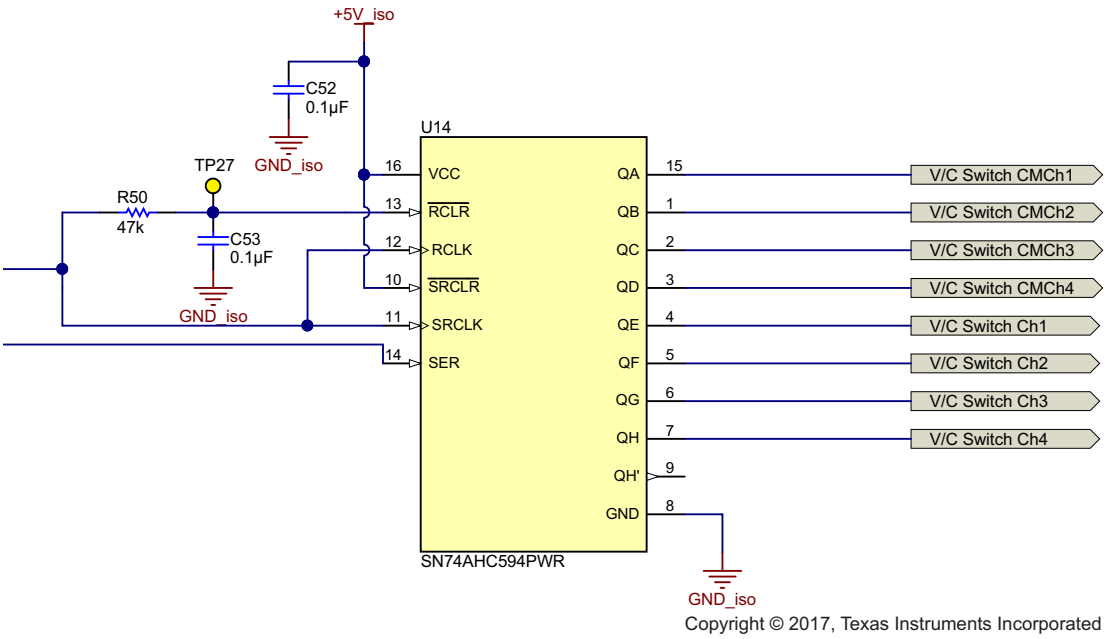

Figure 10. Serial-In Parallel-Out Register

The analog switch of the design (TS5A23157) is typically set in such a way that the two inputs are directed to the channel selection input pins of the MUX36S08 device by setting the inputs IN1 and IN2 high (see Figure 15). These inputs are set low to program the register, which also puts the ADC in a reset state and means that no measurements can be made during the programming of the register. The user does not typically want to measure any of the input signals while the inputs are still configured. Instead, the standard procedure is to first program the inputs and then start the actual measurement procedure.

The SN74AHC594 device is programmed in the same way as the TIDA-00550 device. To start, the $\overline{\text{RCLR}}$ pin of the SN74AHC594 must be pulled to zero, which clears the current status of the outputs. Then, eight data bits, 1/on or 0/off for every channel, must be written into the register. Next, the outputs must be activated by providing one more clock signal on SRCLK. After the programming is finished, the $\overline{\text{RCLR}}$ signal line must be pulled and held high. Pulling $\overline{\text{RCLR}}$ high also reenables the ADC.

The complete programming of the register works as follows:

1. Set input of $\overline{\text{RCLR}}$ and SRCLK low to discharge the RC network
2. Wait until $\overline{\text{RCLR}}$ is low and the outputs are cleared
3. Put in new data byte on SER line and provide clock signal on SRCLK line; make sure that the data is put in fast enough so that the RC network does not charge and $\overline{\text{RCLR}}$ stays low
4. Set input of $\overline{\text{RCLR}}$ and SRCLK high to charge RC network
5. Wait until $\overline{\text{RCLR}}$ is high
6. Clock SRCLK once more to activate outputs
7. Keep $\overline{\text{RCLR}}$ high until the next programming procedure

By putting the RC filter in front of the $\overline{\text{RCLR}}$ input pin, only two general purpose in and out (GPIO) signal lines from the BeagleBone are required to program the SN74AHC594. Figure 11 shows an example of the programming procedure where C1 is the SRCLK signal, C2 the $\overline{\text{RCLR}}$ signal, and C3 the SER signal.

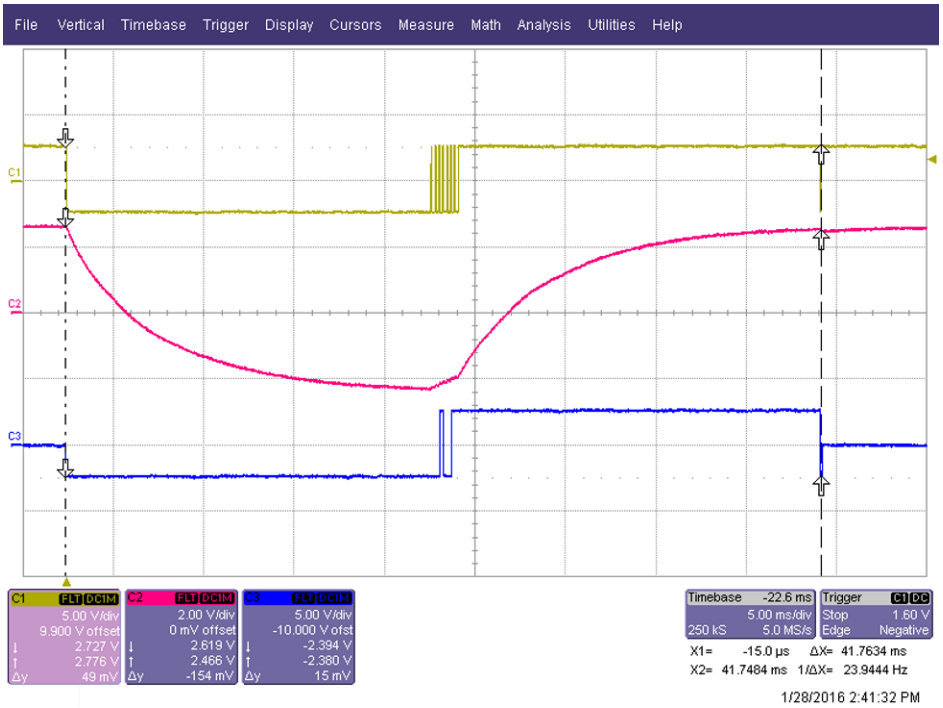

Figure 11. SN74AHC594—Example of Programming Procedure

To indicate whether a channel is configured for voltage or current measurement, eight blue LEDs are placed at the terminal inputs of the design. If an LED is turned ON, the channel is used for current measurement. From left to right, the LEDs represent the following channels:

- CM Channel 4, CM Channel 3, CM Channel 2, CM Channel 1, No CM Channel 4, No CM Channel 3, No CM Channel 2, and No CM Channel 1

Figure 12 shows an example configuration where CM Channel 3, No CM Channel 3, and No CM Channel 2 are configured for current measurement.

NOTE: Setting the current channels first and then configuring the ADC is important; otherwise, the programming of the SN74AHC594 switches the ADC into reset. After the programming, the ADC restarts with this standard configuration.

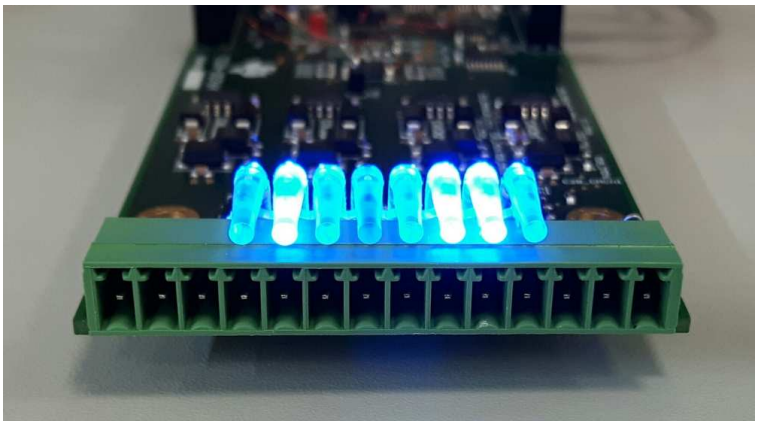

Figure 12. Input Terminals With Current Measurement Configuration for CM Channel 3, No CM Channel 3, and No CM Channel 2

2.3 Analog Digital Converter ADS8681

The ADS8681 is a 16-bit successive-approximation register (SAR) ADC with a sampling rate of 1 MSPS. The ADS device has an internal reference of 4.096 V, which can be scaled up to three times and enables the device to cover an input range of up to ±12.288 V. This feature allows the user to sense all common input voltages in the industrial space without any necessary preprocessing of the input signal. If a smaller input range is preferred, the input range can also be set down to ±2.56 V or 0 V to 5.12 V.

For an input range of ±12.288 V, the ADC has a signal-to-noise ratio (SNR) of 90.25 dB. According to Equation 2, where N equals the number of bits, this specification results in a theoretical effective number of bits (ENOB) of 14.7 bits (see Equation 6). For an input range of 0 V to 5.12 V, the SNR goes down to 87.5 dB, which results in a theoretical ENOB of 14.24 bits.

$$\mathrm{SNR}(\mathrm{dB}) = 6.02 \times \mathrm{N} + 1.76$$

$$\Rightarrow \mathrm{N} = \frac{90.25 - 1.76}{6.02} = 14.70 \tag{6}$$

2.3.1 Input Filter

The ADS8681 has an internal second-order filter with a cutoff frequency f_c of 15 kHz. To achieve a damping of at least 16 × 6.02 + 1.76 = 98.08 dB at a frequency of 1 MHz, an RC filter is put in front of the impedance converter, realized with a OPA192, and precedes the ADC. The resistor value of the RC filter is already given by the signal chain of the system: 5.11 kΩ in front of the MUX + minimum MUX channel resistance of 100 Ω = 5.21 kΩ. Simulation results show that a cutoff frequency of about 37 kHz results in a damping of the system of about –101 dB at 1 MHz. This result also leaves some margin for resistor and capacitor value inaccuracy of up to 5%. Finally, Equation 7 calculates 820 pF as the next standard value for capacitor C.

$$f_C = \frac{1}{2\pi \times R \times C}$$

$$\Rightarrow C = \frac{1}{f_C\, 2\pi \times R} = \frac{1}{37\,\mathrm{kHz} \times 2\pi \times 5.21\,\mathrm{k\Omega}} = 825\,\mathrm{pF} \Rightarrow 820\,\mathrm{pF} \tag{7}$$

Figure 13 shows the resulting alternating current (AC) transfer characteristic of the system. The red line shows the AC transfer characteristic of the internal second-order filter of the ADC only and the blue line shows the complete AC transfer characteristic of the system. Figure 14 shows the schematic section that includes the RC filter.

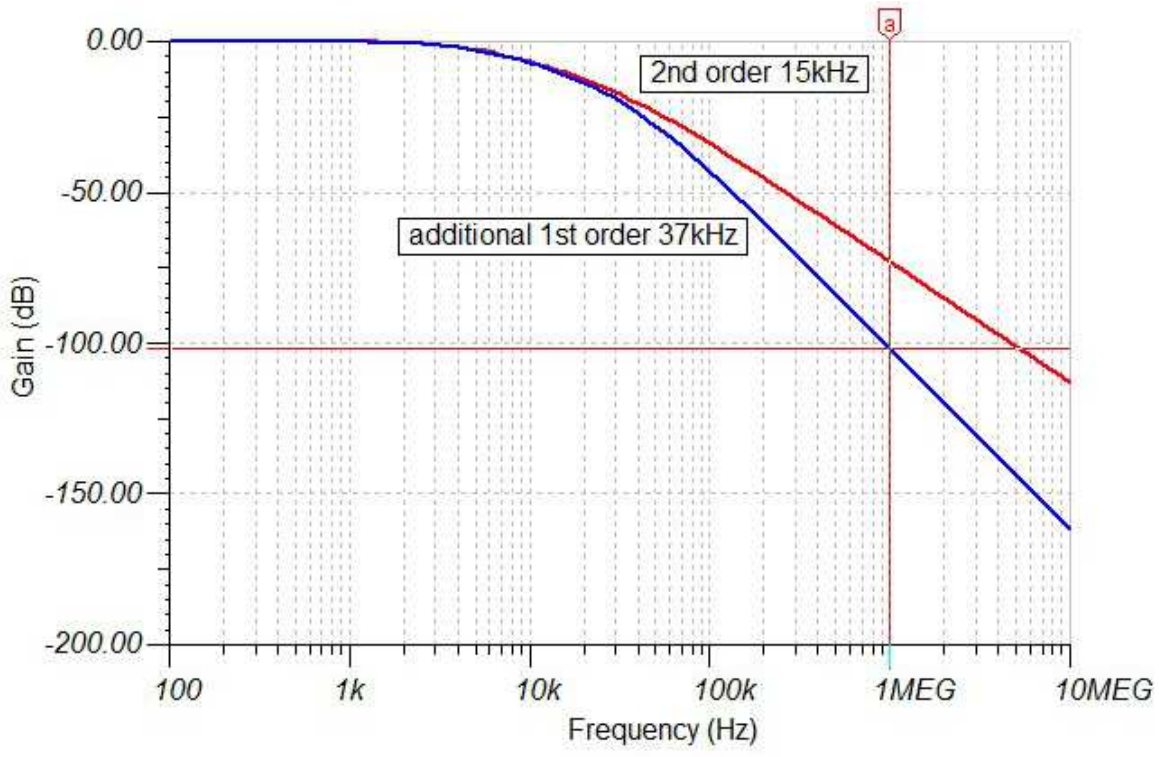

Figure 13. AC Transfer Characteristic of ADS8681 Plus External RC Filter

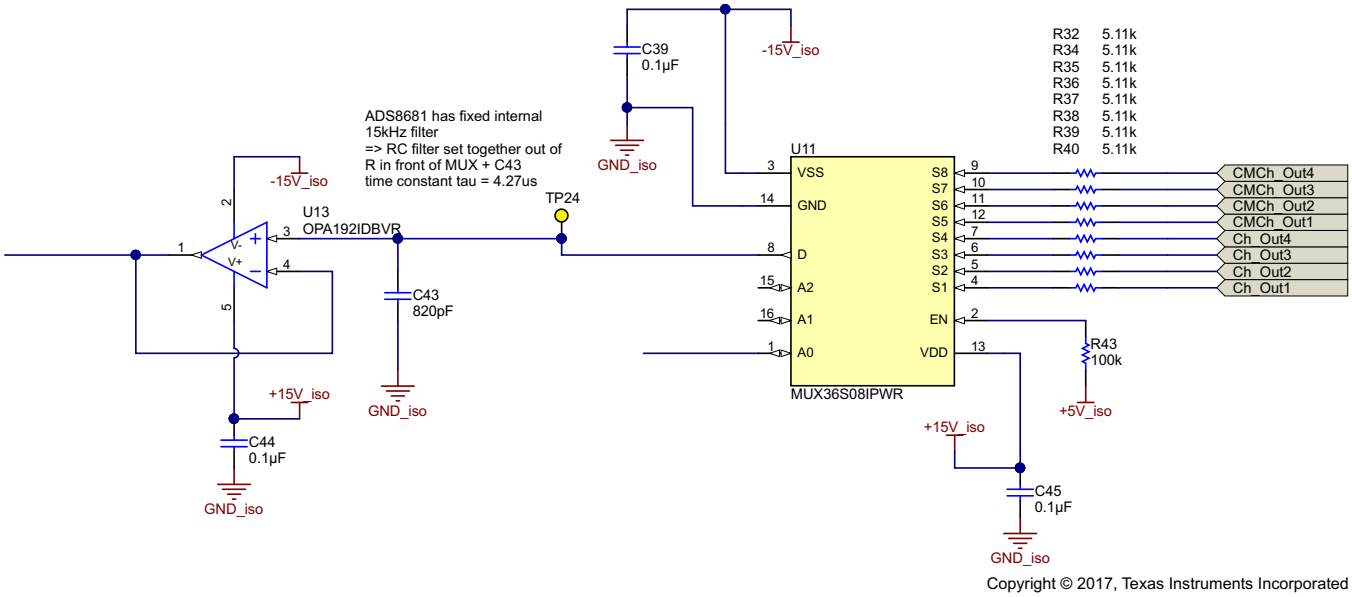

Figure 14. RC Filter in Front of OPA192

2.3.2 Impedance Converter

The output of the MUX is not connected directly to the ADC input, but is instead connected to an impedance converter, which has been built up with an operational amplifier (op amp) OPA192. This op amp is considered an optional part of the design which has its advantages and disadvantages. The disadvantages are that the OPA192 adds noise into the system, adds cost to the signal chain, and makes the required board space larger. However, the advantage is that the op amp facilitates the voltage measurement and makes post processing of the measured signal easier. This is benefit is due to the much higher input impedance of the OPA192 compared to the ADS8681.

Under exemplary conditions assume the following situation: At the input terminals of a no CM channel, a 10-V DC input signal is situated in respect to board GND. The ADS8681 is set to an input range of 0 V to 10.24 V, which results in a resolution of 156.25 µV. For this input range, the ADC has an input impedance of 1.02 MΩ. The overall resistance between the signal input connector and the signal input pin of the ADC is the sum of the channel resistance of the MUX (250 Ω maximum) plus the input protection resistors for the MUX (5.11 kΩ). For a 10-V input signal, this configuration means that there is already a voltage drop of 2.4375 mV across the MUX and a voltage drop of 50 mV across the input resistor (see Equation 8), which equates to 15.6 LSB and 320 LSB, respectively. Software must then be used to estimate and calculate the error introduced by these resistors to obtain a more accurate final result. However, compensating effects such as slightly-different resistor values is not possible due to manufacturing or MUX channel mismatches.

$$\frac{10\ \text{V}}{5.11\,\text{k}\Omega + 250 + 1.02\,\text{M}} = 9.75\ \mu\text{A}$$

$$250\ \Omega \times 9.75\ \mu\text{A} = 2.4375\ \text{mV}$$

$$5.11\,\text{k}\Omega \times 9.75\ \mu\text{A} = 50\ \text{mV}$$

$$\frac{2.4375\ \text{mV}}{\frac{10.24\ \text{V}}{2^{16}}} = 15.6\ \text{LSB}$$

$$\frac{50\ \text{mV}}{\frac{10.24\ \text{V}}{2^{16}}} = 320\ \text{LSB} \tag{8}$$

In cases where the OPA192 device has been placed in front of the ADC, the situation is as follows: The OPA192 has an input impedance of 100 MΩ, an input bias current of ±5 nA max, and a maximum input offset current of ±2 nA. Now, the voltage drop across the MUX and in the input resistor is only 2.5 µV and 51.1 µV (see Equation 9.) So, the combined voltage drop is a lot smaller than the ADC resolution of 156.25 µV, which eliminates the requirement to calculate the estimated voltage drop of the signal path.

$$\frac{10\ \text{V}}{511\,\text{k}\Omega + 250\ \Omega = 100\,\text{M}\Omega} = 10\ \text{nA}$$

$$250\ \Omega \times 10\ \text{nA} = 2.5\ \mu\text{V}$$

$$5.11\,\text{k}\Omega \times 10\ \text{nA} = 51.1\,\mu\text{V} \tag{9}$$

2.3.3 Sampling Speed

The actual voltage value U_C of a capacitor C) of an RC filter that is calculated using Equation 10, where $U_C(t)$ is the actual capacitor voltage after time t, U_0 is the voltage applied to the capacitor, ΔU is the difference between the capacitor voltage $U_{C,t0}$ at time t_0 and the applied voltage U_0, and τ is the time constant of the RC filter.

$$U_C(t) = U_0 + \Delta U \times e^{-\frac{t}{\tau}} = U_0 + \left(U_{C,t_0} - U_0\right) \times e^{-\frac{t}{\tau}} \tag{10}$$

As previously addressed in Section 2.3.1, the RC filter is put in front of the OPA192 device; therefore, the ADC has the time constant $\tau = R \times C = 5.21\ \text{k}\Omega \times 820\ \text{pF} = 4{,}27\ \mu\text{s}$. Equation 10 can be used to calculate the wait time (t) until ΔU is less than ½ LSB of the ADC. The sampled value is not correct until after this time has elapsed.

One assumption is that, at time t_0, the capacitor is charged to a value of +12.288 V. Then, the applied voltage changes to –12.288 V.

Equation 11 and Equation 12 show the calculation steps.

$$\frac{1}{2}\,\mathrm{LSB}\,(\mathrm{ADS8681}) = \frac{1}{2} \times \frac{12.288\ \mathrm{V} \times 2}{2^{16}} = \frac{12.288\ \mathrm{V}}{2^{16}} \tag{11}$$

$$U_C(t) - U_0 = \left(U_{C,t_0} - U_0\right) \times e^{-\frac{1}{\tau}} < \frac{1}{2}\,\mathrm{LSB}\,(\mathrm{ADS8681}) \tag{12}$$

Combine Equation 11 and Equation 12 to produce Equation 13.

$$\left(U_{C,t_0} - U_0\right) \times e^{-\frac{1}{\tau}} < \frac{12.288\ \mathrm{V}}{2^{16}}$$

$$-\frac{1}{\tau} < \mathrm{IN}\left(\frac{12.288\ \mathrm{V}}{2^{16} \times \left(U_{C,t_0} - U_0\right)}\right)$$

$$t > \mathrm{IN}\left(\frac{12.288\ \mathrm{V}}{2^{16} \times \left(U_{C,t_0} - U_0\right)}\right) \times \tau$$

$$\Rightarrow t > -\mathrm{IN}\left(\frac{12.288\ \mathrm{V}}{2^{16} \times \left(12.288\ \mathrm{V} - \left(-12.288\ \mathrm{V}\right)\right)}\right) \times \tau = -\mathrm{IN}\left(\frac{2}{2^{17}}\right) \times \tau = 11.78 \times \tau \tag{13}$$

From the result, it is clear that for a voltage difference that is less than ½ LSB, the capacitor of the RC filter must be charged for about 12τ. For τ = 4.27 µs, this results in a charge or waiting time t of at least 51.24 µs after the MUX has switched to a new channel.

2.3.4 Communication Interface and External Controlling

Standard, four-wire serial peripheral interface (SPI) is used for communication between the ADC and the BeagleBone. If the user wants to reset the ADC, this can be done with another isolated control line originating from the BeagleBone that is connected to the reset pin of the ADC. This control line is also used to control the analog switch TS5A23157 (see Table 12 and Figure 15).

Table 12. TS5A23157—Logic Table

INPUT CONTROL SIGNAL	RESULTING OUTPUT CONNECTION
IN1 + IN2_iso = high	COM1 + COM2 connected to MUX
IN1 + IN2_iso = low	COM1 + COM2 connected to register

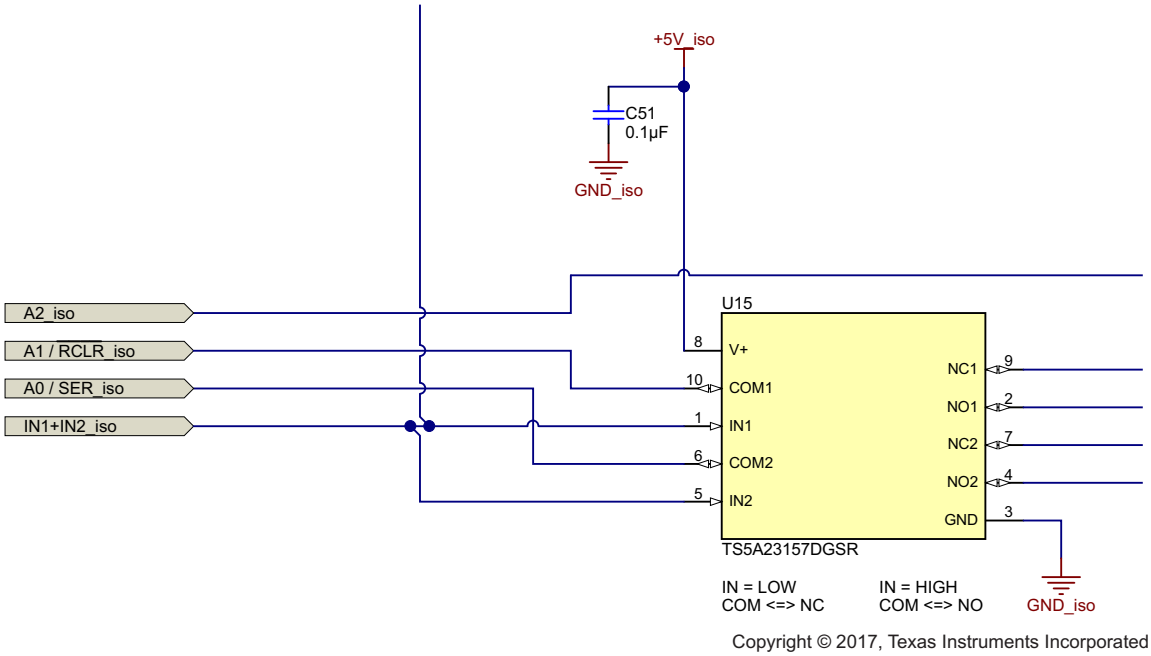

Figure 15. TS5A23157 Connections

3 Test Setup and Results

3.1 Test Setup

Figure 16 shows the test setup for functionality and performance testing of the TIDA-01333 design.

The design is powered by a GW Instek power supply which supplies the actual design with 5 V and the necessary BeagleBone components with 3.3 V. The input signal is provided by a KEYSIGHT B2912A precision source, which has an accuracy of 100 nV and 10 fA.

Switching of the MUX channels and programming of the SN74AHC594 is controlled by an MSP430FR5969 device placed on an MSP430FR5969 LaunchPad™ Development Kit. Visit the tool folder for more information: http://www.ti.com/tool/MSP-EXP430FR5969. The LaunchPad also enables SPI communication to the board. The MSP430FR5969 device on the LaunchPad acts as the master for the SPI. The LaunchPad is connected with a universal serial bus (USB) cable to a laptop on the test bench. Code Composer Studio™ (CCS) software is used to run the test routines for the TIDA-01333 design. Data from the LaunchPad to the laptop is sent over the universal asynchronous receiver transmitter (UART) interface of the MSP430FR6969, which is then displayed on a console running on the laptop.

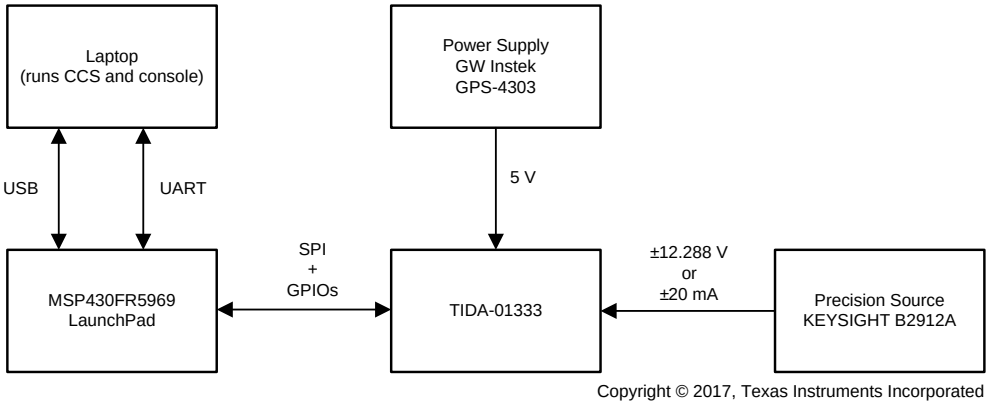

Figure 16. TIDA-01333 Test Setup

3.2 Test Results

Different tests with different DC signals are performed to characterize the TIDA-01333 design. The characterizations are differentiated by no CM channels and CM channels. The test procedure is as follows: First, the DC signal is applied to the input of the ADC. then, 4096 samples are recorded and plotted in a histogram. The standard deviation σ is calculated out of the recorded values. With a known σ, the characterizing DC parameters can be calculated (see Equation 15 to Equation 17). The values in V can be converted to bit values by dividing the V value by the corresponding resolution for this value.

$$V_{noise,RMS} = \sigma \tag{14}$$

$$V_{noise,pp} = V_{noise,RMS} \times 6.6 = \sigma \times 6.6 \tag{15}$$

$$\sigma(bit) = \frac{\sigma(V)}{\frac{\text{full scale range}(V)}{2^N}} \tag{16}$$

$$N_{EFF} = \log_2\left(\frac{2^N}{\sigma(bit)}\right) = \log_2 2^N - \log_2(\sigma(bit)) = N - \log_2(\sigma(bit)) \tag{17}$$

$$N_{Noise\ Free} = \log_2\left(\frac{2^N}{\sigma(bit) \times 6.6}\right) = N_{EFF} - \log_2(6.6) = N_{EFF} - 2.722 \tag{18}$$

V_{NOISE_RMS} represents the root-mean-square noise of the system. The peak-to-peak noise V_{NOISE_PP} represents the range of bits where 99.9% of all recorded samples are included. The V_{NOISE_PP} equals 6.6 times V_{RMS}. N_{EFF} equals the ENOB of the system, which is the ADC plus the complete signal chain. N_{NOISE_FREE} is the effective resolution of the system.

The applied DC signal is either grounded or is coming from a decoupled voltage source. A KEYSIGHT B2912A device is used for this precision source. The precision source has an accuracy of 100 nV and 10 fA.

3.2.1 Channel Offsets

This section describes the test to measure the channel offset for both CM and no CM channels. The input signals to the channels are applied at the input terminals of the board, which means that the performance of the complete system is characterized and not just the performance of the ADC.

The ON-resistance mismatch between the eight MUX channels is 11 Ω maximum for a maximum temperature of 125°C. This channel mismatch is dominated by the 5.11-kΩ resistor in front of the MUX. For this reason, the following tests are done specifically for a single no CM channel and a single CM channel.

3.2.1.1 No CM Channel Offset in Voltage Mode

To test the offset of the no CM channels for voltage sensing, the input of No CM Channel 1 is shorted to GND at the input terminal. All other channels are left open. The input range of the ADC is set to ±2.56 V. The MUX is set to No CM Channel 1. Table 13 lists the results and the histogram in Figure 17 shows the results.

The offset for No CM Channel 1 in voltage mode varies from –1.09375 mV to –0.15625 mV. Most samples have an offset voltage of –0.3125 mV.

Table 13. Test Results for No CM Channel 1 (Voltage Mode, Shorted)

CHANNEL	σ (BITS)	N_{EFF}	N_{NOISE_FREE}	V_{NOISE} (RMS / mV)	V_{NOISE} (pp / mV)
No CM ch1	2.74	14.55	11.82	0.21	1.41

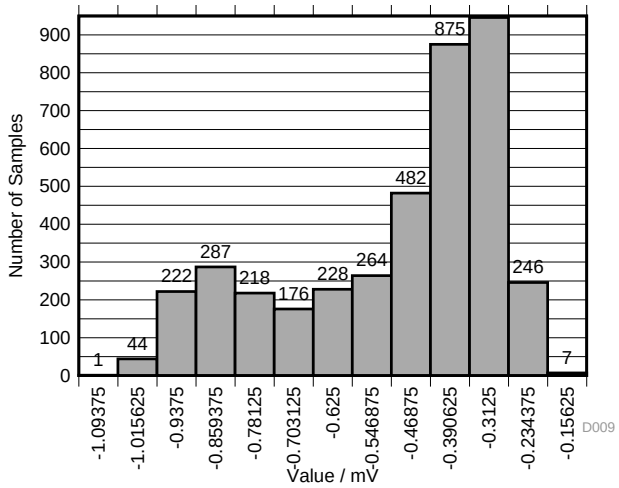

Figure 17. Histogram of Test Results for No CM Channel 1 (Voltage Mode, Shorted)

3.2.1.2 No CM Channel Offset in Current Mode

To test the offset of the no CM channels in current mode, the input of No CM Channel 1 is shorted at the input terminal. All other channels are left open. No CM Channel 1 is set to current mode. The input range of the ADC is set to ±5.12 V, which results in a resolution of 156.25 µV. The MUX is set to No CM Channel 1.

Table 14 lists the results and the histogram in Figure 18 shows the results.

The offset for No CM Channel 1 in current mode varies from –2.34375 mV to –0.3125 mV. Most samples have an offset voltage of –0.625 mV.

Table 14. Test Results for No CM Channel 1 (Current Mode, Shorted)

CHANNEL	σ (BITS)	N_{EFF}	N_{NOISE_FREE}	V_{NOISE} (RMS / mV)	V_{NOISE} (pp / mV)
CM ch1	3.11	14.36	11.64	0.49	3.21

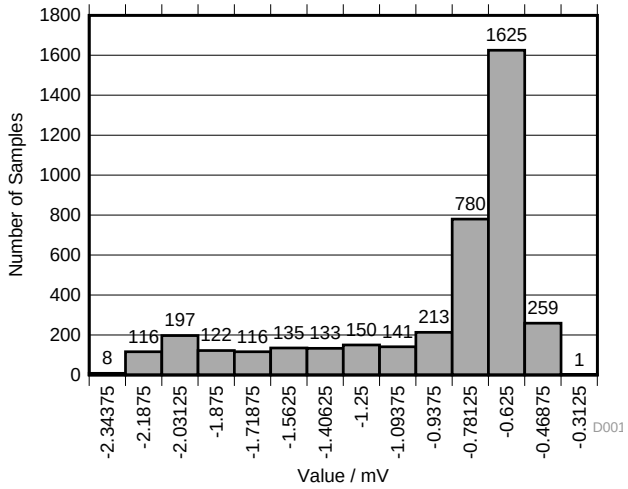

Figure 18. Histogram of Test Results for No CM Channel 1 (Current Mode, Shorted)

3.2.1.3 CM Channel Offset in Voltage Mode

To test the offset of the CM channels for voltage sensing, the input of CM Channel 1 is shorted to GND at the input terminal. All other channels are left open. The input range of the ADC is set to ±2.56 V. The MUX is set to CM Channel 1. Table 15 lists the results and Figure 19 shows a histogram of the results.

The offset for CM Channel 1 in voltage mode varies from –1.25 mV to –0.234375 mV. Most samples have an offset voltage of –0.546875 mV or -0.46875 mV.

Table 15. Test Results for CM Channel 1 (Voltage Mode, Shorted)

CHANNEL	σ (BITS)	N_{EFF}	N_{NOISE_FREE}	V_{NOISE} (RMS / mV)	V_{NOISE} (pp / mV)
CM ch1	2.87	14.48	11.76	0.22	1.48

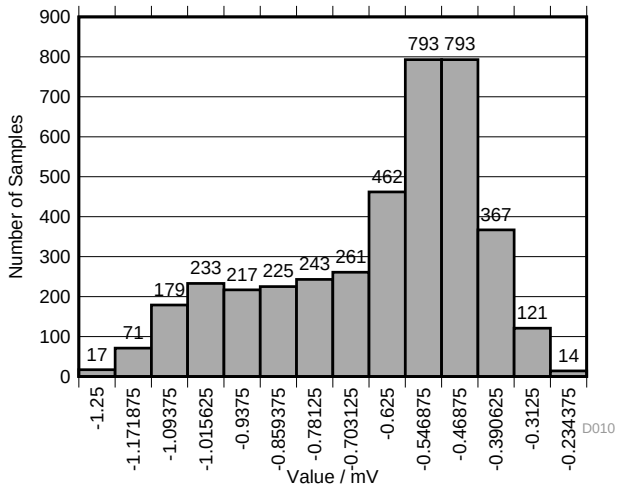

Figure 19. Histogram of Test Results for CM Channel 1 (Voltage Mode, Shorted)

3.2.1.4 CM Channel Offset in Current Mode

To test the offset of the CM channels in current mode, the input of CM Channel 1 is shorted at the input terminal. All other channels are left open. CM Channel 1 is set to current mode. The input range of the ADC is set to ±2.56 V. The MUX is set to CM Channel 1. Table 16 lists the Figure 20 shows a histogram of the results.

The offset for CM Channel 1 in current mode varies from –2.5 mV to –0.46875 mV. Most samples have an offset voltage of –0.78125 mV.

Table 16. Test Results CM Channel 1 (Current Mode, Shorted)

CHANNEL	σ (BITS)	N_{EFF}	N_{NOISE_FREE}	V_{NOISE} (RMS / mV)	V_{NOISE} (pp / mV)
No CM ch1	3.18	14.33	11.61	0.50	3.28

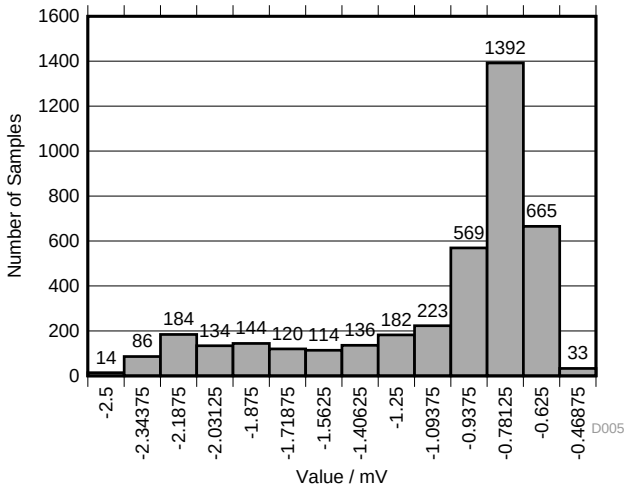

Figure 20. Histogram of Test Results for CM Channel 1 (Current Mode, Shorted)

3.2.1.5 Channel Offsets Conclusion

In the results for both CM channels and no CM channels, the samples are spread wider for current mode and V_{NOISE_PP} is bigger. The additional noise is introduced by the optocoupler plus the current sense resistor across which the voltage is measured.

Moreover, the no CM channel is less noisy compared to the CM channel, which is due to the noise introduced by the INA149 device in the CM channel signal chain.

As previously addressed in Section 2.3.2, removing the impedance converter and connecting the MUX output directly to the ADC input is also possible. However, doing this only slightly improves the system performance.

3.2.2 Voltage Measurement Performance

To successively test the channel performance for voltage mode for both CM channels and no CM channels, 0 V, 5 V and 10 V are applied at the input terminals. For 0 V, the input is shorted; for 5 V and 10 V, the voltage is supplied by the precision source. The input range and therefore the resolution are adjusted for the different input voltages. Then, 4096 samples are taken and plotted in a histogram. Afterwards, σ, N_{EFF}, N_{NOISE_FREE}, V_{NOISE_RMS}, and V_{NOISE_PP} are calculated. Table 17 shows the results for No CM Channel 1 and Table 18 shows the results for CM Channel 1.

Table 17. No CM Channel 1 Performance Over Voltage

V_{INPUT} (V)	RANGE (V)	RES (µV)	σ (BITS)	N_{EFF}	N_{NOISE_FREE}	V_{NOISE_RMS} (mV)	V_{NOISE_PP} (mV)
0	±2.56	78.125	2.74	14.55	11.82	0.21	1.41
5	±5.12	156.25	3.00	14.41	11.69	0.47	3.10
10	±10.24	312.50	2.49	14.68	11.96	0.78	5.14

Table 18. CM Channel 1 Performance Over Voltage

V_{INPUT} (V)	RANGE (V)	RES (µV)	σ (BITS)	N_{EFF}	N_{NOISE_FREE}	V_{NOISE_RMS} (mV)	V_{NOISE_PP} (mV)
0	±2.56	78.125	2.87	14.48	11.76	0.22	1.48
5	±5.12	156.25	3.01	14.41	11.69	0.47	3.10
10	±10.24	312.50	2.54	14.66	11.93	0.79	5.23

The results show that, with increasing resolution, the ENOB is increasing as well, which is the case for every ADC because the input noise is the same, but the resolution is higher.

Table 18 shows that the V_{NOISE_PP} decreases from 0 V to 5 V and then increases from 5 V to 10 V. This change is due to the error introduced by the INA149, which is minimal for output voltages that are higher than 0 V (see Figure 21). As a result, the CM channel shows the best performance for input signals higher than 0 V.

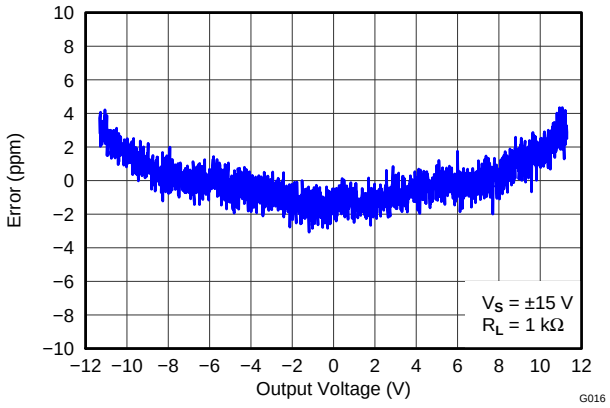

Figure 21. Gain Nonlinearity of INA149

3.2.3 Current Measurement

Both CM channels and no CM channels are tested for increasing input current. The input current increases from 0 mA to 20 mA. The current signal is supplied by the precision source. The maximum expected voltage drop across the shunt resistor and the optocoupler is (200 Ω + 16 Ω) × 20 mA = 4.32 V. Therefore, the input range is set to ±5.12 V. This reference design does not show the histograms for the eight measurements. Table 19 and Table 20 show the results.

Table 19. No CM Channel 1—Current Measurement

I_{IN} (mA)	σ (BITS)	N_{EFF}	N_{NOISE_FREE}	V_{NOISE_RMS} (mV)	V_{NOISE_PP} (mV)
0	3.12	14.36	11.64	0.47	3.21
5	3.12	14.36	11.64	0.49	3.22
10	3.17	14.34	11.61	0.50	3.27
20	5.14	13.64	10.92	0.80	5.30

Table 20. CM Channel 1—Current Measurement

I_{IN} (mA)	σ (BITS)	N_{EFF}	N_{NOISE_FREE}	V_{NOISE_RMS} (mV)	V_{NOISE_PP} (mV)
0	3.18	14.33	11.61	0.50	3.28
5	3.17	14.33	11.61	0.50	3.27
10	3.21	14.32	11.60	0.50	3.31
20	5.09	13.65	10.93	0.80	5.25

The results show that the current measurement is stable for the input range of 0 mA to 10 mA. The reason for the huge increase of σ for the 20-mA measurement is the precision source used. The precision source lowers the resolution if the output current is set to a bigger value than 10 mA; therefore, the test setup works fine up to 20 mA, but is limited due to the current source used.

3.2.4 Performance Discussion and Possible System Improvements

This section discusses the test results and performance of the system and then addresses potential improvements.

3.2.4.1 Performance Discussion

The test results show that the samples of the ADS8681 are widely spread. The reason for this wide spread is that the analog supply of the ADS8681 device is directly supplied by the ISOW7841 device, which has a certain output voltage ripple. This ripple is also seen at the analog input of the ADS8681 and therefore lowers its performance.

The output ripple of the ISOW7841 is dependent on the load connected to its output. For higher loads, the output ripple increases; for lower loads, the output ripple decreases. If all the LEDs on the isolated side are turned off and the ISOW7841 only has to supply the ISO7140 and ADS8681 devices, the result is an output voltage ripple of around 80 mV at a frequency of approximately 20 kHz. As previously explained, this frequency changes with an increasing or decreasing load.

Figure 22 shows the power supply ripple rejection (PSRR) of the ADS8681. The graph shows that the PSRR is at the lowest in the range of 10 kHz to 100 kHz, which means that any voltage ripple at the analog input supply of the ADS8681 device affects the measurement and therefore the performance.

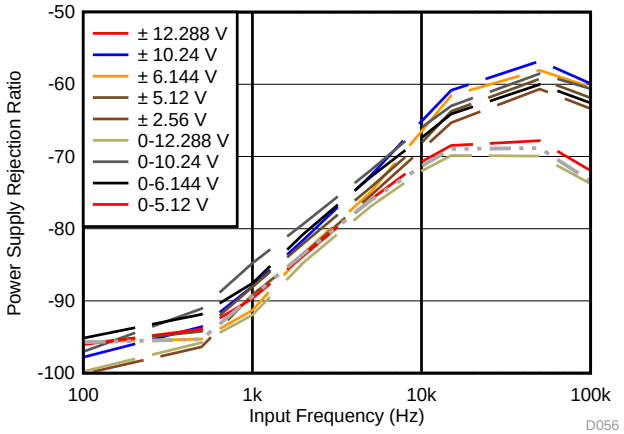

Figure 22. ADS8681 PSRR

3.2.4.2 Possible System Improvements

The system performance can be improved by reducing the voltage ripple of the analog supply voltage of the ADS8681. One way of making this reduction is to put an LDO in between the output of the ISOW7841 device and the analog input of the ADS8681 device. An LDO with a very-low voltage drop, such as the TPS73601, is a good selection for this task. The TPS73601 has a dropout voltage of less than 20 mV for an output current of 100 mA at an ambient temperature of 25°C, which means that the analog supply voltage of the ADS8681 is only slightly lower than the output voltage of the ISOW7841.

Another way of reducing the voltage ripple at the analog input of the ADS8681 is to put either an RC or an LC filter in between the output of the ISOW7841 and the analog input of the ADS8681. The challenge with the RC filter is that the voltage drop across the resistor must be small enough so that the minimum input voltage specification of the ADS8681 (4.75 V) can still be satisfied, for which the maximum input current of the ADS8681 must be considered. To avoid this problem, an LC filter can serve as the better choice. Furthermore, an LC filter offers the benefit of higher damping per decade (–40 dB per decade) compared to an RC filter (–20 dB per decade). Therefore, the cutoff frequency of the filter can be set closer to the output voltage ripple frequency, but still achieve the same damping.

The explained options help to improve the overall performance; however, in the final system setup, the resulting voltages must always be kept in mind. If the user neglects to consider the resulting voltages, the output voltage of the ISOW7841 minus the voltage drop across the LDO or RC filter is lower than the minimum specified input voltage of the ADS8681, which may prevent the system from working correctly.

3.2.5 Channel Crosstalk

According to its datasheet, the MUX36S08 has a channel-to-channel isolation of –85 dB for adjacent channels. To confirm this channel-to-channel isolation on the TIDA-01333 design, the following test is done.

The sampling frequency for the test setup is 17.3 kHz. The input range of the ADC is set to ±10.24 V. The MUX is set to No CM Channel 1. No CM Channel 1 is shorted to GND. A signal of ±10 V at a frequency of 4.325 kHz is applied to No CM Channel 2. This frequency is chosen because it is ¼ the sampling frequency. Then, 4096 measurements are recorded.

Afterward, the recorded samples are divided by 2^{16} to normalize them to the resolution of the ADC. Then, a Fourier analysis is done with the 4096 samples and the absolute values of the imaginary numbers, which are a result of the Fourier analysis, are calculated. These values are then plotted over the frequency range of 0 kHz to 8.65 kHz in steps of 17.3 kHz/4096. Figure 23 shows the resulting plot.

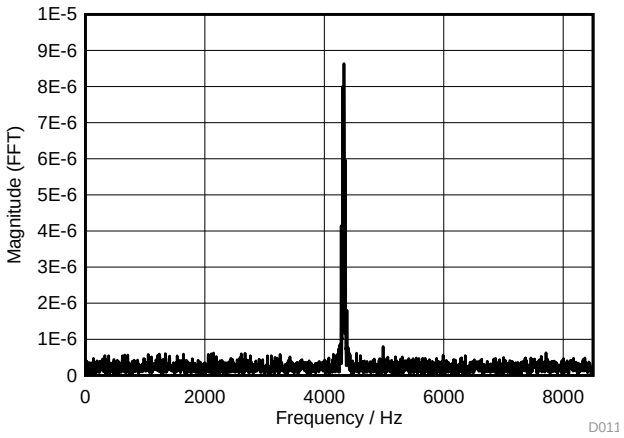

Figure 23. Results for Crosstalk Test

The plot shows the normalized amplitude of the disturbing signal; its maximum is 8.63378×10^6 at 4.325 kHz. The disturbing signal is not always exactly at 4.325 kHz but rather deviates a bit. Therefore, all samples in the range of 4.225 kHz to 4.425 kHz with an amplitude of more than 1×10^6 are added together. These samples add up to 5.36534×10^5. Using Equation 19, the user can calculate that the signal has been attenuated by –85.4 dB.

$$\text{Attenuation}\left(\text{dB}\right) = 20 \times \log\left(5.36534 \times 10^{-5}\right) = -85.4 \text{ dB} \tag{19}$$

3.2.6 Channel Switching

Figure 24 shows the charging curve of the RC filter in front of the ADC. The input signal changes from –12.25 V to +12.25 V. The scope shot shows that the calculated charging time t of 51.24 µs complies with the recorded signal (see Section 2.3.3).

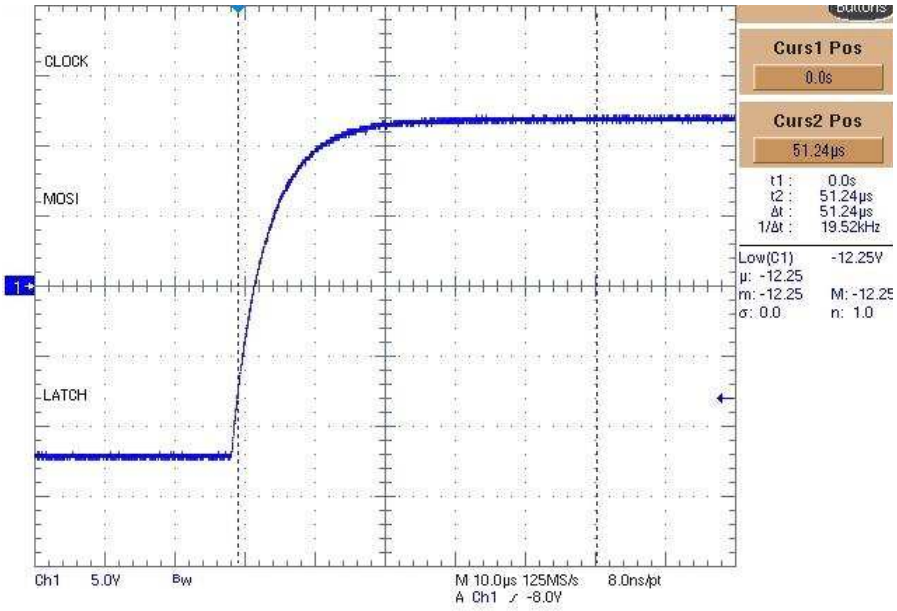

Figure 24. MUX Switching From –12.25 V to +12.25 V

Figure 25 shows the charging curve of the RC filter in front of the ADC for eight switching cycles. The preceding Figure 24 shows that the charging time of the RC filter is 51.24 µs until its charged value is less than ½ bit different to its final value. However, the complete switching sequence for all eight channels takes 460 µs, which is more than 8 × 51.24 µs = 409.84 µs. This result is due to the time that is required to switch between the MUX channels. In this test, the switching is controlled by the MSP430FR5969 device which runs at a speed of 8 MHz.

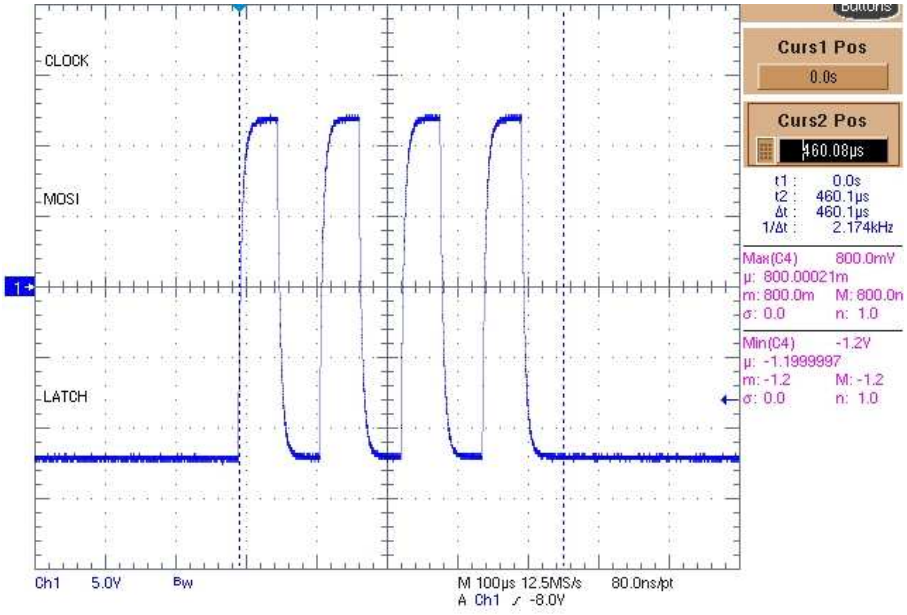

Figure 25. Timing of Eight-MUX Switching Cycles

A total cycle time of around 410 µs results in a maximum theoretical input signal frequency of 2.4 kHz over eight channels. However, the user must consider that the system also requires time for SPI communication between the MCU and the ADC that will reduce the system bandwidth, depending on the speed of the SPI communication.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01333.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01333.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01333.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01333.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01333.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01333.

5 Related Documentation

1. Texas Instruments, *8-ch Isolated High Voltage Analog Input Module Reference Design*, TIDA-00764 Reference Design (TIDUBW9)
2. Texas Instruments, *Dual Channel-to-Channel Isolated Universal Analog Input Module for PLC Reference Design*, TIDA-00550 Reference Design (TIDUBI1)

5.1 Trademarks

6 About the Author

TOBIAS PUETZ is a systems engineer in the Texas Instruments Factory Automation and Control team, where he is working on PLC modules. Tobias brings to this role his expertise in different sensing technologies, power design, and wireless charging as well as software design. Tobias earned his master's degree in electrical engineering and information technology at the Karlsruhe Institute of Technology (KIT), Germany in 2014.

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