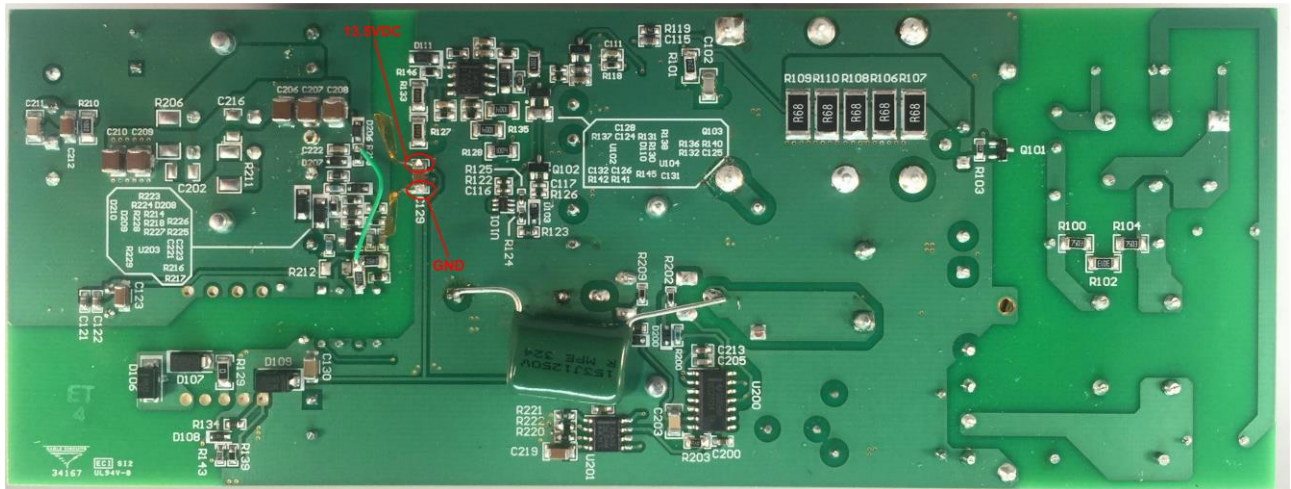## 1   Photo

The photographs below show the top and bottom views of the PMP20694 Rev A board, which is built on PMP20694 Rev A PCB. Notice that Bias Flyback is excluded. **$13.5V_{DC}$ voltage has to be provided to the "Bias" node to PGND after AC input is given in order to test the board**. I.e. $13.5V_{DC}$ needs on C129 at board bottom side.
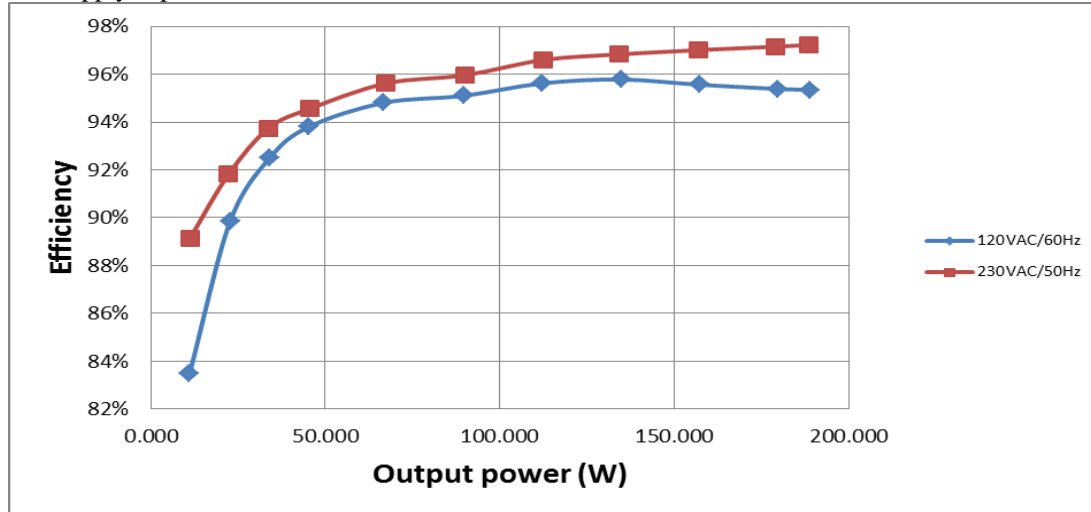
Top Side

Bottom Side

2 Efficiency

The efficiency curves of total supply are shown in the tables and graph below.

2.1 PFC Efficiency

In the test of PFC efficiency, R203 is removed. Constant current load is directly applied to the PFC output. 13.5VDC bias supply is provided at C129.
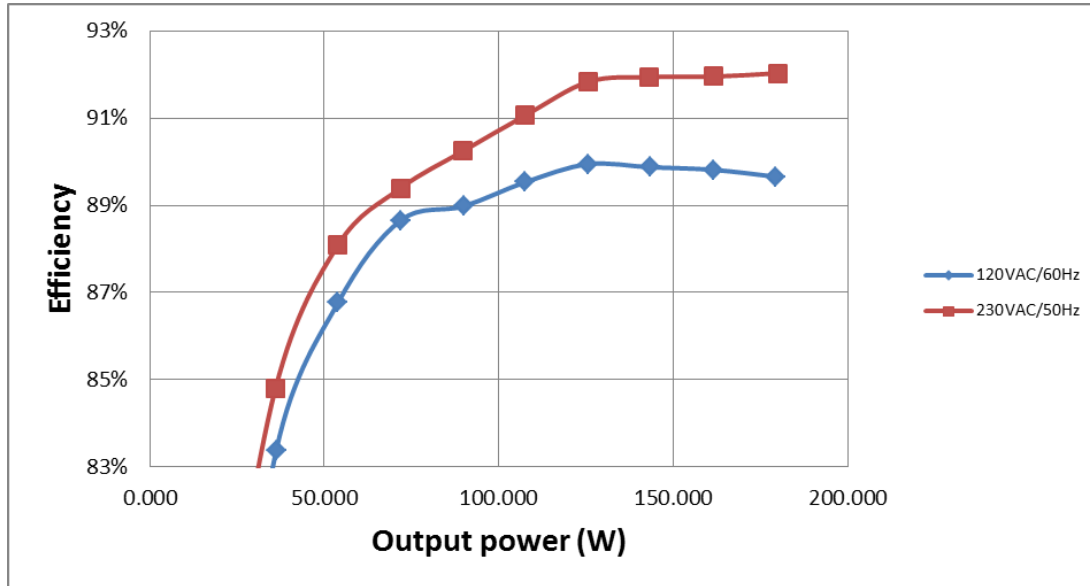

120V$_{AC}$/60Hz

Vin,rms(V)	Iin,rms(A)	Pin(W)	P.F.	THD (%)	Vout(V)	Iout(A)	Pout(W)	Losses(W)	Eff. (%)
120.01	1.654	198.06	0.998	0.640%	449	0.421	188.849	9.2106	95.35%
120.19	1.572	188.47	0.998	0.876%	449	0.400	179.780	8.6904	95.39%
119.99	1.376	164.59	0.997	1.428%	449	0.350	157.285	7.3053	95.56%
120.05	1.176	140.68	0.996	2.295%	449	0.300	134.745	5.9351	95.78%
120.06	0.982	117.25	0.994	3.634%	449	0.250	112.115	5.1347	95.62%
120.08	0.793	94.33	0.991	5.368%	449	0.200	89.710	4.6198	95.10%
120.05	0.595	70.33	0.984	7.445%	449	0.149	66.677	3.6535	94.81%
120.07	0.415	48.25	0.969	11.000%	449	0.101	45.259	2.9908	93.80%
120.18	0.321	36.75	0.952	13.906%	449	0.076	33.989	2.7607	92.49%
120.07	0.230	25.24	0.916	18.208%	449	0.051	22.675	2.5655	89.84%
120.01	0.137	13.23	0.804	38.810%	449	0.025	11.045	2.1866	83.47%

230V$_{AC}$/50Hz

Vin,rms(V)	Iin,rms(A)	Pin(W)	P.F.	THD (%)	Vout(V)	Iout(A)	Pout(W)		Eff. (%)
230	0.861	194.09	0.980	7.13%	449	0.420	188.715	5.3753	97.23%
230	0.819	184.35	0.978	7.49%	449	0.399	179.106	5.2439	97.16%
230	0.723	161.90	0.973	8.26%	449	0.350	157.060	4.8398	97.01%
230	0.624	138.55	0.965	9.32%	449	0.299	134.161	4.3888	96.83%
230	0.531	116.57	0.954	10.61%	449	0.251	112.609	3.9608	96.60%
230	0.436	93.95	0.936	14.19%	449	0.201	90.159	3.7908	95.97%
230	0.341	70.39	0.896	28.07%	449	0.150	67.305	3.0849	95.62%
230.1	0.253	48.24	0.829	40.60%	449	0.102	45.618	2.6216	94.57%
230	0.199	35.97	0.786	41.78%	449	0.075	33.720	2.2501	93.74%
230	0.154	24.30	0.686	53.64%	449	0.050	22.315	1.9847	91.83%
230	0.118	12.54	0.464	59.73%	449	0.025	11.180	1.3619	89.14%

2.2 Converter Efficiency

In the test of converter efficiency, constant current load is directly applied to the 36V output. 13.5VDC bias supply is provided at C129.

120V_AC/60Hz

Vin,rms(V)	Iin,rms(A)	Pin(W)	P.F.	Vout(V)	Iout(A)	Pout(W)	Losses(W)	Eff. (%)
120.05	1.670	200.10	0.998	35.88	5.000	179.400	20.7000	89.66%
119.99	1.502	179.77	0.998	35.88	4.500	161.460	18.3100	89.81%
119.94	1.336	159.74	0.997	35.89	4.000	143.560	16.1800	89.87%
120.1	1.167	139.66	0.996	35.89	3.500	125.615	14.0450	89.94%
119.95	1.007	120.14	0.995	35.89	2.997	107.562	12.5777	89.53%
120.01	0.849	101.04	0.992	35.89	2.505	89.904	11.1356	88.98%
120.09	0.683	81.01	0.988	35.89	2.001	71.816	9.1941	88.65%
120.06	0.528	62.09	0.980	35.89	1.501	53.871	8.2191	86.76%
120.01	0.375	43.39	0.963	35.89	1.008	36.177	7.2129	83.38%
120.07	0.224	24.49	0.912	35.9	0.501	17.986	6.5041	73.44%

230V_AC/50Hz

Vin,rms(V)	Iin,rms(A)	Pin(W)	P.F.	Vout(V)	Iout(A)	Pout(W)		Eff. (%)
230	0.867	195.44	0.980	35.9	5.010	179.859	15.5810	92.03%
230	0.782	175.69	0.976	35.9	4.500	161.550	14.1400	91.95%
230	0.698	155.80	0.971	35.9	3.990	143.241	12.5590	91.94%
230	0.617	136.90	0.964	35.9	3.502	125.722	11.1782	91.83%
230	0.538	118.23	0.955	35.9	2.999	107.664	10.5659	91.06%
230	0.459	99.49	0.942	35.9	2.501	89.786	9.7041	90.25%
230	0.380	80.36	0.921	35.9	2.001	71.836	8.5241	89.39%
230	0.306	61.19	0.870	35.91	1.501	53.901	7.2891	88.09%
230	0.229	42.43	0.805	35.91	1.002	35.982	6.4482	84.80%
230.2	0.153	23.67	0.674	35.91	0.508	18.242	5.4277	77.07%

PMP20694 Rev A Test Results

TEXAS
INSTRUMENTS

3 Thermal Images

The thermal images below show a top view and bottom view of the board. 13.5VDC bias supply is provided at C129. The board is placed vertically during the test. The ambient temperature was 25ºC with no air flow. The output was loaded with 36V/5A.

3.1 120V/60Hz – Top Side
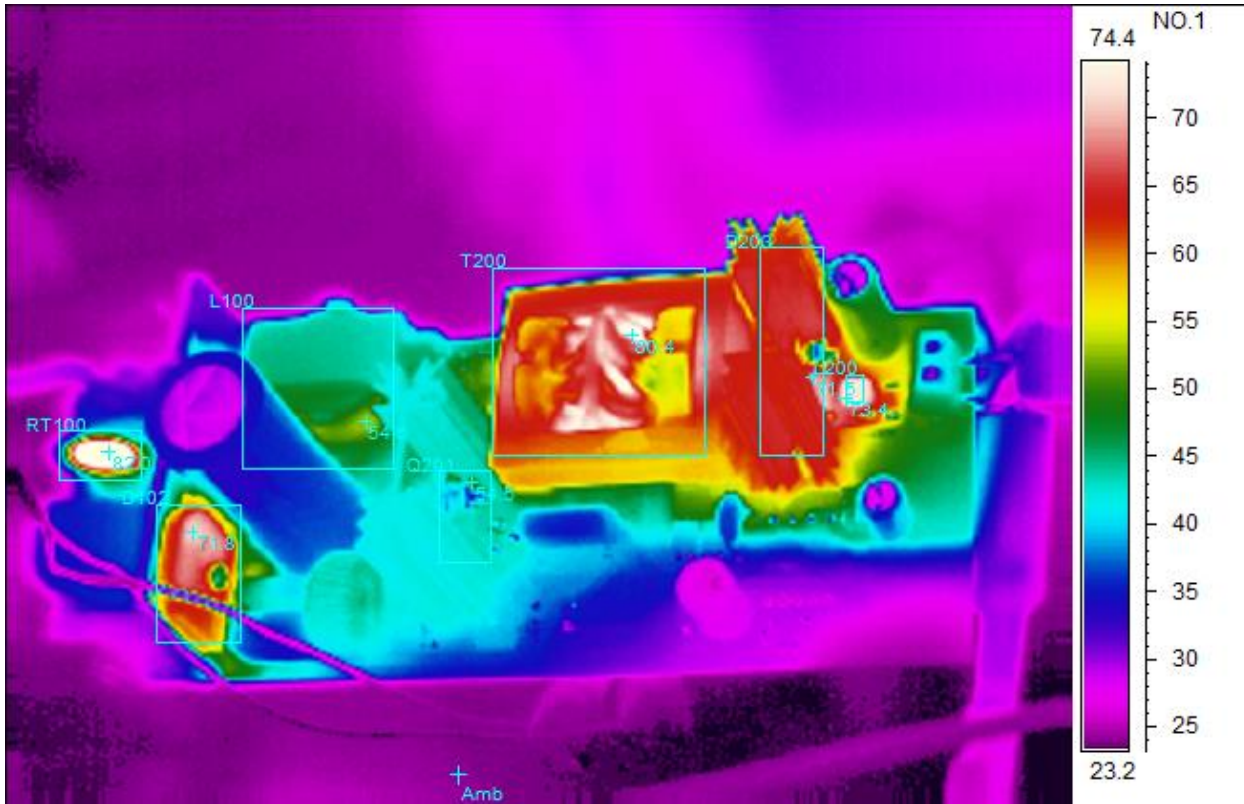
Area analysis	Value
RT100Max	82.0°C
D102Max	71.8°C
L100Max	54.6°C
Q201Max	54.5°C
T200Max	80.4°C
L200Max	73.4°C
D203Max	71.5°C

3.2   120V/60Hz – Bottom Side

PMP20694 Rev A Test Results
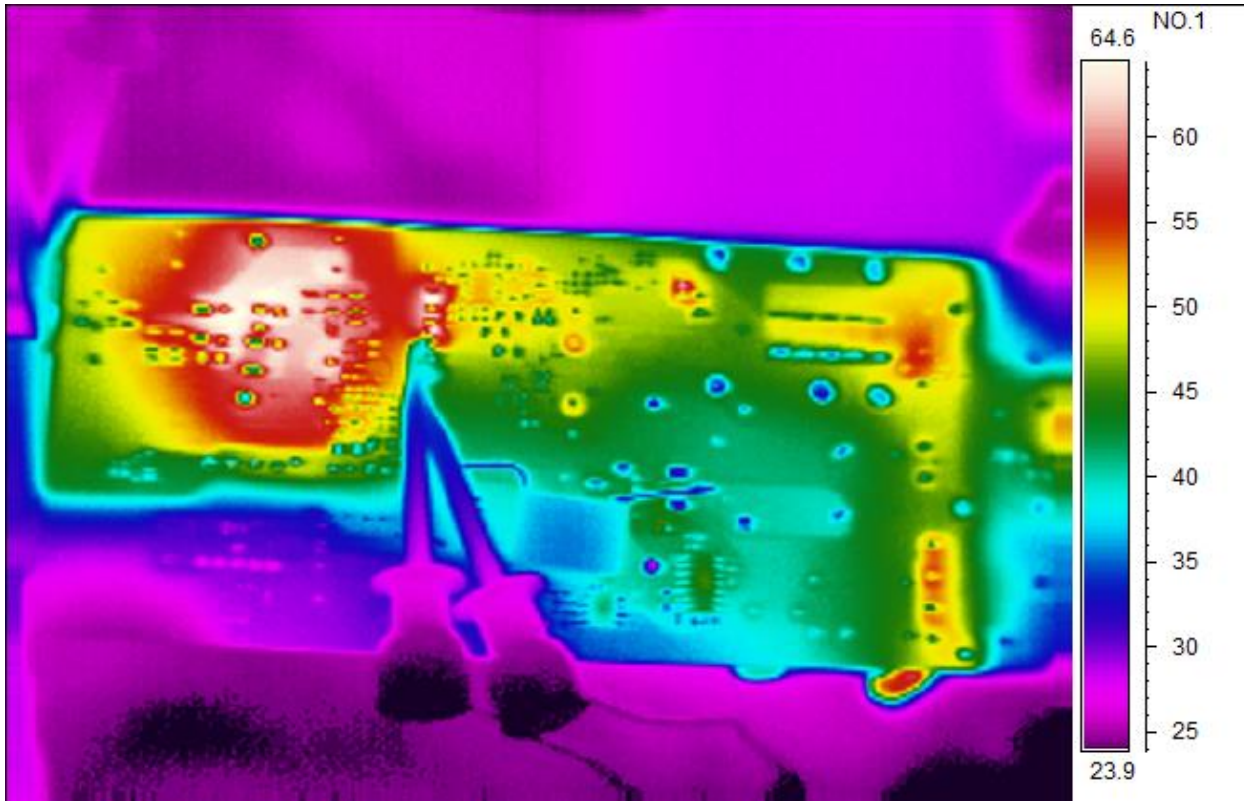
3.3   230V/50Hz – Top Side
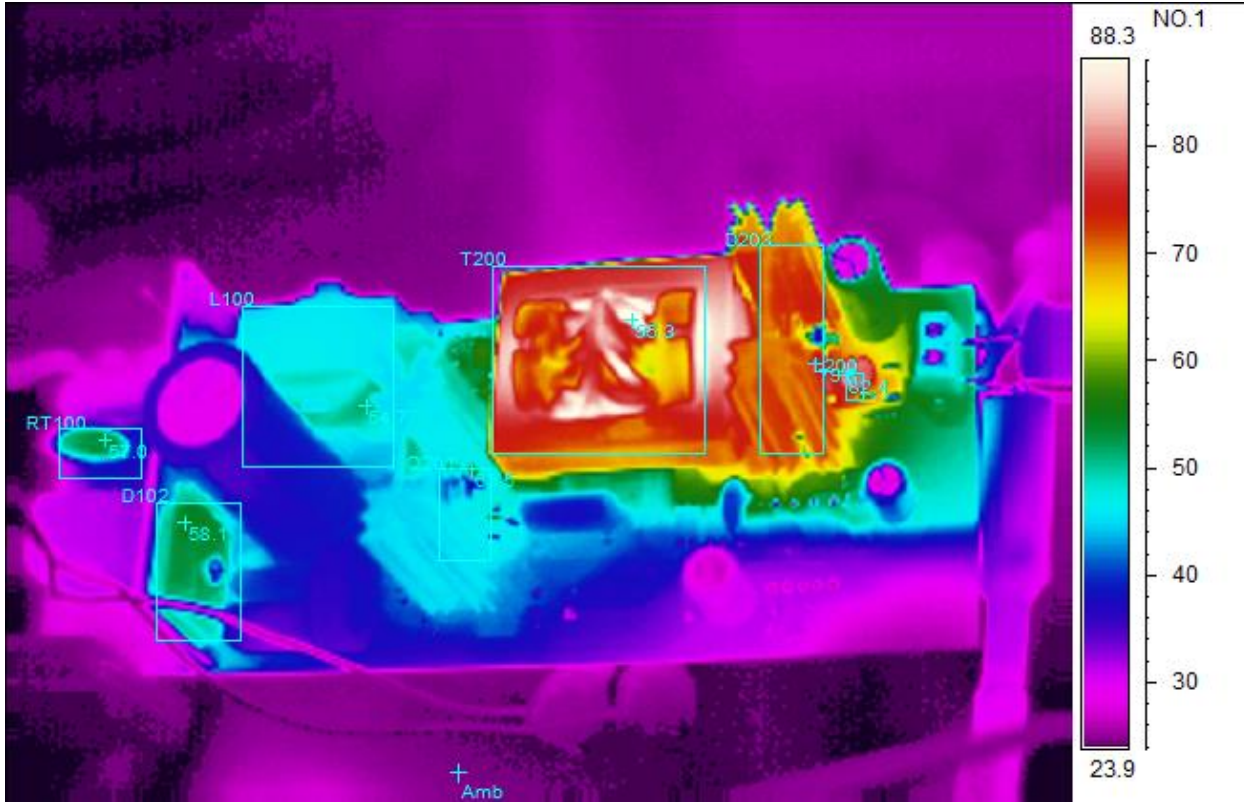
Area analysis	Value
RT100Max	57.0°C
D102Max	58.1°C
L100Max	54.7°C
Q201Max	63.5°C
T200Max	95.3°C
L200Max	82.4°C
D203Max	79.8°C

3.4   230V/50Hz –Bottom Side

Power Management Solutions
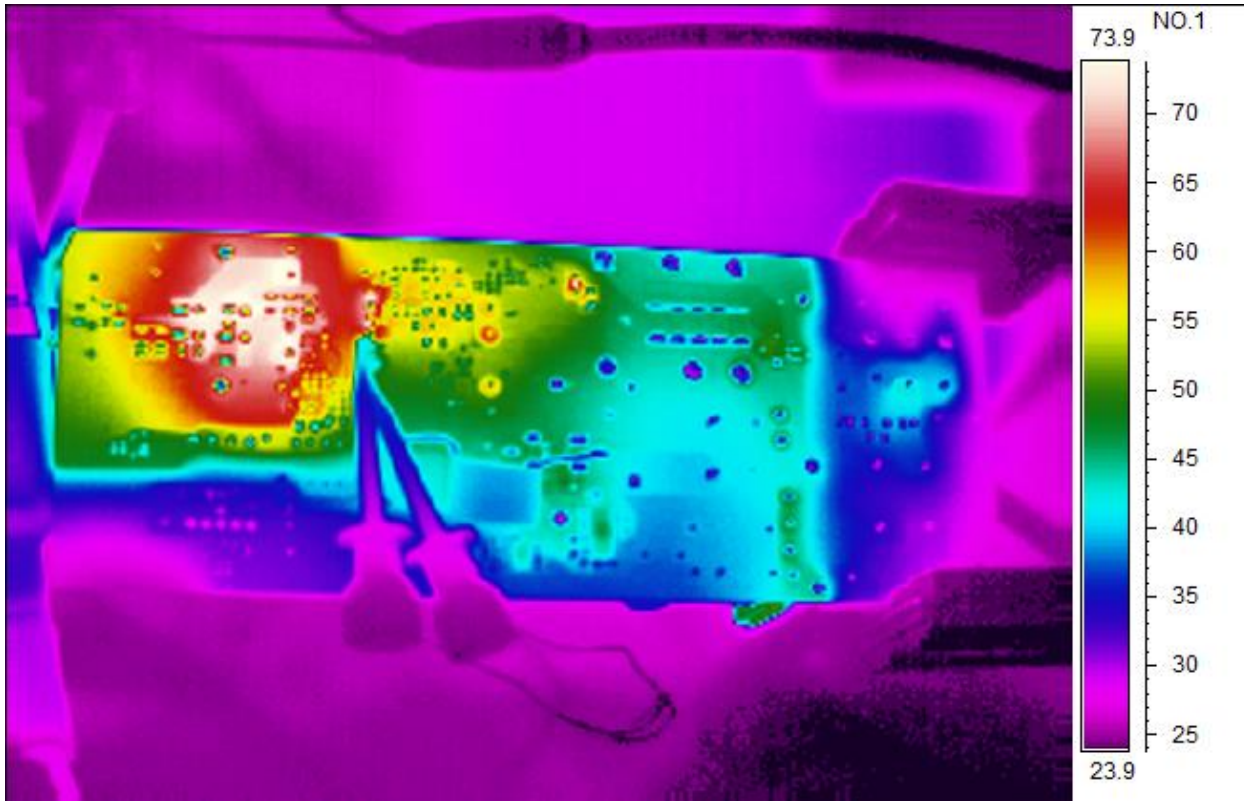
4 Startup

During the startup test, 13.5V$_{DC}$ voltage is provided to the "Bias" node to PGND after AC input is given.

4.1 Start Up @ 120V$_{AC}$/60Hz, 36V/0A:

Measure	P1:pkpk(C2)	P2:mean(C3)	P3:rms(C3)	P4:max(C3)	P5:freq(C4)	P6:- - -
value	36.0 V	75 mA	461 mA	7.7 A	---	
status						

4.2 Start Up @ 120V$_{AC}$/60Hz, 36V/5A:

Measure	P1:pkpk(C2)	P2:mean(C3)	P3:rms(C3)	P4:max(C3)	P5:freq(C4)	P6:- - -
value	36.0 V	-67 mA	1.11 A	10.2 A	---	
status						
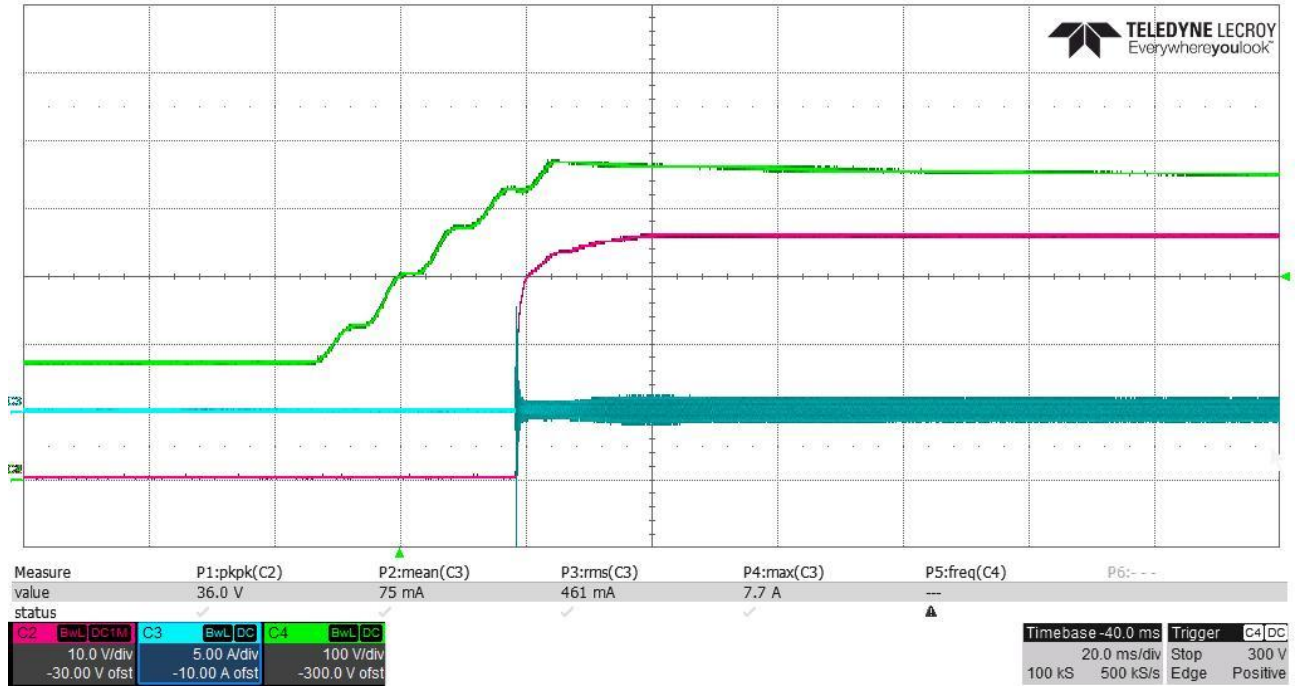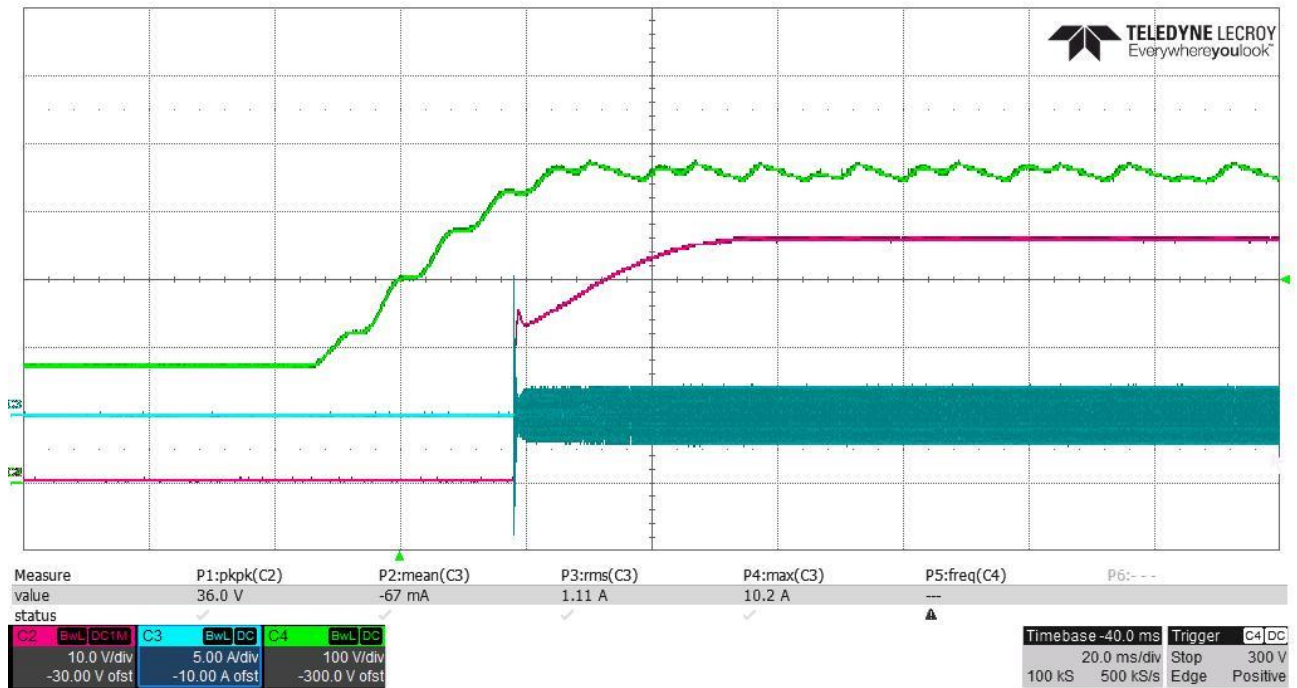
5 Turn off

This test is processed with 120VAC/60Hz input and 36V/5A output.

Measure	P1:pkpk(C2)	P2:mean(C3)	P3:rms(C3)	P4:max(C3)	P5:freq(C4)	P6:- - -
value	36.0 V	73 mA	1.05 A	2.5 A	---	
status						

C2 BwL DC1M	C3 BwL DC	C4 BwL DC
10.0 V/div	5.00 A/div	100 V/div
-30.00 V ofst	-10.00 A ofst	-300.0 V ofst

Timebase	0.0 ms	Trigger	C2 DC
	20.0 ms/div	Stop	18.0 V
100 kS	500 kS/s	Edge	Negative

TEXAS
INSTRUMENTS
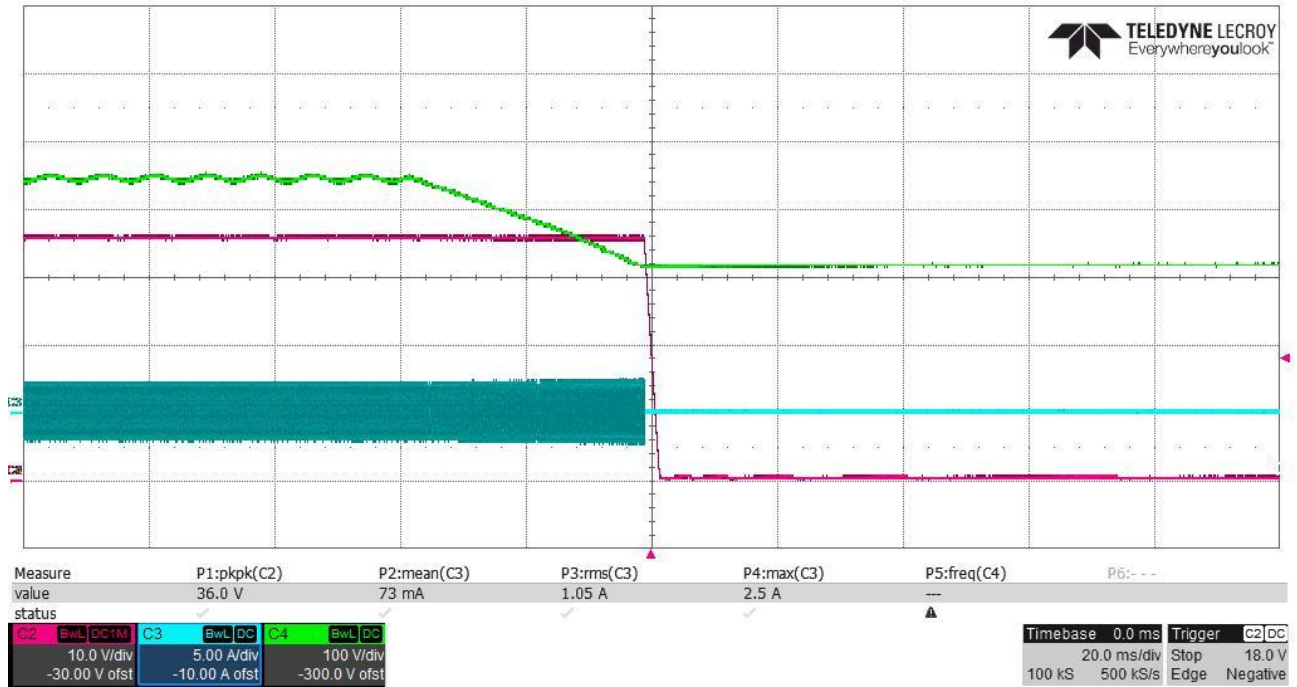
6 36V Output Ripple Voltage

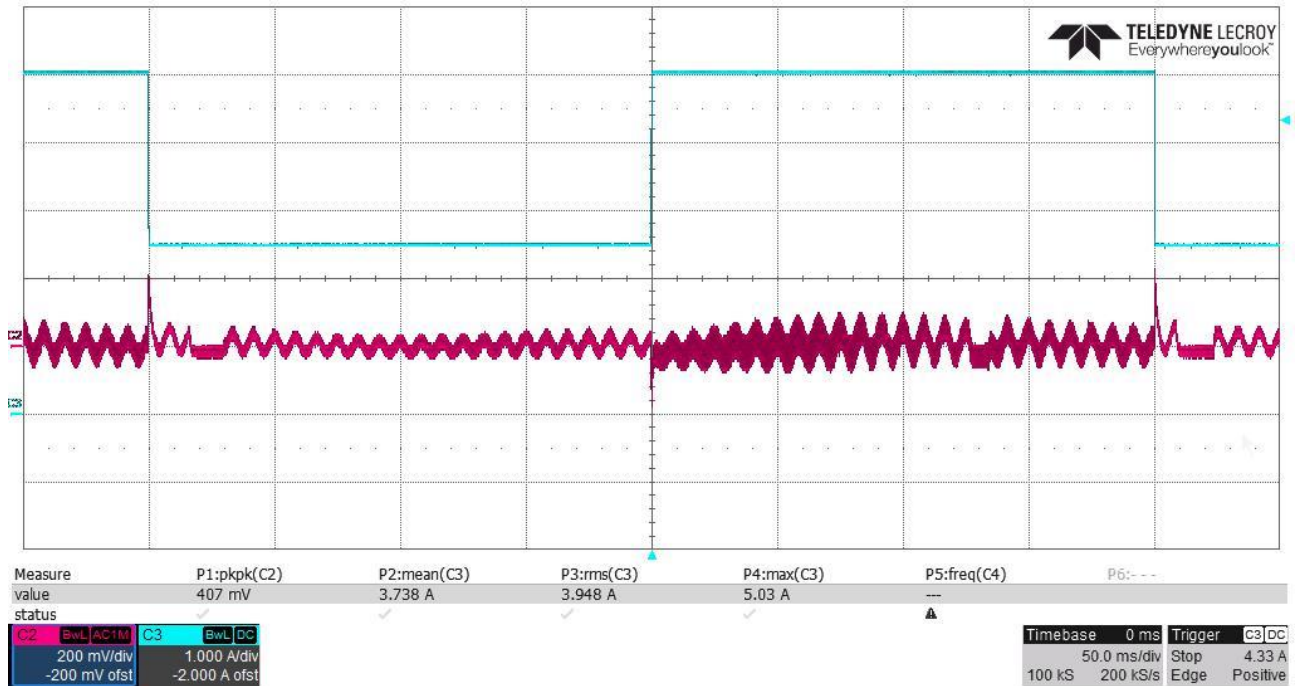The 36Voutput ripple voltage during full load operation (36V/5A) at 120Vac/60Hz is shown in the plot below.

Measure	P1:pkpk(C2)	P2:mean(C3)	P3:rms(C3)	P4:max(C3)	P5:freq(C4)	P6:- - -
value	147 mV	22 mA	1.454 A	2.20 A	130.19 kHz	
status						

C2 BwL AC1M
50.0 mV/div
0 mV offset

Timebase -10.0 ms Trigger C4 DC
5.00 ms/div Stop 224 V
100 kS 2.00 MS/s Edge Positive
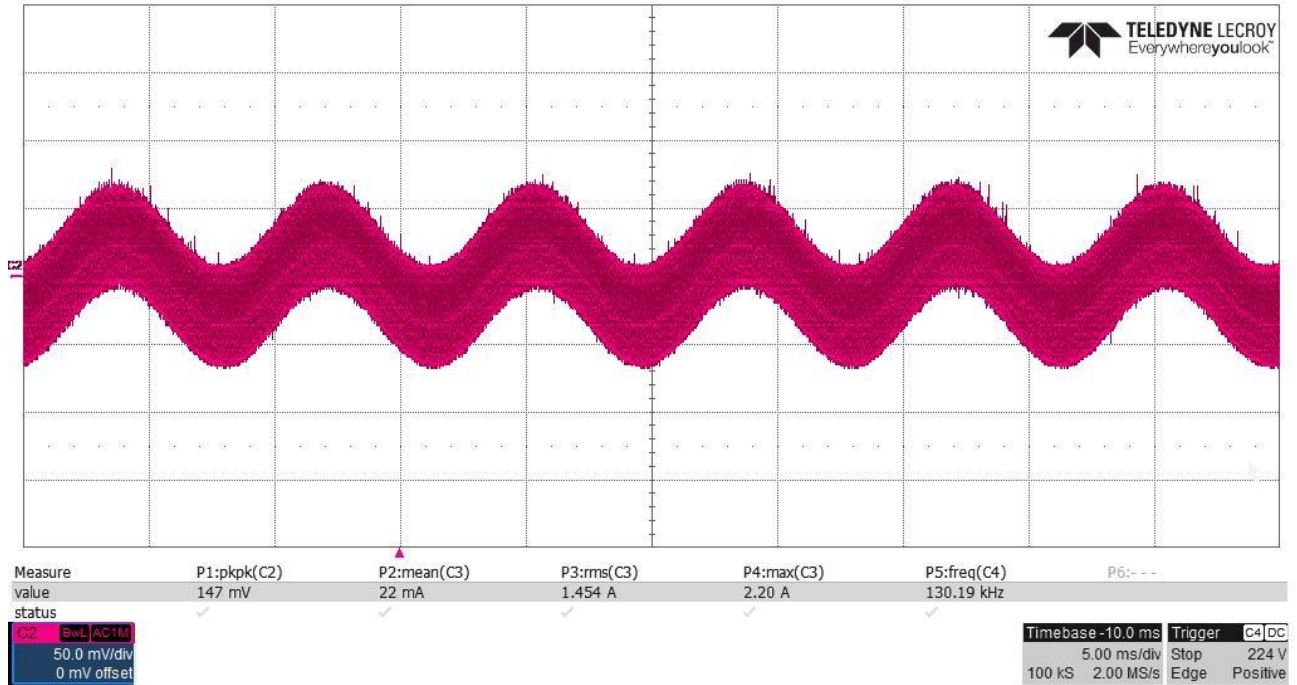
7 Dynamic response

During this test, output current load step from 2.5A to 5A with 120VAC/60Hz input.

Measure	P1:pkpk(C2)	P2:mean(C3)	P3:rms(C3)	P4:max(C3)	P5:freq(C4)	P6:- - -
value	407 mV	3.738 A	3.948 A	5.03 A	---	
status						

C2 BwL AC1M C3 BwL DC
200 mV/div 1.000 A/div
-200 mV ofst -2.000 A ofst

Timebase 0 ms Trigger C3 DC
50.0 ms/div Stop 4.33 A
100 kS 200 kS/s Edge Positive

Power Management Solutions

8   Key Waveforms

8.1   LLC steady state operation @ 120V_AC/60Hz input and 36V/0A output.

CH2: LLC output voltage (AC level); CH3: T200 primary winding current; CH4: Q201 V_{DS} voltage.

Measure	P1:pkpk(C2)	P2:mean(C3)	P3:rms(C3)	P4:max(C3)	P5:freq(C4)	P6:- - -
value	27 mV	25 mA	587 mA	1.00 A	191.93858 kHz	
status						

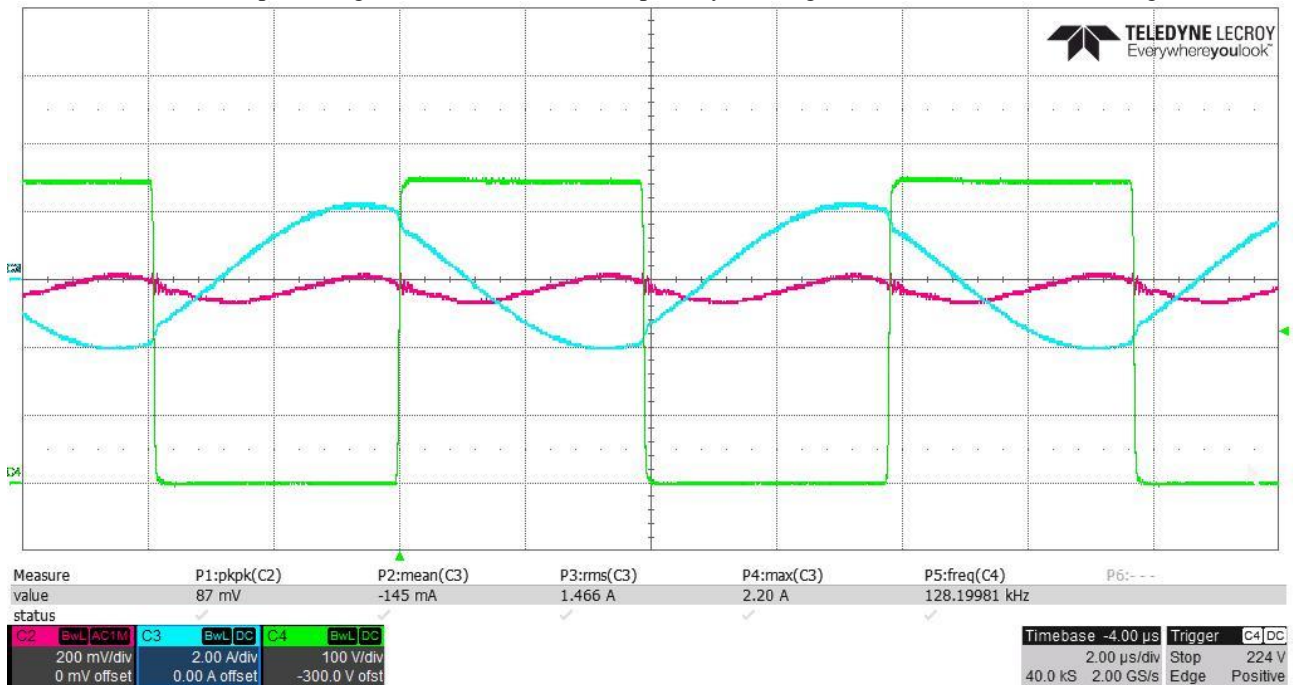| C2 BwL AC1M	C3 BwL DC	C4 BwL DC		Timebase -4.00 µs	Trigger C4 DC
200 mV/div	2.00 A/div	100 V/div		2.00 µs/div	Stop 224 V
0 mV offset	0.00 A offset	-300.0 V ofst		40.0 kS 2.00 GS/s	Edge Positive
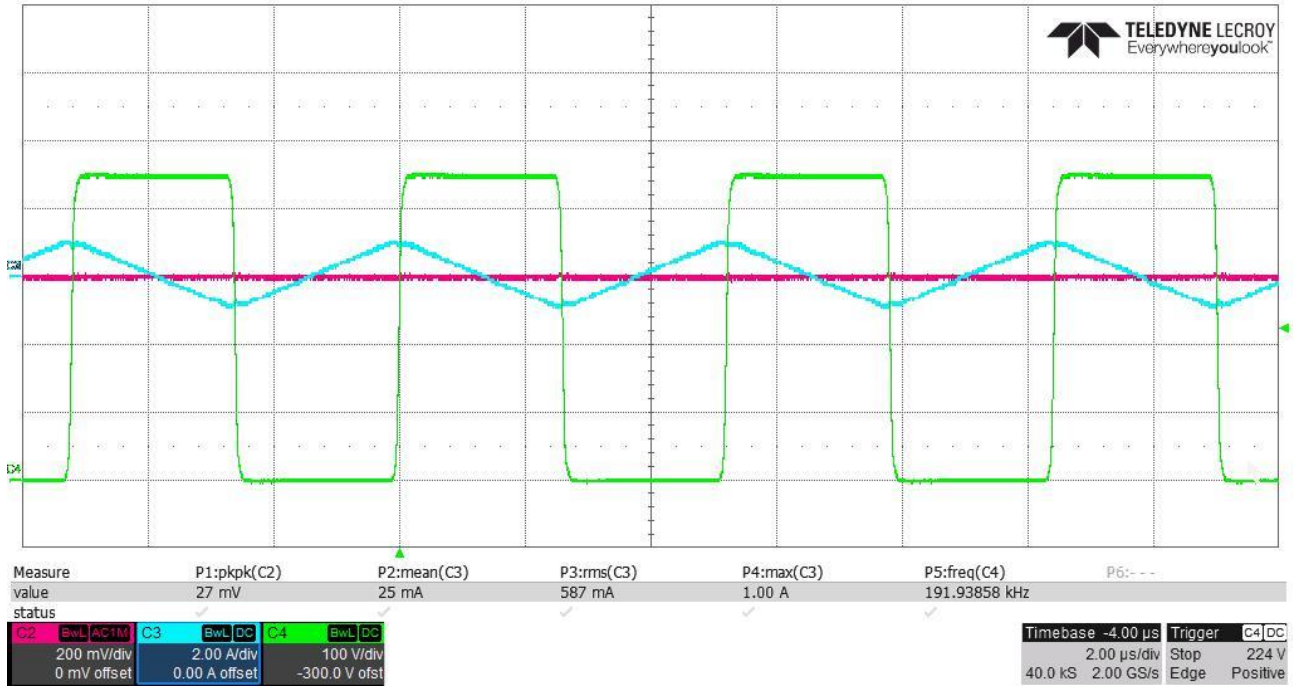
8.1   LLC steady state operation @ 120V_AC/60Hz input and 36V/5A output.

CH2: LLC output voltage (AC level); CH3: T200 primary winding current; CH4: Q201 V_{DS} voltage.

Measure	P1:pkpk(C2)	P2:mean(C3)	P3:rms(C3)	P4:max(C3)	P5:freq(C4)	P6:- - -
value	87 mV	-145 mA	1.466 A	2.20 A	128.19981 kHz	
status						

C2 BwL AC1M	C3 BwL DC	C4 BwL DC		Timebase -4.00 µs	Trigger C4 DC
200 mV/div	2.00 A/div	100 V/div		2.00 µs/div	Stop 224 V
0 mV offset	0.00 A offset	-300.0 V ofst		40.0 kS 2.00 GS/s	Edge Positive

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