Design Guide: TIDA-010962

Automated Test Equipment (ATE) 80V Discrete Floating VI Reference Design

Description

This reference design presents a four-quadrant discrete floating Voltage and Current (VI) design. Voltage output supports ±40V and 0V to 80V ranges, with three current ranges of 500mA, 10mA, and 10μA. The design operates on force voltage (FV), force current (FI), Buffer, and Gang mode with analog feedback loop. With 20-bit force digital-to-analog converter (DAC) and 18-bit, 2-channel analog-to-digital converter (ADC) and precision signal chain, the reference design achieves 0.01% accuracy for controlling and measuring after calibration.

Resources

TIDA-010962	Design Folder
TMS320F280039C	Product Folder
DAC11001B, DAC80502	Product Folder
PGA849, OPA2182, OPA182, OPA593	Product Folder
OPA596, OPA454, THS4552, OPA397	Product Folder
OPA4187, INA592, REF54, RES11A	Product Folder
TLV1872, TMUX6219, TMUX6212, TMUX6221	Product Folder
TMUX6236, TMUX6234, TCAL9539, TPSM63603	Product Folder
TPSM82912, TPS7A9401, TPS7A2018	Product Folder

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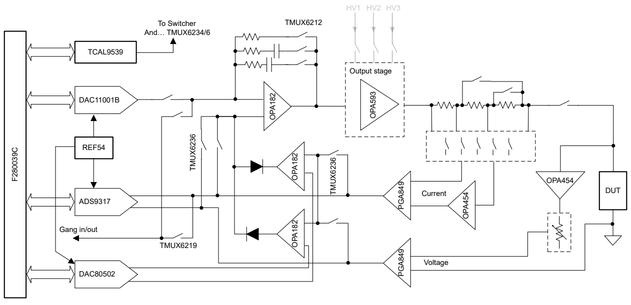
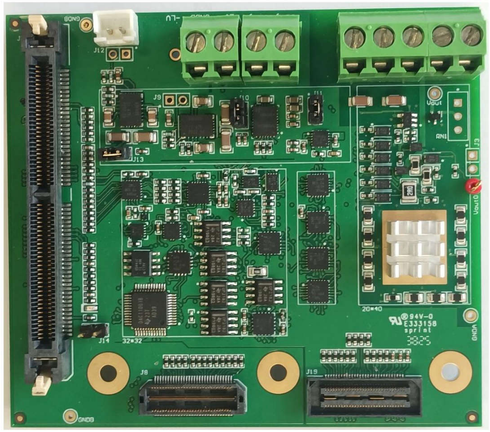
Features

- Supports FV, FI, ganging, buffer output, and stack-up
- Force DAC: 20 bit, up to 1Msps. Sensing ADC: 18 bit, up to 5Msps. Clamp DAC: 15 bit for ±40V, 16 bit for 0V to 80V
- Voltage output range: 0V to 80V, ±40V. Current range: 10μA,10mA, 500mA
- Voltage output accuracy: < 25ppm of full scale (FS) at constant voltage (CV), ±40V range, room temperature
- Current output accuracy: < 30ppm of FS at constant current (CC), ±500mA, room temperature
- Rising time: About 50μs (from –40V to +40V) at open load, ±40V range, 500mA. Settling time: About 20μs (open to full load or reverse)
- Support capacitance load: > 100μF
- Small size: low-voltage signal chain 32mm × 32mm, high-voltage output 20mm × 40mm

Applications

- Parametric measurement unit (PMU)
- Source measurement unit (SMU)





1 System Description

In semiconductor testers, many different function cards perform different testing purposes. These cards include Device Power Supply (DPS), Pin Electronics (PE), Parametric Measurement Unit (PMU), high-voltage (HV) PMU, Digitizer, and Arbitrary Waveform Generator (AWG), and so forth. Each board has single or multiple functions based on design topology. DPS supplies power to design under test (DUT). PE integrates pin driver and Per Pin Parametric Measurement Unit (PPMU) and active load to test many functions. PE performs pattern testing and open or short testing and pin-level testing and so forth. AWG generates arbitrary waveforms to measure Signal-to-Noise Ratio (SNR) and Total Harmonic Distortion (THD), and so forth. PMU tests DUT parameters accurately and supports Force Voltage Measure Current (FVMI) or Force Current Measure Voltage (FIMV) or just Measure Voltage (MV). PMU accurately forces and measures voltage and current of DUT. PMU cards include low-voltage (LV) PMU cards and HV PMU cards for different DUT voltage applications. Low-voltage PMU uses integrated chip design because integrated chips are smaller and increase channel design density.

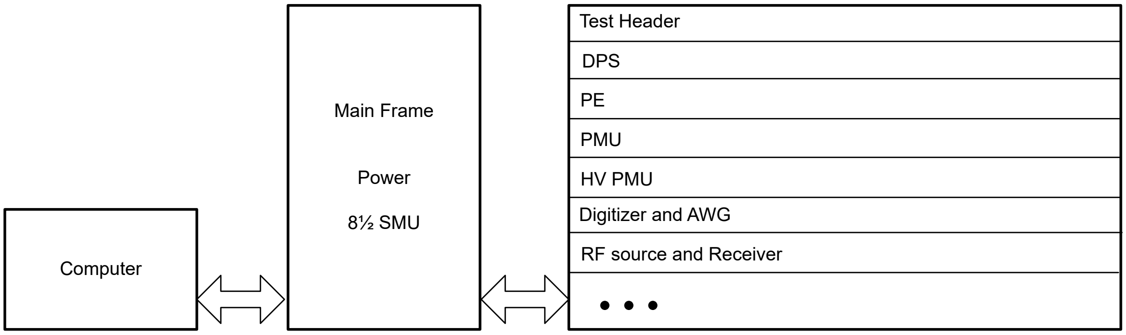


Figure 1-1. ATE Tester Components

High-voltage PMU offers forcing and measuring high voltage and current. HV PMU covers automobile level chips or Battery Management System (BMS) chips or discrete component testing requirements. HV PMU needs high-resolution DAC and ADC to achieve smaller controlling and measuring voltage step. HV PMU maintains accuracy requirements in small output range. In this reference design, 20-bit fast DAC and 18-bit fast ADC achieve very high accuracy fast controlling and measuring with precision signal chain.

1.1 Key System Specifications

PARAMETER	SPECIFICATION
Support working mode	FV, FI, ganging, buffer output, stacking_up
Voltage range	0V–80V, ±40V
Current range	500mA, 10mA, 10µA
Voltage output accuracy	< 25ppm at CV, 500mA, room temperature
Current output accuracy	< 30ppm at CC, 500mA, room temperature
ADC read voltage accuracy	< 20ppm at CV, 500mA, room temperature
ADC read Current accuracy	< 40ppm at CC, 500mA, room temperature
ADC read voltage swing LSB	About 3LSB at CV, 500mA, room temperature
ADC read current swing LSB	About 4LSB at CC, 500mA, room temperature
Rising time	About 50µs at –40V to 40V, open load, CV, 500mA
Settling time	About 20µs at no load to full load, CV, 500mA
Capacitance load	> 100µF

WARNING

TI intends this reference design to be operated in a lab environment only and does not consider the reference design to be a finished product for general consumer use.

TI Intends this reference design to be used only by qualified engineers and technicians familiar with risks associated with handling high-voltage electrical and mechanical components, systems, and subsystems.

High voltage! There are accessible high voltages present on the board. The board operates at voltages and currents that can cause shock, fire, or injury if not properly handled or applied. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property.

Hot surface! Contact can cause burns. **Do not touch!** Some components can reach high temperatures > 55°C when the board is powered on. The user must not touch the board at any point during operation or immediately after operating, as high temperatures can be present.

CAUTION

Do not leave the design powered when unattended.

2 System Overview

2.1 Block Diagram

Figure 2-1 shows power structure of this reference design.

High voltage power rail supplies output stage of OPA593. These two power rails need be isolated, and low voltage rail ground is connected to OPA593 output which make low voltage circuit float on high-voltage output stage as Figure 2-1 diagram showed.

The power rail contains two group power rails. One rail operates at low voltage with input from external +15V. The low-voltage rail powers the DAC, ADC, and signal chain. The other rail operates at high voltage with input from external +43V, –42V or +83V, –2V based on expected voltage range testing. The high voltage power rail supplies the output stage of OPA593. These two power rails require isolation. The low-voltage rail ground connects to the OPA593 output. Figure 2-1 shows how this connection makes the low-voltage circuit float on the high-voltage output stage.

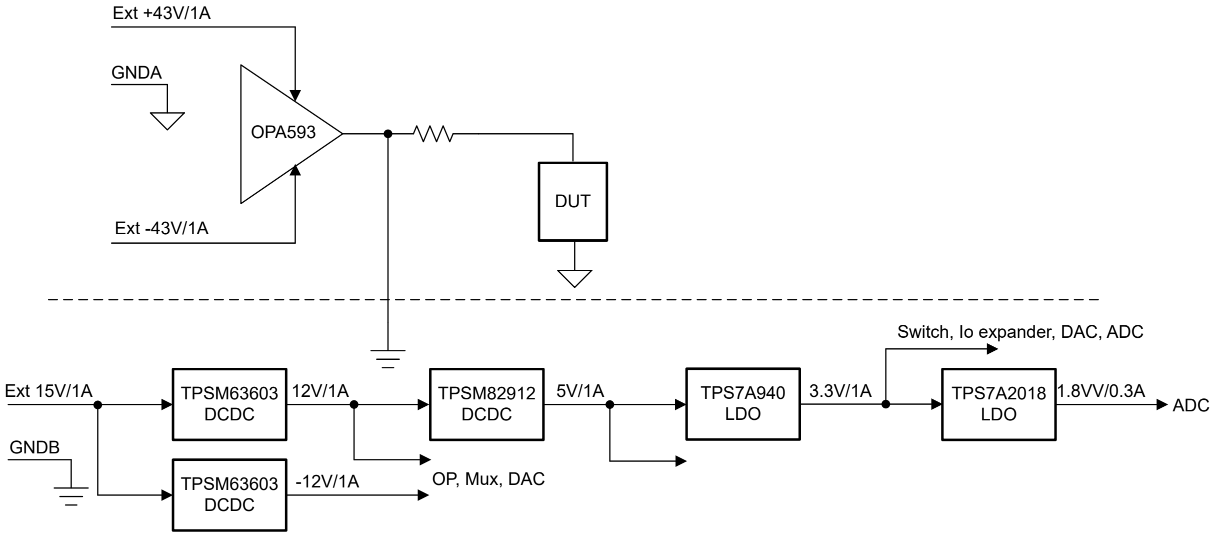


Figure 2-1. TIDA-010962 Power Rail Block Diagram

Figure 2-2 shows the signal chain block diagram of this reference design.

In the force path, DAC11001B sets force voltage or current to the force path when the clamp does not trigger. Twelve compensation options consist of four resistors and three capacitors. In the power output stage, four parallel OPA593 chips meet 500mA output capacity for all temperature ranges. Three current range selections use series topology design.

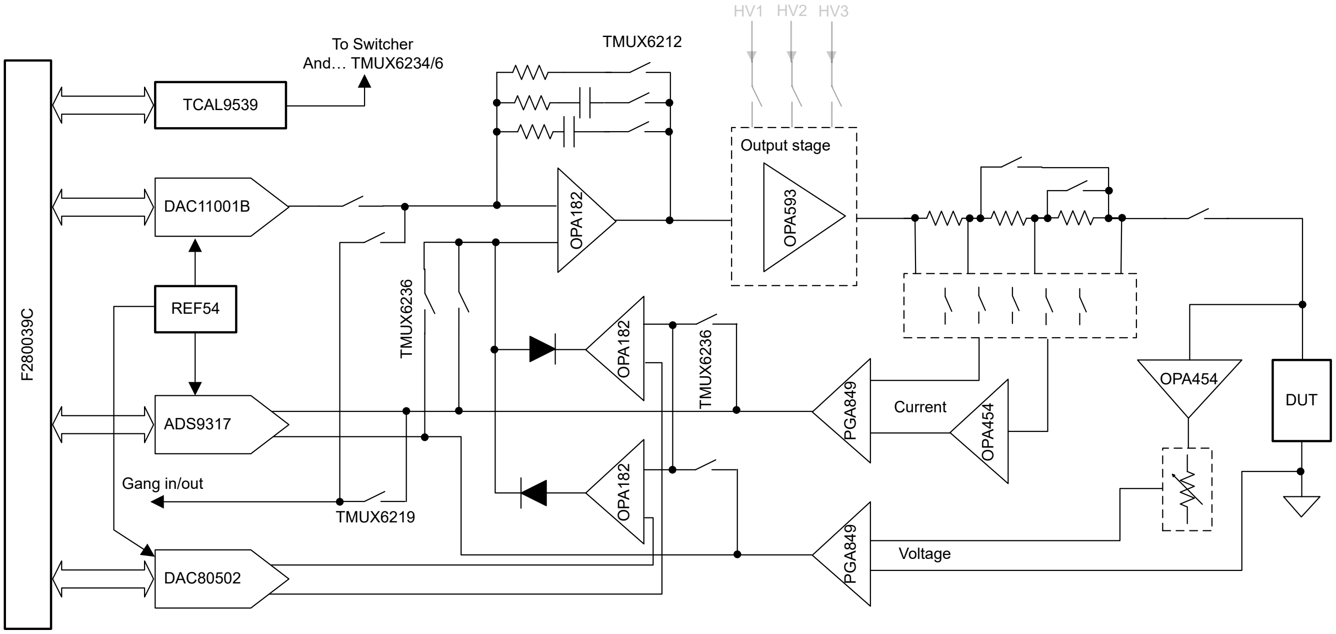


Figure 2-2. TIDA-010962 Signal Chain Block Diagram

In the sensing path, OPA454 acts as a low-leakage amplifier and buffers voltage from the output rail. PGA849 functions as a high-precision programmable gain amplifier to sense differential current and remote DUT voltage. Differential DUT voltage and current signals are achieved after PGA849. These signals connect to the force loop or clamp loop based on constant voltage (CV) or constant current (CC) settings. ADS9317 operates as a high resolution and high-speed data converter with dual channels to sample voltage and current. Current signals can output or input externally for Gang function mode. REF54 generates a low-drift 4.096V reference voltage for all related components such as ADC, DAC, and bias voltage. Single reference voltage design benefits long-term drift calibration.

2.2 Design Considerations

This reference design presents a high-precision analog closed-loop design. Designers must carefully address the considerations in this section.

2.2.1 Loop Bandwidth

Forcing and sensing path bandwidth directly influences loop transient response. Regardless of compensation, the larger the forcing and sensing bandwidths are, the faster the transient becomes. OPA593 has 10MHz bandwidth and 45V/µs slew rate, with Full Power Bandwidth (FPBW) of 180kHz, and OPAx182 has 5MHz and 10V/µs slew rate, and PGA849 has 10MHz bandwidth and 35V/µs.

2.2.2 Fast Setting and Sampling

DAC11001B appears in this reference design. The component presents a 20-bit, high precision, 1Msps, 1µs settling DAC. The component can output positive and negative with respective reference input. Maximum Integral Nonlinearity (INL) reaches 1 Least Significant Bit (LSB). The component has excellent THD; –118dB at 20kHz.

ADS9317 presents 18-bit, 5Msps, 2 LSB INL dual-channel ADC. The component integrates an averaging feature for stabilizing data output.

2.2.3 Low Temperature Drift and Long-Term Drift

Temperature drift design influences calibrated accuracy. OPAx182 maximum offset drift 20nV/°C, PGA849 maximum offset drift 1µV/°C (4V output) and maximum gain drift 2ppm/°C, REF54 0.5ppm/°C. RES11A maximum TCR 2ppm/°C. An important temperature drift component is a high current sensing resistor. The component directly influences accuracy and linearity. Choose a sensing resistor with a power rating of 2× the maximum power consumption.

For long-term drift, the drift mostly comes from a reference component. REF54410 has 32ppm in first 2000hr.

2.2.4 Output Capacity

The maximum output that this reference design can support is 500mA. A single OPA593 device only has 250mA output capability. Considering temperature influence, the design uses four paralleled OPA593 devices as Figure 2-3 shows. A 2Ω series resistor balances current among the four OPA593 amplifiers.

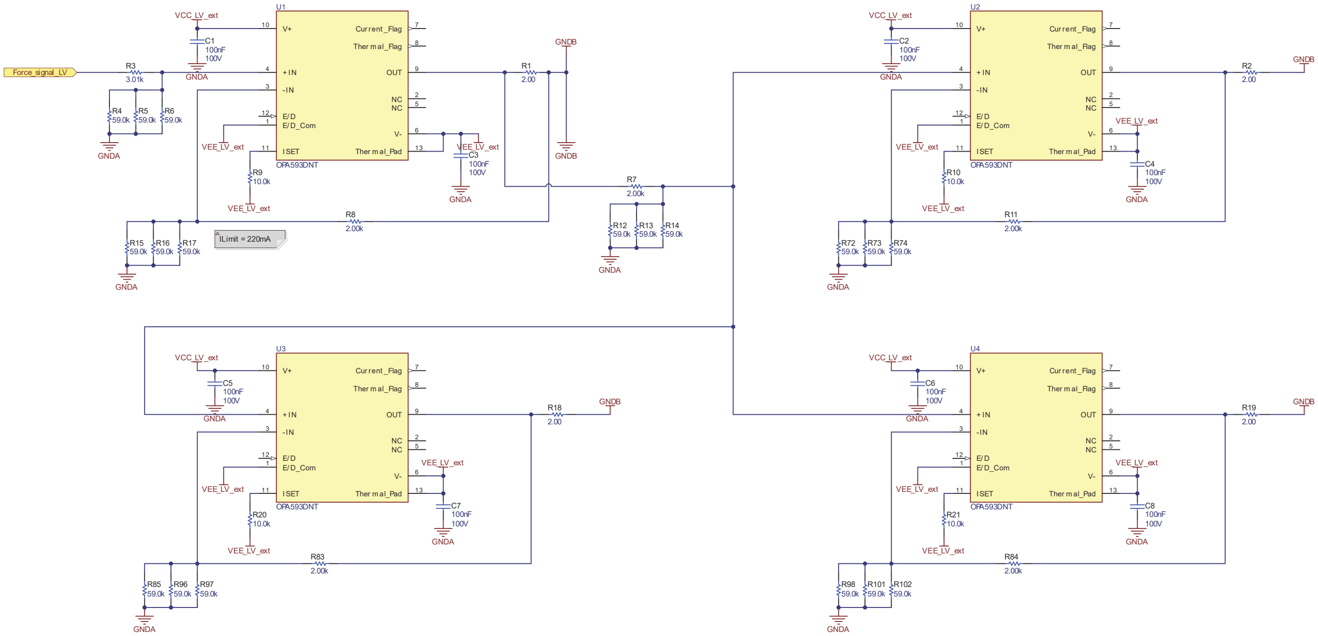


Figure 2-3. 4 × OPA593 Output, 500mA Current

2.2.5 Linearity

Several points influence output linearity. One point involves the OPA593 power supply. OPA593 operates as a rail-to-rail output power op amp but requires headroom with output current and temperature. Figure 2-4 shows this relationship. The design provides 3V margin for positive supply and 2V margin for negative supply based on the specification.

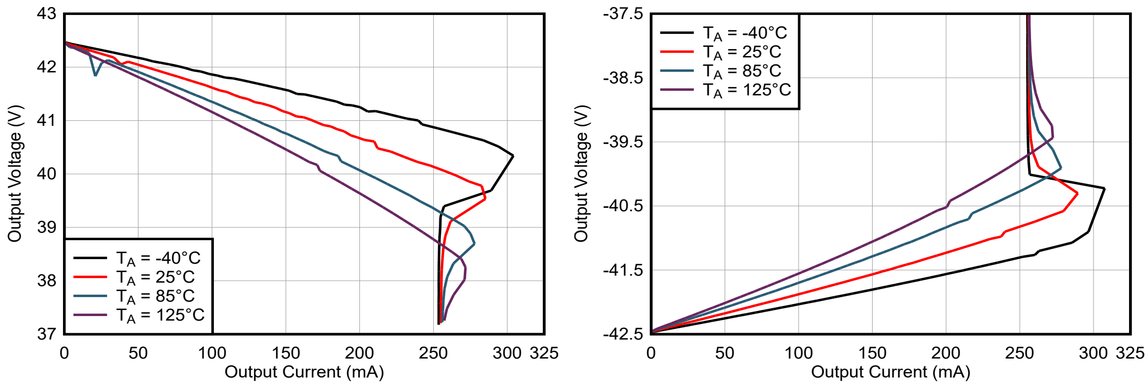


Figure 2-4. OPA593 Output Current vs Temperature

Because OPA593 does not operate as a rail-to-rail input power operational amplifier, the input voltage needs 3.5V less than positive power supply. Figure 2-5 shows the addition of an input divider.

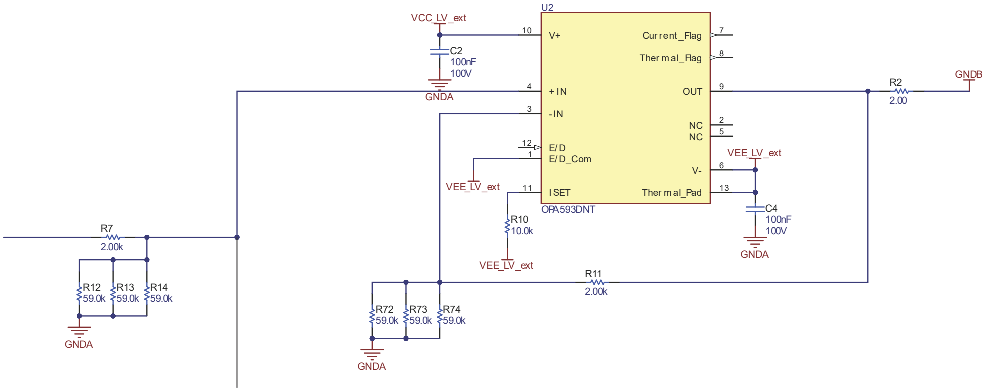


Figure 2-5. OPA593 Input Divider

In the control loop, the multiplexer and the switcher have internal resistance which can be inserted into the precision comparison circuit. The op-amp buffer can remove this resistance. Otherwise, linearity and temperature drift performance degrades. Figure 2-6 illustrates the force and sensing comparison buffer operation.

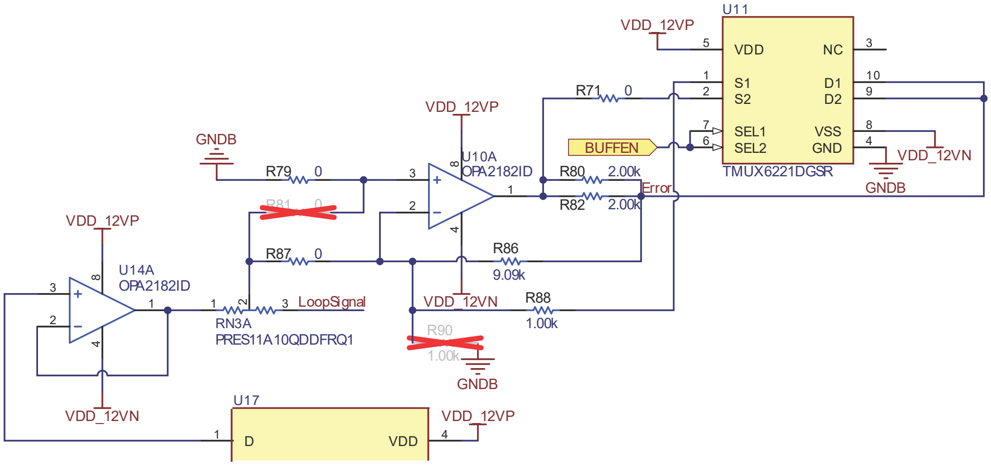


Figure 2-6. Comparison Buffer

Heat creates a big influence point. Selecting appropriate power rating and package components becomes critical. Choose a higher power rating sensing resistor or voltage divider, and maintain good cooling conditions.

2.2.6 Current Leakage

When measuring or forcing µA current to the DUT, component leakage becomes a key factor in force path connection. OPA454 has a typical 1.4pA and less than 10pA at temperatures below 80°C. When high-voltage output and DUT short suddenly occur, the OPA454 helps convert high voltage to low voltage range with external circuitry to avoid damaging low voltage circuits. Figure 2-7 illustrates this circuitry.

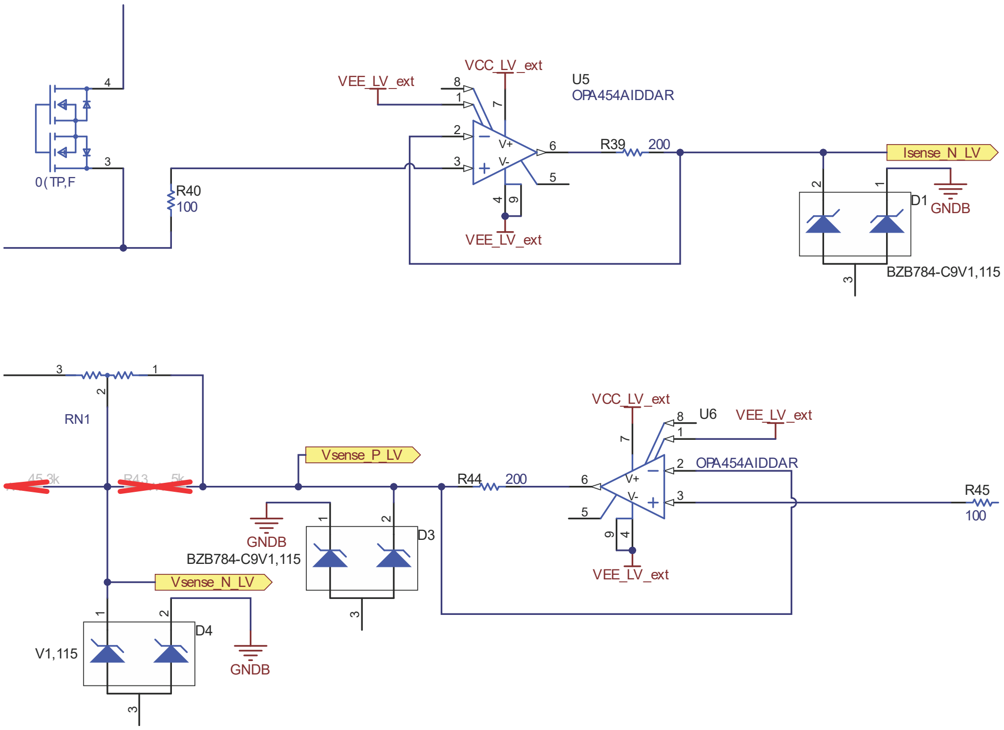


Figure 2-7. Voltage and Current Sensing Buffer

Figure 2-8 and Figure 2-9 show OPA454 bias current with input voltage. The OPA454 works well for nA-level current range design.

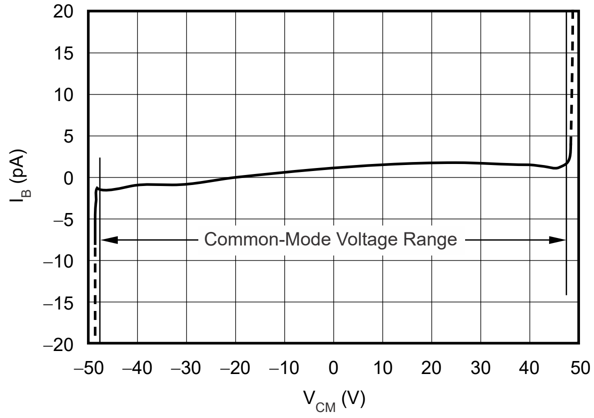


Figure 2-8. Sensing Buffer OPA454 Current Leakage

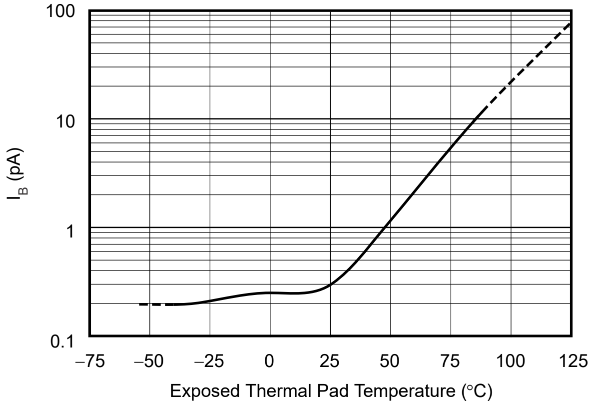
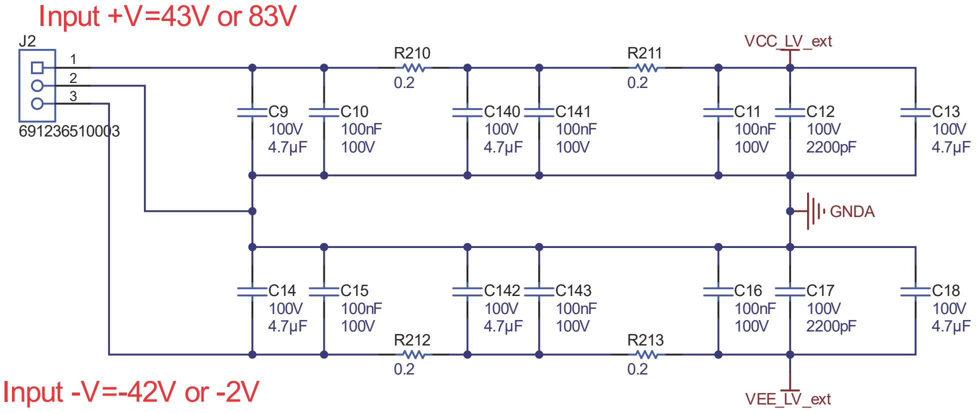


Figure 2-9. Unique Title Required

2.2.7 Reduce Noise

A major noise source comes from power. In this design, for external high-voltage input, two π filters reduce noise, see Figure 2-10. Considering size and voltage drop, two 200mΩ resistors and a 4.7µF capacitor achieve less than 50kHz bandwidth. When using 47µF, bandwidth becomes less than 5kHz, see Figure 2-11.


Input +V=43V or 83V

Input -V=-42V or -2V

Figure 2-10. HV Input Filter

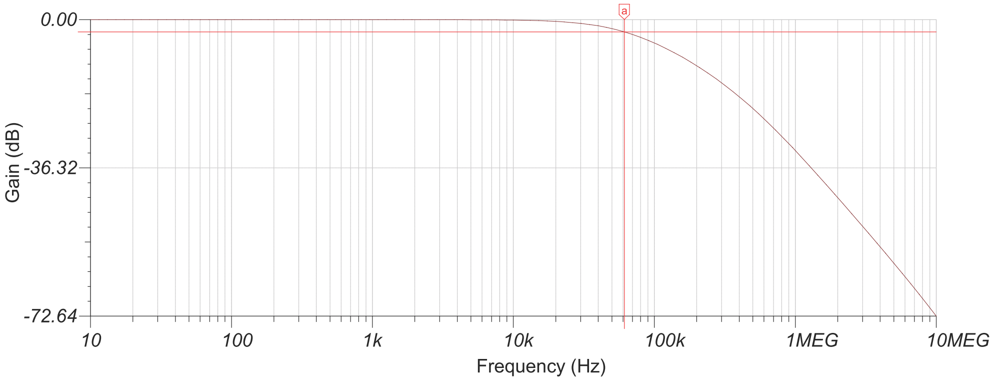


Figure 2-11. HV Input Filter Bandwidth

For the low-voltage power rail, TPSM63603 power module noise ripple remains less than 14mV at 1A. This module generates +12V and –12V with IBB topology for all signal chain components. TPSM82912 operates as a low-noise and low-ripple buck power module with noise ripple less than 10µV_{RMS}. This module generates 5V to DAC and reference power. TPS7A9401 functions as an ultra-high Power Supply Rejection Ratio (PSRR) Low Dropout Regulator (LDO) with 110dB at 1kHz and generates 3.3V for ADC and DAC. TPS7A2018 also operates as an ultra-low-noise LDO with 95dB at 1kHz and generates 1.8V for the ADC core.

The OPA593 device has a maximum 120dB and over 60dB at 10kHz PSRR. The 10nV/$\sqrt{Hz}$ at 1kHz input noise provides sufficient performance for low output noise. This configuration reduces output noise to the minimum level.

2.2.8 Reduce Glitch When Switching Current Range

Figure 2-12 shows how the TIDA-010962 adopts series current-sensing resistor topology. The series impedance does not change to 0Ω suddenly when switching to different current ranges. Furthermore, switching becomes smoother by optimizing switching logic and short clamp input.

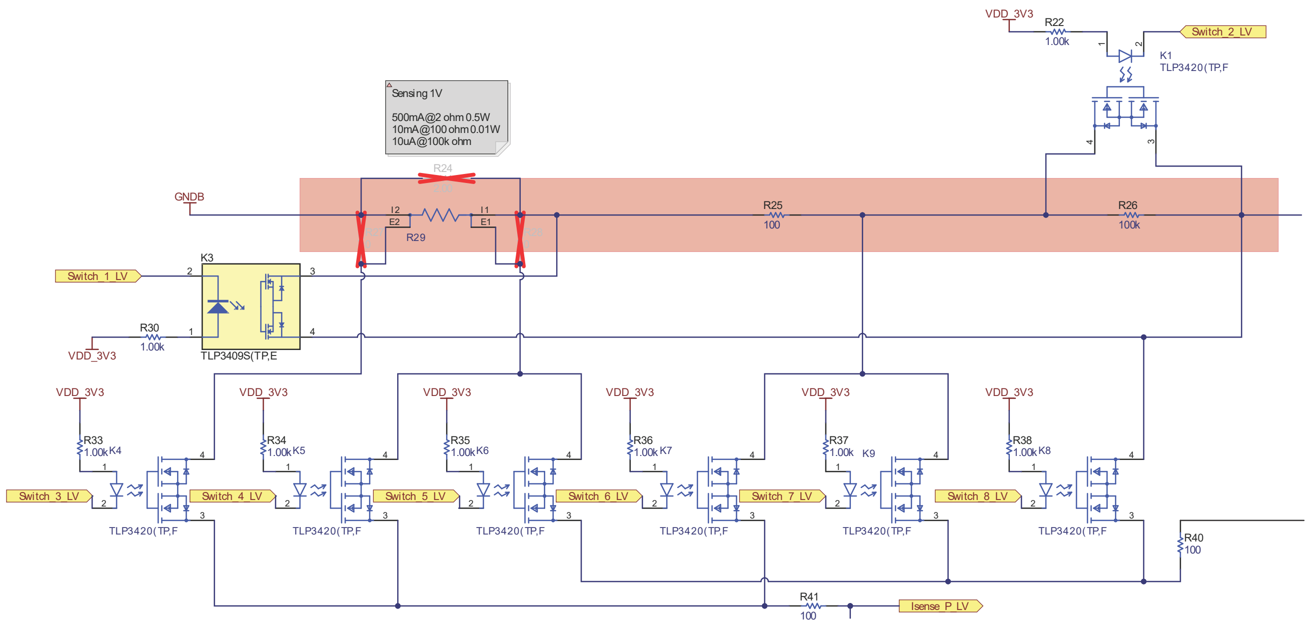


Figure 2-12. Series Current-Sensing Resistors

2.2.9 Heat Design

Heat becomes a very important design point with a large influence on linearity and accuracy.

2.2.9.1 OPA593

Because OPA593 operates as a linear output op amp, each OPA593 device needs to output 125mA when maximum output reaches 500mA. Despite thermal resistance as small as 4.3°C/W, heat ramps up without good heat sink design. The heat plate is on the bottom of OPA593. Place four OPA593 devices on the bottom of board and place a heat sink on the opposite side, see Figure 2-13.

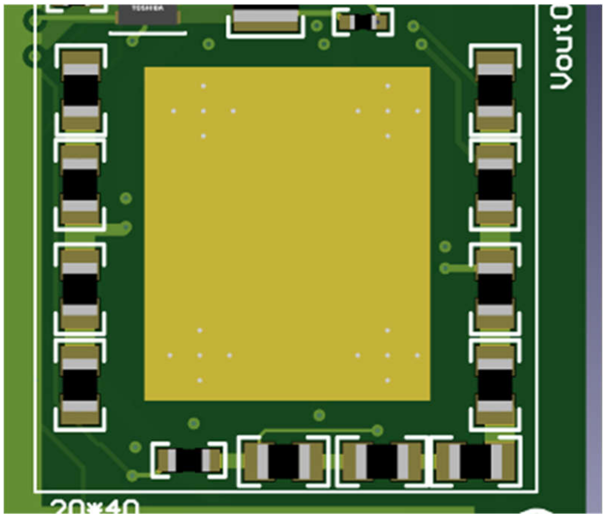


Figure 2-13. Thermal Pad of 4 × OPA593

2.2.9.2 OPA593 Divider Resistor and Series Resistor

Excessively large resistance of the divider affects OPA593 bandwidth, while excessively small resistance cannot handle power consumption when the output reaches high levels. OPA593 input approaches 83V, with a rough calculation showing 0.3W. Figure 2-14 shows the circuit using three parallel, 0805, 59kΩ resistor can dissipate 0.25W.

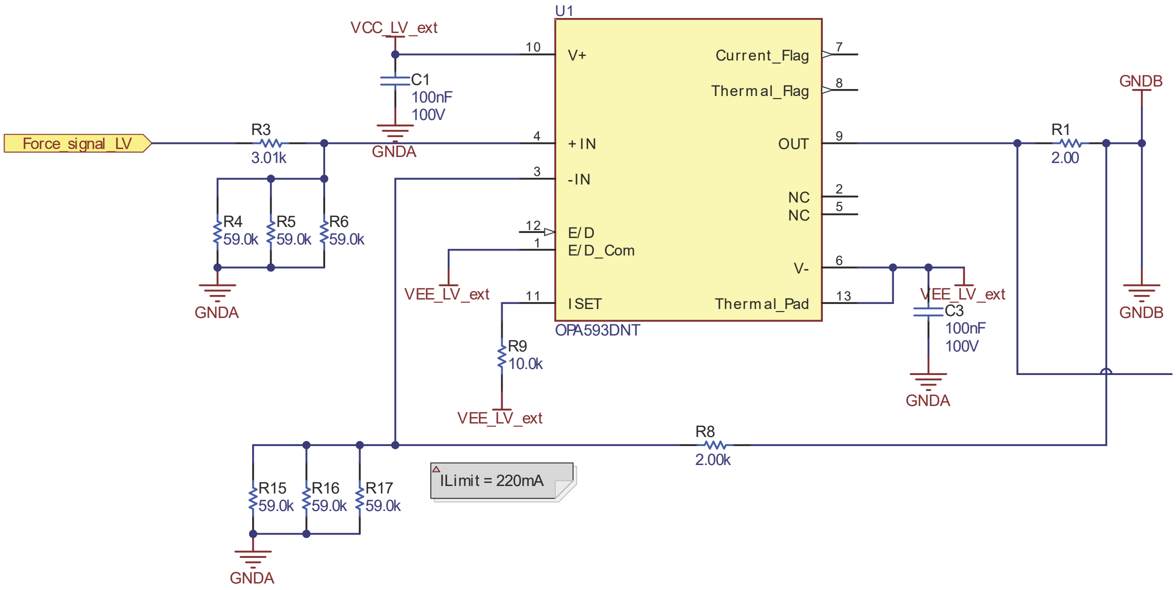


Figure 2-14. Parallel Resistors in OPA593 Input

For a balanced current series resistor, the circuit needs to conduct 125mA at minimum. Select a 0805 packaged, 2Ω resistor, with a maximum power of 0.03W.

2.2.9.3 Current Sensing Resistor and Feedback Voltage Divider

For the 500mA current range, the sensing resistor measures 2Ω, with total power of 0.5W. Engineers strongly recommend selecting a 1W rating and low Temperature Coefficient of Resistance (TCR) precision resistor. Place a heat dissipation area in the layout to quickly sink heat from the resistor, see Figure 2-15.

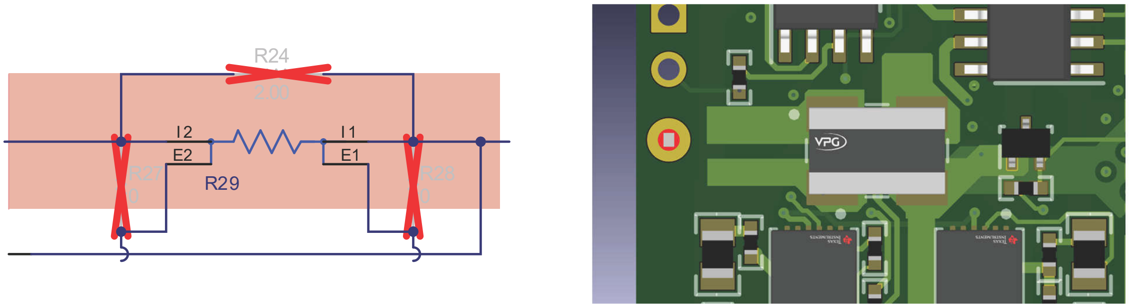


Figure 2-15. 500mA Current Sensing Resistor Thermal Pad

For the voltage divider (see Figure 2-16), the maximum output reaches 80V. Similar to the previous reason, the large resistance affects loop bandwidth. When selecting an 18kΩ/2kΩ divider, TI recommends 0.5W at minimum and use the lowest TCR divider resistor.

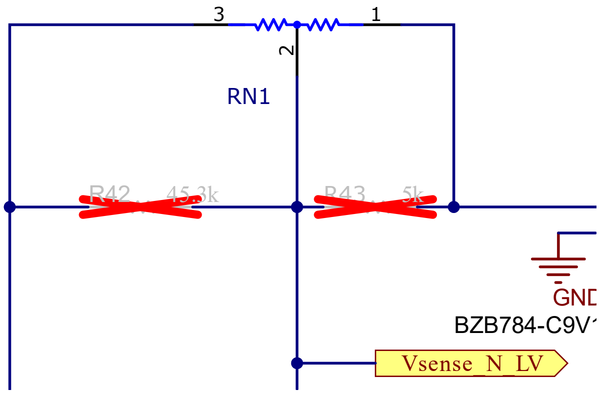


Figure 2-16. Precision Voltage Divider

2.2.9.4 Clamp Resistor

When clamping activates, the clamp circuit takes over loop control and the force op-amp output reaches +12V or –12V power rail. This resistor also influences compensation and bandwidth, so the select two-paralleled 0805, 2kΩ, resistors to handle the current (see Figure 2-17). The total power reaches 0.144W.

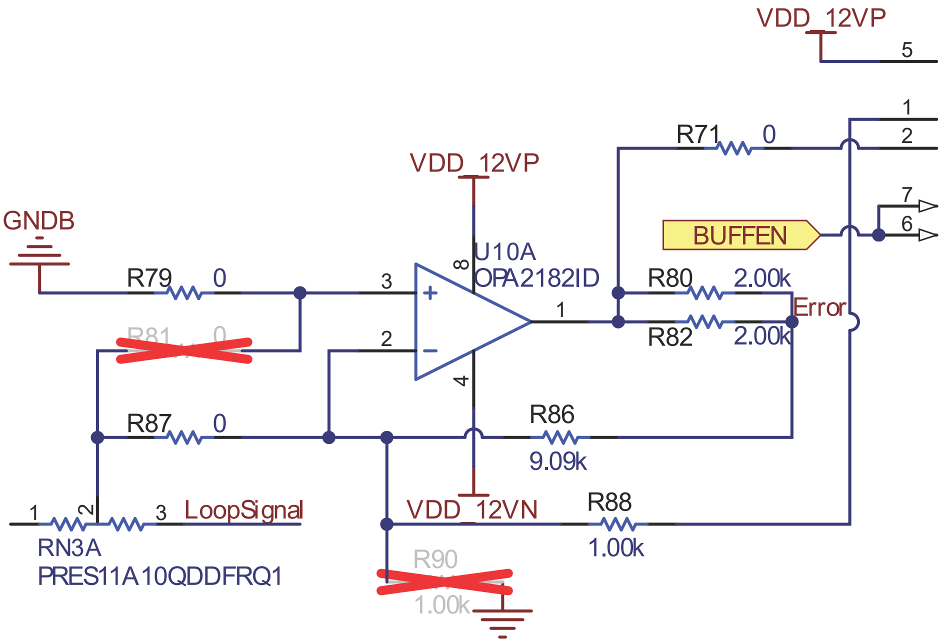


Figure 2-17. Parallel Resistors for Clamp

2.3 Highlighted Products

2.3.1 REF54

The REF54 operates as a high-precision, low-drift, low current consumption series voltage reference device. This device offers low temperature drift coefficient (0.8ppm/°C), low noise (0.11ppmp-p), and high accuracy (±0.02%) while consuming 260μA current. The REF54 with low long-term drift (25ppm) and excellent load and line regulation helps meet strict performance requirements of high-precision applications. The C grade temperature range covers 0°C to 70°C and the Q grade covers –40°C to +125°C.

In this design, REF54410 generates 4.096V for all socket reference input, benefiting long-term drift calibration.

Important features include:

- Low temperature drift coefficient: 0.8ppm/°C maximum (C grade), 1.5ppm/°C maximum (Q grade)

- Low noise (0.1Hz to 10Hz): 0.11ppmp-p with CNR = 100µF, 0.45ppmp-p with CNR = Open
- High accuracy: ±0.02% maximum
- Low quiescent current: 380µA maximum
- Low long-term stability (1khr): 25ppm
- Voltage options: 2.5V, 3V, 4.096V, 4.5V, 5V

2.3.2 DAC11001B

The 20-bit DAC11001B operates as a highly accurate, low-noise, voltage-output, single-channel, digital-to-analog converter (DAC) with excellent linearity across all output ranges. The unbuffered voltage output offers low noise performance (7nV/√Hz) in combination with a fast settling time (1µs). The device integrates an enhanced deglitch circuit with code-independent ultra-low glitch (1nV-s) to enable clean waveform ramps with ultra-low total harmonic distortion (THD).With external references, DAC output ranges from V_{REFPF} to V_{REFNF} can be achieved, including asymmetric output ranges.

Important features include:

- 20-bit monotonic: 1-LSB DNL (maximum)
- Integral linearity: 1-LSB INL (maximum)
- Low noise: 7nV/√Hz
- Code independent low glitch: 1nV-s
- Excellent THD: –118dB at 20kHz f_{OUT}, 1MHz f_{DAC}
- Fast settling: 1µs
- Flexible output ranges: V_{REFPF} to V_{REFNF}, up to ±15V

2.3.3 DAC80502

The DAC80502 is a dual-channel 16-bit DAC offering linearity of < 1 LSB and high accuracy combined with a tiny package(2.5mm × 2.5mm). The device incorporates a power-on-reset circuit that makes sure the DAC output powers up at zero scale or midscale based on the status of the RSTSEL pin, and remains at that scale until a valid code is written to the device. The digital interface of the DACx0502 can be configured to SPI or I2C mode using the SPI2C pin.

Important features include:

- 16-bit performance: 1-LSB INL and DNL (maximum)
- Low glitch energy: 4nV-s
- Wide power supply: 2.7V to 5.5V
- Buffered output range: 5V, 2.5V, or 1.25V
- Low power: 1mA per channel at 5.5V
- Integrated 5ppm/˚C (maximum), 2.5V precision reference
- SPI or I2C compatible

2.3.4 ADS9317

The ADS931x operates as a high-speed, dual, simultaneous-sampling ADC with an integrated reference and reference buffer. The ADS931x delivers excellent AC performance. The device includes an integrated 128 average function. The device supports a serial peripheral interface (SPI) compatible protocol. This interface makes the ADS931x easy to pair with a diversity of microcontrollers. The device supports two serial outputs for each ADC channel or one serial output for each ADC channel and so forth.

Important features include:

- 18-bit, 5MSPS/channel
- Two fully differential, simultaneously sampled channels
- Supports 5V and 3.3V analog supply operation
- SNR: 95dB at 5MSPS
- INL: ±2 LSB, DNL: ±0.75 LSB
- Internal reference
- Integrated buffer for external reference input
- Simple data average up to 128 samples

2.3.5 OPA593

The OPA593 is a high-voltage (85V), high-precision, wide-bandwidth (10MHz), high-output-current (250mA), unity-gain-stable, power operational amplifier (op amp). The OPA593 uses a laser trimming technique to improve the offset voltage (20µV, typical) and offset voltage drift (0.4µV/°C, typical) and thus avoids the need for calibration. An external resistor can be used to limit the current with specified accuracy.

Important features include:

- Wide power-supply range: 8V (±4V) to 85V (±42.5V)
- Low offset voltage: ±20µV
- Low offset voltage drift: ±0.4µV/°C
- High output current: 250mA
- Wide gain bandwidth: 10MHz
- High slew rate: 45V/µs, rising
- Low noise: 7nV/√Hz at 10kHz
- Rail-to-rail output
- Quiescent current: Enabled: 3.25mA, Disabled: 250µA
- Specified current limit accuracy

2.3.6 OPA596

The OPA596 and OPA2596 (OPAx596) devices are high-voltage (85V), high slew rate (100V/µs), micro-power (420µA), unity-gain stable op amps. With small bias current and rail-to-rail output and low noise, this device provides an excellent buffer for high-voltage applications.

Important features include:

- High slew rate: 100V/µs
- Low power consumption: 420µA
- Wide power-supply range: ±4V to ±42.5V, 8V to 85V
- Multiplexer-friendly inputs
- Input below the negative rail
- Rail-to-rail output
- Gain bandwidth: 3.75MHz
- Low noise: 12.8nV/√Hz
- Low input bias current: 5pA
- Low input offset voltage: ±1mV
- Output current drive: ±30mA

2.3.7 PGA849

The PGA849 is a wide-bandwidth, low-noise programmable gain instrumentation amplifier for differential-to-single-ended conversion. The PGA849 is equipped with eight binary gain settings, from an attenuating gain of 0.125V/V to a maximum of 16V/V, using three digital gain selection pins. The super-beta input transistors offer an impressively low input bias current, which in turn provides a very low input current noise density of 0.3pA/√Hz. Integrated protection circuitry on the input pins handles overvoltages of up to ±40V beyond the power-supply voltages.

Important features include:

- Differential to single-ended conversion
- Eight pin-programmable binary gains: G (V/V) = ⅛, ¼, ½, 1, 2, 4, 8, and 16
- Low gain error drift: ±2ppm/°C (maximum)
- Wide bandwidth: 10MHz at all gains
- High slew rate: 35V/µs at G ≥ ½ V/V
- Settling time : 700ns to 0.01%, 950ns to 0.0015%
- Input stage noise: 8.6nV/√Hz at G = 16V/V
- Filter option to achieve better SNR
- Independent input and output power-supply pins
- Input overvoltage protection to ±40V beyond supplies
- Input-stage supply range: 8V to 36V or ±4V to ±18V

- Independent output power-supply pins: 4.5V to 36V or ±2.25V to ±18V

2.3.8 OPA454

The OPA454 device is a low-cost op amp with high voltage (100V) and relatively high current drive (50mA). This device is unity-gain stable and has a gain-bandwidth product of 2.5MHz. OPA454 is internally protected against overtemperature conditions and current overloads. The device is fully specified to perform over a wide power-supply range of ±5V to ±50V or on a single supply of 10V to 100V.

Important features include:

- Wide power-supply range: ±5V (10V) to ±50V (100V)
- High-output load drive: I/O > ±50mA
- Wide output voltage swing: 1V to rails
- Bias current: 1.4pA(typical)
- Common-mode voltage: (V–) +2.5V to approximately (V+) –2.5V

2.3.9 OPA4187

The OPA4187 op amp uses auto-zeroing techniques to simultaneously provide low-offset voltage (1µV), and near zero drift over time and temperature. These miniature, high-precision,low-quiescent current amplifiers offer high-input impedance and rail-to-rail output swing within 5mV of the rails into high-impedance loads. The input common-mode range includes the negative rail. Either single or dual supplies can be used in the range of 4.5V to 36V (±2.25V to ±18V).

Important features include:

- Low offset voltage: 10µV (maximum)
- Zero drift: 0.001µV/°C
- Low noise: 15nV/$\sqrt{\text{Hz}}$
- PSRR: 160dB
- Common Mode Rejection Ratio (CMRR): 140dB
- Amplifier Open Loop (AOL) gain: 160dB
- Quiescent Current: 100µA
- Wide supply voltage: ±2.25V to ±18V
- Rail-to-rail output operation
- Input includes negative rail
- Low bias current: 100pA (typical)

2.3.10 THS4552

The THS4552 fully differential amplifier offers an easy interface from single-ended sources to the differential output required by high-precision analog-to-digital converters (ADCs). Designed for exceptional DC accuracy, low noise, and robust capacitive load driving, this device is an excellent choice for data acquisition systems where high precision is required along with the best signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR) through the amplifier and ADC combination. The THS4552 features the negative rail input required when interfacing a DC-coupled, ground-centered, source signal to a single-supply differential input ADC. Very low DC error and drift terms support the emerging 16- to 20-bit successive-approximation register (SAR) input requirements.

Important features include:

- Bandwidth: 150MHz (G = 1V/V)
- Differential output slew rate: 220V/µs
- Gain bandwidth product: 135MHz
- Negative rail input (NRI), rail-to-rail output (RRO)
- Wide output common-mode control range
- Single-supply operating range: 2.7V to 5.4V
- 25°C input offset: ±175µV (maximum)
- Input offset voltage drift: ±2.0µV/°C (maximum)
- Differential input voltage noise: $3.3\text{nV}/\sqrt{\text{Hz}}$
- HD2: –128dBc at 2 VPP, 100kHz
- HD3: –139dBc at 2 VPP, 100kHz
- < 50ns settling time: 4V step to 0.01%
- 18-bit settling time: 4V step, < 500ns

2.3.11 RES11A

The RES11A is a matched pair of resistive dividers, implemented in thin-film SiCr with Texas Instruments' modern, high-performance, analog CMOS process. The device has a nominal input resistance of 1kΩ, for low thermal and current noise, and is available in several nominal ratios to meet a wide array of system needs. The RES11A series features high ratio-matching precision, with the measured ratio of each divider within ±0.05% (±500ppm) of the nominal. This precision is maintained over the temperature range, with a maximum ratio drift of only ±2ppm/°C. Additionally, the biased long-term stability of the device has been proven through thorough characterization.

Important features include:

- Wide temperature range: –40°C to +125°C
- Highly precise ratio tolerance: ±0.05% (maximum)
- Low drift: ±2ppm/°C TCR ratio (maximum)
- Small Outline Transistor (SOT-23)

3 System Design Theory

This reference design supports following working modes:

- Force Voltage and Clamp Current
- Force Current and Clamp Voltage
- Voltage buffer output, open loop and no Clamp feature
- Gang Master, act master in gang multiple boards, gang signal is star connection. Working in FV mode, has clamp current feature.
- Gang Slaver, act slaver in gang multiple boards. Working in FI mode, has Clamp voltage feature, and force signal is from the Master board through the gang connection.

3.1 Force Voltage Mode

For voltage path, low bias current OPA454 buffer acts on DUT voltage, a precision 1:9 resistor divider on DUT achieves 1/10 DUT voltage, then the low drift and high bandwidth PGA849 converts differential signal to single-end signal. DUT voltage signal compares with force voltage through precision RES11A network resistor and drives output stage.

For current path, same as voltage, an OPA454 blocks current leakage and a paired differential current signal connects to PGA849. Then DUT current signal compares with clamp voltage through precision RES11A resistor to trigger clamp loop if this occurs.

Place multiple 1st order compensation options in force path, this eliminates output error when output operates as step signal. Figure 3-1 and Figure 3-2 show TINA simulation and result.

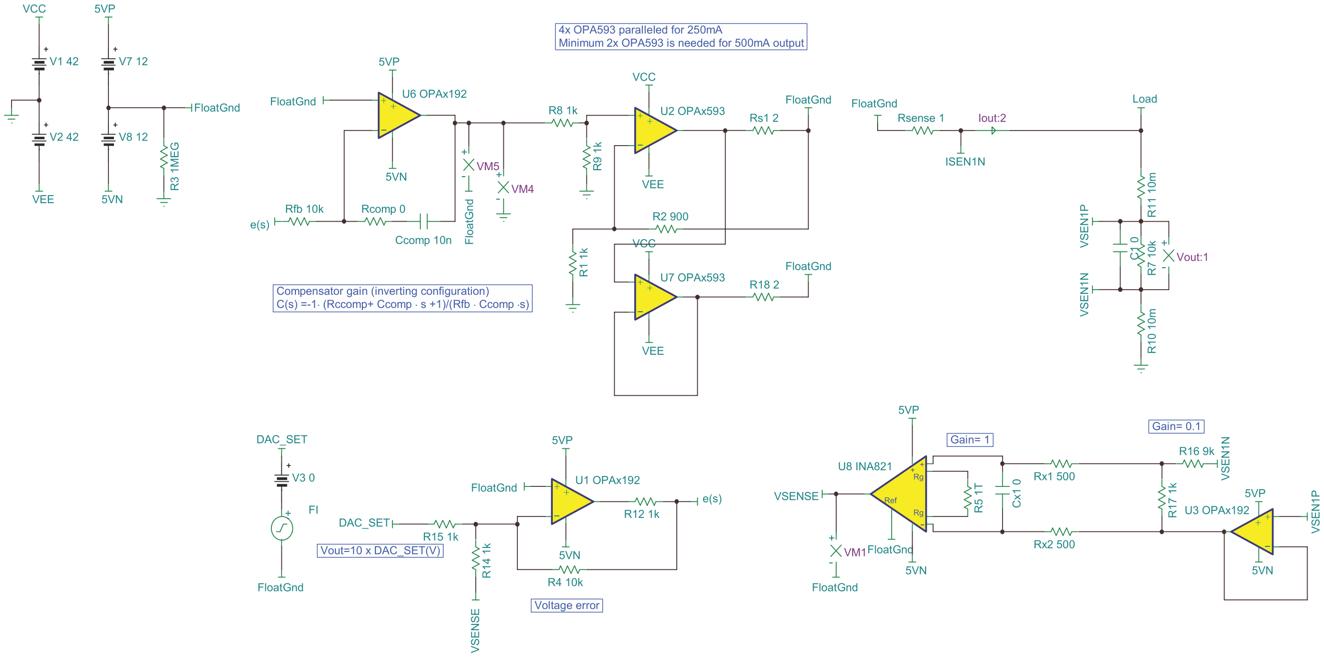


Figure 3-1. FV Mode TINA Simulation

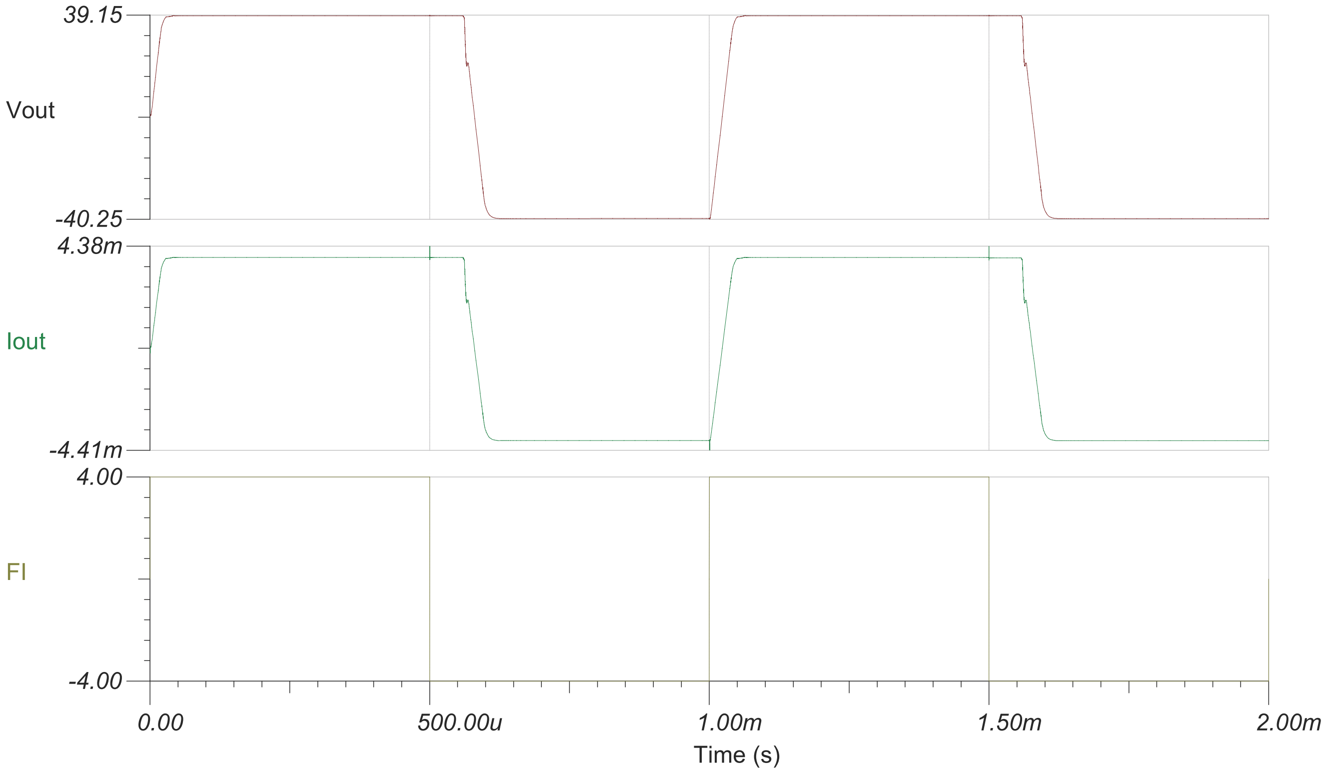


Figure 3-2. FV Mode TINA Simulation Result

From simulation, ±40V can be achieved when force setting reaches ±4V. Rising time approaches 50µs which matches real circuit testing.

In Figure 3-3 the red arrow shows force voltage workflow, and the blue arrow shows clamp workflow. If clamp condition triggers, clamp loop takes over control loop to force current to clamp DAC setting.

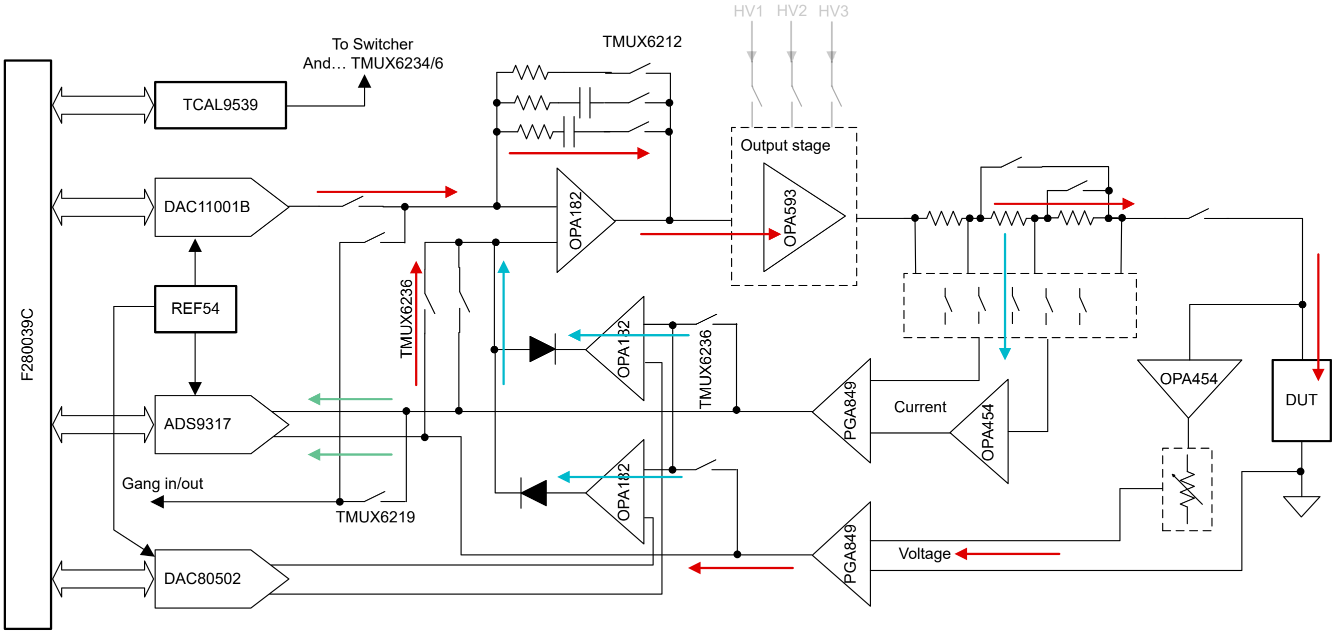


Figure 3-3. Workflow of Force Voltage and Clamp Current

3.2 Force Current Mode

In force current mode, DAC11001B forces a voltage to the loop, and the current signal connects in the control loop, and the current sensing resistor voltage compares with the force voltage to determine output current.

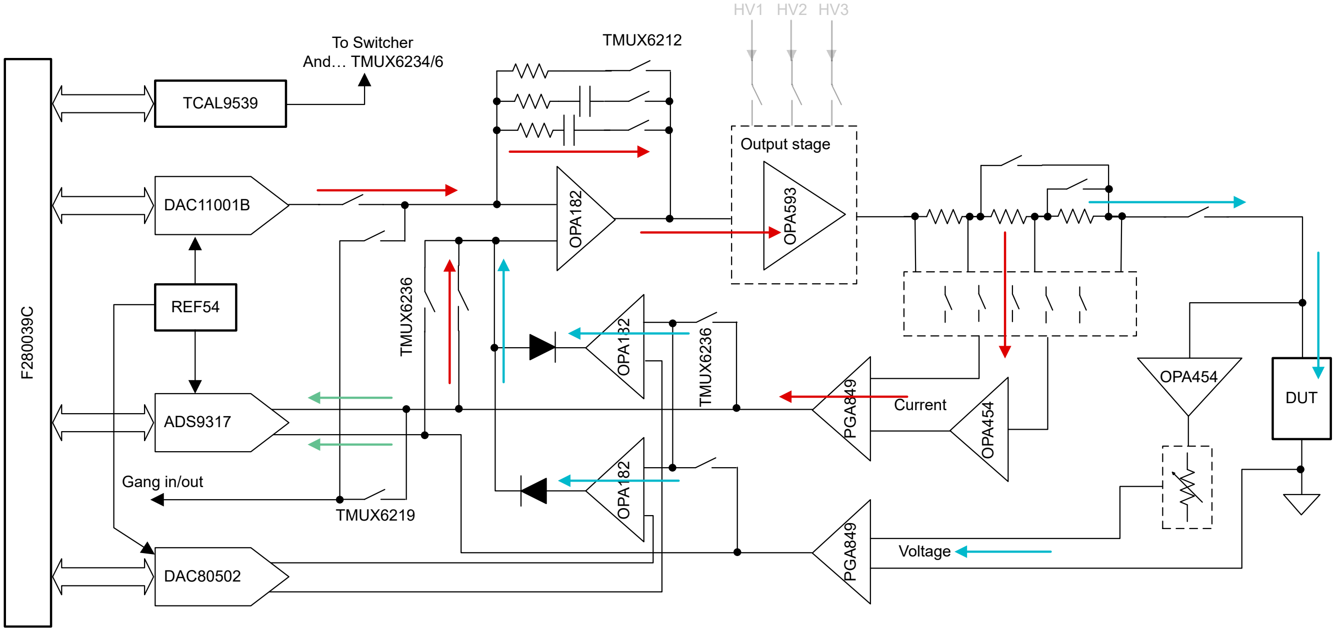
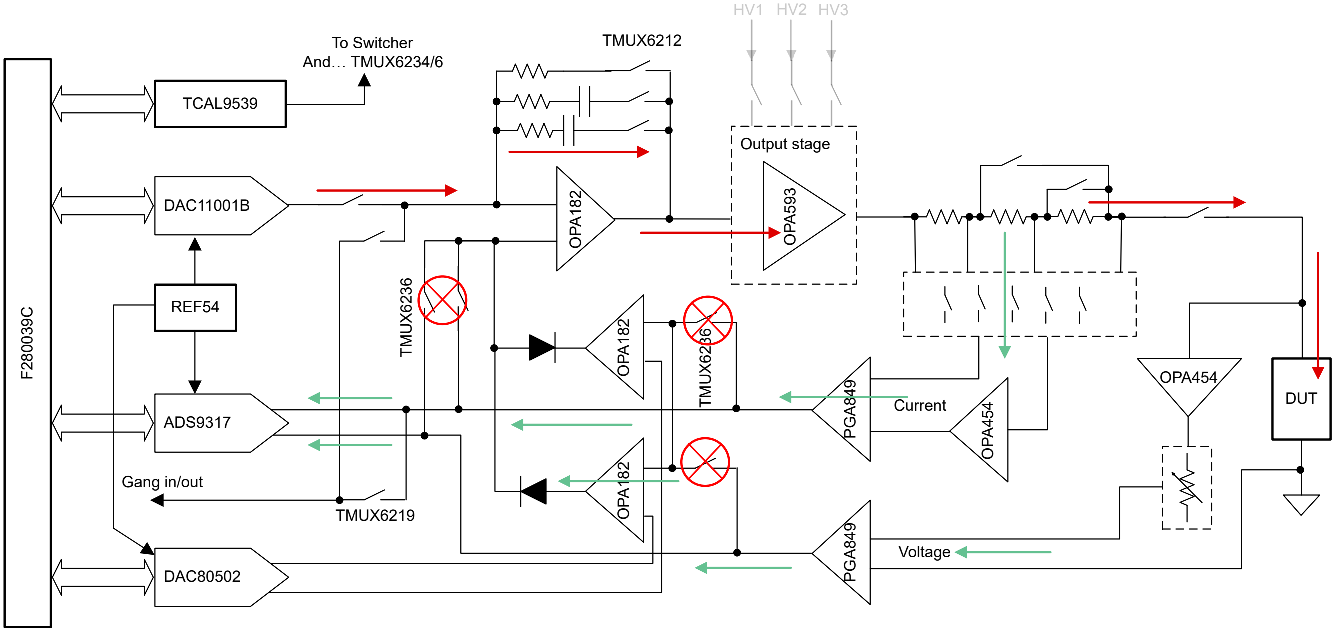


Figure 3-4. Force Current and Clamp Voltage Workflow

In Figure 3-4, the red arrow shows force current workflow and the blue arrow shows the clamp voltage workflow.

3.3 Buffer Mode

In buffer mode, close loop breaks in feedback circuits regardless of DUT voltage or current, see Figure 3-5. The output path gain sets to about 20×. Buffer mode provides a very high bandwidth output path and independent sensing path. This benefits sending waveform or digital control loop implementation.

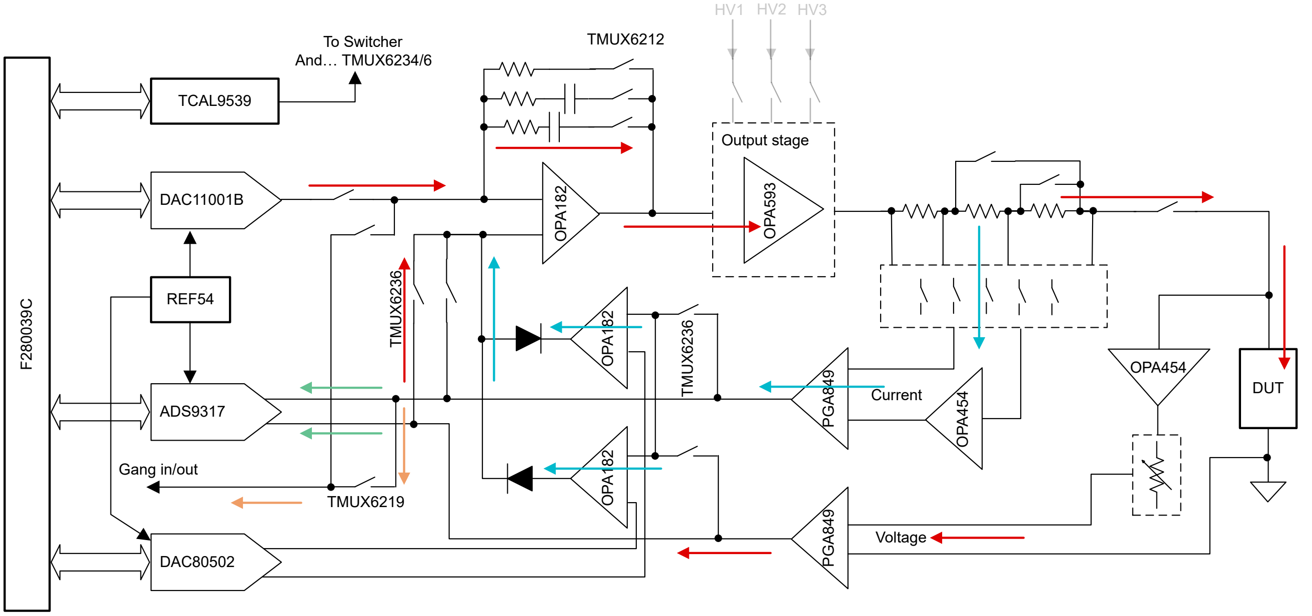


Red arrows show the force path. Green arrows show the sensing path.

Figure 3-5. Buffer Mode Workflow

3.4 Gang_Master Mode

Gang master mode operates very similarly to force voltage mode except current sensing signal sends to outside for slave use.

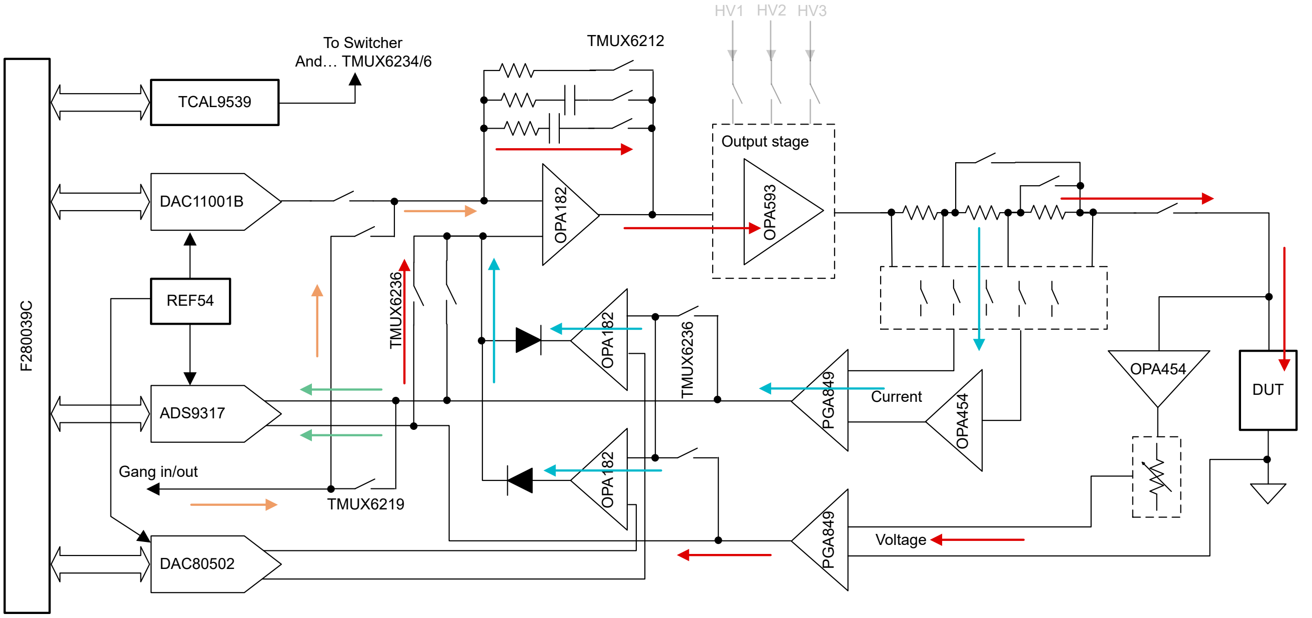


The yellow path is the gang signal output.

Figure 3-6. Gang Master Mode Workflow

3.5 Gang_Slaver Mode

Gang slaver mode operates similarly to force current mode except the force signal comes from the gang master board. The force DAC of the slaver board does not work in this mode, but the voltage clamp circuit continues to work.



The yellow path is the gang signal from the master board.

Figure 3-7. Gang Slaver Mode Workflow

Figure 3-8 illustrates the gang simulation where three independent channels operate. The force voltage is set to 3.5V which means a force of 35V on the DUT. Figure 3-9 shows that the output current of every channel reaches 389mA.

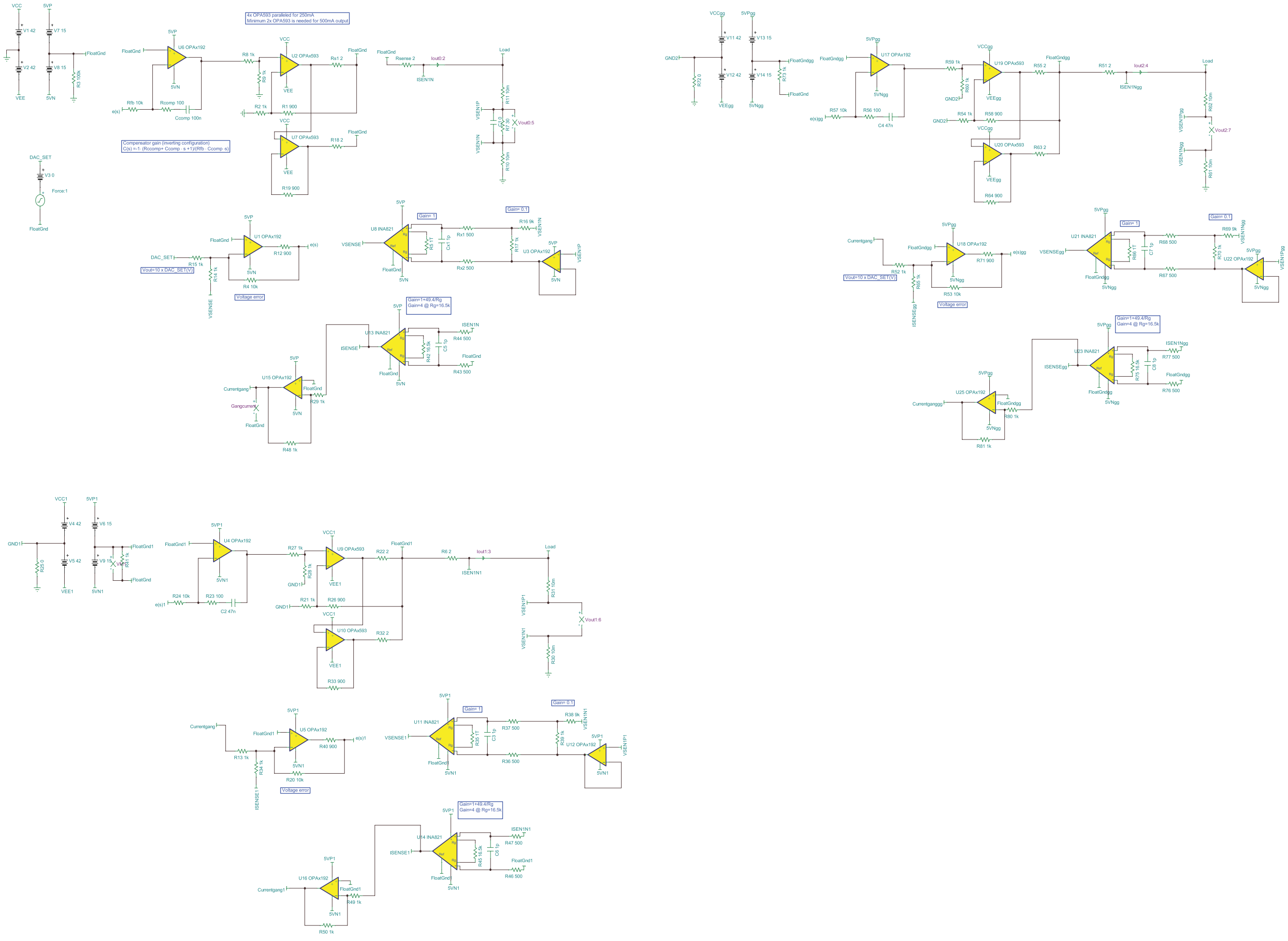


Figure 3-8. Gang Mode TINA Simulation Schematic

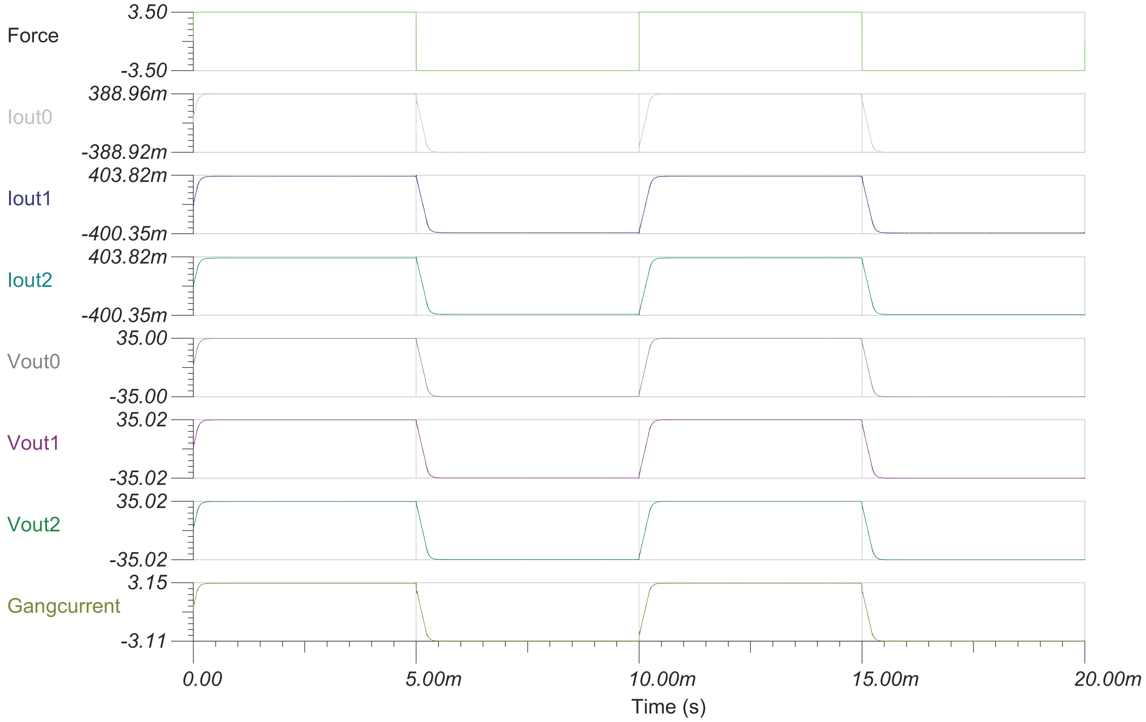


Figure 3-9. Gang Mode TINA Simulation Output

4 Hardware, Software, Testing Requirements, and Test Results

4.1 Hardware Requirements

4.1.1 Support Working Mode

TIDA-010962 is a floating VI reference design, with two voltage ranges and three current range options. Table 4-1 shows the supported modes.

Table 4-1. TIDA-010962 Supported Modes

VOLTAGE RANGE	CURRENT RANGE	CV	CC	BUFFER	GANG_MASTER	GANG_SLAVE
±40V	±500mA	Yes	Yes	Yes	Yes	Yes
	±10mA	Yes	Yes	Yes	No	No
	±10µA	Yes	Yes	Yes	No	No
0V–80V	±500mA	Yes	Yes	No	No	No
	±10mA	Yes	Yes	No	No	No
	±10µA	Yes	Yes	No	No	No

4.1.2 Power Supply

TIDA-010962 needs two groups of isolated power, one external low voltage +15V, the other high voltage positive and negative power. These are +43V, –42V connected for ±40V range working or +83V, –2V connected for 0V to 80V range working.

Table 4-2. TIDA-010962 Power Supply

POWER SUPPLY	VOLTAGE (V)	MINIMUM CURRENT (MA)	NOTE
HV Power(±40V)	+43	800	Option 1: connect to HV connector
	–42	800	
HV Power(0V–80V)	+83	800	Option 2: connect to HV connector
	–2	800	
LV Power	+15	500	Connect to LV connector
Internal Power Rail	–15	500	Internal voltage, connection not required, just for reference
	5	200	
	3.3	100	
	1.8	100	

Figure 4-1 shows the TIDA-010962 VI chart, illustrating the voltage difference between high voltage power supply and output voltage and current.

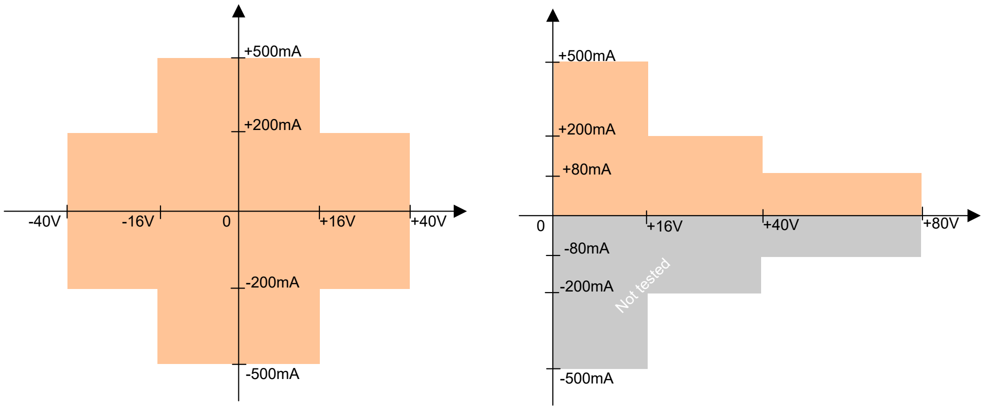


Figure 4-1. TIDA-010962 Board VI Chart

4.1.3 Hardware Connection

WARNING

TI intends this reference design to be operated in a lab environment only and does not consider the reference design to be a finished product for general consumer use.

TI Intends this reference design to be used only by qualified engineers and technicians familiar with risks associated with handling high-voltage electrical and mechanical components, systems, and subsystems.

High voltage! There are accessible high voltages present on the board. The board operates at voltages and currents that can cause shock, fire, or injury if not properly handled or applied. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property.

Hot surface! Contact can cause burns. **Do not touch!** Some components can reach high temperatures > 55°C when the board is powered on. The user must not touch the board at any point during operation or immediately after operating, as high temperatures can be present.

CAUTION

No protection circuit such as Transient Voltage Suppressor (TVS) or reverse protection exists for the interface or internal circuits. Any electrostatic discharge can damage the board. Incorrect or reverse power supplies connected to board can also damage the board.

TIDA-010962 reference design board does not support hot plugging at any time. When connecting or disconnecting the C2000 control card to or from the base board, follow this sequence: first power off both LV and HV supplies, then disconnect the USB cable from the PC.

Set the board to *Out Off* status before changing the DUT value or type during evaluation testing.

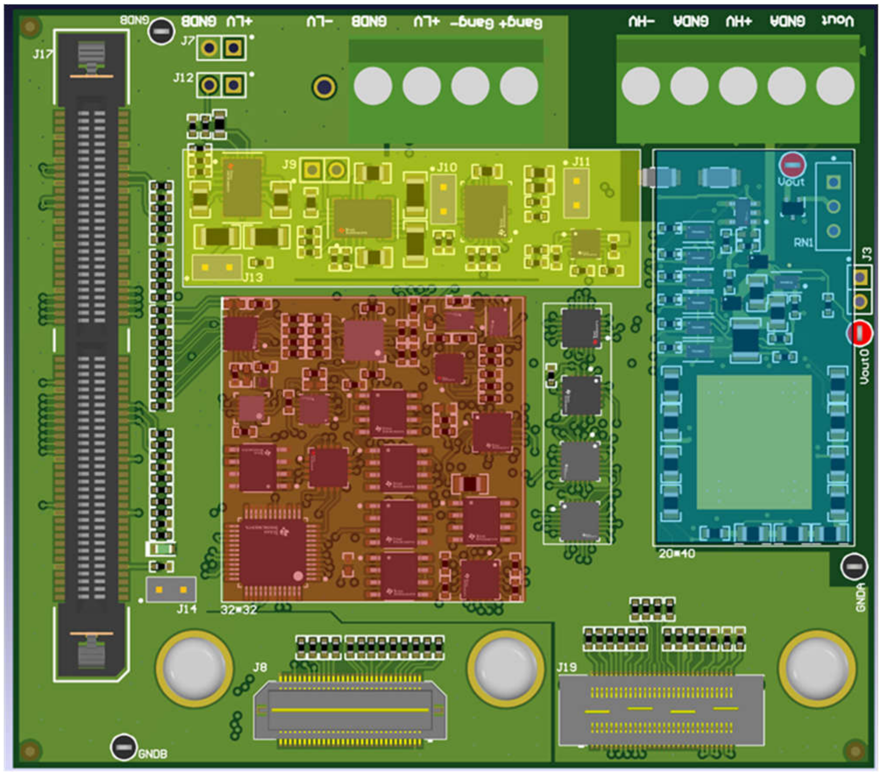


Figure 4-2. TIDA-010962 PCB Board Function Area

Figure 4-2 shows the top view of the reference design hardware. Jumpers J10, J11, and J13 are ±12V and +5V power connection jumpers that are installed after manufacturing. Do not remove these jumpers. There is a heat sink pasted on the output stage before delivery. Upon receipt of the board, verify that the heat sink is still properly attached.

The yellow area is the LV power rail that provides ±12V, +5V, and 3.3V for the signal chain. The blue area is the HV power area, which includes the power output stage and voltage and current sensing circuits. The red area is the LV signal chain, which includes ADC, DAC, closed-loop, and clamp circuits.

The J17 connector is the C2000 control card socket. The *LV+* and *GNDB* pins of this connector are for the LV +15V power supply. The *+HV*, *GNDA*, and *–HV* pins are for the HV +43V, –42V or +83V, –2V power supply. The *Vout* pin and the adjacent *GNDA* pin are for connecting the DUT. J7 is the socket for plugging in the fan.

Figure 4-3 shows the finished cable connection.

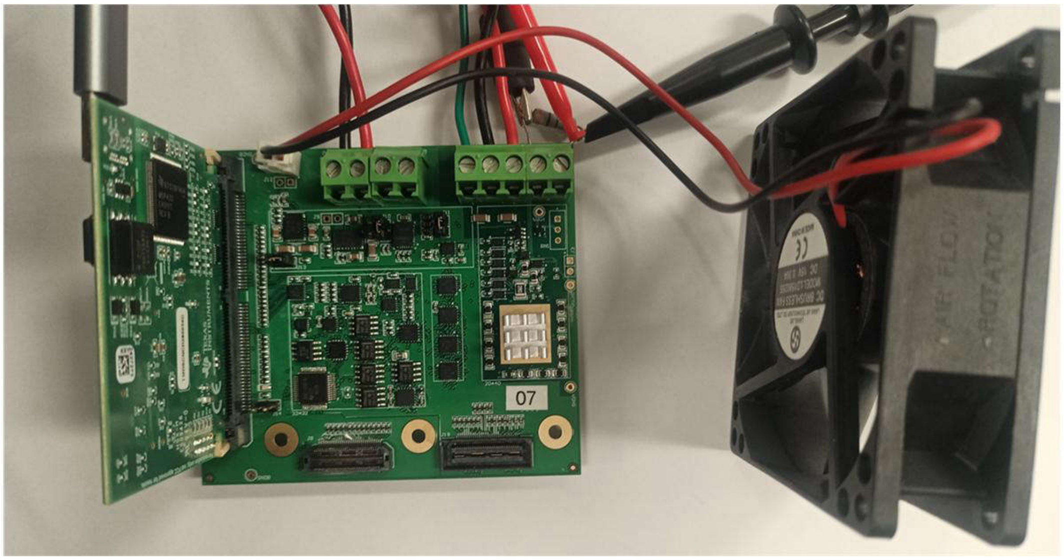


Figure 4-3. Test Setup

Cable and power connection sequence:

1. Verify the heat sink is properly attached in the correct position
2. Insert the *TMDSCNCD280039C* control card into the J17 slot and connect the USB Type-C® port of the USB cable to the control card. Do not connect the Type-A port of the USB cable to the PC at this step.
3. Connect a fan to J7 to provide board heat dissipation
4. Connect the LV power supply: +15V to LV+ and LV GND to GNDB. Do not power up at this step.
5. Connect the HV power supply: +43V to HV+, HV GND to GNDA, and –42V to HV– (+83V, –2V connection follows the same pattern). Do not power up at this step.
6. Connect the DUT: Vout is the output and GNDA is ground (resistor or capacitor)
7. If evaluating the Gang function, connect two-wire cables to Gang+ and Gang– of each board. Each board must have isolated LV and HV power supplies.
8. Connect an oscilloscope or 6½-digit digital multimeter to the DUT for measurement

Note

For easier evaluation, the control loop feedback connection point is located before the output switch. To accurately measure the output voltage, there are two options: measure the *Vout* test point before the output switch, or implement remote feedback from the DUT by connecting the remote sensing connector (J3) to the DUT (not supported in the current BOM).

9. Power up the board
    a. Power on LV (+15V)
    b. Power on the HV supply (+43V, –42V or +83V, –2V). If the HV power supplies are separate, power on the positive HV supply first, then the negative HV supply.
10. Connect the Type-A port of the USB cable to the PC after the LED blinks on the board
11. Open *FVI80GUI.exe* on the PC to start testing
12. After completing evaluation, power off the HV supply first, then power off the LV supply, and finally disconnect the USB cable from the PC.

Note

If the GUI tool is opened before connecting the USB cable, the GUI does not detect the communication port.

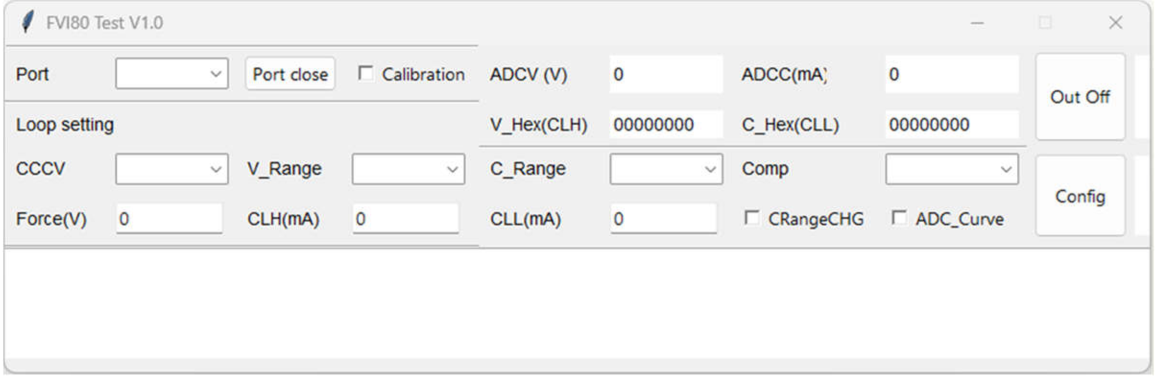
CAUTION

Before removing the C2000 control card from the base board, turn off the power and disconnect the USB cable first, or the board sustains damage.

4.2 Software Requirements

4.2.1 PC GUI

Figure 4-4 shows the Graphical User Interface (GUI) dialog box that appears after running *FVI80GUI.exe* in Microsoft® Windows®.



ADCV (V) 0
ADCC(mA) 0
V_Hex(CLH) 00000000
C_Hex(CLL) 00000000
Force(V) 0
CLH(mA) 0
CLL(mA) 0

Figure 4-4. GUI Display

4.2.1.1 Control Window

The *Port list box* allows selection of the serial port that communicates with the C2000 control card. Before selection, check which serial port number represents the correct port. The *Device Manager* in Microsoft Windows shows this information in Figure 4-5, where the red highlight indicates the communication port with the board.

Note

The GUI detects PC serial ports only at start-up. If the software cannot find the correct serial port, close the GUI and run the application again.

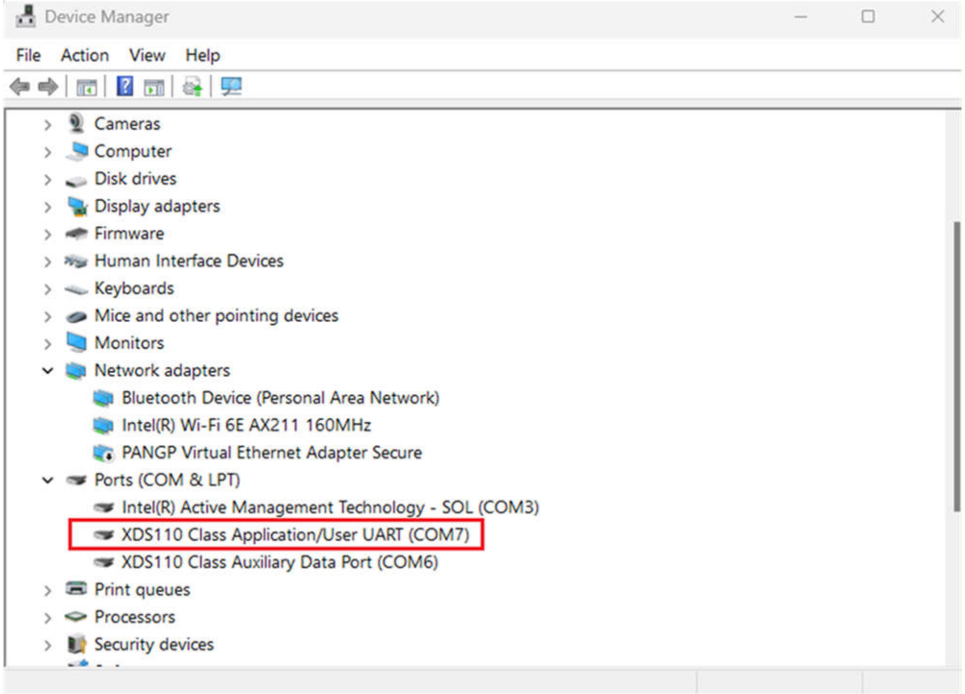


Figure 4-5. PC Device Manager Dialog

Clicking the *Port close* button opens the selected serial port. The loop configuration can then be set in the *CCCV*, *V_Range*, *C_Range* and *Comp* list boxes. Input the force voltage in *ForceV* with values between –40V to approximately 40V when ±40V range is selected or between 0V to about 80 when 0V to 80V range is selected. When 500mA current range is selected, set the high clamp value in *CLH* from 500mA to about 0mA and set the low clamp value *CLL* from –500mA to about 0mA. When 10mA or 10μA current range is selected, set the high clamp value in *CLH* from 10mA to about 0mA and set the low clamp value *CLL* from –10mA to about 0mA. After completing configuration, click the *Config* button or *Out Off* to download the configuration to the board.

ADCV(V) and ADCC(mA) and V_HEX(CLH) and C_HEX(CLL) display ADC read voltage and current values and raw Hex data. V_HEX(CLH) and C_HEX(CLL) have another function that indicates Clamp status. When the background color becomes red, the corresponding clamp is occurring.

4.2.1.2 ADC Read Raw Data Window

If *ADC_Curve* is checked, a plot interface pops out that shows ADC raw data, see Figure 4-6. Two plots show ADC read voltage and the current raw data. Each plot title contains a central value that shows the sampling central data. The y-axis shows error LSB data from the *central* Hex value. The x-axis represents sampled data that shows 50 total samples with a time step of 0.5s

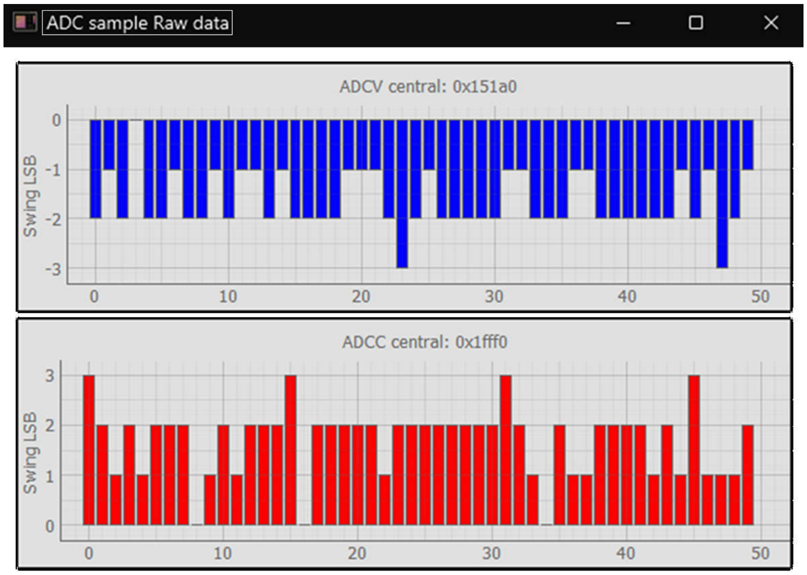
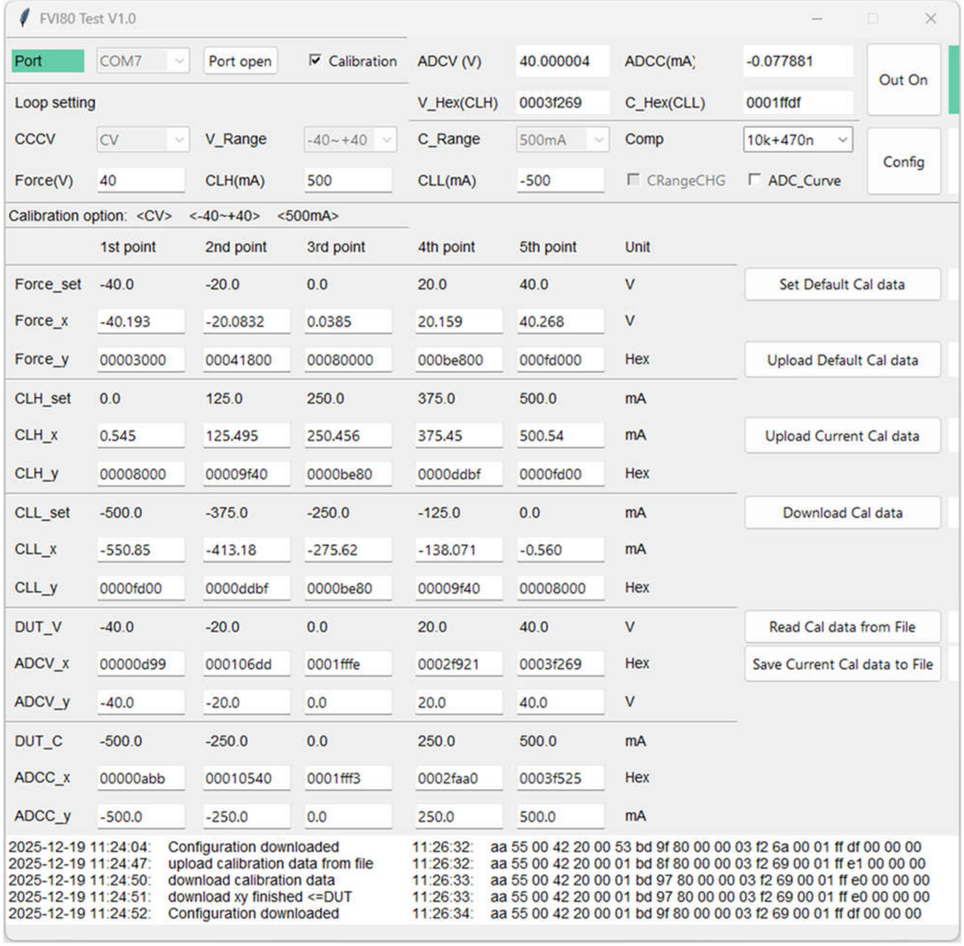


Figure 4-6. ADC Swing LSB Window

4.2.1.3 Calibration Window

If *Calibration* is checked, a calibration area as shown in Figure 4-7 appears.



Port: COM7

☑ Calibration

ADCV (V): 40.000004

ADCC(mA): -0.077881

Loop setting

V_Hex(CLH): 0003f269

C_Hex(CLL): 0001ffdf

CCCV: CV

V_Range: -40~+40

C_Range: 500mA

Comp: 10k+470n

Force(V): 40

CLH(mA): 500

CLL(mA): -500

☐ CRangeCHG

☐ ADC_Curve

Calibration option: <CV> <-40~+40> <500mA>

	1st point	2nd point	3rd point	4th point	5th point	Unit
Force_set	-40.0	-20.0	0.0	20.0	40.0	V
Force_x	-40.193	-20.0832	0.0385	20.159	40.268	V
Force_y	00003000	00041800	00080000	000be800	000fd000	Hex
CLH_set	0.0	125.0	250.0	375.0	500.0	mA
CLH_x	0.545	125.495	250.456	375.45	500.54	mA
CLH_y	00008000	00009f40	0000be80	0000ddbf	0000fd00	Hex
CLL_set	-500.0	-375.0	-250.0	-125.0	0.0	mA
CLL_x	-550.85	-413.18	-275.62	-138.071	-0.560	mA
CLL_y	0000fd00	0000ddbf	0000be80	00009f40	00008000	Hex
DUT_V	-40.0	-20.0	0.0	20.0	40.0	V
ADCV_x	00000d99	000106dd	0001fffe	0002f921	0003f269	Hex
ADCV_y	-40.0	-20.0	0.0	20.0	40.0	V
DUT_C	-500.0	-250.0	0.0	250.0	500.0	mA
ADCC_x	00000abb	00010540	0001fff3	0002faa0	0003f525	Hex
ADCC_y	-500.0	-250.0	0.0	250.0	500.0	mA

```
2025-12-19 11:24:04:  Configuration downloaded          11:26:32:  aa 55 00 42 20 00 53 bd 9f 80 00 00 03 f2 6a 00 01 ff df 00 00 00
2025-12-19 11:24:47:  upload calibration data from file 11:26:32:  aa 55 00 42 20 00 01 bd 8f 80 00 00 03 f2 69 00 01 ff e1 00 00 00
2025-12-19 11:24:50:  download calibration data         11:26:33:  aa 55 00 42 20 00 01 bd 97 80 00 00 03 f2 69 00 01 ff e0 00 00 00
2025-12-19 11:24:51:  download xy finished <=DUT        11:26:33:  aa 55 00 42 20 00 01 bd 97 80 00 00 03 f2 69 00 01 ff e0 00 00 00
2025-12-19 11:24:52:  Configuration downloaded          11:26:34:  aa 55 00 42 20 00 01 bd 9f 80 00 00 03 f2 69 00 01 ff df 00 00 00
```

Figure 4-7. Calibration Window

There are 12 calibration options based on CCCV, Vrange, and Crange selection. Each option has calibration data.

Note

The buffer reuses CV, 40V, and 500mA data. Gang_M reuses CV data, Gang_S reuses CC data. This means changing calibration data in Buffer mode overrides the corresponding CV, 40V, and 500mA calibration data.

Each calibration option has five setting or reading items that require calibration: force, high clamp, low clamp, and reading of ADC voltage and current. However, not all items require calibration at once during evaluation. For each setting or reading item, five calibrated points change when performing calibration, and all five calibration points require completion at once.

For each calibration item, three lines exist. *_set* shows the set value in *Force(V)* or *CLH* or *CLL*. For ADC, this means setting the corresponding output value first in the configuration area. _x represents the input calibrated x value, which is the main change area in all calibration cases. *Force(V)* or *CLH* or *CLL* are read from the DMM. *ADCV_x* and *ADCC_x* are read from the contents of *V_Hex(CLH)* and *C_Hex(CLL)*. *_y* represents the input calibrated y value, which is automatically generated and rarely changed in most calibration cases except buffer mode or small current clamp cases that have significant mismatch between input and output.

Equation 1 shows the calculation of ±40V and 500mA. For other calculation options, contact TI field team or TI e2e.

$$\text{Force\_y} = \frac{4.096 - \frac{\text{Force}}{10}}{4.096} \times 2^{19};\ \ \text{CLH\_y} = \frac{4.096 + \frac{\text{CLH} \times 8}{1000}}{4.096} \times 2^{15};\ \ \text{CLL\_y} = \frac{4.096 - \frac{\text{CLL} \times 8}{1000}}{4.096} \times 2^{15} \tag{1}$$

After finishing calibration for at least five points, clicking the *Download Cal data* button downloads the selected calibration option to the board.

Whenever starting a new calibration for a calibrated option, set the board to default calibration status by clicking the *Set Default Cal data* button.

Calibration data can be saved and read in Microsoft Windows by clicking the *Read …* or *Save…* buttons.

4.3 Test Setup

4.3.1 Source Mode Connection

Figure 4-8 shows the setup for testing source mode features. The DUT can be a resistor or capacitor or both. Pay attention to capacitor polarity and resistor power rating. For the power supply, the voltage difference must align with Figure 4-1, otherwise the output experiences oscillation from OPA593 heat protection.

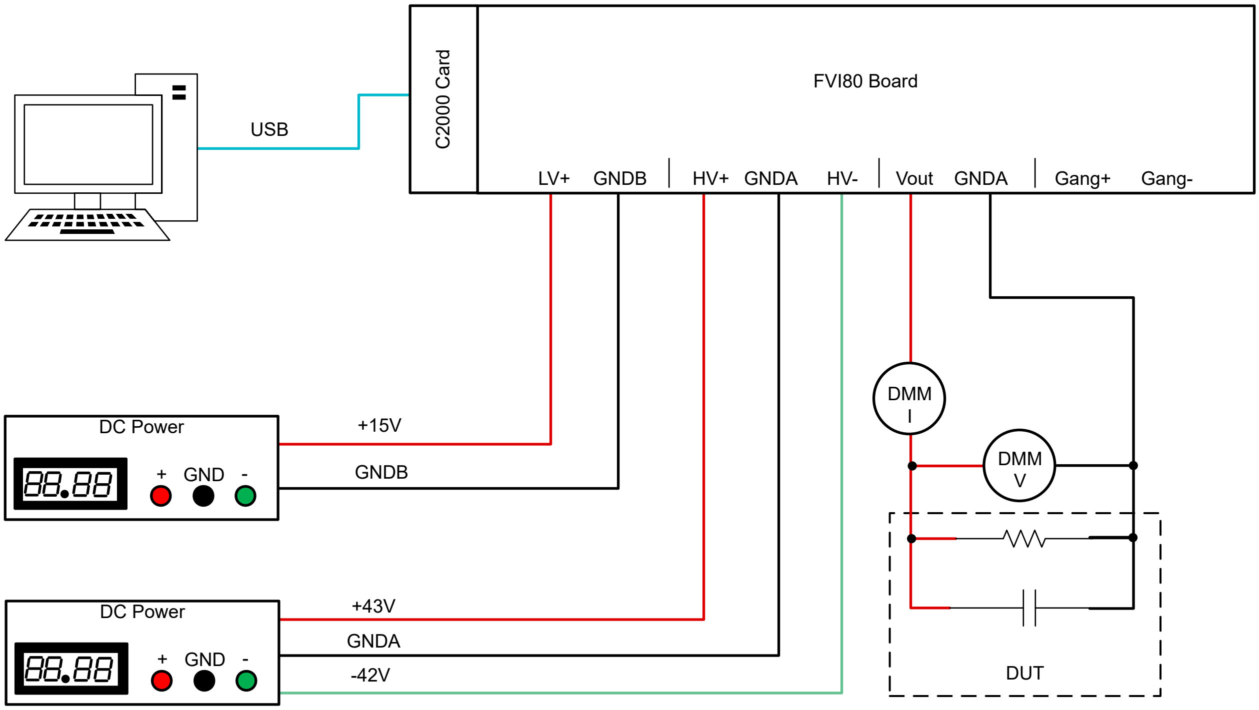


Figure 4-8. TIDA-010962 Connection for Source Working Mode

4.3.2 Sink Mode Connection

Figure 4-9 shows the setup for testing sink mode features. The DUT is a DC power supply that sets output voltage and current limitation. The TIDA-010962 board can be set to FV or FI mode.

For example, set the DC power supply to 15V with 100mA current limitation. Set the TIDA-010962 board to FV mode with force = 10V, CLH = 500, CLL = –500. The ADC read or DMM shows 10V and –100mA. If CLL = –50 is set, the ADC read or DMM shows 15V and –50mA because low clamp occurs. If the TIDA-010962 board is set to FI mode with force = –50, CLH = 40, CLL = –40, the ADC read or DMM shows 15V and –50mA. If CLH = 10 is set, the ADC read or DMM shows 10V and –100mA because high clamp occurs. The DC power supply current limitation must be set within TIDA-010962 current rating at this moment, otherwise the board experiences damage.

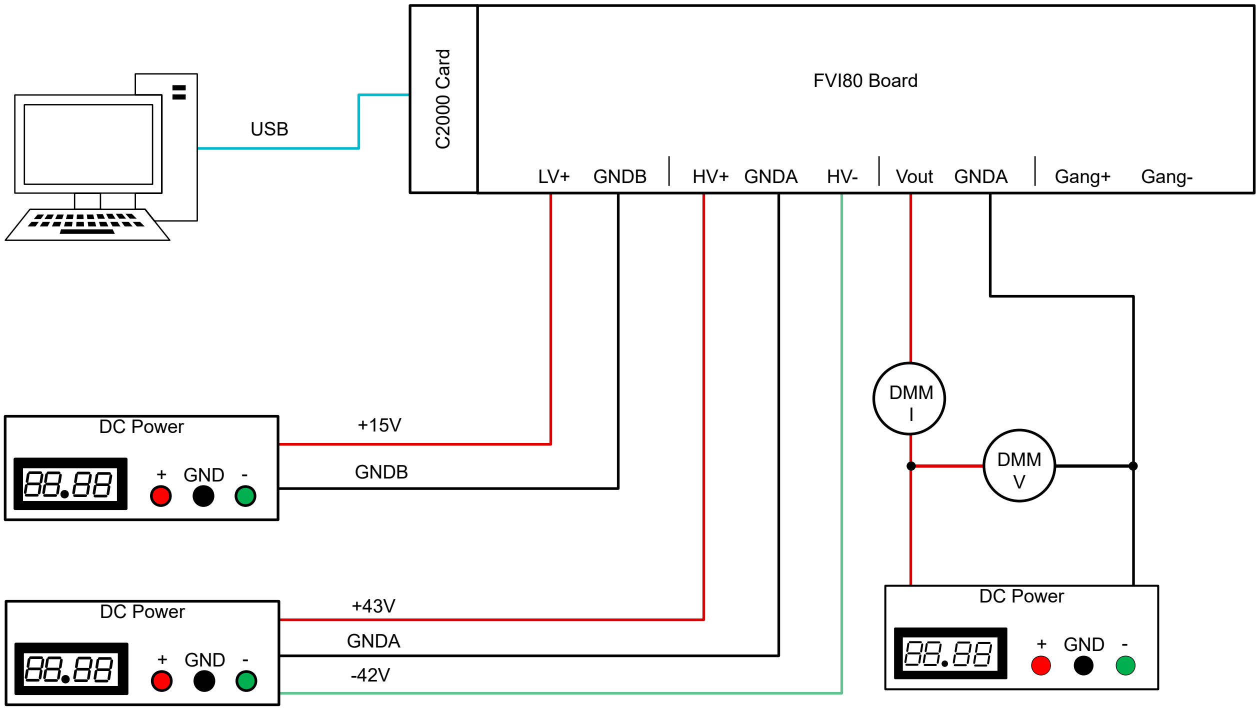


Figure 4-9. TIDA-010962 Connection for Sink Working Mode

4.3.3 Gang Mode Connection

Figure 4-10 shows the Gang mode connection for testing. One board serves as Gang Master, others serve as Gang slaves. All board power supplies are isolated. Connect the DUT to all board Vout+ and GNDA together. Connect all Gang+ together. Connect all Gang– together.

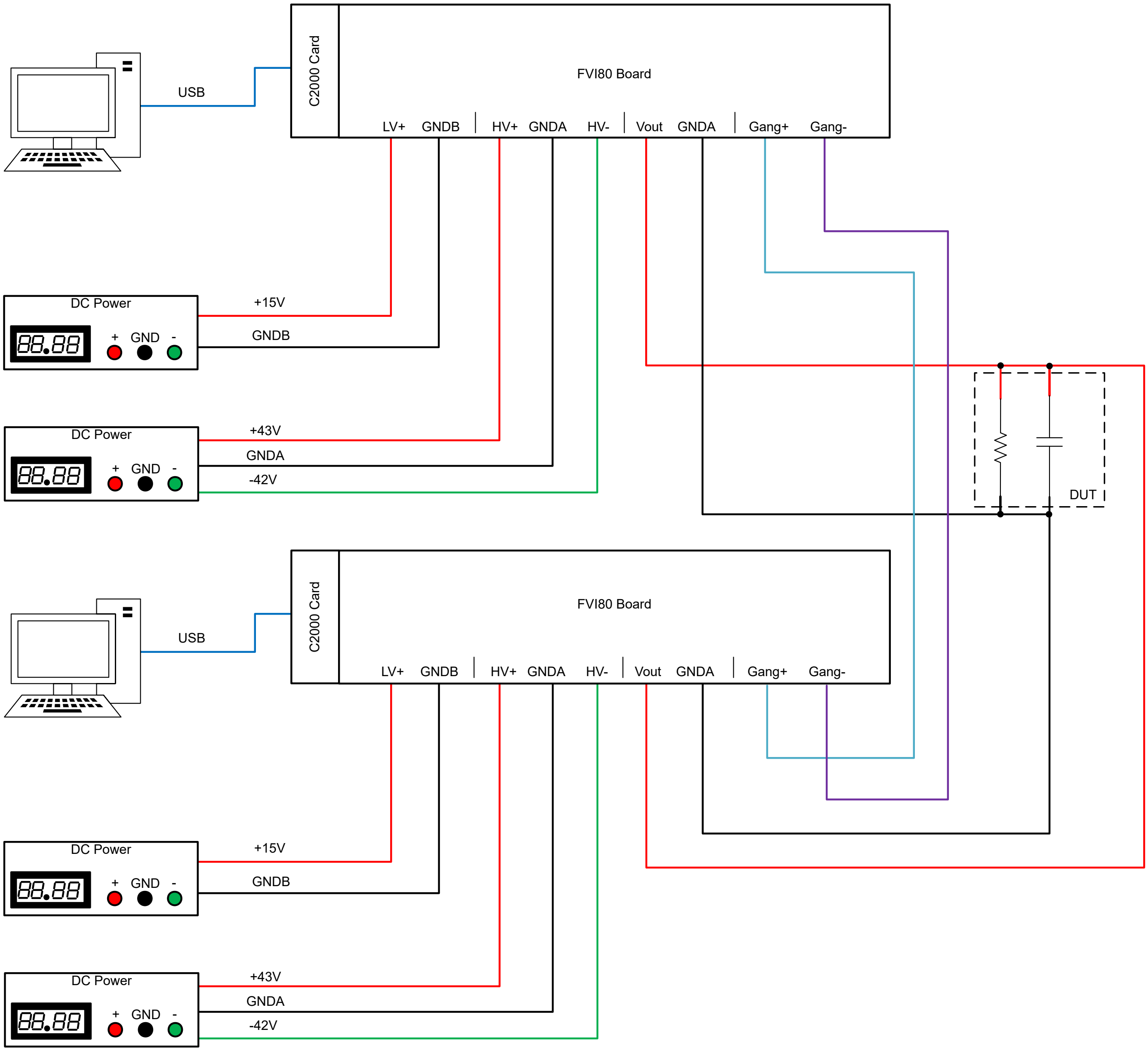


Figure 4-10. TIDA-010962 Connection for Gang Working Mode

4.4 Test Results

4.4.1 Linearity and Accuracy

4.4.1.1 FV ±40V, 500mA, Comp = 10k+470nF, DUT = 3MΩ

Because the DUT voltage divider connects with a pair of normal resistors, not precision resistors, the TCR of the divider performs poorly. Output linearity error becomes worse because of rising temperatures. A reserve position exists for a precision divider if more accurate testing is needed.

Figure 4-11 and Figure 4-12 show Force output and ADC read and DMM read data error before calibration.

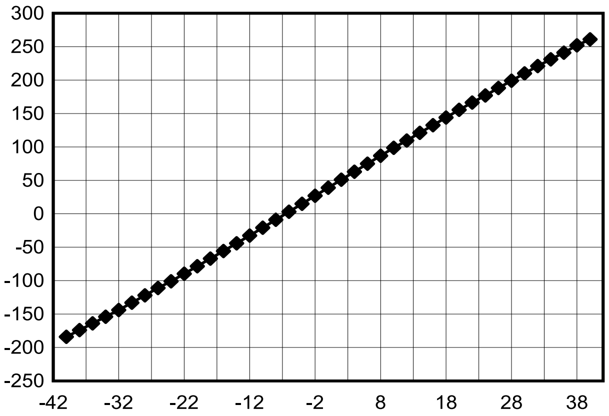


Figure 4-11. Voltage Output Error Before Calibration in FV ±40V, 500mA Mode (y-mV, x-V)

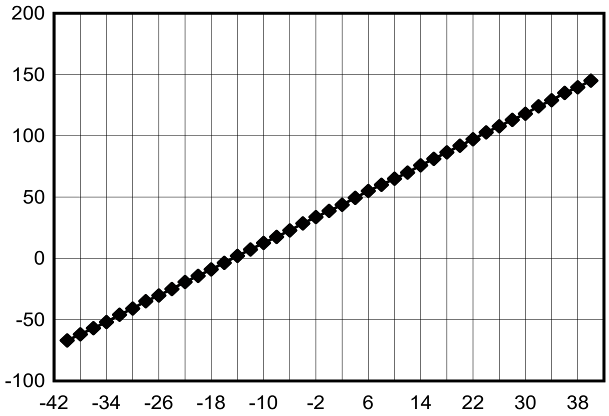


Figure 4-12. ADC Voltage Read Error Before Calibration in FV ±40V 500mA Mode (y-mV, x-V)

Figure 4-13 and Figure 4-14 show data error of force and ADC read after calibration.

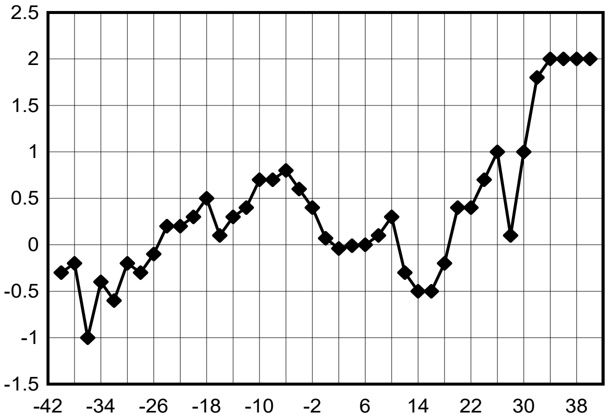


Figure 4-13. Voltage Output Error After Calibration in FV ±40V, 500mA Mode (y-mV, x-V)

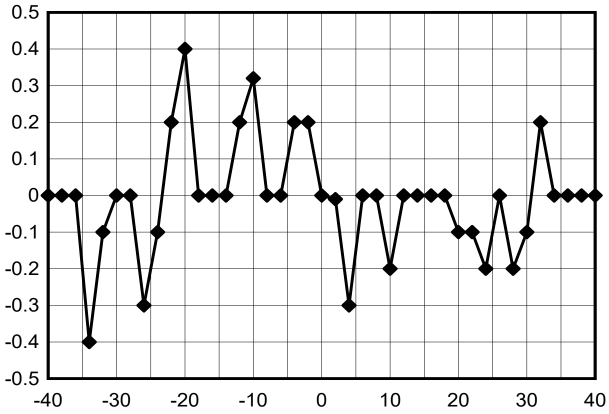


Figure 4-14. ADC Voltage Read Error After Calibration in FV ±40V, 500mA Mode (y-mV, x-V)

Table 4-3 shows the measured data.

Table 4-3. Measured Data

	BEFORE CALIBRATION				AFTER CALIBRATION			
set (V)	**output (V)**	**ADC Read (V)**	**Output Error (mV)**	**Read Error (mV)**	**Read From DMM (V)**	**Read From ADC (V)**	**Output Error (mV)**	**Read Error (mV)**
–40	–40.184	–40.067	–184	–67	–40.0003	–40	–0.3	0
–38	–38.174	–38.062	–174	–62	–38.0002	–38	–0.2	0
–36	–36.164	–36.057	–164	–57	–36.001	–36	–1	0
–34	–34.154	–34.052	–154	–52	–34.0004	–34.0004	–0.4	–0.4
–32	–32.144	–32.046	–144	–46	–32.0006	–32.0001	–0.6	–0.1
–30	–30.133	–30.041	–133	–41	–30.0002	–30	–0.2	0
–28	–28.122	–28.035	–122	–35	–28.0003	–28	–0.3	0
–26	–26.111	–26.0303	–111	–30.3	–26.0001	–26.0003	–0.1	–0.3
–24	–24.101	–24.025	–101	–25	–23.9998	–24.0001	0.2	–0.1
–22	–22.0897	–22.0193	–89.7	–19.3	–21.9998	–21.9998	0.2	0.2
–20	–20.0785	–20.0143	–78.5	–14.3	–19.9997	–19.9996	0.3	0.4
–18	–18.067	–18.009	–67	–9	–17.9995	–18.000	0.5	0
–16	–16.0557	–16.0037	–55.7	–3.7	–15.9999	–16	0.1	0
–14	–14.0442	–13.998	–44.2	2	–13.9997	–14	0.3	0
–12	–12.0326	–11.9928	–32.6	7.2	–11.9996	–11.9998	0.4	0.2
–10	–10.0209	–9.9874	–20.9	12.6	–9.9993	–9.99968	0.7	0.32
–8	–8.0089	–7.9825	–8.9	17.5	–7.9993	–8	0.7	0
–6	–5.9969	–5.9772	3.1	22.8	–5.9992	–6	0.8	0
–4	–3.985	–3.9715	15	28.5	–3.9994	–3.9998	0.6	0.2
–2	–1.973	–1.9663	27	33.7	–1.9996	–1.9998	0.4	0.2
0	0.03897	0.03875	38.97	38.75	0.00007	0	0.07	0
2	2.051	2.0437	51	43.7	1.99996	1.99999	–0.04	–0.01
4	4.0629	4.0494	62.9	49.4	3.99999	3.9997	–0.01	–0.3
6	6.0749	6.055	74.9	55	6	6	0	0
8	8.0868	8.06	86.8	60	8.0001	8	0.1	0
10	10.0987	10.065	98.7	65	10.0003	9.9998	0.3	–0.2
12	12.1095	12.07	109.5	70	11.9997	12	–0.3	0
14	14.1211	14.0759	121.1	75.9	13.9995	14	–0.5	0
16	16.1325	16.0812	132.5	81.2	15.9995	16	–0.5	0
18	18.144	18.0865	144	86.5	17.9998	18	–0.2	0
20	20.1555	20.0919	155.5	91.9	20.0004	19.9999	0.4	–0.1
22	22.1664	22.0972	166.4	97.2	22.0004	21.9999	0.4	–0.1
24	24.177	24.1028	177	102.8	24.0007	23.9998	0.7	–0.2
26	26.1882	26.1078	188.2	107.8	26.001	26	1	0
28	28.199	28.113	199	113	28.0001	27.9998	0.1	–0.2
30	30.21	30.118	210	118	30.001	29.9999	1	–0.1
32	32.221	32.124	221	124	32.0018	32.0002	1.8	0.2

Table 4-3. Measured Data (continued)

	BEFORE CALIBRATION				AFTER CALIBRATION			
set (V)	output (V)	ADC Read (V)	Output Error (mV)	Read Error (mV)	Read From DMM (V)	Read From ADC (V)	Output Error (mV)	Read Error (mV)
34	34.231	34.129	231	129	34.002	34	2	0
36	36.241	36.135	241	135	36.002	36	2	0
38	38.252	38.1396	252	139.6	38.002	38	2	0
40	40.261	40.145	261	145	40.002	40	2	0

4.4.1.2 FV, 0V to 80V, 500mA, Comp = 10k+470nF, DUT = 3MΩ

Figure 4-15 and Figure 4-16 show the errors before calibration.

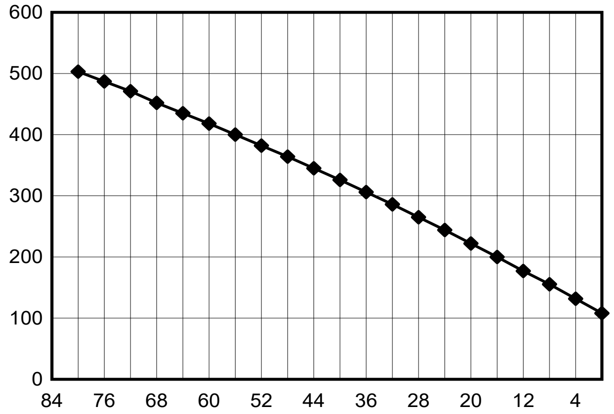


Figure 4-15. Voltage Output Error Before Calibration in FV 0-80V 500mA Mode (y-mV, x-V)

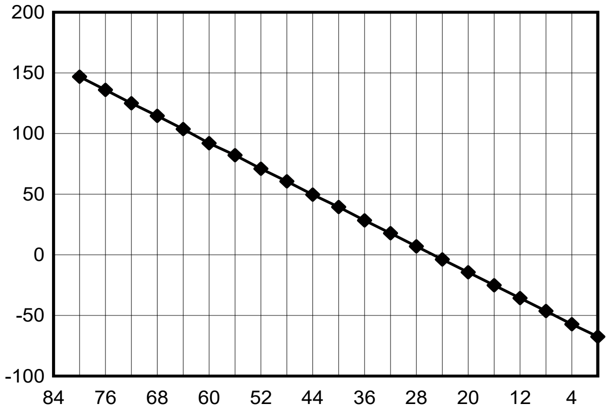


Figure 4-16. ADC Voltage Read Error Before Calibration in FV 0-80V SPAN Mode (y-mV, x-V)

Figure 4-17 and Figure 4-18 show the errors after calibration.

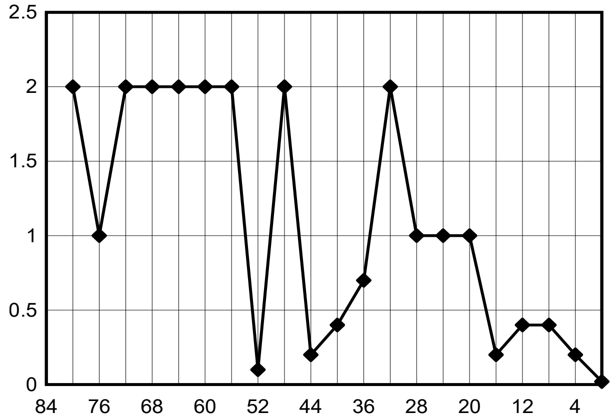


Figure 4-17. Voltage Output Error After Calibration in FV 0-80V 500mA Mode(y-mV, x-V)

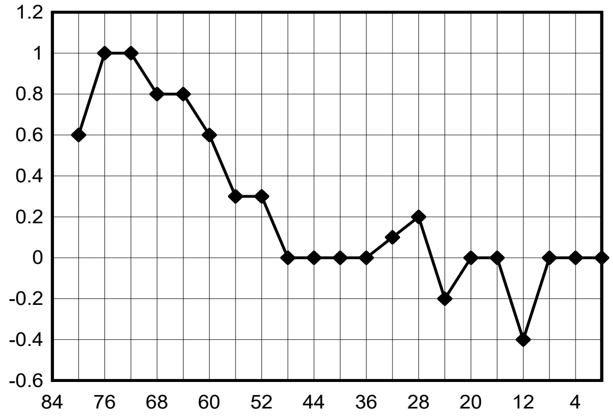


Figure 4-18. ADC Voltage Read Error After Calibration in FV 0-80V 500mA Mode (y-mV, x-V)

4.4.1.3 FI, ±40V, 10mA, Comp = 10k + 470nF, DUT = 3MΩ

Because the current sensing resistor connects with a normal resistor, not a precision resistor, output current linearity error becomes worse because of rising temperature. A reserve position exists for a precision sensing resistor if more accurate testing is needed.

Figure 4-19 and ADC Current Read Error Before Calibration in FV ±40V 10mA Mode (y-µA, x-mA) show the errors before calibration.

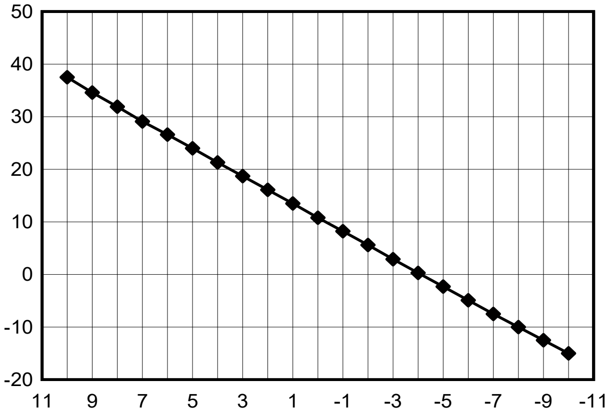


Figure 4-19. Current Output Error Before Calibration in FV ±40V 10mA Mode (y-µA, x-mA)

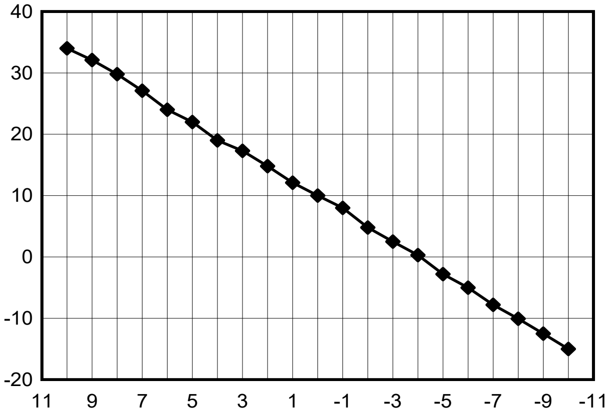


Figure 4-20. ADC Current Read Error Before Calibration in FV ±40V 10mA Mode (y-µA, x-mA)

Figure 4-21 and Figure 4-22 show the errors after calibration.

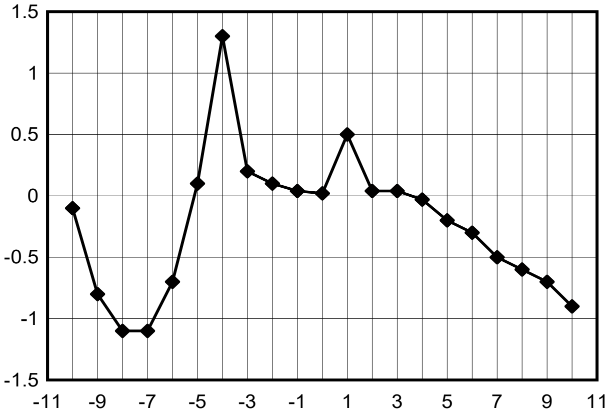


Figure 4-21. Current Output Error After Calibration in FV ±40V 10mA Mode (y-µA, x-mA)

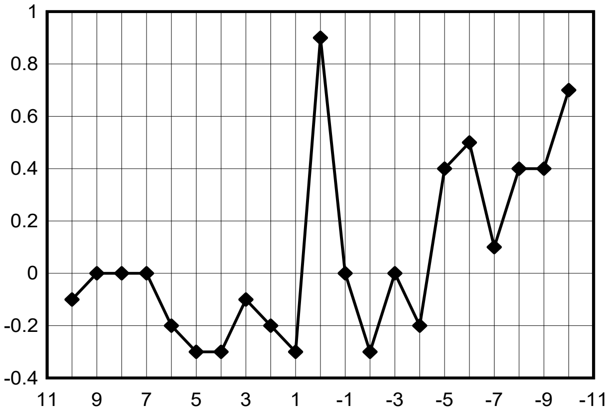


Figure 4-22. ADC Current Read Error After Calibration in FV ±40V 10mA Mode (y-µA, x-mA)

4.4.1.4 Buffer, ±40V, 10mA, Comp = 10k + 470nF, DUT = 3MΩ

Figure 4-23 and Figure 4-24 show the errors before calibration.

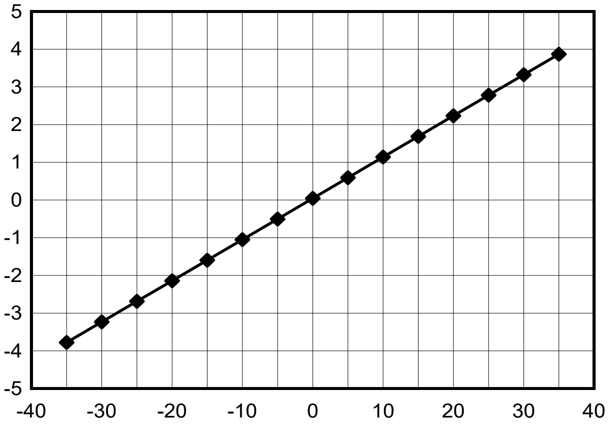


Figure 4-23. Voltage Output Error Before Calibration in Buffer ±40V 500mA Mode (y-V, x-V)

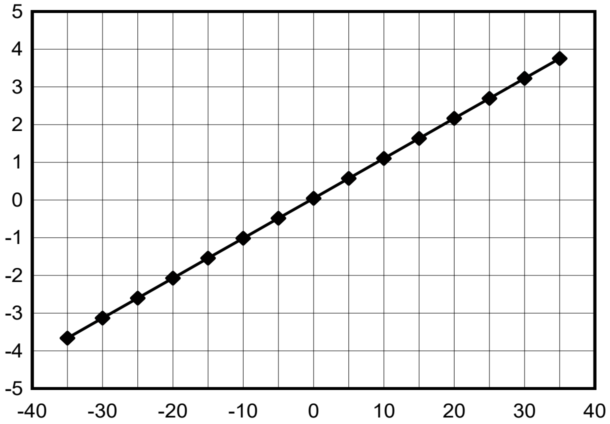


Figure 4-24. ADC Voltage Read Error Before Calibration in Buffer ±40V 500mA Mode (y-V, x-V)

Figure 4-25 and Figure 4-26 show the errors after calibration.

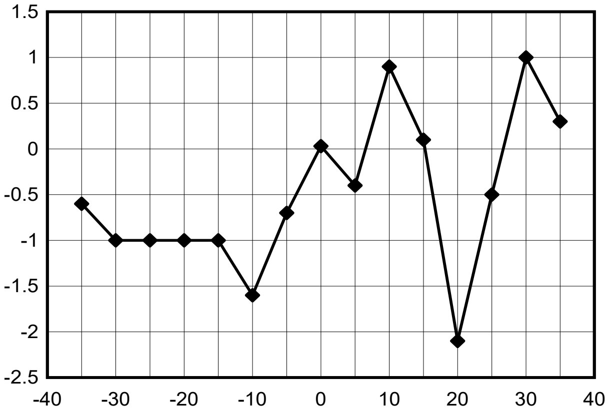


Figure 4-25. Voltage Output Error After Calibration in Buffer ±40V 500mA Mode (y-mV, x-V)

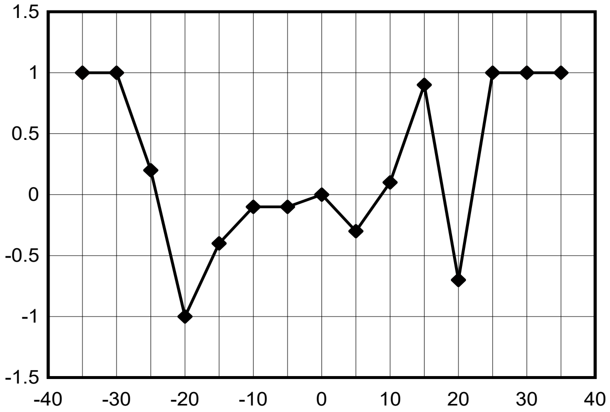


Figure 4-26. ADC Voltage Read Error After Calibration in Buffer ±40V 500mA Mode (y-mV, x-V)

4.4.2 Transient

Figure 4-27 through Figure 4-32 show the transient test results under varying conditions.

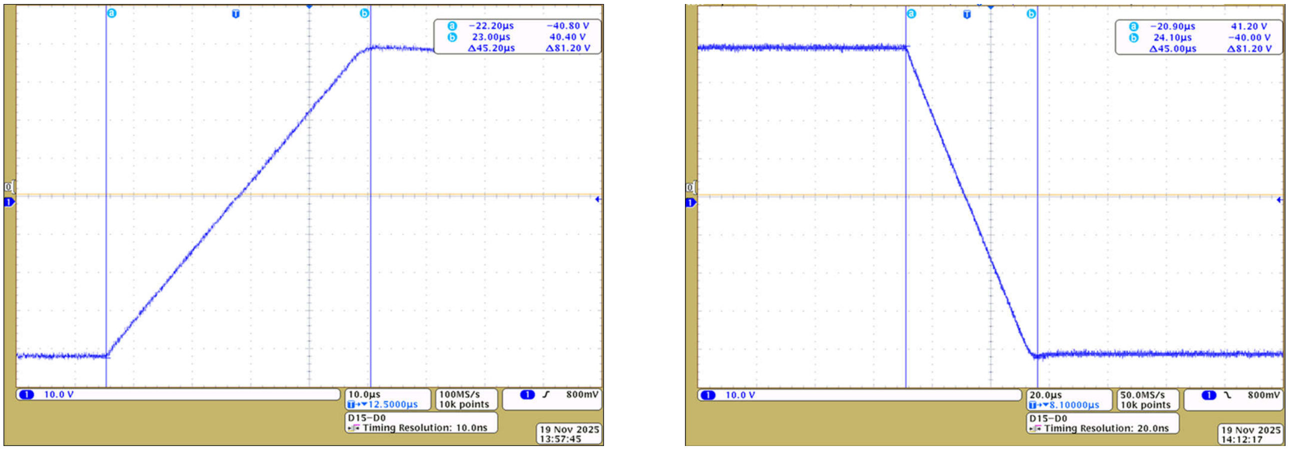


Figure 4-27. Transient of FV ±40V, 500mA, Comp = 10k+10nF, DUT = 3MΩ

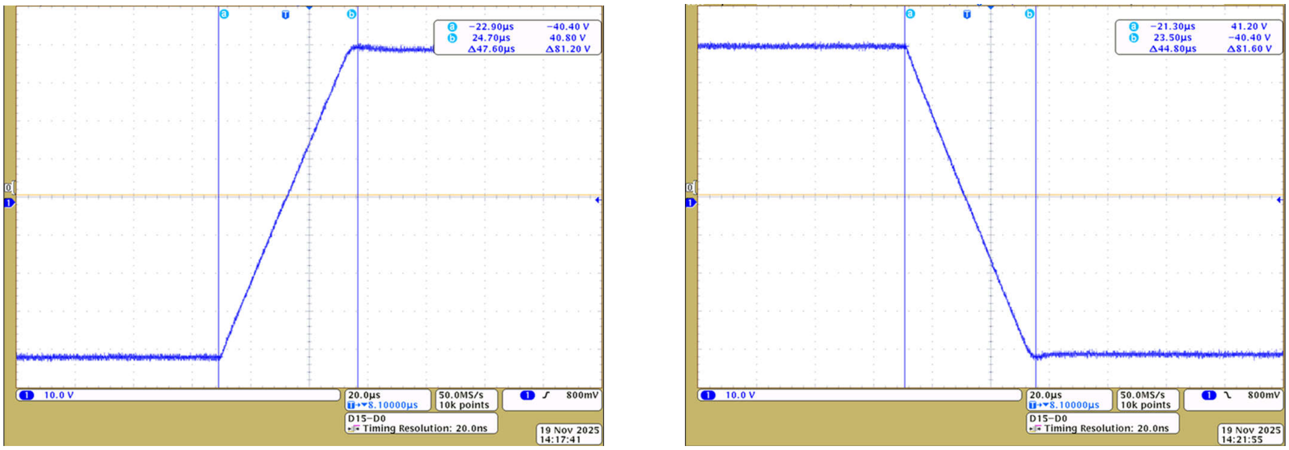


Figure 4-28. Transient of FV ±40V, 10mA, Comp = 10k+10nF, DUT = 3MΩ

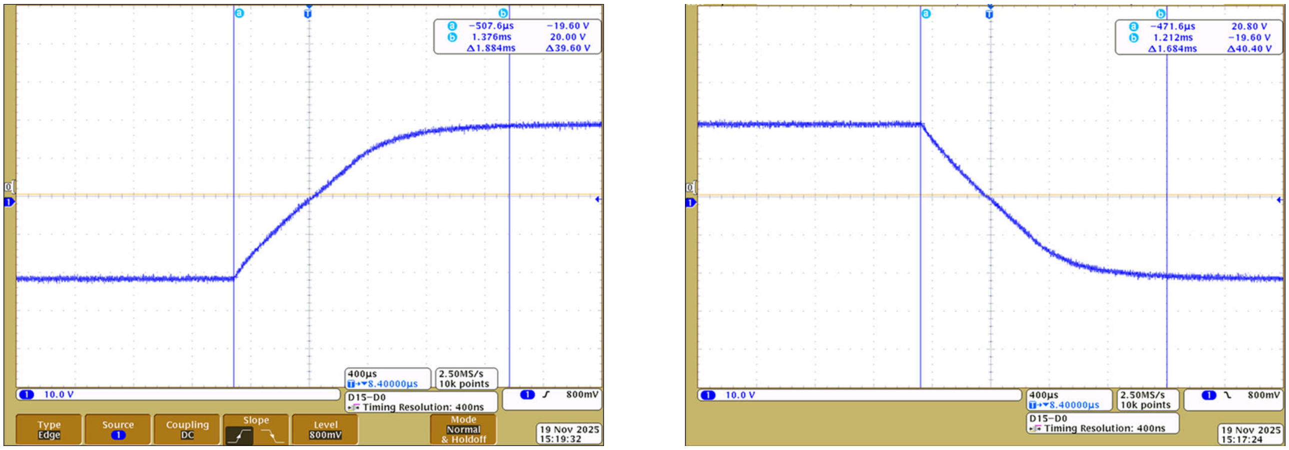


Figure 4-29. Transient of FV ±40V, 10µA, Comp = 10k+470nF, DUT = Oscilloscope

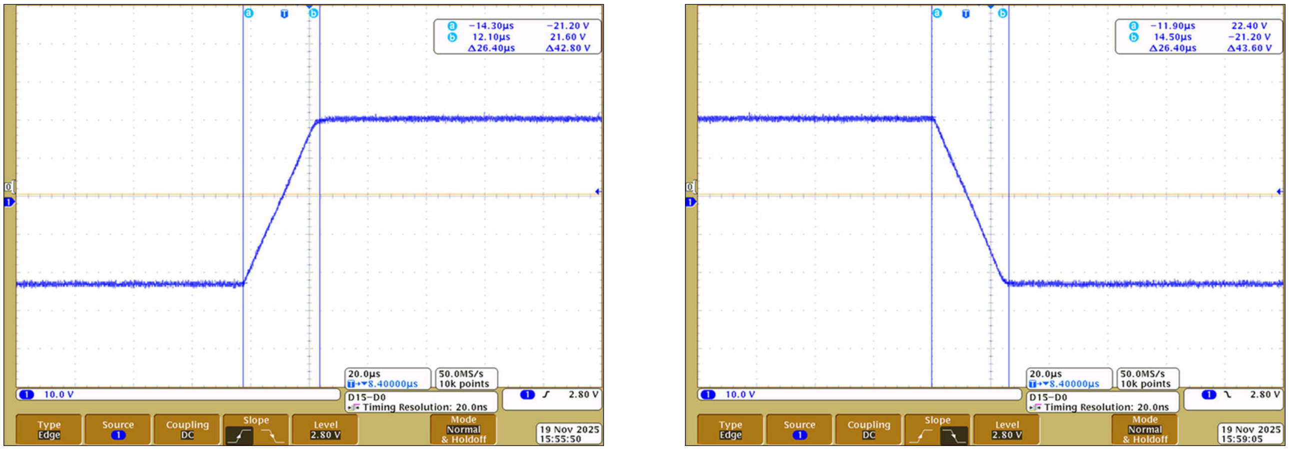


Figure 4-30. Transient of FI ±40V, 500mA, Comp = 10k+10nF, DUT = 43Ω

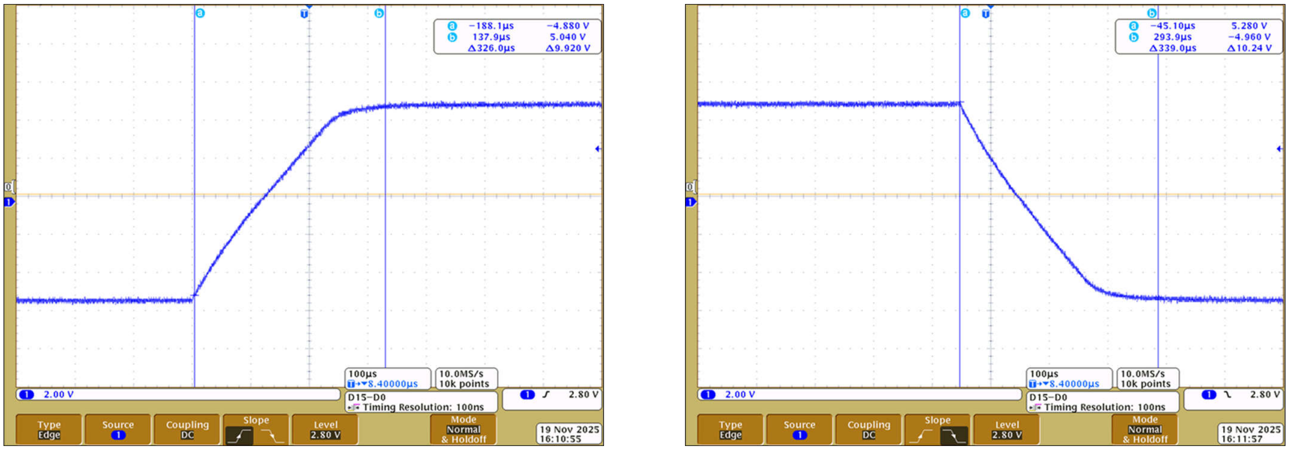


Figure 4-31. Transient of FI ±40V, 10mA, Comp = 10k+470nF, DUT = 510Ω

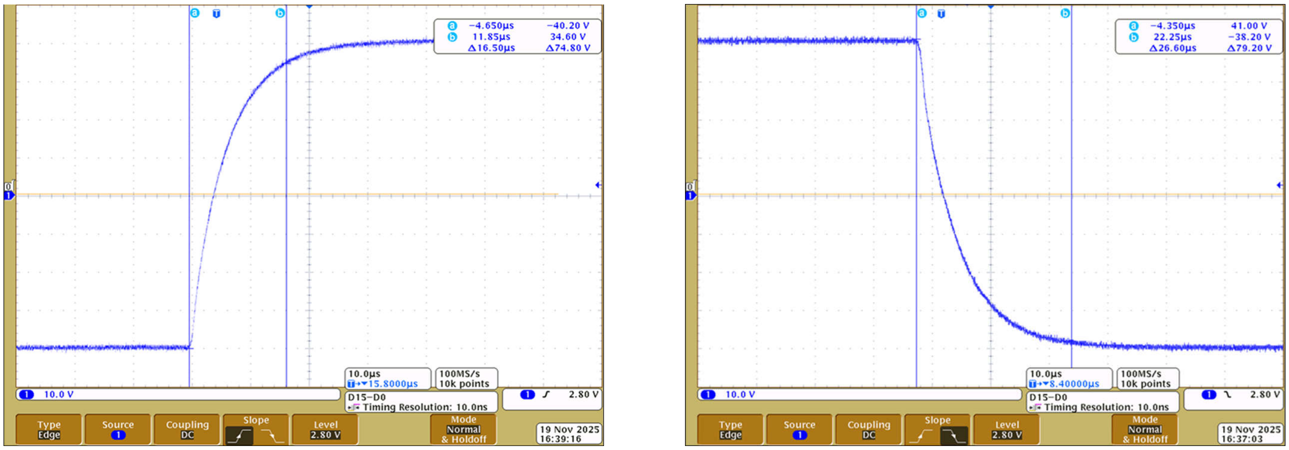


Figure 4-32. Transient of Buffer, ±40V, 500mA, Comp = 10k+5.6k||1nF, DUT = 3MΩ

4.4.3 Capacitance Load

Figure 4-33 and Figure 4-34 show the capacitance load test results under varying conditions.

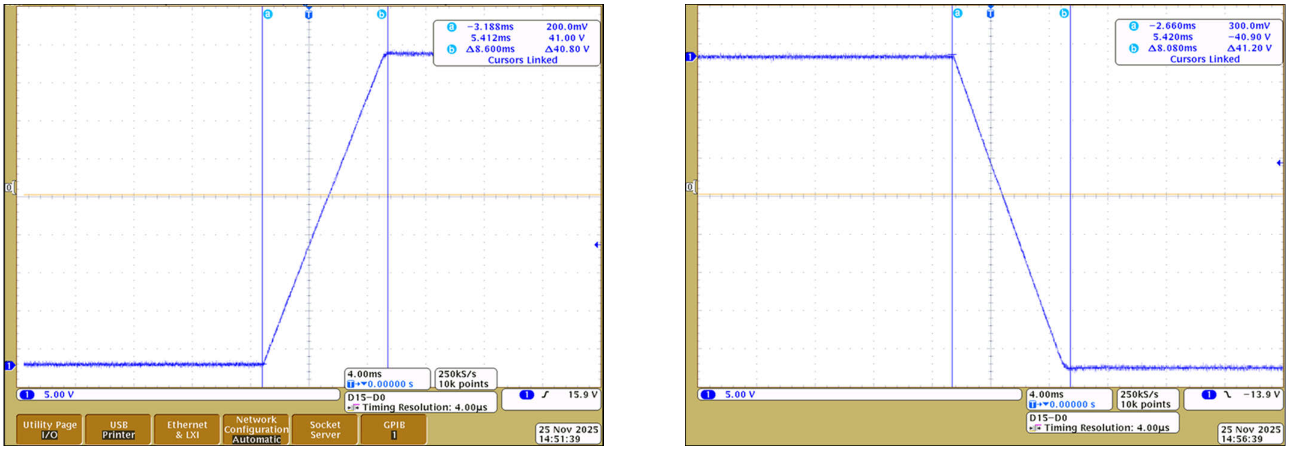


Figure 4-33. Transient of CV, ±40V, 500mA, Comp = 10k+470nF, DUT = 3 × 33μF (AL, 400V rating)

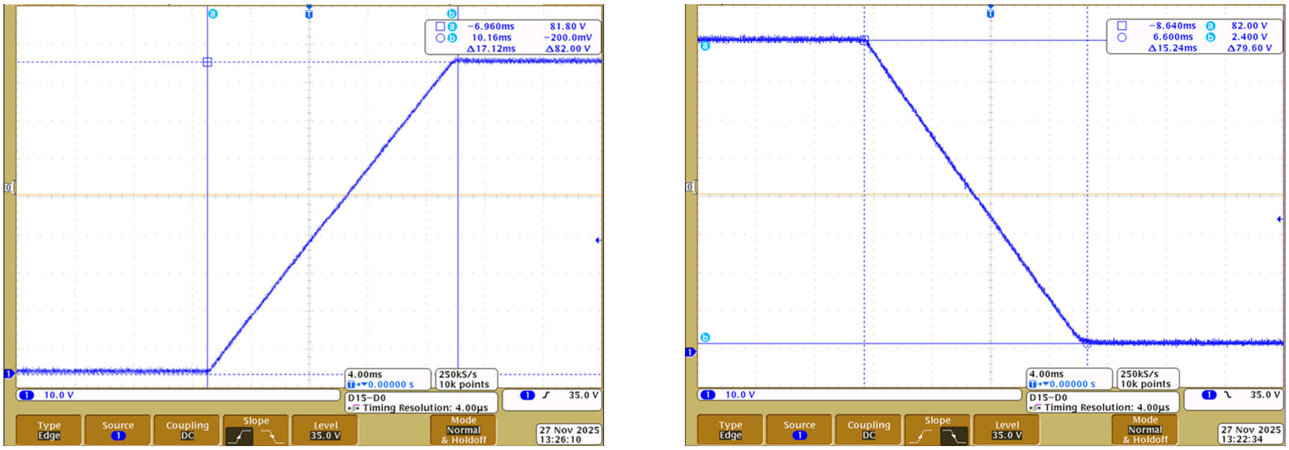
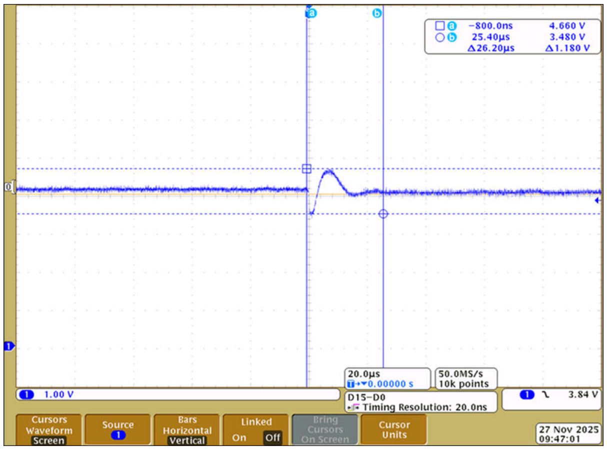


Figure 4-34. Transient of CV, 0V to 80V, 500mA, Comp = 10k+470nF, DUT = 3 × 33μF (AL, 400V rating)

4.4.4 Glitch

Figure 4-35 shows glitch appears only when switching from 500mA to 10mA current range. Glitch is hard to see when switching from 10mA to 500mA.



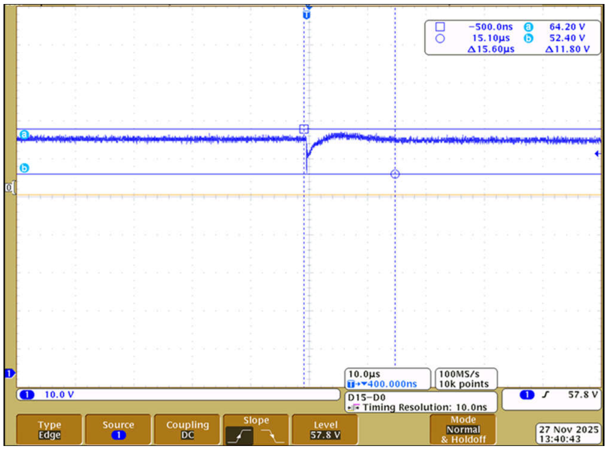
CV, Force = 4V, ±40V, 500mA, Comp = 10k+10nF, DUT = 510Ω

Figure 4-35. Transient of Switching Glitch from 500mA to 10mA Current Range

When switching from 500mA to 10mA range, changing Comp = 15k+10nF reduces voltage overshoot.

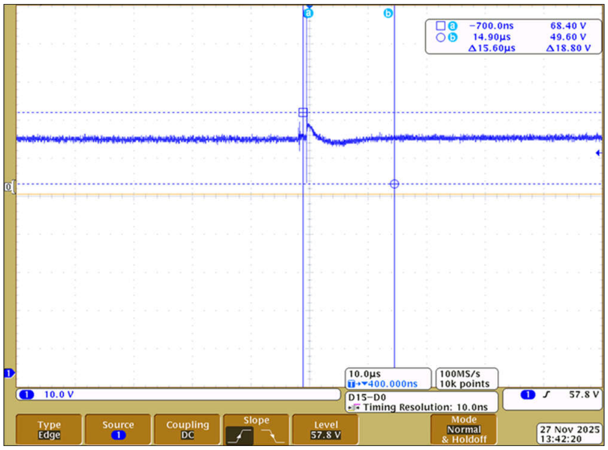
4.4.5 Settling Time

Figure 4-36 shows switching from 0mA to 470mA at 60V CV by manually connecting the DUT cable. Figure 4-37 shows switching from 470mA to 0mA at 60V CV by manually disconnecting the DUT cable.



CV, 0V to 80V SPAN, 500mA Range, ±500mA Clamp,
DUT = 128Ω, Comp = 20k+10n

Figure 4-36. Transient of Settling from Open Load to *Full* Load

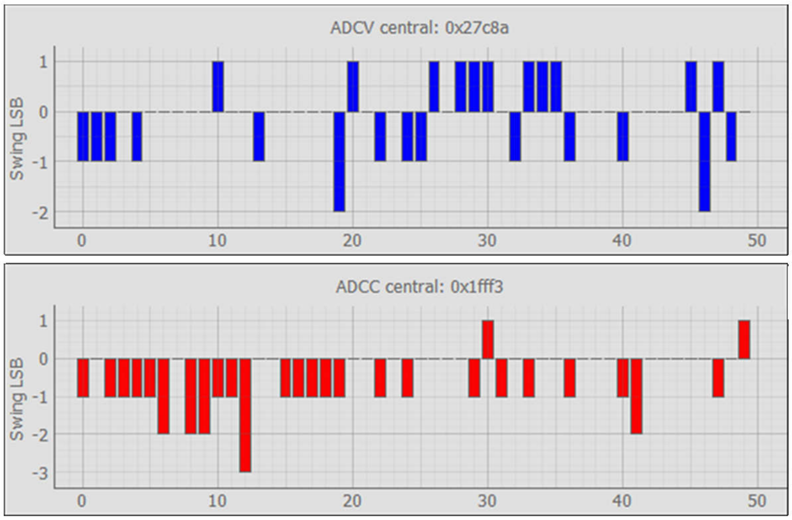


CV, 0V to 80V SPAN, 500mA Range, ±500mA Clamp,
DUT = 128Ω, Comp = 20k+10n

Figure 4-37. Transient of Settling from *Full* Load to Open Load

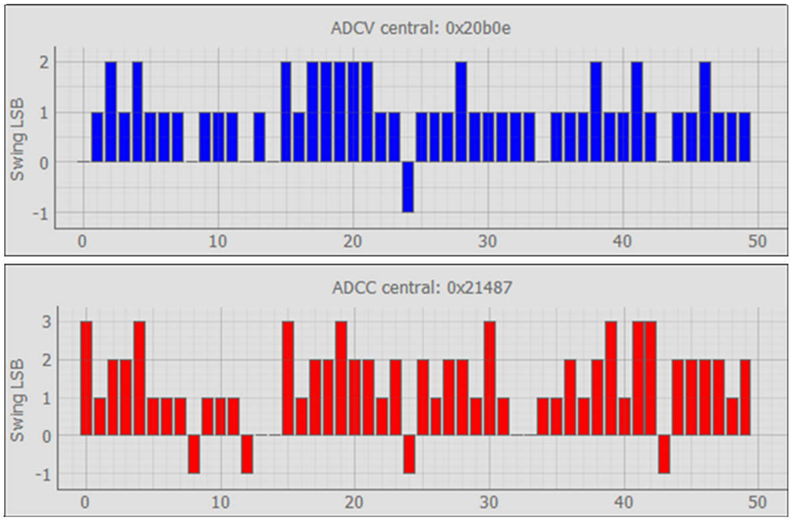
4.4.6 ADC Swing LSB

Figure 4-38 and Figure 4-39 show ADC swing LSB force voltage and force current charts.



CV, 500mA, Comp = 10k+470nF, Force = 10V, DUT = open

Figure 4-38. Swing LSB in Force Voltage



CC, 500mA, Comp=10k+470nF, Force = 20mA, DUT = 410Ω

Figure 4-39. Swing LSB in Force Current

5 Design and Documentation Support

5.1 Design Files

5.1.1 Schematics

To download the schematics, see the design files at TIDA-010962.

5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010962.

5.1.3 PCB Layout Recommendations

5.1.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-010962.

5.2 Tools and Software

Tools

TMDSCNCD280039C	F280039C control Card Evaluation Module

Software

CCSTUDIO	Code Composer Studio (CCS) Integrated Development Environment (IDE)
UNIFLASH	UniFlash flash programming tool
FVI80GUI	TIDA-010962 PC Control GUI

5.3 Documentation Support

1. Texas Instruments, *DAC11001B 20-Bit, Low-Noise, Ultra-Low Harmonic Distortion, Fast-Settling, High-Voltage-Output, Digital-to-Analog Converter (DAC) Datasheet*
2. Texas Instruments, *DACx0502, Dual, 16-Bit, 14-Bit, and 12-Bit, 1-LSB INL, Voltage-Output DACs With Precision Internal Reference Datasheet*
3. Texas Instruments, *TCAL9539 Low-Voltage 16-Bit I2C-Bus, SMBus I/O Expander with Interrupt Output, Reset, and Configuration Registers Datasheet*
4. Texas Instruments, *TMS320F28003x Real-Time Microcontrollers Datasheet*

5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6 About the Author

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7 Acknowledgment

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