具有反激式直流/直流控制器的 TPS2375x IEEE 802.3at PoE 接口

1 特性

- 使用状态标志进行 IEEE 802.3at 分类
- 可在宽负载范围内提供高效解决方案
- 可对高达 25.5W 的受电设备供电
- 耐用的 100V，0.5Ω 热交换金属氧化物半导体场效应晶体管 (MOSFET)
- 同步整流器禁用信号
- PowerPAD™薄型小外形尺寸 (TSSOP) 封装
- 具有完整的 PoE 接口和直流/直流控制器
- 适配器 ORing 支持
- 可编程频率
- TPS23752 支持超低功耗睡眠模式
- -40°C 至 125°C 的工作结点温范围

2 应用

- 符合 IEEE 802.3at 标准的器件
- 视频和网络语音 (VoIP) 电话
- 多频带访问点
- 监控摄像机
- 微微基站

3 说明

TPS23751 是一个整合有以太网供电 (PoE) 受电设备 (PD) 接口和电流模式直流/直流控制器的 16 引脚集成电路， 专门针对 在宽负载范围内要求实现高效率的应用进行了优化。

PoE 接口执行符合 IEEE 802.3at 标准的类型 2 硬件类别。它还包括一个辅助电源检测 (APD) 输入和一个禁用功能 (DEN)。0.5Ω、100V 的导通 MOSFET 最大限度地减少了热耗散，并大大提高了电源利用率。

该直流/直流控制器 具有 内部软启动、引导启动电流源、带有斜坡补偿的电流模式控制、消隐和电流限制等特性。通过禁用同步整流并进入可变频率运行 (VFO) 可提高轻负载时的效率。

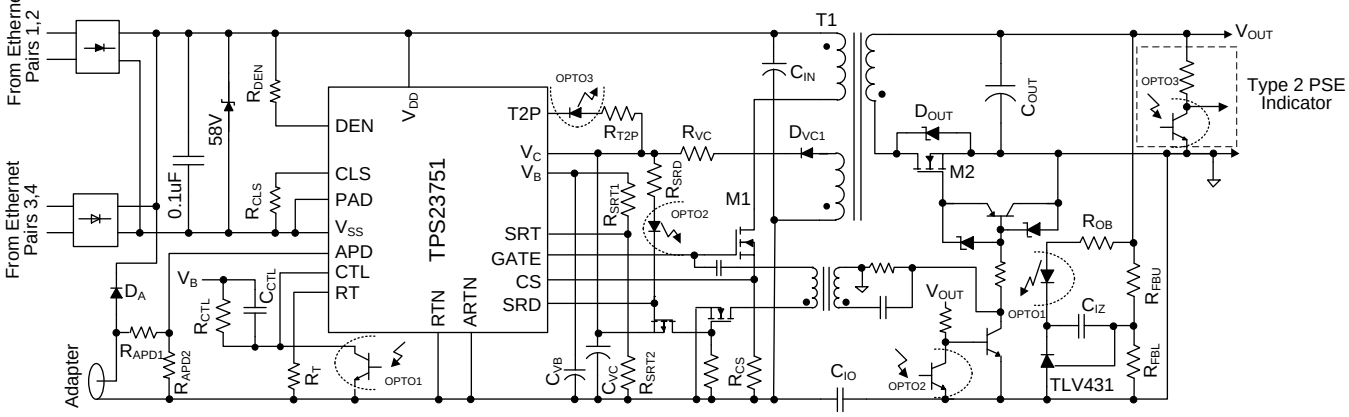
TPS23752 是 TPS23751 的 20 引脚扩展版本并具有额外的睡眠模式功能。睡眠模式将会禁用转换器以最大限度地减少功耗，同时仍然生成 IEEE802.3at 所需的维持功率特征 (MPS)。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS23751	TSSOP (16)	5.00mm x 4.40mm
TPS23752	TSSOP (20)	6.50mm x 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

图 1. 典型应用电路



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (November 2015) to Revision E — **Page**

- 已更改 数据表标题改为*具有反激式直流/直流控制器的 TPS2375x IEEE 802.3at PoE 接口* ... 1

Changes from Revision C (January 2014) to Revision D — **Page**

- 添加了 *ESD 额定值* 表、*特性 说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分。 ... 1

Changes from Revision B (July 2013) to Revision C — **Page**

- Changed the T2P startup delay MAX value From: 0 ms To: 7 ms ... 9

Changes from Revision A (August 2012) to Revision B — **Page**

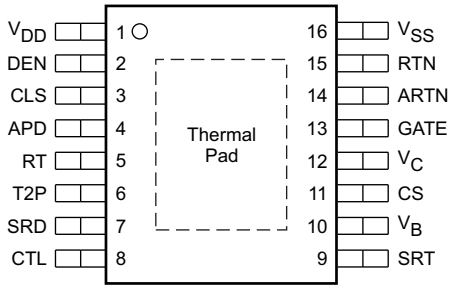
- Added "THERMAL SHUTDOWN" to the CONTROLLER SECTION ... 7
- Added text to the V_C Pin Description: "The Sleep Mode output voltage is high enough to drive..." ... 19
- Added text to the Sleep Mode Operation (TPS23752 only) " For more information regarding ..." ... 19

Changes from Original (July 2012) to Revision A — **Page**

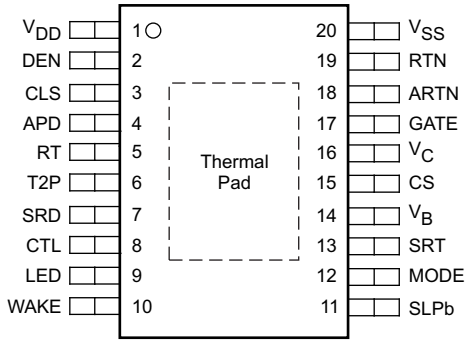
- 已更改 从产品预览改为生产数据 ... 1

5 Pin Configuration and Functions

PWP Package
16-Pin TSSOP
Top View



PWP Package
20-Pin TSSOP
Top View



Pin Functions

NAME	PIN		I/O	DESCRIPTION
	TPS23751	TPS23752		
V_{DD}	1	1	I	Connect to positive PoE input power rail. Bypass with 0.1 µF to V_{SS}.
DEN	2	2	I/O	Connect 24.9 kΩ to V_{DD} for detection. Pull to V_{SS} to disable pass MOSFET.
CLS	3	3	I/O	Connect resistor from CLS to V_{SS} to program classification current.
APD	4	4	I	Raise 1.5 V above ARTN to disable pass MOSFET and force T2P active.
RT	5	5	I	Connect a resistor from RT to ARTN to set switching frequency.
T2P	6	6	O	Active low indicates type-2 PSE connected or APD active.
SRD	7	7	O	Disable external synchronous rectifiers in VFO Mode.
CTL	8	8	I	Control loop input to PWM
LED	—	9	O	Open-drain drive for external LED controlled by SLPb, MODE, and WAKE.
WAKE	—	10	I/O	Pull WAKE low to re-enable the DC-DC converter from Sleep Mode.
SLPb	—	11	I	Pull low during normal operation to enter Sleep Mode.
MODE	—	12	I	Enables pulsed MPS when entering Sleep Mode. Control LED in normal operation.
SRT	9	13	I	Set the threshold of PWM to VFO transition
V_B	10	14	O	5 V bias supply. Bypass with a minimum of 0.1 µF to ARTN.
CS	11	15	I/O	Current sense input. Connect to ARTN-referenced current sense resistor.
V_C	12	16	I/O	DC-DC converter bias voltage. Bypass with 0.47 µF or more to ARTN directly at pin.
GATE	13	17	O	Gate driver output for DC-DC converter switching MOSFET.
ARTN	14	18	PWR	DC-DC converter analog return. Connect to RTN.
RTN	15	19	O	Drain of PoE pass MOSFET. Connect to ARTN.
V_{SS}	16	20	PWR	Connect to negative power rail derived from PoE source.
Pad			—	Always connect PowerPAD™ to V_{SS}. A large fill area is required to assist in heat dissipation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Voltage	DEN, V_{DD}	–0.3	100	V
	ARTN(2), RTN(3)	–0.6	100	
	CLS(4)	–0.3	6.5	
	[CTL, MODE, RT, SLPb, SRT, V_B(4), WAKE] to ARTN	–0.3	6.5	
	CS to ARTN	–0.3	V_B	
	[LED, APD SRD, T2P, V_C] to ARTN	–0.3	18	
	GATE(4) to ARTN	–0.3	VC + 0.3	
Current, sinking	RTN(5)	Internally limited		mA
	LED		15	
	T2P, SRD		5	
	DEN		1	
Current, sourcing	CLS		65	mA
	V_C	Internally limited		
	V_B	Internally limited		
Current, average sourcing or sinking	GATE		25	mA_{RMS}
T_{JMAX}		Internally limited		°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) ARTN must be connected to RTN.
(3) With I_{RTN} = 0.
(4) Do not apply voltages to these pins.
(5) SOA limited to RTN = 80 V at 1.2 A.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings: Surge

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	System level at RJ-45 (1)	Contact	8000	V
			Air	15000	

(1) ESD per EN61000-4-2. A power supply containing the TPS23751 or TPS23752 was subjected to the highest test levels in the standard. Refer to the ESD section.

6.4 Recommended Operating Conditions(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	ARTN, RTN, V_{DD}	0		57	V
	[LED, APD ,SRD, T2P, V_C] to ARTN	0		18	
	[CTL,CS, MODE, SLPb, SRT, WAKE] to ARTN	0		V_B	
	SRT to ARTN	0.5		1.5	
Sinking current	RTN			1.2	A
	SRD, T2P			2	mA
	LED			10	
Sourcing current	V_B(2)			5	mA
Continuous RTN current ($T_J \le 125°C$)(3)				825	mA
Resistance	R_{CLS}(2)	60			Ω
	R_{WAKE}			392	kΩ
Capacitance	V_B(2)	0.08			µF
Junction temperature		–40		125	°C

(1) ARTN tied to RTN
(2) Do not apply voltage supply to these pins.
(3) This is minimum current-limit value. Viable systems will be designed for maximum currents below this value with reasonable margin. IEEE 802.3at permits 600mA continuous loading.

6.5 Thermal Information

THERMAL METRIC(1)		TPS23751 PWP (TSSOP) 16 PINS	TPS23752 PWP (TSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.5	38.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.9	23.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.1	25.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20.8	20.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.0	1.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.6 Electric Characteristics - Controller Section

Unless otherwise noted, 40 V ≤ V_{DD} ≤ 57 V; V_{CTL} = V_{MODE} = V_{SLPb} = V_B; V_{SRT} = 0.5 V; V_{APD} = V_{CS} = V_{ARTN} = V_{RTN}; CLS, GATE, LED, SRD, T2P open; R_{WAKE} = 392 kΩ; R_{DEN} = 24.9 kΩ; R_T = 34 kΩ; C_{VB} = C_{VC} = 0.1 µF;
–40 ≤ T_J ≤ 125°C. Typical values are at 25°C. All voltages referred to V_{SS}.
V_C = 12 V, V_{DEN} = V_{VSS}, V_{ARTN} = V_{RTN} = V_{SS}

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_C (GATE DRIVE SUPPLY)							
Output voltage; TPS23752 only		V_{VDD} = 48 V, Sleep mode		12	12.8	13.8	V
I_{VC_ST}	Startup source current	V_{VDD} = 48 V, V_C = 0 V		1.1	1.5	2.1	mA
		V_{VDD} = 10.9 V, V_C = 8.6 V		0.9	1.3	1.8	
I_{VC_OP}	Operating current	V_{VC} = 12 V, V_{CTL} = V_B		0.9	1.8	3.0	mA
t_{ST}	Bootstrap start up time, C_{VC} = 22 µF	V_{VDD} = 48 V, measure time from V_{VC} (0) → V_{CUV}		103	155	203	ms
V_{CUV}	UVLO threshold	V_{VC} rising until V_{SRD} ↓		8.6	8.9	9.2	V
V_{CUVH}		Hysteresis		3	3.2	3.4	V
V_B (BIAS SUPPLY)							
	Output voltage	7.5 V ≤ V_{VC} ≤ 18 V, 0 ≤ I_{VB} ≤ 5 mA		4.75	5.00	5.25	V
APD (AUXILIARY POWER DETECT)							
V_{APDEN}	APD threshold voltage	V_{APD} ↑, measure with respect to ARTN		1.43	1.50	1.57	V
V_{APDH}		Hysteresis		0.28	0.30	0.32	V
	Leakage current	V_{APD} = 18 V				10	µA
RT (OSCILLATOR)							
F_{SW}	Switching frequency in PWM mode	R_T = 34.0 kΩ. Measure at GATE		226	251	276	kHz
F_{VFO}	Switching frequency in VFO mode	V_{CTL} = 1.75 V, R_T = 34.0 kΩ. Measure at GATE		105	135	165	kHz
D_{MAX}	Maximum duty cycle	V_{CTL} = V_B, Measure at GATE		75%	80%	85%	
CTL (CONTROL – PWM INPUT)							
V_{CTL_VFO}	V_{CTL} at PWM/VFO transition point	V_{SRT} = 0.5 V	V_{CTL} ↓ until V_{SRD}↑	1.90	2.00	2.10	V
			Hysteresis (1)		35		mV
		V_{SRT} = 1.0 V	V_{CTL} ↓ until V_{SRD}↑	2.15	2.25	2.35	V
			Hysteresis (1)		40.50		mV
T_{SSD}	Internal soft start delay time	V_{CTL} = 3.5 V, measure from switching start to V_{CSMAX}		1.87	3.01	5.09	ms
	Input resistance			70	105	145	kΩ
V_{ZF}	Zero frequency threshold (ZF)	V_{CTL} ↓ until GATE stops switching		1.40	1.50	1.60	V
V_{ZDC}	Zero duty cycle (ZDC) threshold (VFO disabled)	V_{SRT} = V_{ARTN}, V_{CTL} ↓ until GATE stops switching		1.55	1.75	1.95	V
	Gain, V_{CS} to V_{CTL} (1)				5.0		V/V
CS (CURRENT SENSE)							
V_{CSMAX}	Maximum threshold voltage	V_{CS}↑ until V_{GATE} ↓		0.22	0.25	0.28	V
V_{CS_VFO}	Peak V_{CS} in VFO mode	1.60 V ≤ V_{CTL} ≤ 1.90 V, V_{SRT} = 0.5 V, V_{CS} ↑ until V_{GATE}↓		40	50	60	mV
		1.85 V ≤ V_{CTL} ≤ 2.15 V, V_{SRT} = 1.0 V, V_{CS}↑ until V_{GATE} ↓		85	100	115	mV
V_{PK}	Internal slope compensation voltage, see Figure 2	D = D_{MAX}		32	40	50	mV
I_{CS_RAMP}	Ramp component of I_{CS}	D = D_{MAX}		12	16	25	µA
I_{CSDC}	DC component of I_{CS}			1	2	3	µA
D_{SLOPE_ST}	Slope compensation ramp start relative to switching period. Refer to Figure 2			30%	34%	39%	
t_1	Turn off delay	V_{CS} = 0.3 V, measure $t_{prf50–50}$, see Figure 3			50	90	ns
t_{BLNK}	Blanking period			100	150	200	ns
	Off state pulldown resistance				290	500	Ω

(1) Parameters provided for reference only, and do not constitute part of TI published specifications for purposes of TI product warranty.

Electric Characteristics - Controller Section (continued)

Unless otherwise noted, 40 V ≤ V_{DD} ≤ 57 V; V_{CTL} = V_{MODE} = V_{SLPb} = V_B; V_{SRT} = 0.5 V; V_{APD} = V_{CS} = V_{ARTN} = V_{RTN}; CLS, GATE, LED, SRD, T2P open; R_{WAKE} = 392 kΩ; R_{DEN} = 24.9 kΩ; R_T = 34 kΩ; C_{VB} = C_{VC} = 0.1 µF;
–40 ≤ T_J ≤ 125°C. Typical values are at 25°C. All voltages referred to V_{SS}.
V_C = 12 V, V_{DEN} = V_{VSS}, V_{ARTN} = V_{RTN} = V_{SS}

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GATE (GATE DRIVER)					
Peak source current	GATE high, pulsed measurement	0.35	0.60	1.00	A
Peak sink current	GATE low, pulsed measurement	0.70	1.00	1.40	A
Rise time (1)	$t_{prr10–90}$, C_{GATE} = 1 nF; see Figure 4		40		ns
Fall time (1)	$t_{pff90–10}$, C_{GATE} = 1 nF; see Figure 4		27		ns
Pull-up resistance				20	Ω
Pull-down resistance				10	Ω
SRD (SYNCHRONOUS RECTIFIER DISABLE)					
Output low voltage	I_{SRD} = 2 mA sinking		0.25	0.45	V
Leakage current	V_{CTL} = 1.75 V, V_{SRD} = 18 V			10	µA
SRT (SYNCHRONOUS RECTIFIER THRESHOLD)					
Leakage current	0 V ≤ V_{SRT} ≤ 5 V			1	µA
THERMAL SHUTDOWN					
Shutdown	T_J rising	135	145	155	°C
Hysteresis (1)			20		°C

6.7 Electrical Characteristics - Sleep Mode (TPS23752 Only)

Unless otherwise noted, 40 V ≤ V_{DD} ≤ 57 V; V_{CTL} = V_{MODE} = V_{SLPb} = V_B; V_{SRT} = 0.5 V; V_{APD} = V_{CS} = V_{ARTN} = V_{RTN}; CLS, GATE, LED, SRD, T2P open; R_{WAKE} = 392 kΩ; R_{DEN} = 24.9 kΩ; R_T = 34 kΩ; C_{VB} = C_{VC} = 0.1 µF;
–40 ≤ T_J ≤ 125°C. Typical values are at 25°C. All voltages referred to V_{SS}.
V_{DD} = 48 V, V_{APD} = V_{ARTN} = V_{RTN} = V_{VSS}, V_{VC} = 13 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SLPb						
	SLPb threshold	V_{SLPb} falling until I_{LED}↑	1.10	1.66	2.10	V
	Input pullup current		4	5.7	8	µA
MODE						
	MODE threshold	MODE falling unti I_{LED} ↑	1.10	1.66	2.10	V
	MODE hysteresis (1)			1.6		V
	Input pullup current		4	5.7	8	µA
WAKE						
	Output voltage	Sleep mode	2.43	2.50	2.57	V
R_{WKPLUP}	Pull-up resistance		3.95	5.33	6.88	kΩ
LED						
	Output low voltage	SLPb ↓, I_{LED} = 10 mA	0.60	0.90	1.50	V
	Leakage current	V_{LED} = 18 V			10	µA
SLEEP SUPPLY CURRENT						
	Sleep supply current when APD is enabled	V_{APD} = 2 V; SLPb ↓, measure I_{VDD}		0.5	1	mA
	MPS supply current	Pulsed mode: V_{MODE} = 0 V; SLPb ↓, Measure I_{VDD} 0 ≤ I_{LED} ≤ 10 mA	10.0	10.6	11.5	mApk
		DC mode: V_{MODE} = V_B, then SLPb ↓, Measure I_{VDD} 0 ≤ I_{LED} ≤ 10 mA	10.0	10.6	11.5	mA
	MPS pulsed mode duty cycle	MPS pulsed current duty cycle	28.80%	28.88%	28.95%	
		MPS pulsed current ON time	75	87.5		ms
		MPS pulsed current OFF time		215	250	ms

(1) Parameters provided for reference only, and do not constitute part of TI published specifications for purposes of TI product warranty.

6.8 Electrical Characteristics - PoE Interface Section

Unless otherwise noted, 40 V ≤ V_{DD} ≤ 57 V; V_{CTL} = V_{MODE} = V_{SLPb} = V_B; V_{SRT} = 0.5 V; V_{APD} = V_{CS} = V_{ARTN} = V_{RTN}; CLS, GATE, LED, SRD, T2P open; R_{WAKE} = 392 kΩ; R_{DEN} = 24.9 kΩ; R_T = 34 kΩ; C_{VB} = C_{VC} = 0.1 µF;
–40 ≤ T_J ≤ 125°C. Typical values are at 25°C. All voltages referred to V_{SS}.
Unless otherwise noted, V_{VC} = V_{APD} = V_{CS} = V_{ARTN} = V_{RTN}.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEN (DETECTION AND ENABLE)						
	Bias current	DEN open, I_{VDD} + I_{DEN} + I_{RTN}, V_{VDD} = 10.1 V, not in mark	3	5	12	µA
	DEN leakage current	V_{DEN} = V_{VDD} = 57 V		0.1	5	µA
	Detection current	I_{VDD} + I_{DEN} + I_{RTN}, V_{VDD} = 1.4 V	53.8	56.5	58.3	µA
		I_{VDD} + I_{DEN} + I_{RTN}, V_{VDD} = 10.1 V	395	410	417	
V_{PD_DIS}	Disable threshold	DEN falling	3	3.6	5	V
	Hysteresis		50	113	200	mV
CLS (CLASSIFICATION)						
I_{CLS}	Classification current	13 V ≤ V_{VDD} ≤ 21 V, Measure I_{VDD} + I_{DEN} + I_{RTN}				mA
		R_{CLS} = 1270 Ω	1.80	2.17	2.60	
		R_{CLS} = 243 Ω	9.90	10.60	11.20	
		R_{CLS} = 137 Ω	17.60	18.60	19.40	
		R_{CLS} = 90.9 Ω	26.50	27.90	29.30	
		R_{CLS} = 63.4 Ω	38.00	39.90	42.00	
V_{CL_ON} V_{CL_H}	Class lower threshold	V_{VDD} rising, V_{CLS} ↑	11.9	12.5	13	V
		Hysteresis	1.4	1.6	1.7	V
V_{CU_OFF} V_{CU_H}	Class upper threshold	V_{VDD} rising, V_{CLS} ↓	21	22	23	V
		Hysteresis	0.50	0.75	0.90	V
V_{MSR}	Mark reset threshold	V_{VDD} falling	3	3.9	5	V
	Mark state resistance	2-point measurement at 5 V and 10.1 V	6	9.1	12	kΩ
	Leakage current	V_{VDD} = 57 V, V_{CLS} = 0 V, measure I_{CLS}			1	µA
RTN (PASS DEVICE)						
$r_{DS(on)}$	On resistance	V_{VC} = V_{APD} = V_{ARTN} = V_{CS} = V_{VDD}	0.20	0.45	0.75	Ω
	Current limit	V_{VC} = V_{APD} = V_{ARTN} = V_{CS} = V_{VDD}, V_{RTN} =1.5 V, Measure I_{RTN}	0.85	1.00	1.20	A
	Inrush current	V_{VC} = V_{APD} = V_{ARTN} = V_{CS} = V_{DD}, V_{RTN} = 2 V, V_{DD} = 20 V → 48 V	100	140	180	mA
	Inrush termination	Percentage of inrush current	80%	90%	99%	
	Foldback threshold	V_{RTN} ↑	11.0	12.3	13.6	V
	Foldback deglitch time	V_{RTN} rising to when current limit changes to inrush current limit	500	800	1500	µs
	Input bias current	V_{VDD} = V_{RTN} = 30 V, Measure I_{RTN}			30	µA
	RTN leakage current	V_{RTN} = V_{VDD} = 100 V, V_{DEN} = V_{VSS}			50	µA
T2P (TYPE 2 PSE INDICATION)						
V_{T2P}	Output low voltage	I_{T2P} = 2 mA, after 2-event classification and softstart is complete, V_{VC} = 12 V, V_{CTL} = 3 V, V_{ARTN} = V_{VSS}		0.26	0.60	V
t_{T2P}	T2P startup delay	V_{CTL} = 3 V, V_{APD} = 2 V, Measure from switching start to V_{T2P} ↓	2	4.3	7	ms
	Leakage current	V_{T2P} = 18 V, V_{ARTN} = V_{VSS}			10	µA
PoE – PD UVLO						
V_{UVLO_R}	UVLO rising threshold		36.3	38.1	40	V
	UVLO falling threshold		30.5	32.0	33.6	
SUPPLY CURRENT						
	Operating current	Measure I_{VDD}, V_{VDD} = 48 V, 40 V ≤ V_{VDD} ≤ 57 V		210	500	µA

Electrical Characteristics - PoE Interface Section (continued)

Unless otherwise noted, 40 V ≤ V_{DD} ≤ 57 V; V_{CTL} = V_{MODE} = V_{SLPb} = V_B; V_{SRT} = 0.5 V; V_{APD} = V_{CS} = V_{ARTN} = V_{RTN}; CLS, GATE, LED, SRD, T2P open; R_{WAKE} = 392 kΩ; R_{DEN} = 24.9 kΩ; R_T = 34 kΩ; C_{VB} = C_{VC} = 0.1 µF;
–40 ≤ T_J ≤ 125°C. Typical values are at 25°C. All voltages referred to V_{SS}.
Unless otherwise noted, V_{VC} = V_{APD} = V_{CS} = V_{ARTN} = V_{RTN}.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Off-state current	ARTN and V_{VC} open, V_{VDD} = 30 V, Measure I_{VDD}			300	µA
THERMAL SHUTDOWN					
Shutdown	T_J rising	135	145	155	°C
Hysteresis (1)			20		°C

(1) Parameters provided for reference only, and do not constitute part of TI published specifications for purposes of TI product warranty.

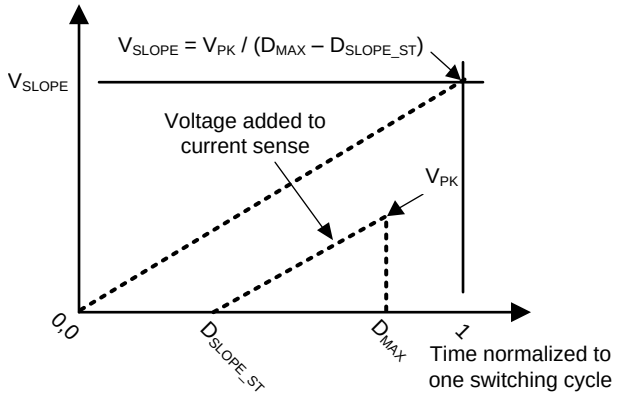


Figure 2. Current Mode Compensation Ramp

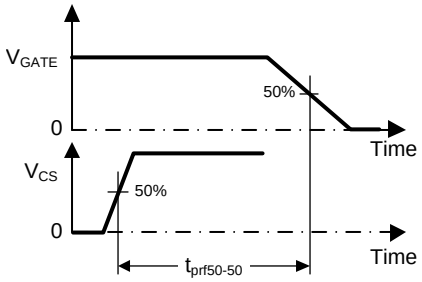


Figure 3. Time Delay from V_{CS} to V_{GATE}

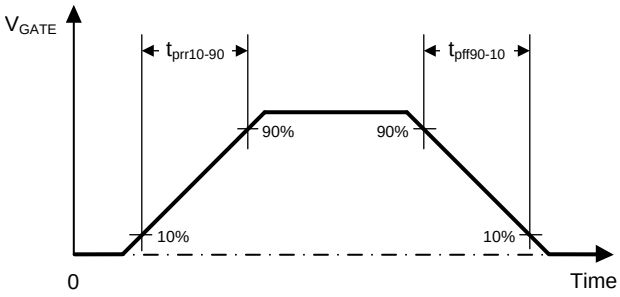


Figure 4. Rise Time and Fall Time of V_{GATE}

6.9 Typical Characteristics

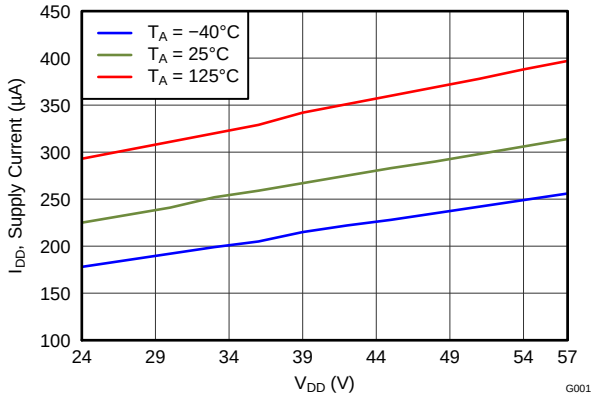


Figure 5. Supply Current vs Supply Voltage

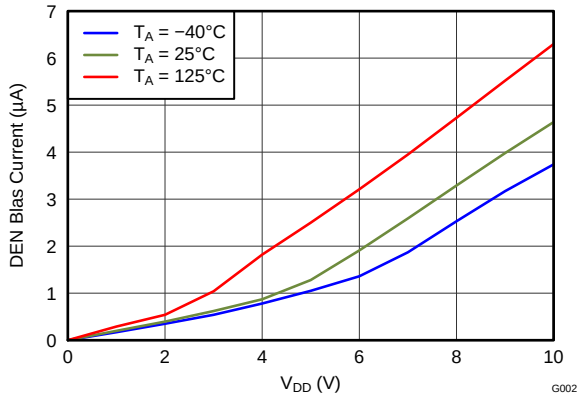


Figure 6. DEN Bias Current vs Supply Voltage

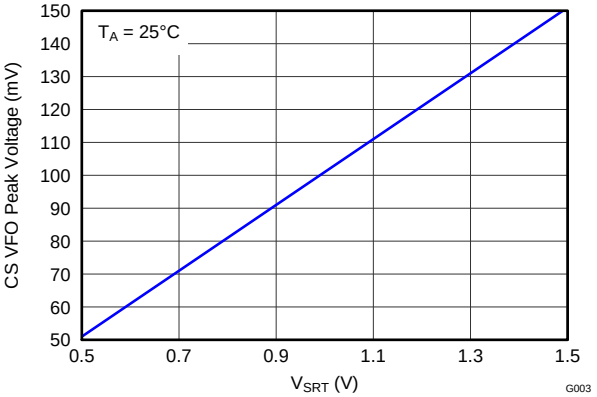


Figure 7. CS VFO Peak Voltage vs SRT Voltage

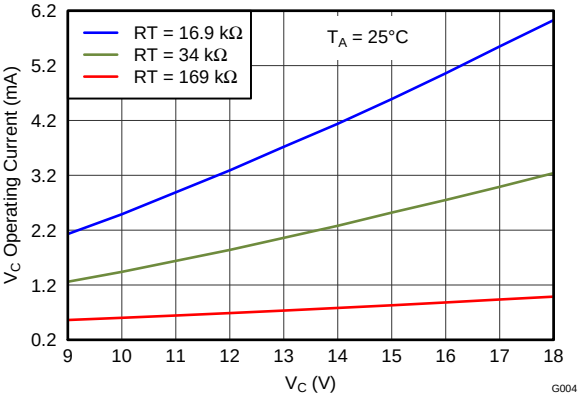


Figure 8. VC Operating Current vs VC Voltage

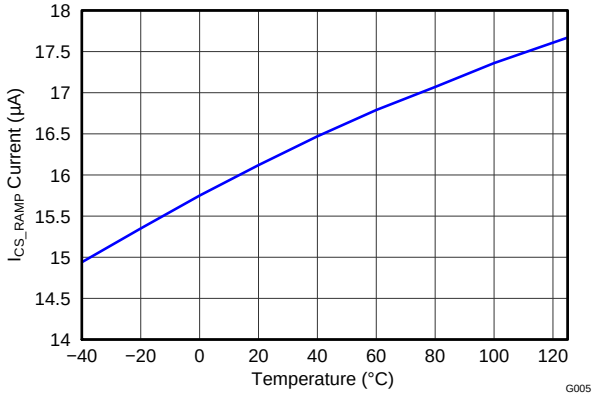


Figure 9. CS Ramp Current vs Temperature

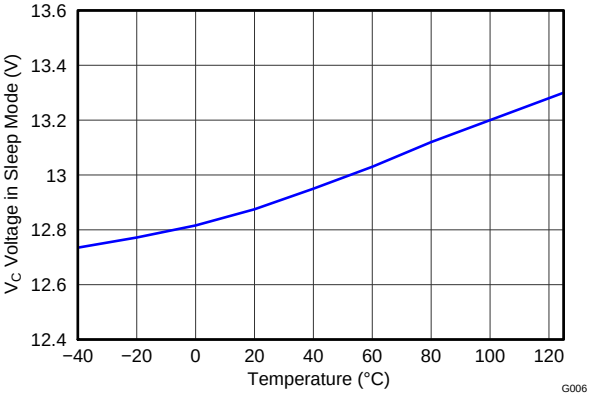


Figure 10. VC Voltage in Sleep Mode vs Temperature

Typical Characteristics (continued)

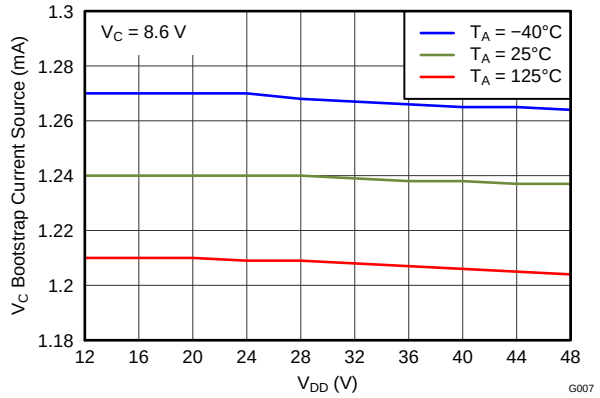


Figure 11. VC Bootstrap Current Source vs Supply Voltage

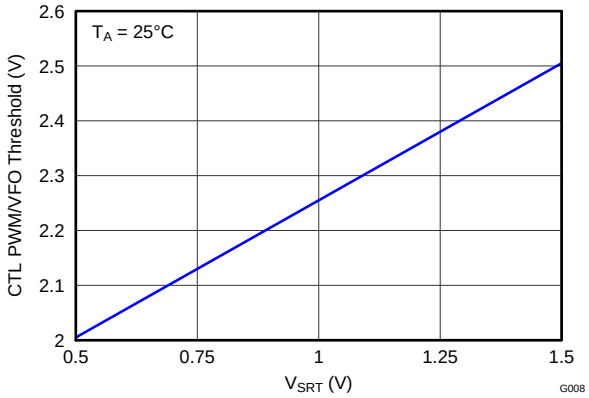


Figure 12. CTL PWM/VFO Threshold vs SRT Voltage

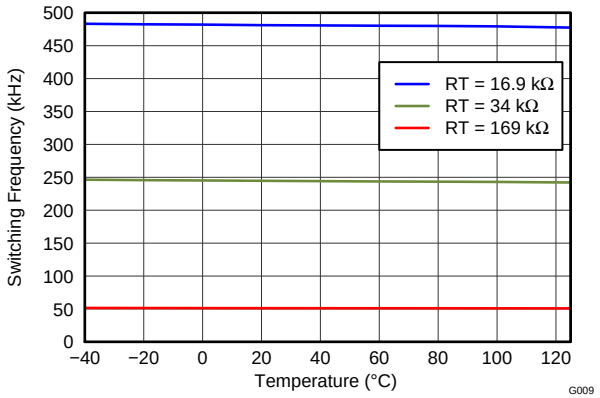


Figure 13. Switching Frequency vs Temperature

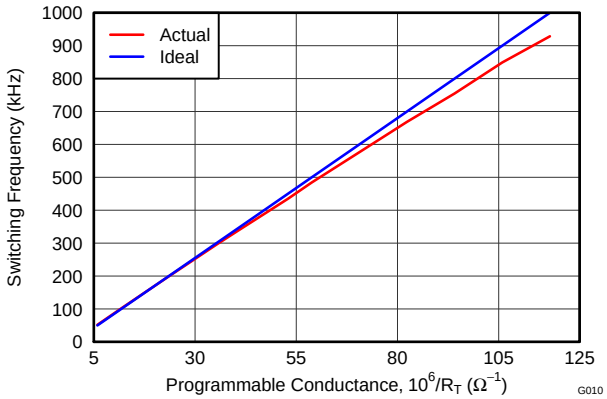


Figure 14. Switching Frequency vs Programmable Conductance

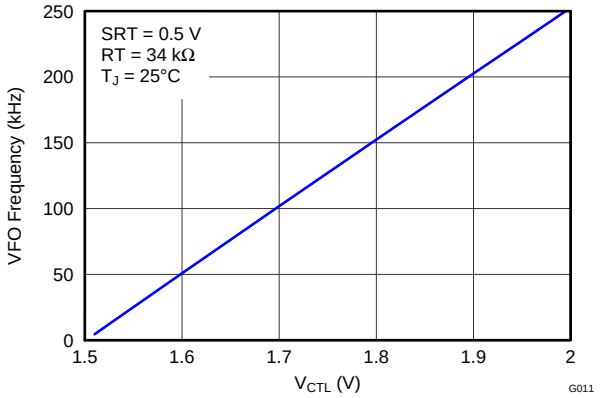


Figure 15. VFO Frequency vs CTL Voltage

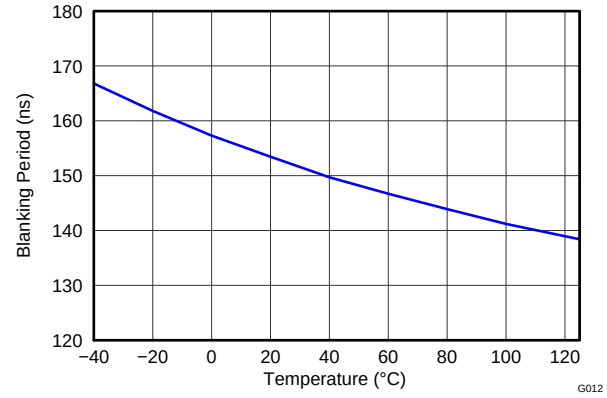


Figure 16. Blanking Period vs Temperature

Typical Characteristics (continued)

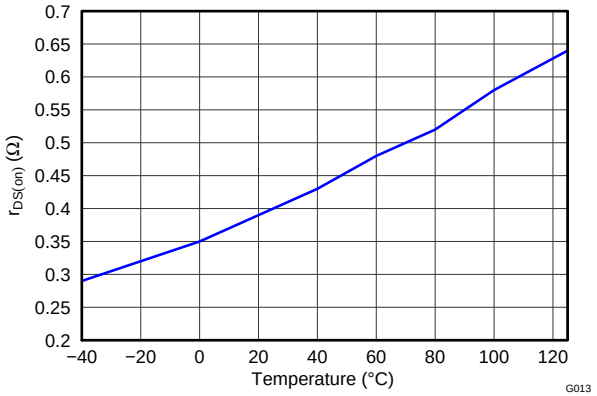


Figure 17. rDS(on) vs Temperature

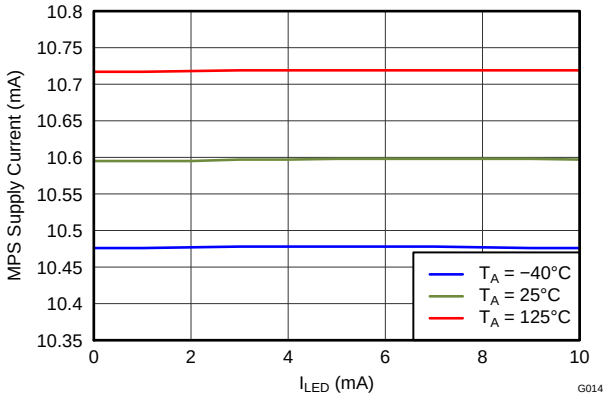


Figure 18. MPS Supply Current vs LED Current

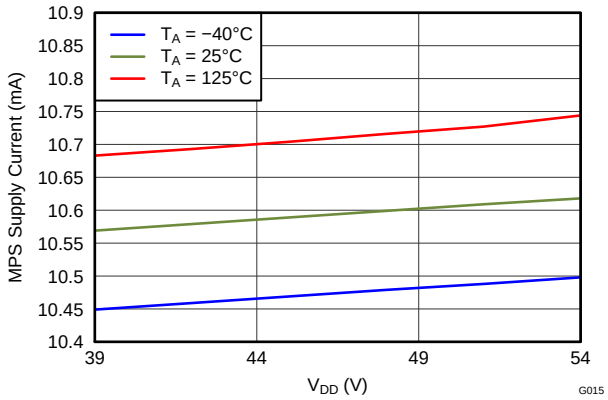


Figure 19. MPS Supply Current vs Supply Voltage

7 Detailed Description

7.1 Overview

The TPS23751 and TPS23572 devices have a PoE that contains all of the features needed to implement an IEEE802.3at type-2 powered device (PD) such as Detection, Classification, Type 2 Hardware Classification, and 140-mA inrush current mode DC-DC controller optimized specifically for isolated converters.

The TPS23751 and TPS23752 devices integrate a low 0.5-Ω internal switch to allow for up to 0.85 A of continuous current through the PD during normal operation.

The TPS23751 and TPS23752 devices contain several protection features such as thermal shutdown, current limit foldback, and a robust 100-V internal switch.

7.2 Functional Block Diagrams

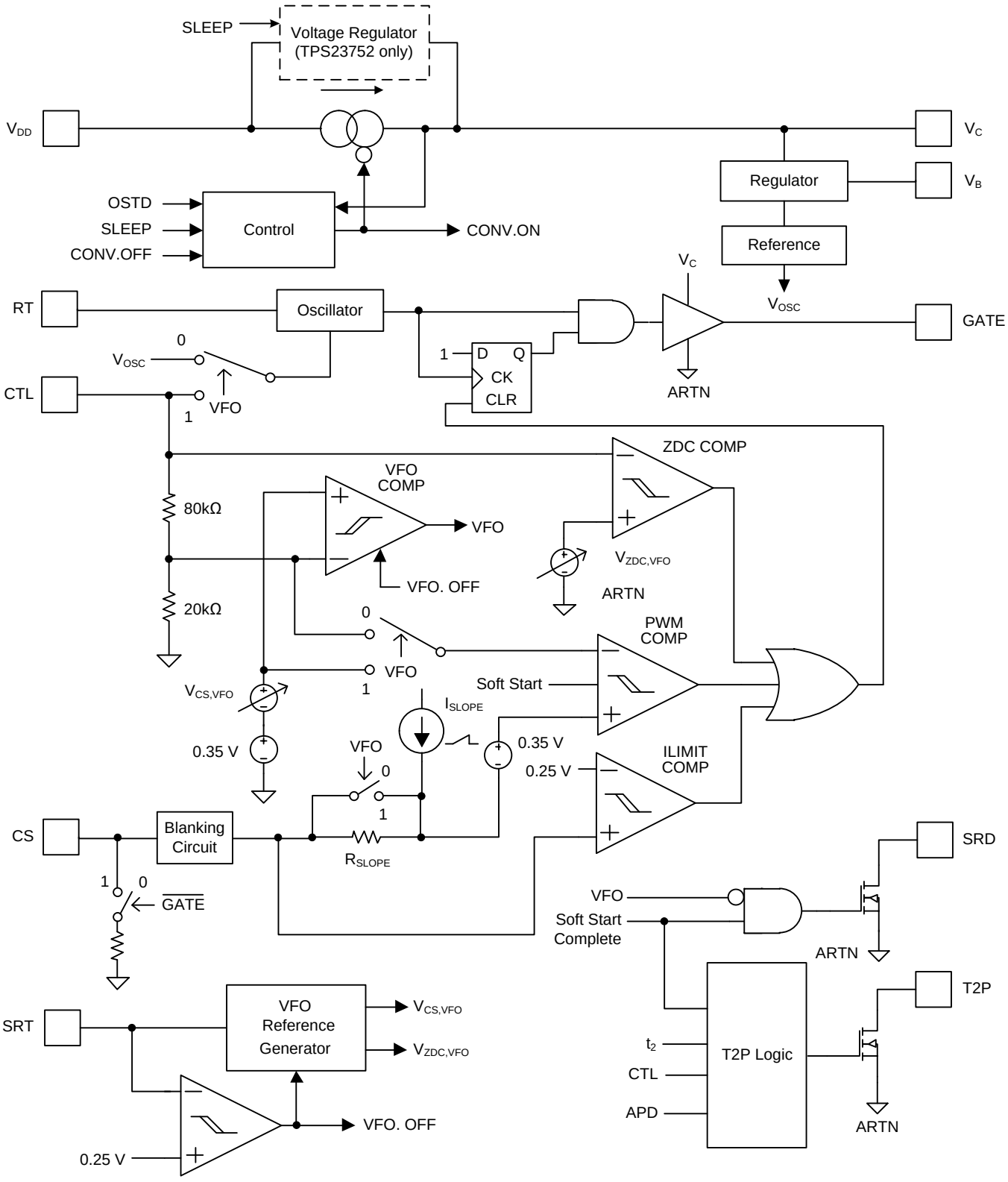


Figure 20. DC-DC Controller

Functional Block Diagrams (continued)

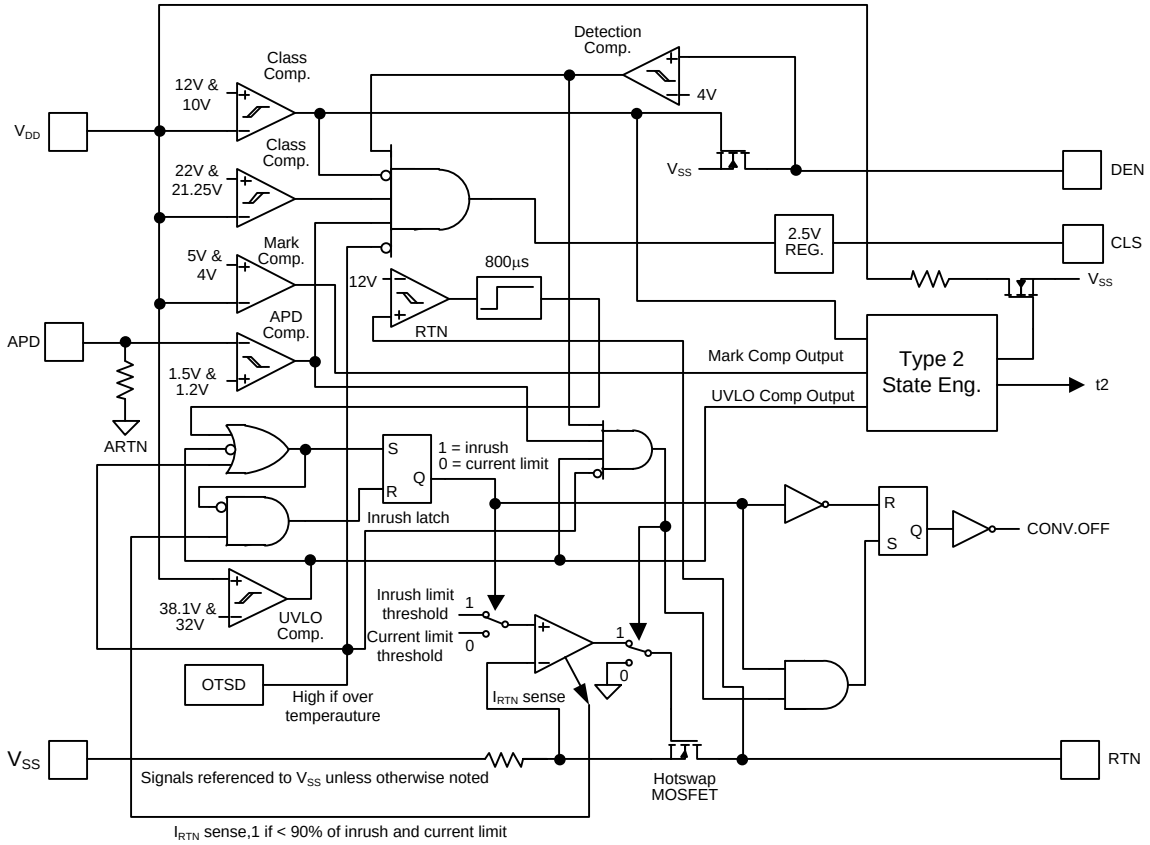


Figure 21. PoE

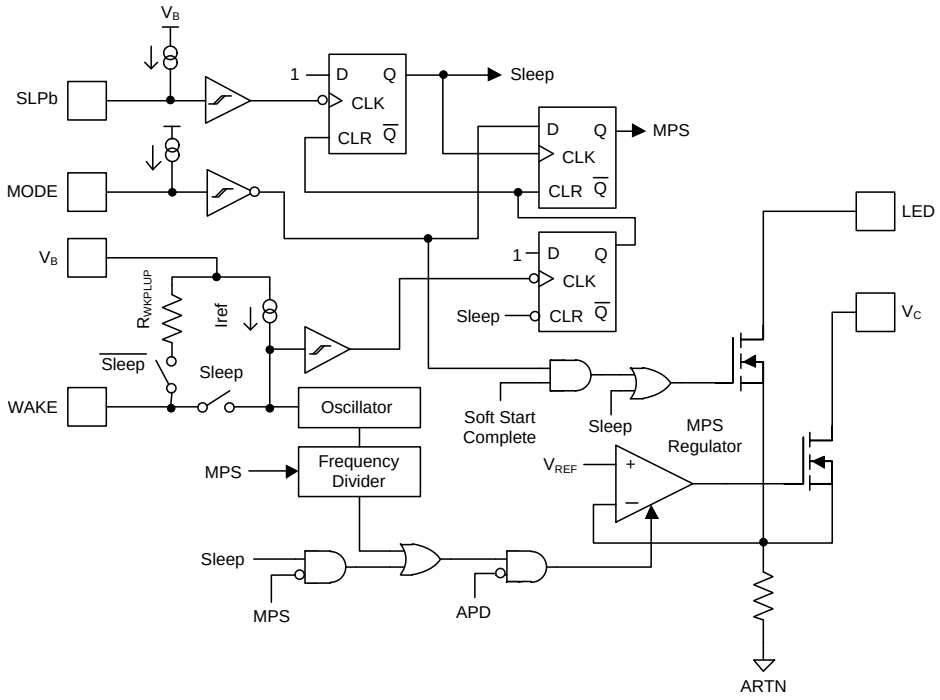


Figure 22. Sleep Mode Functionality (TPS23752 Only)

7.3 Feature Description

7.3.1 Pin Description

The following descriptions refer to the functional block diagrams.

APD: (Auxiliary Power Detect): The APD pin is used in applications that may draw power either from the Ethernet cable or from an auxiliary power source. A voltage of more than about 1.5 V on the APD pin relative to RTN turns off the internal pass MOSFET, disables the CLS output, and enables the T2P output. A resistor divider (R_{APD1} – R_{APD2} in Figure 32) provides system-level ESD protection for the APD pin, discharges leakage from the blocking diode (D_A in Figure 32), and provides input voltage supervision to ensure that switch-over to the auxiliary voltage source does not occur at excessively low voltages. If not used, connect APD to ARTN. When the TPS23752 operates in Sleep Mode, holding APD higher than its rising threshold, V_{APDEN}, disables the maintain power signature (MPS).

ARTN: The ARTN pin is the local ground return for the DC-DC controller. Connections to the ARTN pin should return to a local ground plane beneath the DC-DC converter primary circuitry. For most applications, this ground plane should also connect to RTN.

CLS: An external resistor (R_{CLS} in Figure 32) connected between the CLS pin and V_{SS} provides a classification signature to the PSE. The controller places a voltage of approximately 2.5 V across the external resistor whenever the voltage differential between V_{DD} and V_{SS} lies between about 10.9 V and 22 V. The current drawn by this resistor, combined with the internal current drain of the controller and any leakage through the internal pass MOSFET, creates the classification current. Table 1 lists the external resistor values required for each of the PD power ranges defined by IEEE802.3at. The maximum average power drawn by the PD, including all losses within the DC-DC converter as well as power supplied to the downstream load, should not exceed the maximum power indicated in Table 1. Holding APD high disables the classification signature.

High-power PSEs may perform two classification cycles if Class 4 is presented on the first cycle.

Table 1. Class Resistor Selection

CLASS	MINIMUM POWER at PD (W)	MAXIMUM POWER at PD (W)	RESISTOR R_{CLS} (Ω)
0	0.44	12.95	1270
1	0.44	3.84	243
2	3.84	6.49	137
3	6.49	12.95	90.9
4	12.95	25.5	63.4

CS (Current Sense): The CS pin serves as the current sense input for the DC-DC controller. The CS pin senses the voltage at the high side of the current sense resistor (R_{CS} in Figure 32). This voltage drives the current limit comparator and the PWM comparator (see Block Diagram of DC-DC controller). A leading-edge blanking circuit prevents MOSFET turn-on transients from falsely triggering either of these comparators. During the off time, and also during the blanking time that immediately follows, the CS pin is pulled to ARTN through an internal pulldown resistor.

The current limit comparator terminates the on-time portion of the switching cycle as soon as V_{CS} exceeds approximately 250 mV and the leading edge blanking interval has expired. If the converter is not in current limit, then either the PWM comparator or the maximum duty cycle limiting circuit terminates the on time.

An internal slope compensation circuit generates a current that imposes a voltage ramp at the positive input of the PWM comparator to suppress sub-harmonic oscillations. This current flows out of the CS pin. If desired, the magnitude of the slope compensation can be increased by the addition of an external resistor in series with the CS pin. The beginning of the slope compensation ramp is delayed to provide a smoother transition from PWM to VFO mode, as shown in Figure 2. Slope compensation, including that generated by any external resistance, is disabled in VFO mode.

CTL (Control): The CTL pin receives the control voltage from the external error amplifier. Typically this error amplifier consists of a TL431 shunt regulator driving an optocoupler, but other configurations are possible. The voltage differential between CTL and ARTN regulates power flow through the DC-DC converter. The voltage V_{CTL_VFO} set by the SRT pin represents the boundary between PWM and VFO mode. In the PWM mode of operation, the CTL voltage determines the threshold at which the PWM comparator terminates the on-time interval. During VFO mode, the inductor peak current is fixed and the CTL voltage varies the switching frequency. During PWM mode the switching frequency is fixed and the CTL voltage varies the duty cycle.

DEN (Detection and Enable): The DEN pin implements two separate functions. A resistor (R_{DEN} in *Figure 32*) connected between V_{DD} and DEN generates a detection signature whenever the voltage differential between V_{DD} and V_{SS} lies between approximately 1.4 and 10.9 V. Beyond this range, the controller disconnects this resistor to save power. For applications that wish to comply with the requirements of IEEE802.3at, the external resistance should equal 24.9 kΩ.

If the resistance connected between V_{DD} and DEN is divided into two roughly equal portions, then the application circuit can disable the PD by grounding the tap point between the two resistances. This action simultaneously spoils the detection signature and thereby signals the PSE that the PD no longer requires power.

GATE: The gate drive pin drives the main switching MOSFET of the DC-DC converter. The internal gate driver circuitry draws power from V_C and returns it to ARTN. GATE is held low whenever the converter is disabled.

LED (TPS23752 only): The LED pin drives an external status LED. Connect the LED and its series current-limiting resistor from V_C to the LED pin. While in Sleep Mode, the controller pulls the LED pin to ARTN. The LED pin is also pulled low during normal operation after the soft start is complete whenever the MODE pin is low. The LED pin should draw as little current as possible to help minimize the power consumed by the PD in Sleep Mode. If a status LED is not required, leave this pin open.

MODE (TPS23752 only): The MODE pin in combination with the SLPb pin sets the type of MPS (DC or pulsed) during Sleep Mode. Holding this pin high when the SLPb pin transitions low causes the TPS23752 to generate a DC MPS by drawing a total of 10.6 mA (typical) from the Ethernet cable. Holding this pin low when the SLPb pin transitions low causes the TPS23752 to generate a pulsed MPS. Either MPS ensures that the PSE does not disconnect power from the PD while it is asleep. An MPS is not generated if the APD pin is held high (> 1.5 V). During normal operation, pulling MODE low causes the LED pin to pull low.

RT (Timing Resistor): A timing resistor (R_T in Figure 32) connected between this pin and ARTN sets the PWM switching frequency f_{SW} according to Figure 32.

$$f_{SW} = \frac{8.5 \times 10^9\ \Omega}{R_T}\ \text{Hz} \quad (1)$$

The switching frequency remains constant during PWM operation, but decreases as V_{CTL} falls below V_{CTL_VFO}. RT is a high impedance pin. Keep the connections short and isolate them from potential noise sources.

RTN: The RTN pin provides the negative power return path for the converter. Once V_{DD} exceeds the UVLO threshold (V_{UVLO_R}), the internal pass MOSFET pulls RTN to VSS. Inrush limiting prevents the RTN current from exceeding about 140 mA until the bulk capacitance (C_{IN} in Figure 32) is fully charged. Inrush ends and the converter begins operating when the RTN current drops below about 125 mA. The RTN current is subsequently limited to about 1 A. If RTN ever exceeds about 12 V, then the controller returns to inrush limiting.

RTN should be connected to ARTN for most applications.

SLPb: (TPS23752 only): The SLPb pin controls entry into Sleep Mode. A falling-edge transition applied to this pin during normal operation initiates Sleep Mode. This mode of operation disables converter switching, increases the current limit of the internal V_C regulator, and pulls the LED output low. Cycling V_{DD} or pulling the WAKE pin low terminates the Sleep Mode and restores normal operation.

SRD (Synchronous Rectifier Disable): This open-drain output pulls to ARTN whenever the DC-DC converter is enabled, inrush and soft start are complete, and the voltage at the CTL pin exceeds the threshold V_{CTL_VFO} set by the SRT pin. A low voltage on the SRD pin signals the synchronous rectifier to begin operation. If the CTL pin voltage drops below V_{CTL_VFO}, then the SRD output goes high impedance to disable the synchronous rectifier. This action ensures that the synchronous rectifier does not operate during VFO mode.

SRT (Synchronous Rectifier Threshold): The SRT pin sets the thresholds V_{CTL_VFO} and V_{CS_VFO}, at which the DC-DC converter switches between PWM and VFO. The application circuit normally uses a resistor divider (R_{SRT1} – R_{SRT2} in Figure 32) to generate a voltage of 0.5 to 1.5 V at the SRT pin. When the voltage on the CTL pin exceeds V_{CTL_VFO}, the converter operates in PWM mode and the SRD pin is pulled low to enable the synchronous rectifier. When the voltage on CTL falls below V_{CTL_VFO}, the converter operates in VFO and the SRD pin goes high impedance to disable the synchronous rectifier. Tying SRT to ARTN disables the VFO mode.

T2P (Type-2 PSE Indicator): The controller pulls this pin to ARTN whenever type-2 hardware classification has been observed; or the APD pin is pulled high, after the internal T2P delay is complete, and $V_{CTL} \leq 4$ V. Once T2P is valid, V_{CTL} has no effect on the status of T2P. The T2P output will return to a high-impedance state if the part enters thermal shutdown, the pass MOSFET enters inrush limiting, or if a type-2 PSE was not detected and the voltage on APD drops below its threshold. The circuitry that watches for type-2 hardware classification latches its result when the $V_{(VDD-VSS)}$ voltage differential rises above the upper classification threshold. This circuit resets when the $V_{(VDD-VSS)}$ voltage differential drops below the mark threshold. The T2P pin can be left unconnected if it is not used.

V_B (Bias Voltage): The V_B pin is the output of an internal 5 V regulator fed from V_C. A ceramic bypass capacitor with a minimum capacitance of no less than 80 nF must connect from V_B to ARTN. V_B may be used to bias the feedback optocoupler. For the TPS23752, V_B may also bias pullups for SLPb and MODE.

V_C (Controller Voltage): The V_C pin connects to the auxiliary bias supply for the DC-DC controller. The MOSFET gate driver draws current directly from V_C. V_B is regulated down from V_C to provide power for the rest of the internal control circuitry. A startup current source from V_{DD} to V_C controlled by a comparator with hysteresis implements the converter bootstrap startup. V_C must receive power from an auxiliary source, such as an auxiliary winding on the flyback transformer, to sustain normal operation after startup. A low-ESR bypass capacitor, such as a ceramic capacitor, must connect from V_C to ARTN to supply the gate drive current required to drive the external switching MOSFET.

The TPS23752 regulates V_C to 12.8 V while in Sleep Mode to regulate the brightness of the Sleep-Mode LED. The Sleep Mode output voltage is high enough to drive at least three LED's in series when additional brightness is required. This reduces the required value of R_{LED} and associated power consumption for a given LED bias current.

V_{DD}: The V_{DD} pin connects to the positive side of the input supply. The V_{DD} pin provides operating power to the PD controller, allows this circuit to monitor the input line voltage, and serves as the source for DC-DC startup current. In the TPS23752, it also supplies the LED and MPS current during Sleep-Mode operation

V_{SS}: The V_{SS} pin connects to the negative rail of the input supply. It serves as a local ground for the PD control circuitry. The PowerPAD™ must connect to V_{SS} to ensure proper operation.

WAKE (TPS23752 only): The WAKE pin performs several functions. During Sleep Mode, it outputs a current-limited 2.5 V. Pushing the external pushbutton (S_{WAKE} in Figure 32) during Sleep Mode connects the WAKE pin to optocoupler, OPTO6. An internal current comparator detects this excess current drawn by OPTO6 and re-enables the DC-DC converter out of Sleep Mode. The WAKE pin now connects back to the internal pullup resistor (R_{WKPLUP} in the Sleep Mode block diagram) to provide bias current for OPTO6. The optocoupler alerts the system controller that the button has been pressed during sleep operation. Circuit board routing should protect WAKE from noise sources on the board.

7.4 Device Functional Modes

7.4.1 PoE Overview

The following text is intended as an aid in understanding the operation of the TPS23751 and TPS23752 but not as a substitute for the IEEE 802.3at standard. The IEEE 802.3at standard is an update to IEEE 802.3-2008 clause 33 (PoE), adding high-power options and enhanced classification. Generally speaking, a device compliant to IEEE 802.3-2008 is referred to as a type 1 device, and devices with high power and enhanced classification are referred to as type 2 devices. Standards change and should always be referenced when making design decisions.

Device Functional Modes (continued)

The IEEE 802.3at standard defines a method of safely powering a PD (powered device) over a cable by power sourcing equipment (PSE), and then removing power if a PD is disconnected. The process proceeds through an idle state and three operational states of detection, classification, and operation. The PSE leaves the cable unpowered (idle state) while it periodically looks to see if something has been plugged in; this operation is referred to as detection. The low power levels used during detection are unlikely to damage devices not designed for PoE. If a valid PD signature is present, the PSE may inquire how much power the PD requires; this operation is referred to as classification. The PSE may then power the PD if it has adequate capacity.

Type 2 PSEs are required to do type 1 hardware classification plus a (new) data-layer classification, or an enhanced type 2 hardware classification. Type 1 PSEs are not required to do hardware or data link layer (DLL) classification. A type 2 PD must do type 2 hardware classification as well as DLL classification. The PD may return the default, 13W current-encoded class, or one of four other choices. DLL classification occurs after power-on and the Ethernet data link has been established.

Once started, the PD must present a Maintain Power Signature (MPS) to assure the PSE that it is still present. The PSE monitors its output for a valid MPS and turns the port off if it loses the MPS. Loss of the MPS returns the PSE to the idle state. Figure 23 shows the operational states as a function of PD input voltage. The upper half is for IEEE 802.3-2008, and the lower half shows specific differences for IEEE 802.3at. The dashed lines in the lower half indicate these states are the same (e.g., Detect and Class) for both.

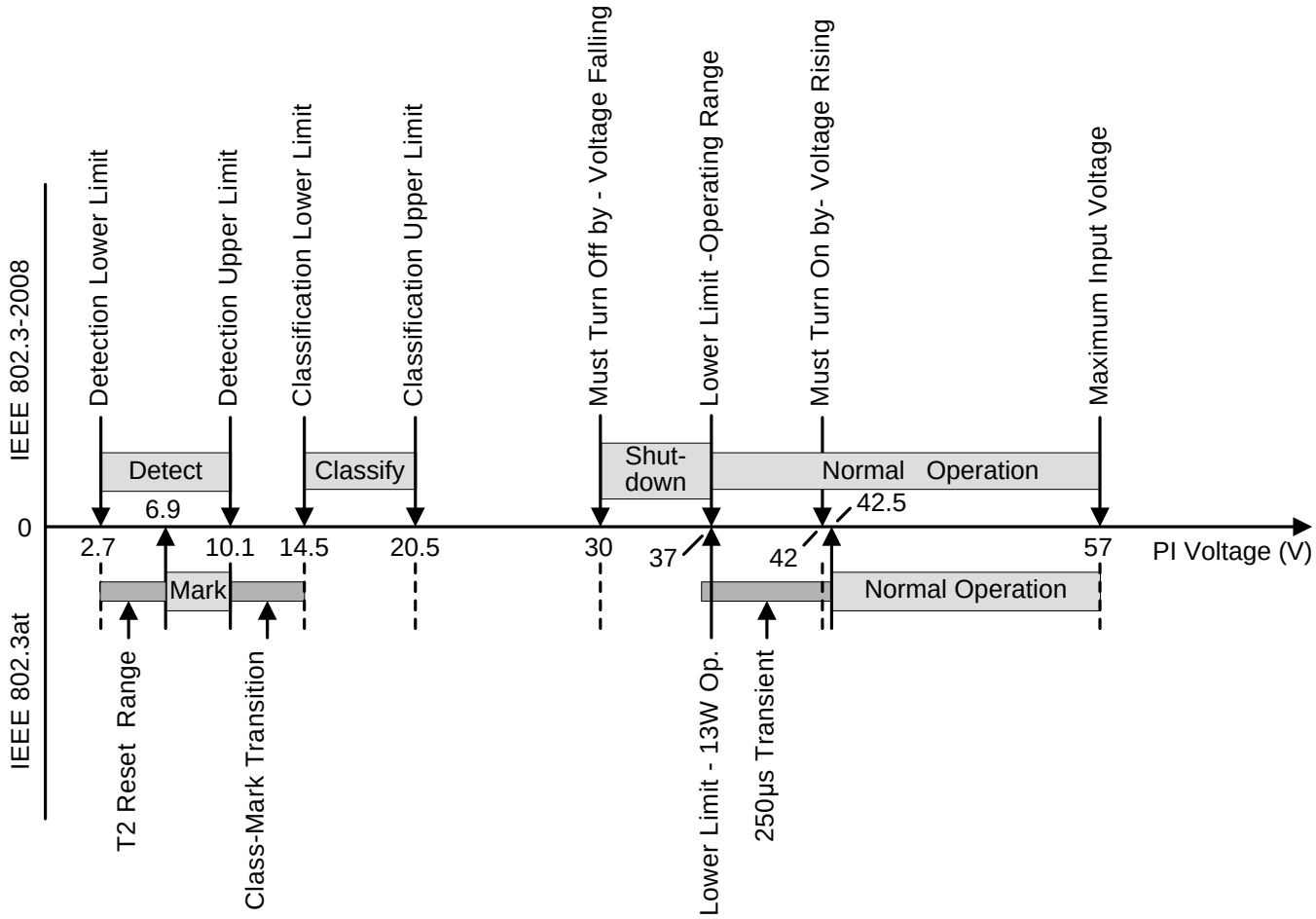


Figure 23. Threshold Voltages

Device Functional Modes (continued)

The PD input, typically an RJ-45 eight-lead connector, is referred to as the power interface (PI). PD input requirements differ from PSE output requirements to account for voltage drops and operating margin. The standard allots the maximum loss to the cable regardless of the actual installation to simplify implementation. IEEE 802.3-2008 was designed to run over infrastructure including ISO/IEC 11801 class C (CAT3 per TIA/EIA-568) that may have had AWG 26 conductors. IEEE 802.3at type 2 cabling power loss allotments and voltage drops have been adjusted for 12.5 Ω power loops per ISO/IEC11801 class D (CAT5 or higher per TIA/EIA-568, typically AWG 24 conductors). Table 2 shows key operational limits broken out for the two revisions of the standard.

Table 2. Comparison of Operational Limits

Standard	Power Loop Resistance (max)	PSE Output Power (min)	PSE Static Output Voltage (min)	PD Input Power (max)	Static PD Input Voltage	
					Power ≤ 12.95W	Power > 12.95W
IEEE802.3at-2008 802.3at (Type 1)	20 Ω	15.4W	44 V	12.95W	37 V – 57 V	N/A
802.3at (Type 2)	12.5Ω	30W	50 V	25.5W	37 V – 57 V	42.5 V – 57 V

The PSE can apply voltage either between the RX and TX pairs (pins 1 - 2 and 3 - 6 for 10baseT or 100baseT), or between the two spare pairs (4 - 5 and 7 - 8). Power application to the same pin combinations in 1000baseT systems is recognized in IEEE 802.3at. 1000baseT systems can handle data on all pairs, eliminating the spare pair terminology. The PSE may only apply voltage to one set of pairs at a time. The PD uses input diode bridges to accept power from any of the possible PSE configurations. The voltage drops associated with the input bridges create a difference between the standard limits at the PI and the TPS23751 and TPS23752 specifications.

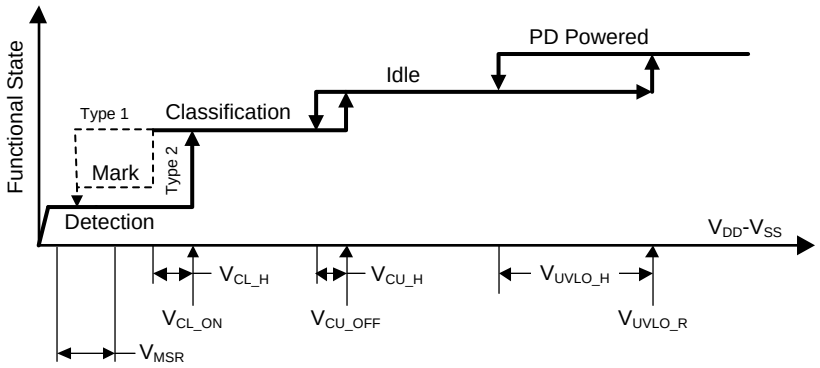
A compliant type 2 PD has power management requirements not present with a type 1 PD. These requirements include the following:

1. Must interpret type 2 hardware classification,
2. Must present hardware class 4,
3. Must implement DLL negotiation,
4. Must behave like a type 1 PD during inrush and startup,
5. Must not draw more than 13W for 80ms after the PSE applies operating voltage (power-up),
6. Must not draw more than 13W if it has not received a type 2 hardware classification or received permission through DLL,
7. Must meet various operating and transient templates, and
8. Optionally monitor for the presence or absence of an adapter (assume high power).

As a result of these requirements, the PD must be able to dynamically control its loading, and monitor T2P for changes. In cases where the design needs to know specifically if an adapter is plugged in and operational, the adapter should be individually monitored, typically with an optocoupler.

7.4.1.1 Threshold Voltages

The TPS23751 and TPS23752 have a number of internal comparators with hysteresis for stable switching between the various states. Figure 24 relates the parameters in the Electrical Characteristics section to the PoE states. The mode labeled Idle between Classification and Operation implies that the DEN, CLS, and RTN pins are all high impedance. The state labeled Mark, which is drawn in dashed lines, is part of the new type 2 hardware class state machine.



NOTE: Variable names refer to Electrical Characteristic table parameters

Figure 24. Threshold Voltages

7.4.1.2 PoE Startup Sequence

The waveforms of Figure 25 demonstrate detection, classification, and startup from a PSE with type 2 hardware classification. The key waveforms shown are $V_{(VDD-VSS)}$, $V_{(RTN-VSS)}$, and I_{PI}. IEEE 802.3at requires a minimum of two detection levels, two class and mark cycles, and startup from the second mark event. V_{RTN} to V_{SS} falls as the TPS23751 or TPS23752 charges C_{IN} following application of full voltage. Subsequently, the converter starts up, drawing current as seen in the I_{PI} waveform.

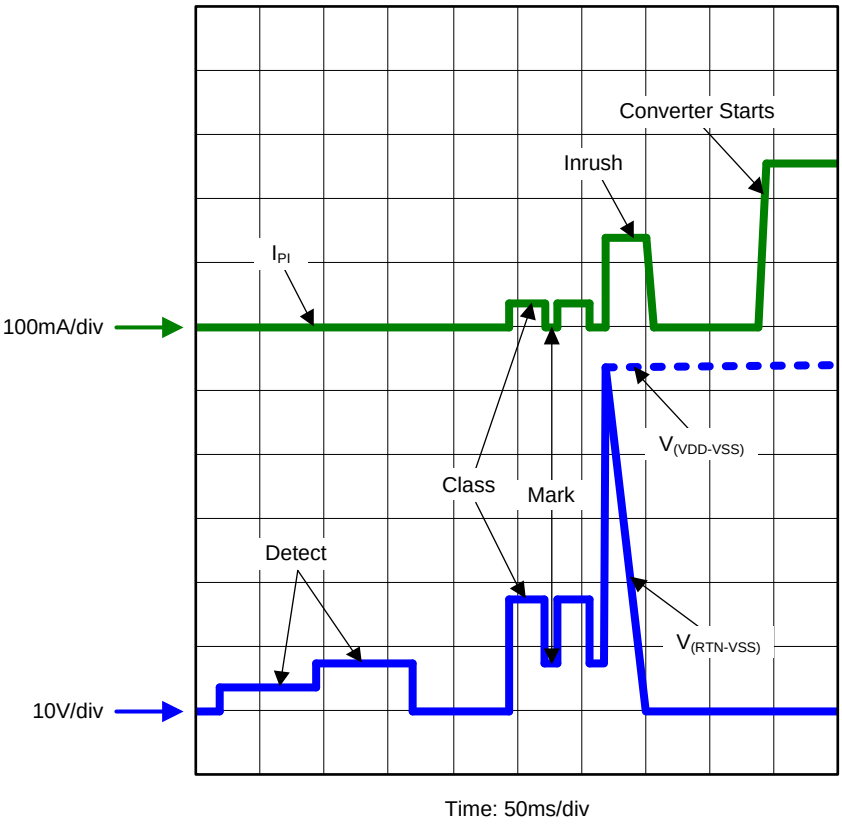


Figure 25. Startup

7.4.1.3 Detection

The TPS23751 or TPS23752 pulls DEN to V_{SS} whenever $V_{(VDD-VSS)}$ is below the lower classification threshold. When the input voltage rises above V_{CL-ON}, the DEN pin goes to an open-drain condition to conserve power. While in detection, RTN is high impedance, and almost all the internal circuits are disabled. An R_{DEN} of 24.9 kΩ (±1%), presents the correct signature. It may be a small, low-power resistor since it only sees a stress of about 5 mW. A valid PD detection signature is an incremental resistance ($\Delta V/\Delta I$) between 23.75 kΩ and 26.25 kΩ at the PI.

The detection resistance seen by the PSE at the PI is the result of the input bridge resistance in series with the parallel combination of R_{DEN} and internal V_{DD} loading. The incremental resistance of the input diode bridge may be hundreds of ohms at the very low currents drawn when 2.7 V is applied to the PI. The input bridge resistance is partially compensated by the TPS23751 or TPS23752 effective resistance during detection.

The type 2 hardware classification protocol of IEEE 802.3at specifies that a type 2 PSE drops its output voltage into the detection range during the classification sequence. The PD is required to have an incorrect detection signature in this condition, which is referred to as a mark event (see Figure 25). After the first mark event, the TPS23751 or TPS23752 presents a signature less than 12 kΩ until it has experienced a $V_{(VDD-VSS)}$ voltage below the mark reset threshold (V_{MSR}). This operation is explained more fully in the Hardware Classification section.

7.4.1.4 Hardware Classification

Hardware classification allows a PSE to determine the power requirements of a PD before powering, and helps with power management once power is applied. Type 2 hardware classification permits high power PSEs and PDs to determine whether the connected device can support high-power operation. A type 2 PD presents class 4 in hardware to indicate that it is a high-power device. A type 1 PSE treats a class 4 device like a class 0 device, allotting 13 W if it chooses to power the PD. A PD that receives a 2-event class understands that it is powered from a high-power PSE and it may draw up to 25.5 W immediately after the 80 ms startup period completes. A type 2 PD that does not receive a 2-event hardware classification may choose to not start, or must start in a 13 W condition and request more power through the DLL after startup. The standard requires a type 2 PD to indicate that it is underpowered if this occurs. Startup of a high-power PD under 13 W implicitly requires some form of powering down sections of the application circuits.

The maximum power entries in Table 1 determine the class the PD must advertise. The PSE may disconnect a PD if it draws more than its stated Class power, which may be the hardware class or a lower DLL-derived power level. The standard permits the PD to draw limited current peaks that increase the instantaneous power above the Table 1 limit, however the average power requirement always applies.

The TPS23751 and TPS23752 implement two-event classification. Selecting an R_{CLS} of 63.4 Ω provides a valid type 2 signature. A TPS23751 or TPS23752 may be used as a compatible type 1 device simply by programming class 0–3 per Table 1. DLL communication is implemented by the Ethernet communication system in the PD and is not implemented by the TPS23751 or TPS23752.

The TPS23751 and TPS23752 disable classification above V_{CU_OFF} to avoid excessive power dissipation. CLS voltage is turned off during PD thermal limiting or when DEN is active. The CLS output is inherently current limited, but should not be shorted to V_{SS} for long periods of time.

Figure 26 shows how classification works for the TPS23751 and TPS23752. Transition from state-to-state occurs when comparator thresholds are crossed (see Figure 23 and Figure 24). These comparators have hysteresis, which adds inherent memory to the machine. Operation begins at idle (unpowered by PSE) and proceeds with increasing voltage from left to right. A 2-event classification follows the (heavy lined) path towards the bottom, ending up with a latched type 2 decode along the lower branch that is highlighted. This state results in a low T2P during normal operation. Once the valid path to type 2 PSE detection is broken, the input voltage must transition below the mark reset threshold to start anew.

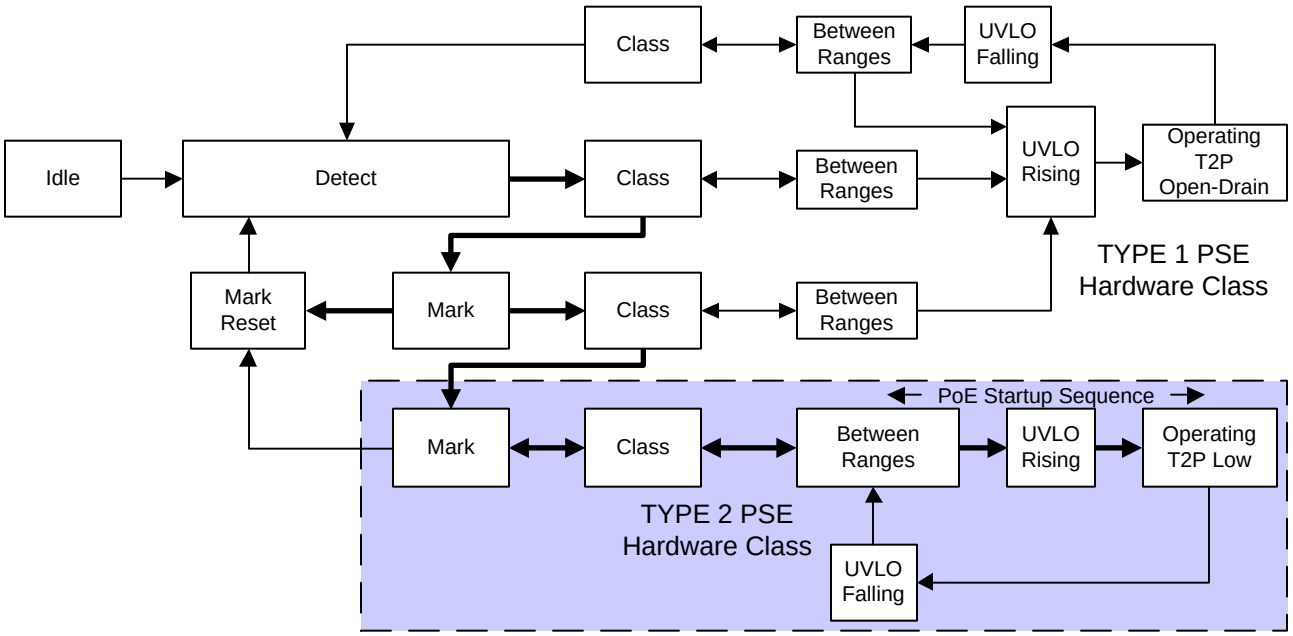


Figure 26. Two-Event Class Internal States

7.4.1.5 Inrush and Startup

IEEE 802.3at has a startup current and time limitation, providing type 2 PSE compatibility for type 1 PDs. A type 2 PSE limits output current to between 400 mA and 450 mA for up to 75 ms after power-up (applying “48 V” to the PI) in order to mirror type 1 PSE functionality. The type 2 PSE supports higher output current after 75 ms. The TPS23751 and TPS23752 implement a 140 mA inrush current, which is compatible with all PSE types. A high-power PD must limit its converter startup peak current. The operational current cannot exceed 400 mA for a period of 80 ms or longer. The TPS23751 and TPS23752 internal soft-start permits control of the converter startup, however the application circuits must assure that their power draw does not cause the PD to exceed the current and time limitation. This requirement implicitly requires some form of powering down sections of the application circuits. T2P becomes valid within t_{T2P} after switching starts, or if an adapter is plugged in while the PD is operating from a PSE.

7.4.1.6 Maintain Power Signature

The MPS is an electrical signature presented by the PD to assure the PSE that it is still present after operating voltage is applied. A valid MPS consists of a minimum dc current of 10 mA (or a 10 mA pulsed current for at least 75 ms every 325 ms) and an ac impedance lower than 26.3 kΩ in parallel with 0.05 µF. The ac impedance is usually accomplished by the minimum operating C_{IN} requirement of 5 µF. When DEN is used to force the hotswap switch off, the dc MPS is not met. A PSE that monitors the dc MPS removes power from the PD when this occurs. A PSE that monitors only the ac MPS may remove power from the PD. Additional TPS23752 MPS features are supported as described in the Sleep Mode section.

7.4.1.7 Startup and Converter Operation

The internal PoE UVLO (Under Voltage Lock Out) circuit holds the hotswap switch off before the PSE provides full voltage to the PD. This prevents the converter circuits from loading the PoE input during detection and classification. The converter circuits discharge C_{IN}, C_{vc}, and C_{vb} while the PD is unpowered. Thus $V_{(VDD-RTN)}$ is a small voltage just after applying full voltage to the PD, as seen in Figure 25. The PSE drives the PI voltage to the operating range once the PSE has decided to power up the PD. When V_{VDD} rises above the UVLO turn-on threshold (V_{UVLO-R}, approximately 38 V) with RTN high, the TPS23751 and TPS23752 enable the hotswap MOSFET with approximately 140 mA (inrush) current limit as seen in Figure 27. Converter switching is disabled while C_{IN} charges and V_{RTN} falls from V_{VDD} to nearly V_{VSS}, however the converter startup circuit is allowed to charge C_{VC} (the bootstrap startup capacitor). Converter switching is allowed if the PD is not in inrush, OTSD is not active, and the V_C UVLO permits it. Once the inrush current falls about 10% below the inrush current limit, the PD current limit switches to the operational level (approximately 1000 mA). Continuing the startup sequence

shown in Figure 27, V_{VC} continues to rise until the startup threshold (V_{CUV} approximately 8.9 V) is exceeded, turning the startup source off and enabling switching. The V_B regulator is always active, powering the internal converter circuits as V_{VC} rises. There is a slight delay between the removal of charge current and the start of switching as the softstart ramp sweeps above the V_{ZDC} threshold. V_{VC} falls as it powers both the internal circuits and the switching MOSFET gates. If the converter control bias output rises to support V_{VC} before it falls to V_{CUV} – V_{CUVH} (approximately 5.7 V), a successful startup occurs. In Figure 27, T2P is active if a type 2 PSE is plugged in.

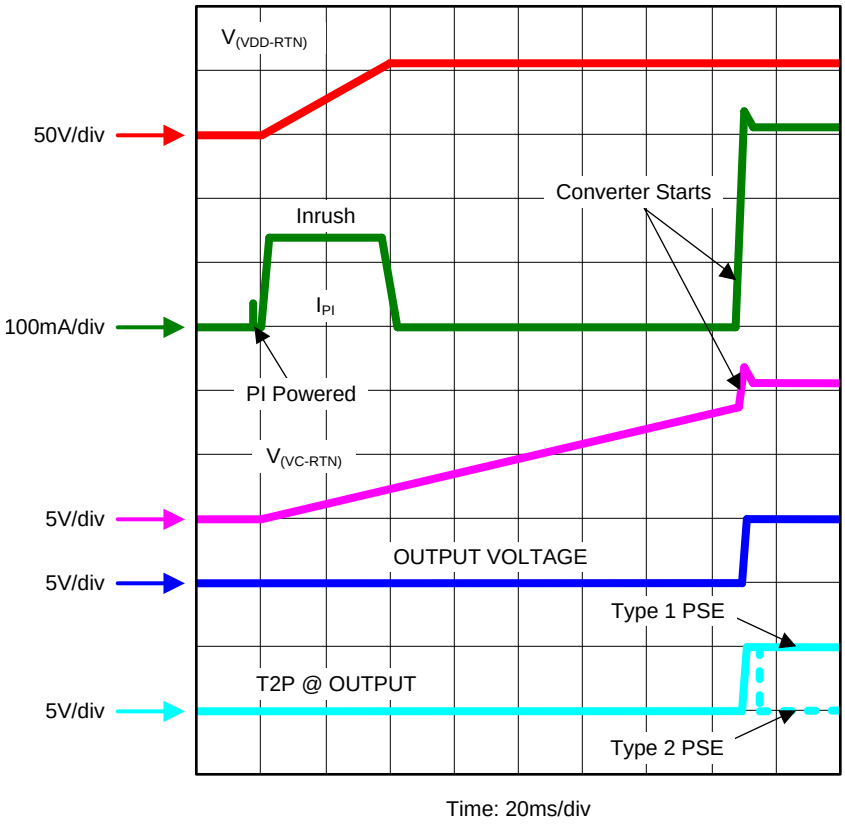


Figure 27. Power Up and Start

If V_{VDD}- V_{VSS} drops below the lower PoE UVLO (V_{UVLO-R} - V_{UVLO-H}, approximately 32 V), the hotswap MOSFET is turned off, but the converter still runs. The converter stops if V_{VC} falls below the converter UVLO (V_{CUV} – V_{CUVH}, approximately 5.7 V), the hotswap is in inrush current limit, 0% duty cycle is demanded by V_{CTL} (V_{CTL} < V_{ZDC}, approximately 1.75 V), or the converter is in thermal shutdown.

7.4.1.8 PD Hotswap Operation

IEEE 802.3at has taken a new approach to PSE output limiting. A type 2 PSE must meet an output current versus time template with specified minimum and maximum sourcing boundaries. The peak output current may be as high as 50 A for 10 µs or 1.75 A for 75 ms. This makes robust protection of the PD device even more important than it was in IEEE 802.3-2008.

The internal hotswap MOSFET is protected against output faults and input voltage steps with a current limit and deglitched (time-delay filtered) foldback. An overload on the pass MOSFET engages the current limit, with V_{RTN}-V_{VSS} rising as a result. If V_{RTN} rises above approximately 12 V for longer than approximately 800 µs, the current limit reverts to the inrush value, and turns the converter off. The 800 µs deglitch feature prevents momentary transients from causing a PD reset, provided that recovery lies within the bounds of the hotswap and PSE protection. Figure 28 shows an example of recovery from a 16 V PSE rising voltage step. The hotswap MOSFET goes into current limit, overshooting to a relatively low current, recovers to approximately 1000 mA full current limit and charges the input capacitor while the converter continues to run. The MOSFET did not go into foldback because V_{RTN}-V_{VSS} was below 12 V after the 800 µs deglitch.

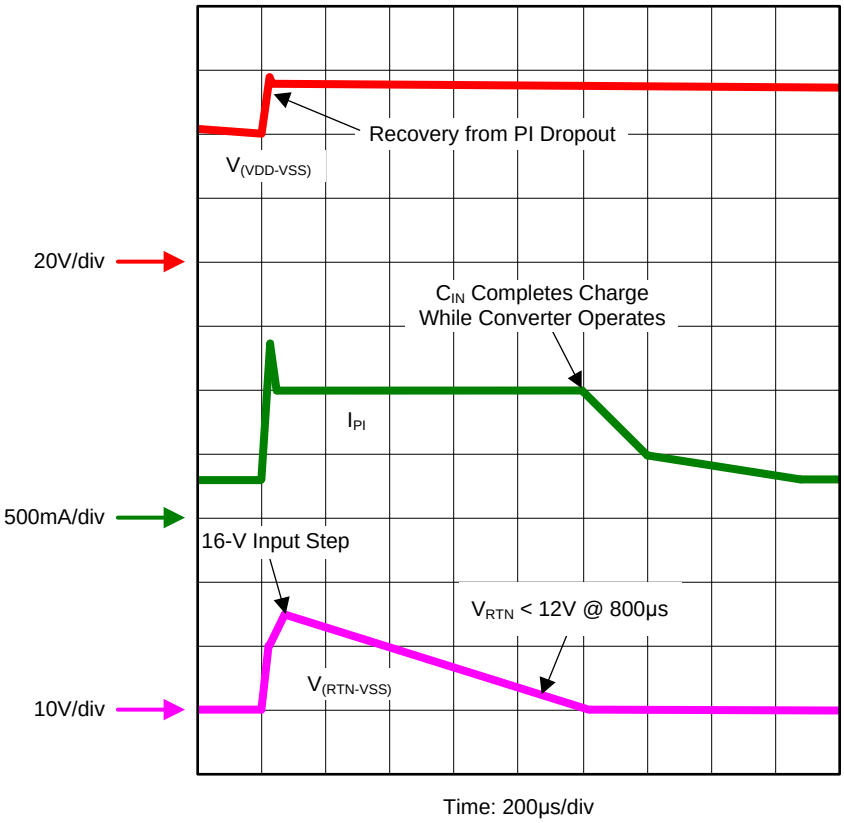


Figure 28. Response to Output Short Circuit

The PD control has a thermal sensor that protects the internal hotswap MOSFET. Conditions like startup or operation into a V_{DD}-to-RTN short cause high power dissipation in the MOSFET. An over-temperature shutdown (OTSD) turns off the hotswap MOSFET and class regulator, which are restarted after the device cools. The hotswap MOSFET is re-enabled with the inrush current limit when exiting from an over-temperature event.

Pulling DEN to V_{SS} during powered operation causes the internal hotswap MOSFET to turn off. The hotswap switch is forced off under the following conditions:

1. V_{APD} above V_{APDEN} (approximately 1.5 V)
2. $V_{(DEN\ –VSS)} < V_{PD\_DIS}$ when $V_{VDD–}$ V_{VSS} is in the operational range,
3. PD OTSD is active, or
4. $V_{(DEN\ –VSS)}$ < PoE UVLO falling threshold (approximately 32 V).

7.4.2 Sleep Mode Operation (TPS23752 only)

These features implement a Sleep Mode, permitting power savings at night (or some other system-driven criteria) by turning the active load circuits off while maintaining enough functionality for the PD to respond to a local power-up request.

The Sleep Mode is initiated by command of a local device controller (microprocessor) when the SLPb input is driven low. Sleep Mode is latched by this event, the converter is disabled, V_{DD} regulates V_C to 12.8 V, and the LED output is active. The LED output sinks current to light an LED biased from the V_C pin with R_{LED} as shown in Figure 32. LED can alert a local user that Sleep Mode is active. The TPS23752 signals the PSE that it wants to remain powered during sleep by drawing enough current to satisfy the IEEE 802.3at DC MPS requirements. If MODE was low when SLPb fell, a pulsed V_{DD} current-draw scheme is implemented; otherwise a DC current is drawn. The input current consists of the TPS23752 bias currents and the LED sink current, assuming no additional loading on V_C or V_B. The MPS current draw is inhibited when APD is active. A local pushbutton switch

(S_{WAKE} in Figure 32) is monitored by the WAKE pin and the latched sleep state exits when the button is pressed. The button is connected to ARTN through an optocoupler LED (OPTO6 in Figure 32) that alerts the device controller the button was pushed during normal operation. The MODE pin also has a second function, serving to activate the LED output when driven low during normal converter operation. For more information regarding the TPS23752 Sleep Mode Feature, see *TPS23752 Maintain Power Signature Operation In Sleep Mode* (SLVA588).

7.4.2.1 Converter Controller Features

The TPS23751 and TPS23752 DC-DC controller implements typical current-mode control as well as variable frequency operation for light load efficiency optimization as shown in the Functional Block Diagram. Features include programmable oscillator, over-current, PWM, VFO, and ZDC comparators, current-sense blanker, softstart, and gate driver. In addition, an internal slope-compensation ramp generator, thermal shutdown, and startup current source with control are provided.

The TPS23751 and TPS23752 are targeted at high efficiency, current mode, synchronous, flyback converters incorporating an external error amplifier. In PWM mode, the external error amplifier and optocoupler drives the CTL pin to demand current from the PWM. The internal current sense to control (CS to CTL pin) gain is 5 V/V. VFO mode can be enabled using a voltage divider on the SRT pin. The TPS23751 and TPS23752 enter VFO mode when V_{CTL} falls below $V_{SRT}/2 + 1.75$ V.

7.4.2.2 PWM and VFO Operation; CTL, SRT, and SRD Pin Relationships to Output Load Current

As the TPS23751 and TPS23752 transition from PWM to VFO mode with decreasing output load current, several things happen to help reduce the light load losses of the DC-DC converter. A summary is shown in Table 3.

Table 3. Comparison of PWM and VFO Modes

MODE	SWITCHING FREQUENCY	INDUCTOR Peak CURRENT	SYNCHRONOUS RECTIFIER (control with SRD pin)	INTERNAL SLOPE COMPENSATION
PWM	Constant; set by R_T	Variable, set by V_{CTL}	Enabled (SRD = LOW)	Enabled
VFO	Variable; set by V_{CTL}	Constant, clamped by V_{SRT}	Disabled (SRD = OPEN)	Disabled

The state of the SRD pin depends on the internal operating mode (PWM or VFO) and is used to enable or disable the synchronous rectifier. In addition to disabling the synchronous rectifier, the TPS23751 and TPS23752 reduce the switching frequency in VFO mode to maintain output regulation.

Synchronous rectification provides an efficiency advantage over a standard diode rectifier at medium to heavy loads, but not at lighter loads. The SRD feature can provide a means to recover the light load losses by disabling the synchronous rectifier and allowing the standard diode rectifier to take over as illustrated in Figure 29 by the VFO/PWM mode efficiency curve.

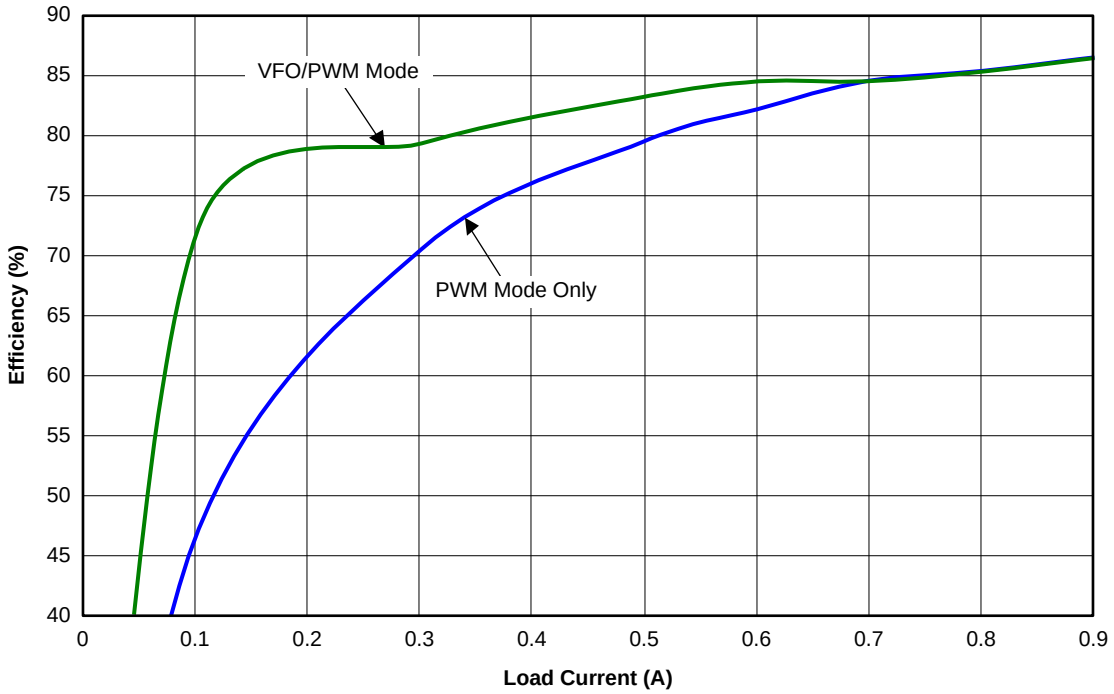


Figure 29. TPS23751 and TPS23752 Light Load Efficiency versus Mode

Figure 30 illustrates operation through the VFO to PWM to VFO transitions. As load current increases, so does V_{CTL}. When V_{CTL} exceeds the rising threshold, the TPS23751 and TPS23752 transition from VFO to PWM mode, and SRD goes low. The converter now operates with fixed frequency and current demand set by V_{CTL}. As load current decreases, so does V_{CTL}. When V_{CTL} decays below the falling threshold, the TPS23751 and TPS23752 transition from PWM to VFO mode, and SRD goes high. The converter now operates with variable frequency set by V_{CTL}, and fixed current demand set by V_{SRT}.

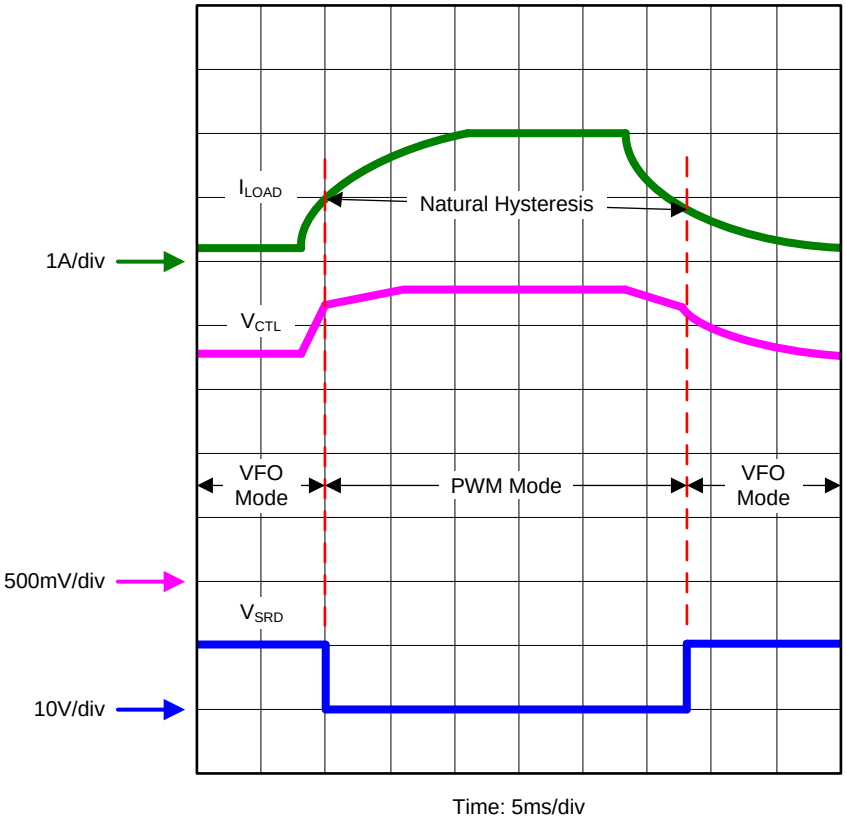


Figure 30. Converter Mode Transition

There is a natural load current hysteresis for I_{LOAD} which can be seen in Figure 30 between the transition points. For increasing I_{LOAD}, the transition current is slightly higher than for decreasing I_{LOAD}. This condition is due partially to CTL pin hysteresis (approximately 35mV) and partially due to CTL pin operating point versus mode. V_{CTL} is slightly higher in PWM mode than in VFO mode for given output load at or near the transition point.

7.4.2.3 Bootstrap Topology

The internal startup current source (I_{VC_ST}) and control logic implement a bootstrap-type startup as discussed in the Startup and Converter Operation section. The startup current source charges C_{VC} from V_{DD} when the converter is disabled (either by the PD control or the V_C control) to store enough energy to start the converter. Steady-state operating power must come from a converter (bias winding) output or other source. Loading on V_C and V_B must be minimal while C_{VC} charges, otherwise the converter may never start. The optocoupler does not load V_B when the converter is off for most situations, however care should be taken in ORing topologies where the output is powered when PoE is off.

The converter shuts off when V_C falls below its lower UVLO. This can happen when power is removed from the PD, or during a fault on a converter output rail. When one output is shorted, all the output voltages fall including the one that powers V_C. The control circuit discharges V_C until it hits the lower UVLO and turns off. A restart is initiated as described in the *Startup and Converter Operation* section if the converter turns off and there is sufficient V_{DD} voltage. This type of operation is sometimes referred to as *hiccup mode* which provides robust output short protection by providing time-average heating reduction of the output rectifier.

Below V_{CUV}, the bootstrap control logic disables most of the converter controller circuits except the V_B regulator and internal reference. GATE is low when the converter is disabled.

The bootstrap source provides reliable startup from widely varying input voltages, and eliminates the continual power loss of external resistors. The startup current source does not charge above the maximum recommended V_{VC} if the converter is disabled and there is sufficient V_{DD} to charge higher.

7.4.2.4 Current Slope Compensation and Current Limit

Current-mode control requires addition of a compensation ramp to the sensed inductive (transformer or inductor) current for stability at duty cycles near and over 50%. The TPS23751 and TPS23752 have a maximum duty cycle limit of 80%, permitting the design of wide input-range converters with lower voltage stress on the output rectifiers. While the maximum duty cycle is 80%, converters may be designed that run at duty cycles well below this for a narrower, 36 V to 57 V PI range. The TPS23751 and TPS23752 provide fixed internal slope compensation which suffices for most applications.

The TPS23751 and TPS23752 provide internal, frequency independent, slope compensation (V_{PK} = 40 mV at D_{MAX}) starting from D_{SLOPE_ST} to the PWM comparator input for current-mode control-loop stability. This voltage is not applied to the current-limit comparator whose threshold is 0.25 V (V_{CSMAX}). If the provided slope is not sufficient, the effective slope may be increased by addition of R_S per Figure 33. The additional slope voltage is provided by ($I_{CS\_RAMP} \times R_S$). There is also a small dc offset caused by the I_{CSDC} (approximately 2.0 μA) current. The peak current limit does not have duty cycle dependency unless R_S is used which is easier designing the current limit to a fixed value. See the *Current Slope Compensation* section for more information.

The internal comparators monitoring CS are isolated from the CS pin by the blanking circuits while GATE is low, and for a short time (blanking period) just after GATE switches high. A 500 Ω (max) equivalent pulldown resistor on CS is applied while GATE is low.

7.4.2.5 RT

The RT pin programs the (free-running) oscillator frequency of the TPS23751 and TPS23752 in PWM mode. The internal oscillator sets the maximum duty cycle at 80% and controls the slope-compensation ramp circuit. In VFO mode, the RT pin is driven by V_{CTL}.

7.4.2.6 T2P, Startup and Power Management

T2P (type 2 PSE) is an active-low multifunction pin that indicates if

$$[(\text{PSE} = \text{Type\_2}) + (V_{APD} > 1.5\ \text{V}) + (V_{CTL} < 4\ \text{V}) \times (\text{PD current limit} \neq \text{Inrush})].$$

The term with V_{CTL} prevents an optocoupler connected to the secondary-side from loading V_C before the converter is started. The APD term allows the PD to operate from an adapter at high-power if a type 2 PSE is not present, assuming the adapter has sufficient capacity. Applications must monitor the state of T2P to detect power source transitions. Transitions could occur when a local power supply is added or dropped or when a PSE is enabled on the far end. The PD may be required to adjust the load appropriately. The usage of T2P is demonstrated in Figure 32.

In order for a type 2 PD to operate at less than 13 W the first 80 ms after power application, the various delays must be estimated and used by the application controller to meet the requirement. The bootup time of many applications processors may be long enough to eliminate the need to do any timing. Figure 27 illustrates the T2P delay after the converter starts.

7.4.2.7 Thermal Shutdown

The DC-DC controller has an OTSD that can be triggered by heat sources including the V_B regulator, GATE driver, bootstrap current source, and bias currents. The controller OTSD turns off V_B, the GATE driver, and forces the V_C control into an under-voltage state.

7.4.2.8 Adapter ORing

Many PoE-capable devices are designed to operate from either a wall adapter or PoE power. A local power solution adds cost and complexity, but allows a product to be used if PoE is not available in a particular installation. While most applications only require that the PD operate when both sources are present, the TPS23751 and TPS23752 supports forced operation from either of the power sources. Figure 31 illustrates three options for diode ORing external power into a PD. Only one option would be used in any particular design. Option 1 applies power to the TPS23751 and TPS23752 PoE input, option 2 applies power between the TPS23751 and TPS23752 PoE section and the power circuit, and option 3 applies power to the output side of the converter. Each of these options has advantages and disadvantages. Many of the basic ORing configurations and much of the discussion contained in the application note *Advanced Adapter ORing Solutions using the TPS23753* (SLVA306), apply to the TPS23751 and TPS23752.

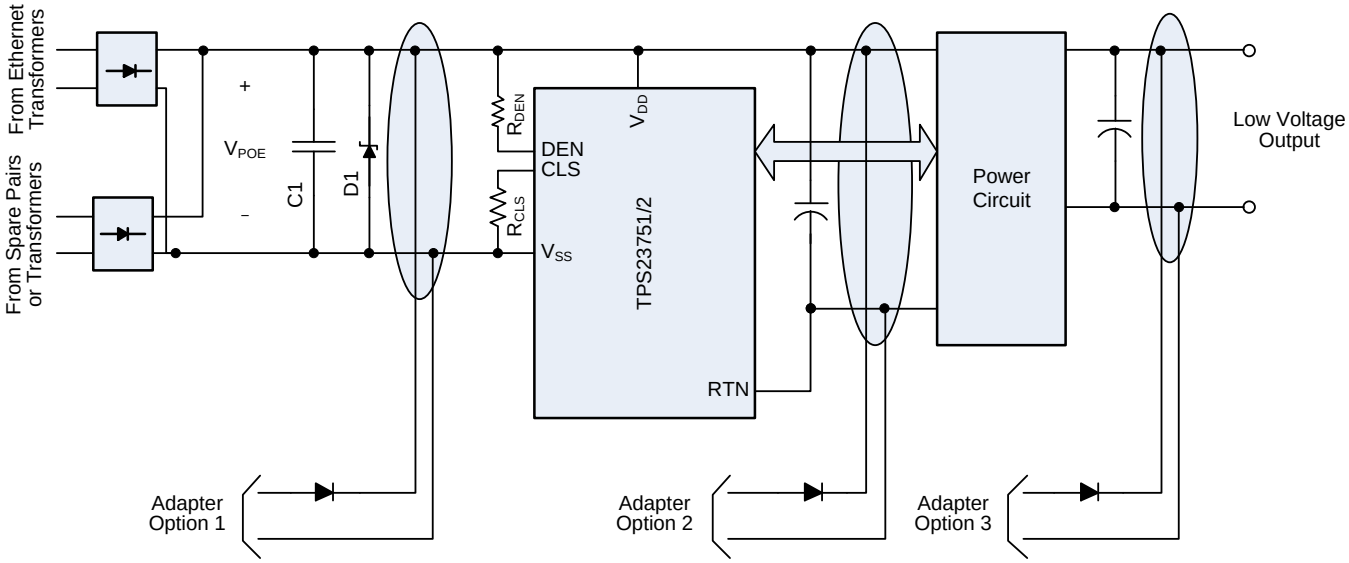


Figure 31. ORing Configurations

The IEEE standards require that the Ethernet cable be isolated from ground and all other system potentials. The adapter must meet a minimum 1500 Vac dielectric withstand test between the output and all other connections for ORing options 1 and 2. The adapter only needs this isolation for option 3 if it is not provided by the converter.

Adapter ORing diodes are shown for all the options to protect against a reverse voltage adapter, a short on the adapter input pins, or damage to a low-voltage adapter. ORing is sometimes accomplished with a MOSFET in option 3.

7.4.2.9 Using DEN to Disable PoE

The DEN pin may be used to turn the PoE hotswap switch off by pulling it to V_{SS} while in the operational state, or to prevent detection when in the idle state. A low voltage on DEN forces the hotswap MOSFET off during normal operation.

7.4.2.10 ORing Challenges

Preference of one power source presents a number of challenges. Combinations of adapter output voltage (nominal and tolerance), power insertion point, and which source is preferred determine solution complexity. Several factors adding to the complexity are the natural high-voltage selection of diode ORing (the simplest method of combining sources), the current limit implicit in the PSE, and PD inrush and protection circuits (necessary for operation and reliability). Creating simple and seamless solutions is difficult, if not impossible, for many of the combinations. However, the TPS23751 and TPS23752 offer several built-in features that simplify some combinations.

Several examples demonstrate the limitations inherent in ORing solutions. Diode ORing a 48 V adapter with PoE (option 1) presents the problem that either source may have the higher voltage. A blocking switch would be required to assure that one source dominates. A second example combines a 12 V adapter with PoE using option 2. The converter draws approximately four times the current at 12 V from the adapter than it does from PoE at 48 V. Transition from adapter power to PoE may demand more current than can be supplied by the PSE. The converter must be turned off while the C_{IN} capacitance charges, with a subsequent converter restart at the higher voltage and lower input current. A third example involves the loss of the MPS when running from the adapter, causing the PSE to remove power from the PD. If ac power is then lost, the PD stops operating until the PSE detects and powers the PD.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS23751 and TPS23752 support power supply topologies that require a single PWM gate drive with current-mode control. Figure 32 provides an example of a synchronous rectifier flyback converter.

8.2 Typical Application

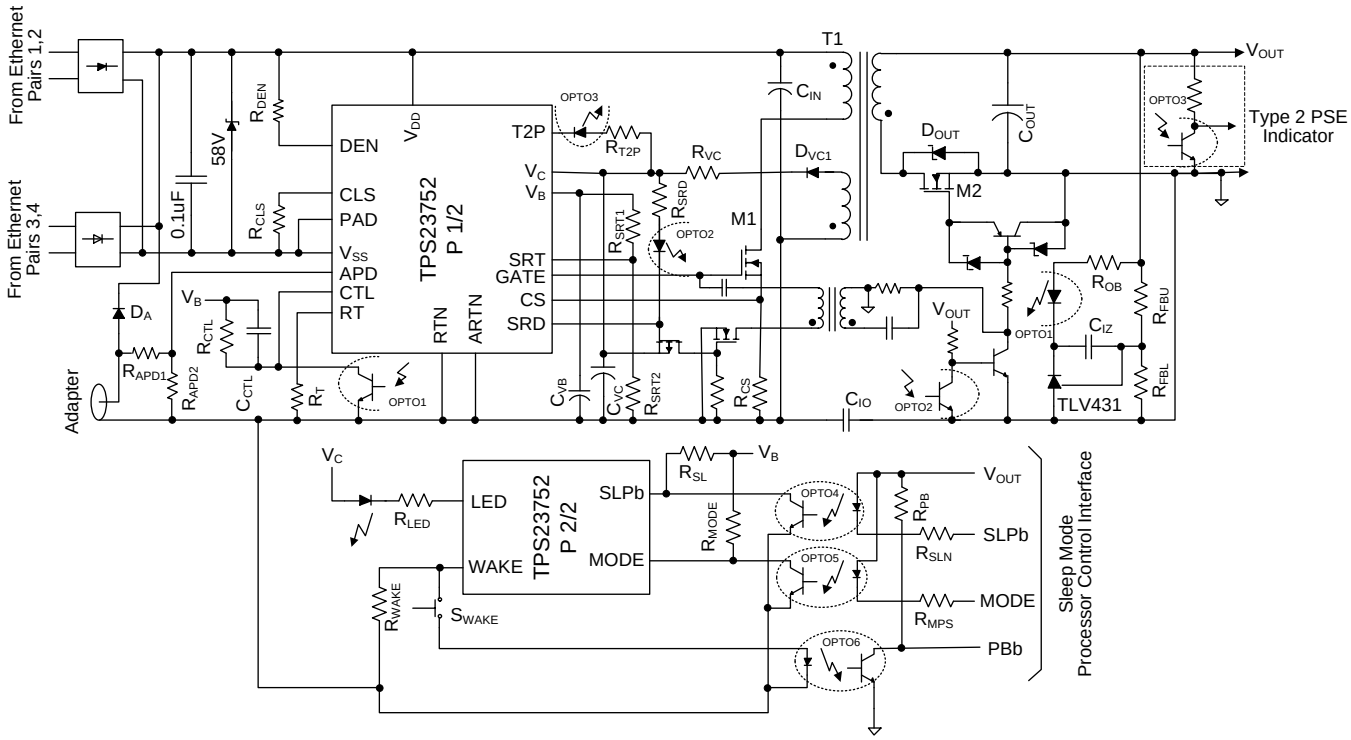


Figure 32. TPS23752 Application Circuit

8.2.1 Design Requirements

Selecting a converter topology along with a design procedure is beyond the scope of this applications section. Examples to help in programming the TPS23751 and TPS23752 are shown below. Additional special topics are included to explain the ORing capabilities, frequency dithering, and other design considerations. For more specific converter design examples refer to the following application notes:

- Designing with the TPS23753 Powered Device and Power Supply Controller, SLVA305
- Advanced Adapter ORing Solutions using the TPS23753, SLVA306
- TPS23751EVM-104 EVM: Evaluation Module for TPS23751, SLVU754
- TPS23752EVM-145 EVM: Evaluation Module for TPS23752, SLVU753

Typical Application (continued)

8.2.2 Detailed Design Procedure

8.2.2.1 Input Bridges and Schottky Diodes

Using Schottky diodes instead of PN junction diodes for the PoE input bridges reduces the power dissipation in these devices by about 30%. There are, however, some things to consider when using them.

The IEEE standard specifies a maximum backfeed voltage of 2.8 V. A 100-kΩ resistor is placed between the unpowered pairs and the voltage is measured across the resistor. Schottky diodes often have a higher reverse leakage current than PN diodes, making this a harder requirement to meet. To compensate, use conservative design for diode operating temperature, select lower-leakage devices where possible, and match leakage and temperatures by using packaged bridges.

Schottky diode leakage currents and lower dynamic resistances can impact the detection signature. Setting reasonable expectations for the temperature range over which the detection signature is accurate is the simplest solution. Increasing R_{DEN} slightly may also help meet the requirement.

Schottky diodes have proven less robust to the stresses of ESD transients than PN junction diodes. After exposure to ESD, Schottky diodes may become shorted or leak. Care must be taken to provide adequate protection in line with the exposure levels. This protection may be as simple as ferrite beads and capacitors.

As a general recommendation, use 1 A or 2 A, 100-V rated discrete or bridge diodes for the input rectifiers.

8.2.2.2 Protection, D_1

A TVS, D_1, across the rectified PoE voltage per Figure 32 must be used. A SMAJ58A, or equivalent, is recommended for general indoor applications. Adequate capacitive filtering or a TVS must limit input transient voltage to within the absolute maximum ratings. Outdoor transient levels or special applications require additional protection.

8.2.2.3 Capacitor, C_1

The IEEE 802.3at standard specifies an input bypass capacitor (from V_{DD} to V_{SS}) of 0.05 μF to 0.12 μF. Typically a 0.1 μF, 100 V, 10% ceramic capacitor is used.

8.2.2.4 Detection Resistor, R_{DEN}

The IEEE 802.3at standard specifies a detection signature resistance, R_{DEN} between 23.75 kΩ and 26.25 kΩ, or 25 kΩ ±5%. A resistor of 24.9 kΩ ±1% is recommended for R_{DEN}.

8.2.2.5 Classification Resistor, R_{CLS}

Connect a resistor from CLS to V_{SS} to program the classification current according to the IEEE 802.3at standard.

The class power assigned should correspond to the maximum average power drawn by the PD during operation.

Select R_{CLS} according to Table 1. For a high power design, choose class 4 and R_{CLS} = 63.4 Ω.

8.2.2.6 APD Pin Divider Network, R_{APD1}, R_{APD2}

The APD pin can be used to disable the TPS23751 and TPS23752 internal hotswap MOSFET, giving the adapter source priority over the PoE. For an example calculation, see literature number SLVA306.

8.2.2.7 Setting the PWM-VFO Threshold using the SRT pin

The TPS23751 and TPS23752 internally compares modified voltages at the SRT and CTL pins to determine the operating mode. The designer should consider the light load operating point (considering the value of V_{CTL}) where synchronous rectifier (M2 in Figure 32) gate drive and switching losses nearly match conduction losses of the rectifier diode (D_{OUT} in Figure 32). Typically, the designer characterizes circuit efficiency, output load, and control pin (V_{CTL}) voltage and then select the transition point. Both VFO → PWM (occurs at higher load current due to natural hysteresis) and PWM → VFO (occurs at slightly lower load current) transitions should be considered when choosing the V_{SRT} setpoint. As an example:

1. Assume that the desired efficiency transition threshold occurs at 18% of full load and V_{CTL} = 2.0 V

Typical Application (continued)

2. Determine where to set V_{SRT}.
   Transition to VFO mode when $V_{CTL} = 2.0\ V$
   $$V_{SRT} = 2 \times V_{CTL} - 3.5\ V = 2 \times 2.0\ V - 3.5\ V = 0.5\ V \quad (2)$$
3. Set V_{SRT} using a voltage divider from V_B to ARTN as shown in Figure 32.
4. Choose R_{SRT1} = 100 kΩ and then calculate R_{SRT2} as follows:
   $$R_{SRT2} = \frac{R_{SRT1} \times V_{SRT}}{V_B - V_{SRT}} = \frac{100\ k\Omega \times 0.5\ V}{5\ V - 0.5\ V} = 11.1\ k\Omega \quad (3)$$
5. Select 11 kΩ for R_{SRT2}.

8.2.2.8 Setting Frequency (R_T)

The converter switching frequency in PWM mode is set by connecting resistor, R_T from the RT pin to ARTN (see Figure 32). The frequency may be set as high as 1 MHz with some loss in programming accuracy as well as converter efficiency. As an example:

1. Assume a desired switching frequency (f_{SW}) of 250 kHz.
2. Compute R_T:
   $$R_T = \frac{8.5 \times 10^9\ \Omega}{f_{SW}(Hz)} = \frac{8.5 \times 10^9\ \Omega}{250000} = 34000\ \Omega \quad (4)$$
3. Select 34 kΩ for R_T.

8.2.2.9 Current Slope Compensation

The TPS23751 and TPS23752 provide a fixed internal compensation ramp that suffices for most applications. R_S (see Figure 33) may be used if the internally provided slope compensation is not enough. Most current-mode control papers and application notes define the slope values in terms of V_{PP}/T_S (peak ramp voltage / switching period). Assuming that the desired slope, V_{SLOPE_D} (in mV/period), as shown in Figure 2, is based on the full period, compute R_S per the following equation where V_{PK} and I_{CS_RAMP} are from the electrical characteristics table with voltages in mV and current in μA.

$$R_S(\Omega) = \frac{V_{SLOPE\_D}(mV) - \frac{V_{PK}(mV)}{\left(D_{MAX} - D_{SLOPE\_ST}\right)}}{\frac{I_{CS\_RAMP}(\mu A)}{\left(D_{MAX} - D_{SLOPE\_ST}\right)}} \times 1000 \quad (5)$$

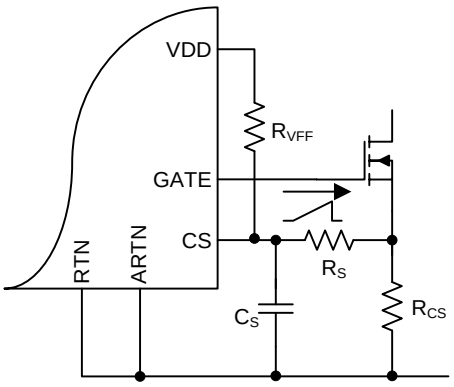


Figure 33. Additional Slope Compensation

C_S may be required if the presence of R_S causes increased noise, due to adjacent signals like the gate drive, to appear at the C_S pin.

Typical Application (continued)

8.2.2.10 Voltage Feed-Forward Compensation

Voltage feed-forward compensation can provide additional benefits including a flatter output fold-back current limit characteristic (versus input voltage), and a reduction of voltage stress on the primary switching MOSFET at high line and output overload. Voltage feed-forward can simply be applied by adding a resistor, R_{VFF} between VDD and CS as shown in Figure 33. The current through R_{VFF} and R_S provides a small dc offset on the CS pin which reduces the output fold back current limit.

A simple way to choose R_{VFF} is to first determine the natural circuit output fold back current at minimum line input voltage. For example, if the circuit requirements are to deliver a regulated 5 V output at 5 A from a 24 V dc adapter, then low line input could be as low as 21.6 V including tolerance. R_{VFF} must be set large enough to allow the required current to be delivered prior to output voltage fold back. Natural circuit output fold back current and primary MOSFET voltage stress should also be characterized at high line in order to assess the improvement provided by the addition of R_{VFF}.

For a given SRT setpoint, the addition of R_{VFF} reduces the output current at which the VFO to PWM (and PWM to VFO) transition occurs. This requires that the designer increase V_{SRT} to account for the reduction due to R_{VFF}.

8.2.2.11 Estimating Bias Supply Requirements and Cvc

The bias supply (V_C) power requirements determine C_{VC} sizing and hiccup frequency during a fault. The first step is to determine the power and current requirements of the power supply control circuitry, then select C_{VC}. The following example assumes that control current draw is constant with voltage with no loading by the feedback and T2P optocouplers to simplify the process:

1. Let V_{QG} be the gate voltage swing that the MOSFET Q_G is rated to (often 10 V).

$$P_{GATE} = V_C \times f_{SW} \times \left(Q_{GATE} \times \frac{V_C}{V_{QG}} \right) \tag{6}$$

   Compute gate drive power if V_C is 12 V and Q_{GATE} is 17 nC

$$P_{GATE} = 12\,V \times 250\,kHz \times 17\,nC \times \frac{12}{10} = 61.2\,mW \tag{7}$$

   This equation illustrates why MOSFET Q_G should be an important consideration in selecting the switching MOSFETs.

2. Estimate the required bias current at some intermediate voltage during the C_{VC} discharge. For the TPS23751 and TPS23752, 12 V provides a reasonable estimate. Add the operating bias current to the gate drive current.

$$I_{DRIVE} = \frac{P_{GATE}}{V_C} = \frac{61.2\,mW}{12\,V} = 5.1\,mA$$

$$I_{TOTAL} = I_{DRIVE} + I_{VC\_OP} = 5.1\,mA + 1.8\,mA = 6.9\,mA \tag{8}$$

3. Compute the required C_{VC} based on startup within the typical softstart delay of 3.01 ms.

$$C_{VC1} + C_{VC2} = \frac{T_{SSD} \times I_{TOTAL}}{V_{CUVH}} = \frac{3.01\,ms \times 6.9\,mA}{3.2\,V} = 6.49\,\mu F \tag{9}$$

4. Choose a 10 µF electrolytic and 0.47 µF ceramic capacitor each rated for 16 V (minimum). Compute the initial time to start the converter when operating from PoE. Using a typical bootstrap current of 1.5 mA, compute the time to startup.

$$T_{ST} = \frac{(C_{VC1} + C_{VC2}) \times V_{CUV}}{I_{VC\_ST}} = \frac{10.47\,\mu F \times 8.9\,V}{1.5\,mA} = 62.1\,ms \tag{10}$$

5. Compute the fault duty cycle and hiccup frequency

$$T_{RECHARGE} = \frac{(C_{VC1} + C_{VC2}) \times V_{CUVH}}{I_{VC\_ST}} = \frac{(10\,\mu F + 0.47\,\mu F \times 3.2\,V)}{1.5\,mA} = 22.3\,ms \tag{11}$$

Typical Application (continued)

$$T_{DISCHARGE} = \frac{(C_{VC1} + C_{VC2}) \times V_{CUVH}}{I_{TOTAL}} = \frac{(10\,\mu F + 0.47\,\mu F) \times 3.2\,V}{6.9\,mA} = 4.9\,ms \quad (12)$$

$$\text{Duty Cycle}: D = \frac{T_{DISCHARGE}}{T_{DISCHARGE} + T_{RECHARGE}} = \frac{4.9\,ms}{4.9\,ms + 22.3\,ms} = 18.0\% \quad (13)$$

$$\text{Hiccup Frequency}: F = \frac{1}{T_{DISCHARGE} + T_{RECHARGE}} = \frac{1}{4.9\,ms + 22.3\,ms} = 37\,Hz \quad (14)$$

8.2.2.12 Switching Transformer Considerations and R_{VC}

Care in design of the transformer and V_C bias circuit is required to obtain hiccup overload protection. Leading-edge voltage overshoot on the bias winding may cause V_C to peak-charge, preventing the expected tracking with output voltage. Some method of controlling overshoot is usually required. The method may be as simple as a series resistor, or an R-C filter in front of D_{VC1}. Good transformer bias-to-output-winding coupling results in reduced overshoot and better voltage tracking.

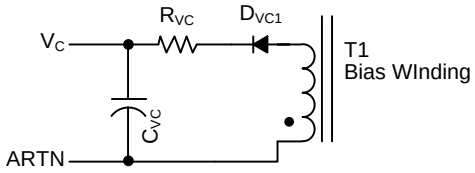


Figure 34. V_C Pin Interface

R_{VC} as shown in Figure 34 helps to reduce peak charging from the bias winding. Reduced peak charging becomes especially important when tuning hiccup mode operation during output overload. Typical values for R_{VC} are between 10 Ω and 100 Ω.

8.2.2.13 T2P Pin Interface

The T2P pin is an active-low, open-drain output which indicates that a high power source is available. An optocoupler can interface the T2P pin to circuitry on the secondary side of the converter. A high-gain optocoupler and a high-impedance (for example, CMOS) receiver are recommended. Design of the T2P optocoupler interface can be accomplished as follows:

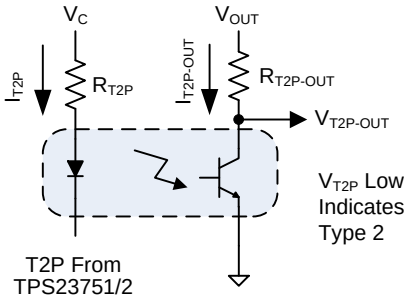


Figure 35. T2P Interface

1. As shown in Figure 35, let V_C = 12 V, V_{OUT} = 5 V, $R_{T2P-OUT}$ = 10 kΩ, V_{T2P} = 260 mV, $V_{T2P-OUT}$ = 400 mV.

$$I_{T2P-OUT} = \frac{V_{OUT} - V_{T2P-OUT}}{R_{T2P-OUT}} = \frac{5 - 0.4}{10000} = 0.46\ mA \quad (15)$$

2. The optocoupler current transfer ratio, CTR, is not needed to determine R_{T2P}. A device with a minimum CTR of 100% at 1 mA LED bias current, I_{T2P}, is selected. Note that in practice, CTR varies with temperature, LED bias current, and aging. These variations may require some iteration using the CTR-versus- I_{DIODE} curve on the optocoupler data sheet.

Typical Application (continued)

a. The approximate forward voltage of the optocoupler diode, V_{FWLED}, is 1.1 V from the data sheet.

$$I_{T2P\text{-}MIN} = \frac{I_{T2P\text{-}OUT}}{CTR} = \frac{0.46\,mA}{1.00} = 0.46\,mA, \text{ Select } I_{T2P} = 1mA$$

b.

$$R_{T2P} = \frac{V_C - V_{T2P} - V_{FWLED}}{I_{T2P}} = \frac{12\,V - 0.26\,V - 1.1V}{1mA} = 10.6\,k\Omega$$

c. Select a 10.7 kΩ resistor. (16)

8.2.2.14 Softstart

Converters require a softstart on the voltage error amplifier to prevent output overshoot on startup. Figure 36 shows a common implementation of a secondary-side softstart that works with the typical TL431 error amplifier. The softstart components consist of D_{SS}, R_{SS}, and C_{SS}. They serve to control the output rate-of-rise by pulling V_{CTL} down as C_{SS} charges through R_{OB}, the optocoupler, and D_{SS}. This has the added advantage that the TL431 output and C_{IZ} are preset to the proper value as the output voltage reaches the regulated value, preventing voltage overshoot due to the error amplifier recovery. The secondary-side error amplifier does not become active until there is sufficient voltage on the secondary. The TPS23751 and TPS23752 provide a primary-side softstart which persists long enough (approximately 3ms) for secondary side voltage-loop softstart to take over. The primary-side current-loop softstart controls the switching MOSFET peak current by applying a slowly rising ramp voltage to a second PWM control input. The PWM is controlled by the lower of the softstart ramp or the CTL-derived current demand. The actual output voltage rise time is usually much shorter than the internal softstart period. Initially the internal softstart ramp limits the maximum current demand as a function of time. The current limit, secondary-side softstart, or output regulation assume control of the PWM before the internal softstart period is over.

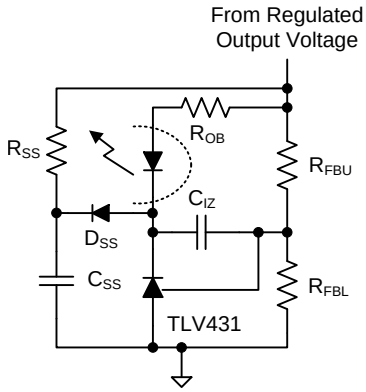


Figure 36. Error Amplifier Soft Start

8.2.2.15 Special Switching MOSFET Considerations

Special care must be used in selecting the converter switching MOSFET. The TPS23751 and TPS23752 minimum switching MOSFET V_{GATE} is approximately 5.5 V, which is due to the V_C lower threshold. This condition occurs during an output overload, or towards the end of a (failed) bootstrap startup. The MOSFET must be able to carry the anticipated peak fault current at this gate voltage.

8.2.2.16 ESD

ESD requirements for a unit that incorporates the TPS23751 or TPS23752 have a much broader scope and operational implications than are used in TI testing. Unit-level requirements should not be confused with reference design testing that only validates the ruggedness of the TPS23751 and TPS23752.

Typical Application (continued)

8.2.2.17 Thermal Considerations and OTSD

Sources of nearby local PCB heating should be considered during the thermal design. Typical calculations assume that the TPS23751 and TPS23752 are the only heat sources contributing to the PCB temperature rise. It is possible for a normally operating TPS23751 or TPS23752 device to experience an OTSD event if it is excessively heated by a nearby device.

8.2.3 Application Curves

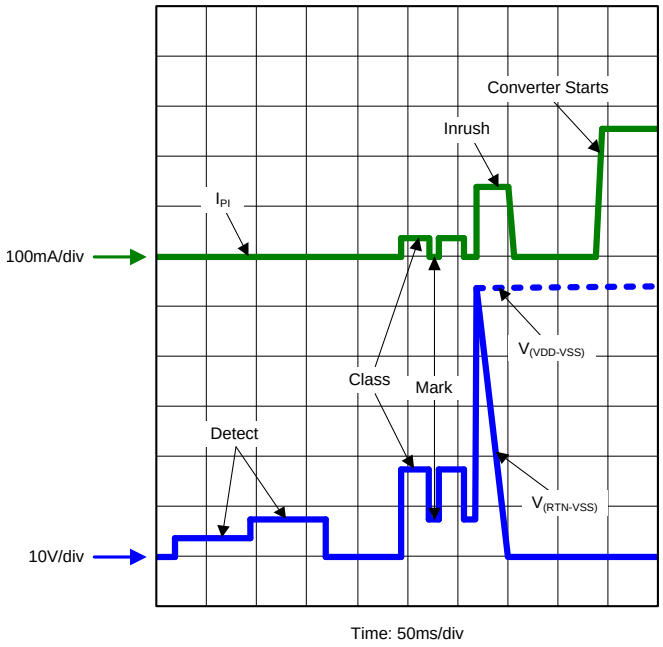


Figure 37. Startup

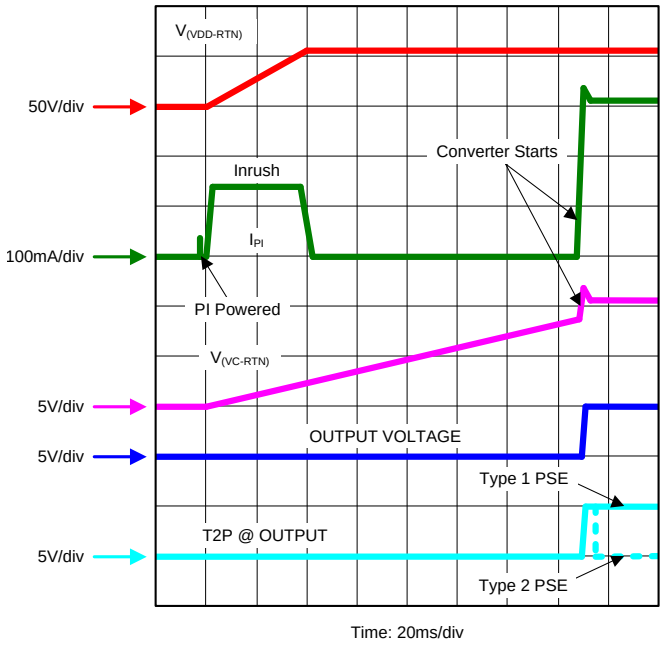


Figure 38. Power Up and Start

9 Power Supply Recommendations

The TPS23751 and TPS23752 converter should be designed such that the input voltage of the converter is capable of operating within the IEEE802.3at recommended input voltage as shown in Table 3 and the minimum operating voltage of the adapter if applicable.

10 Layout

10.1 Layout Guidelines

Printed-circuit-board layout recommendations are provided in the evaluation module (EVM) documentation available for these devices.

10.2 Layout Example

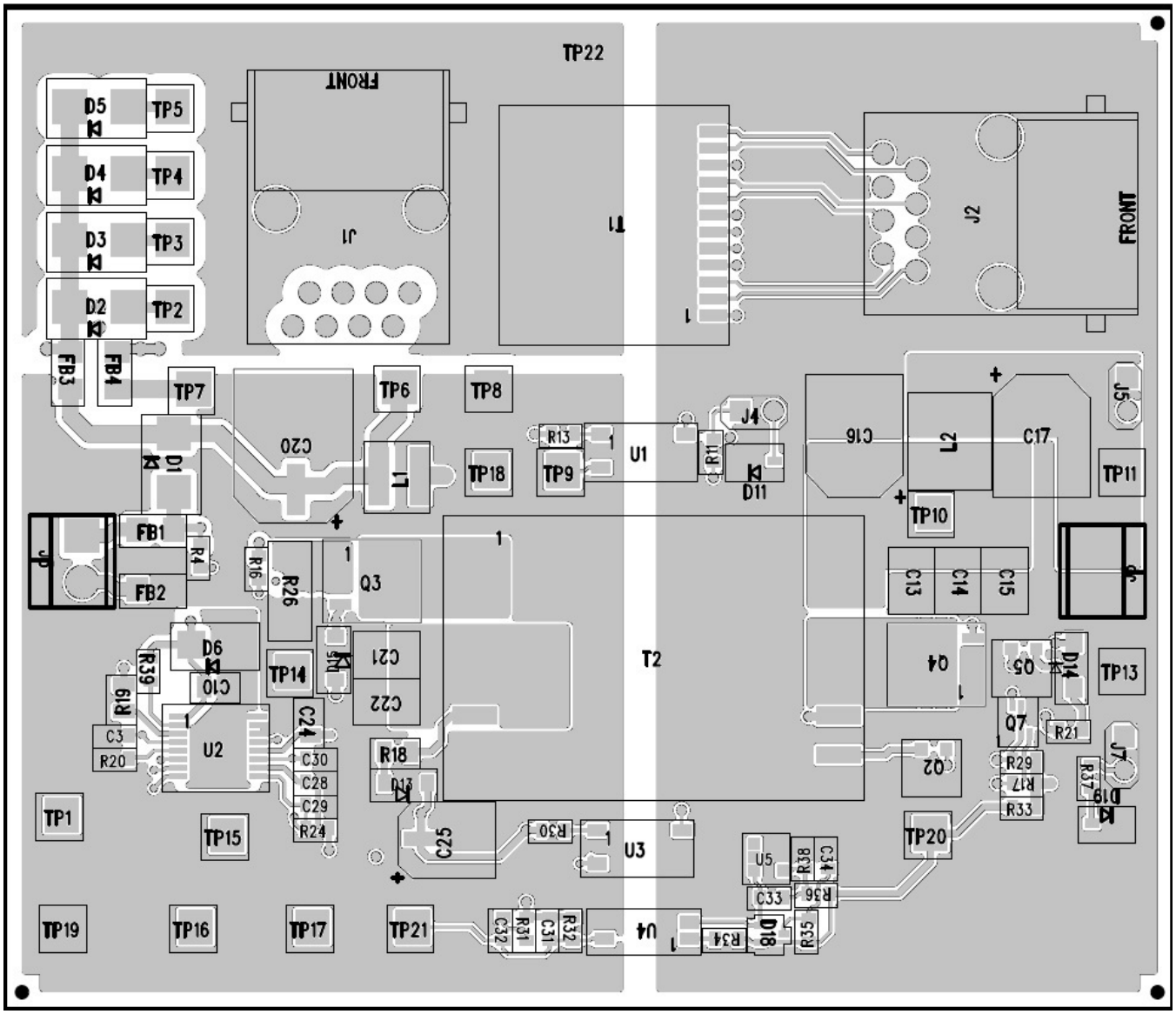


Figure 39. TPS23751EVM-104 EVM Parts Placement and Example Layout

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

《TPS23752 在睡眠模式中维持功率特征运行》，SLVA588

《PoE 受电设备的雷击浪涌注意事项》，SLUA736

《具有增强型 ESD 穿越功能的 IEEE 802.3-2005 PoE 接口和隔离型转换器控制器》，SLVA306

《高功率/高效率 PoE 接口和直流/直流控制器》，SLUA469

11.1.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件以及申请样片或购买产品的快速访问链接。

表 **4.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
TPS23751	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS23752	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.3 商标

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS23751PWP	ACTIVE	HTSSOP	PWP	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	23751	Samples
TPS23751PWPR	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	23751	Samples
TPS23752PWP	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS23752	Samples
TPS23752PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS23752	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

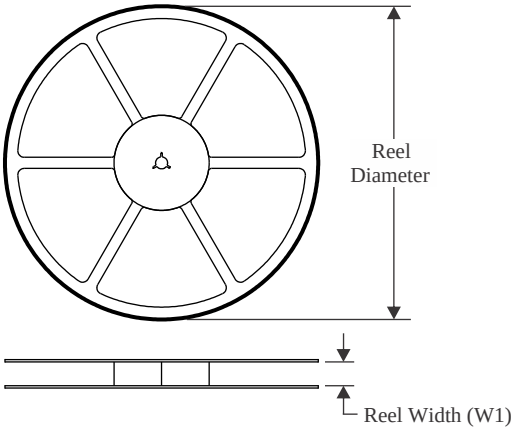
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

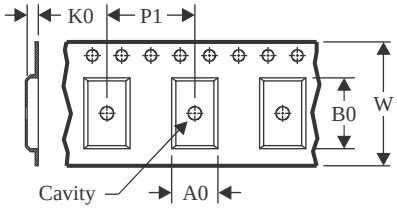
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

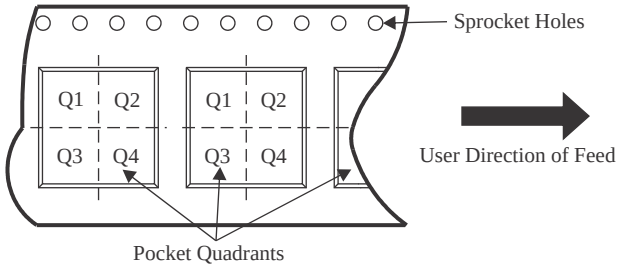


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

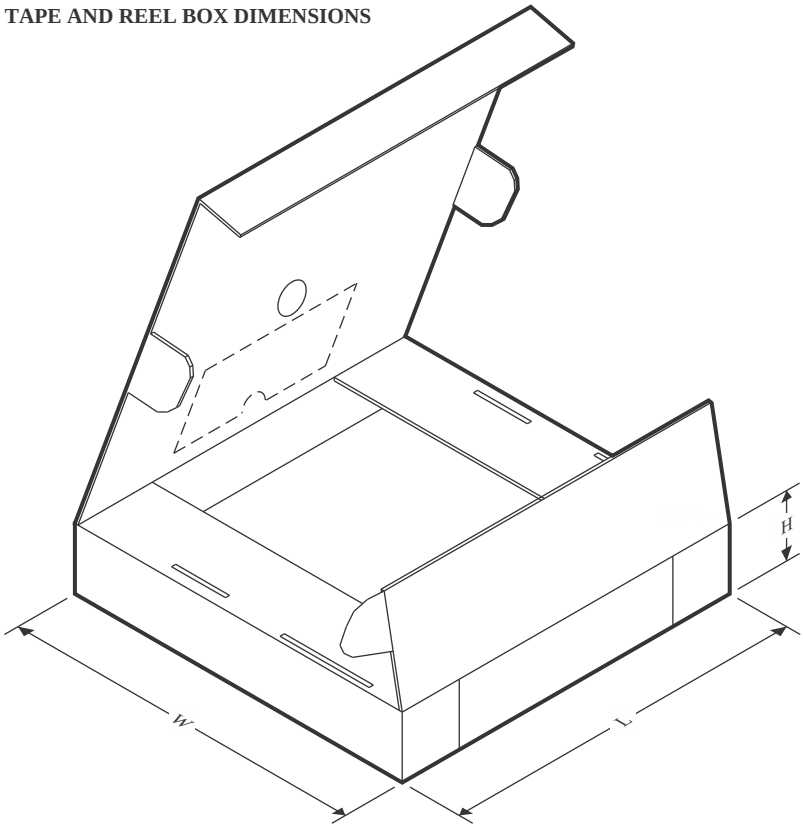
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS23751PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS23752PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

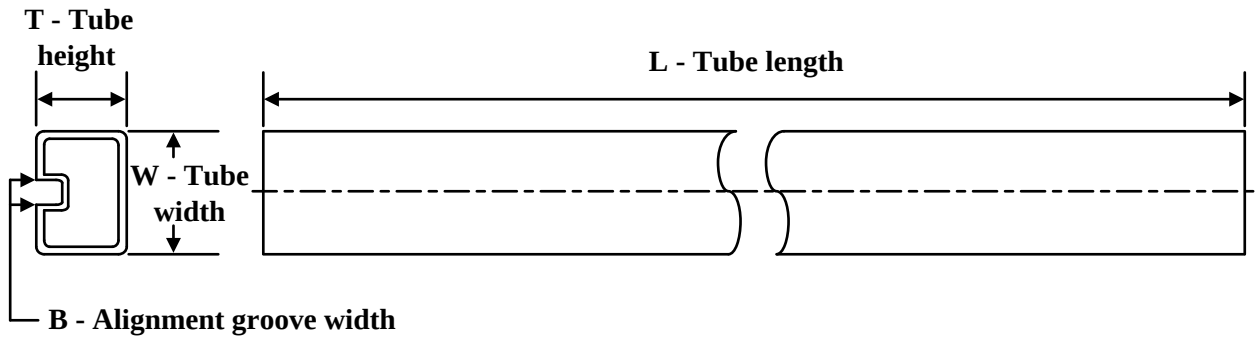
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS23751PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0
TPS23752PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0

TUBE

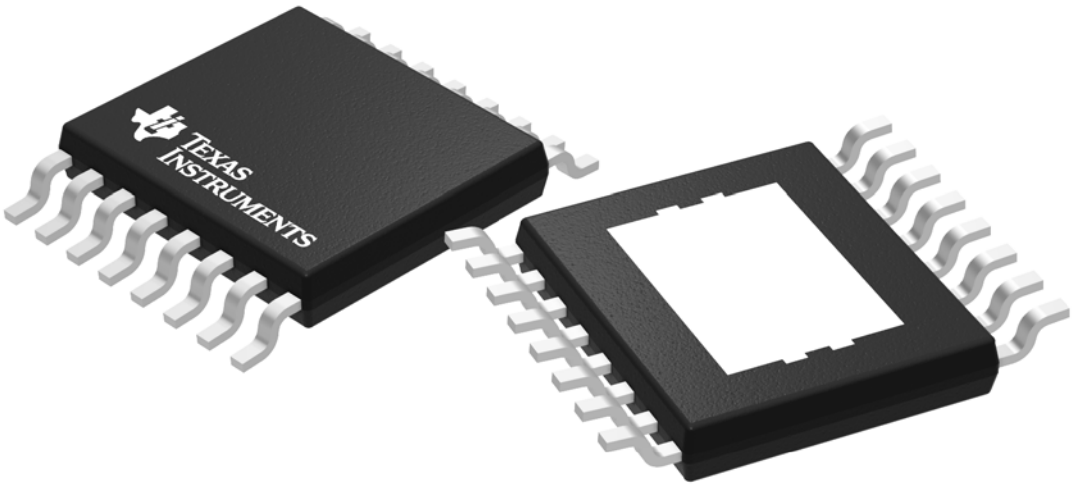


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS23751PWP	PWP	HTSSOP	16	90	530	10.2	3600	3.5
TPS23752PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

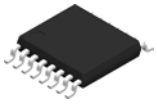
PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

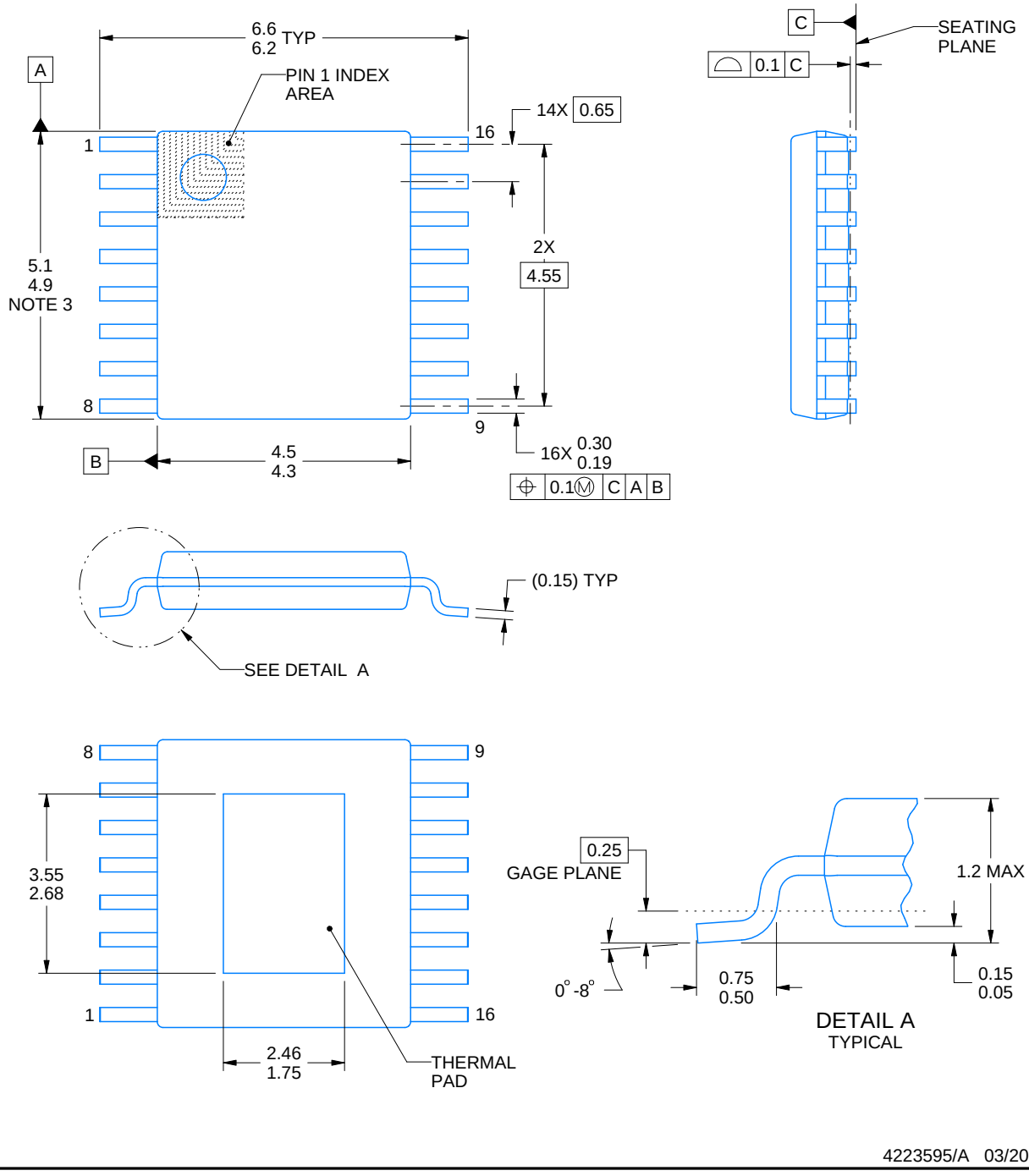
PACKAGE OUTLINE

PWP0016J



PowerPAD™ TSSOP - 1.2 mm max height

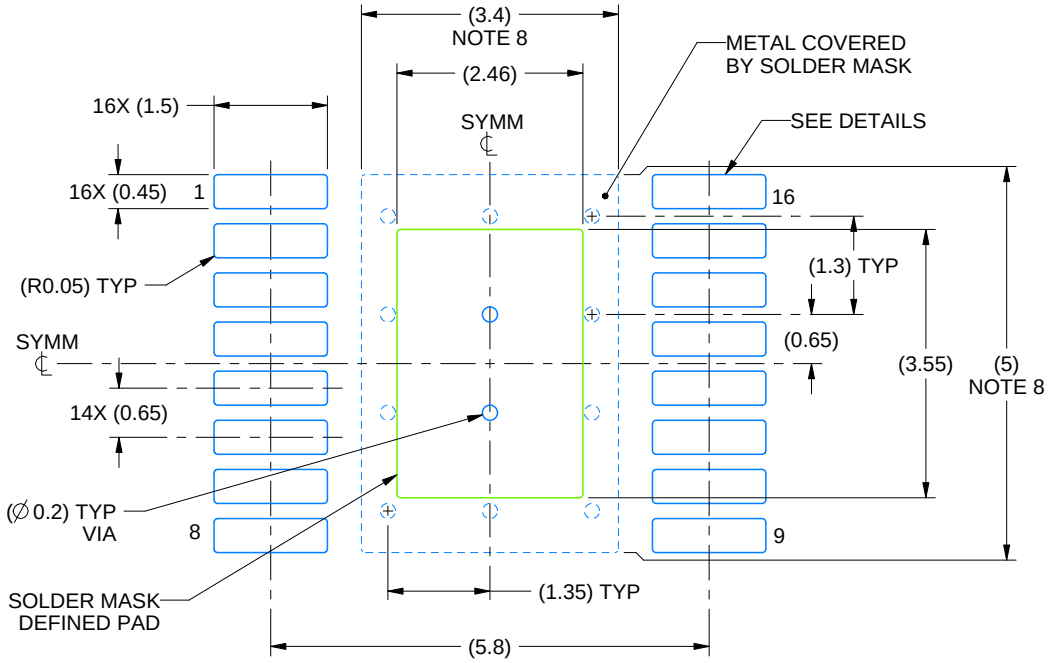
SMALL OUTLINE PACKAGE



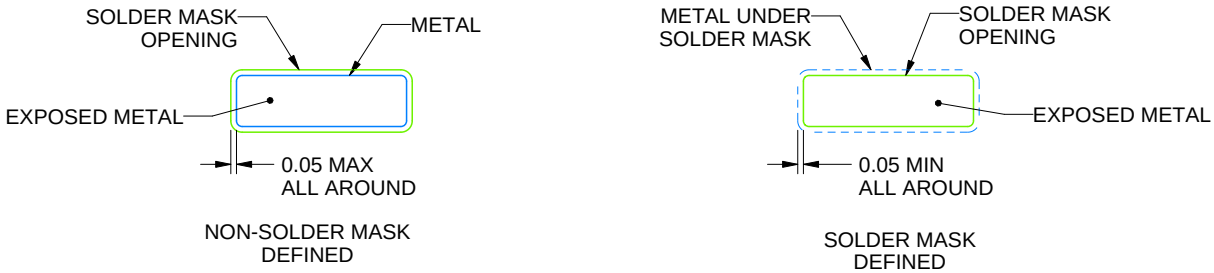
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

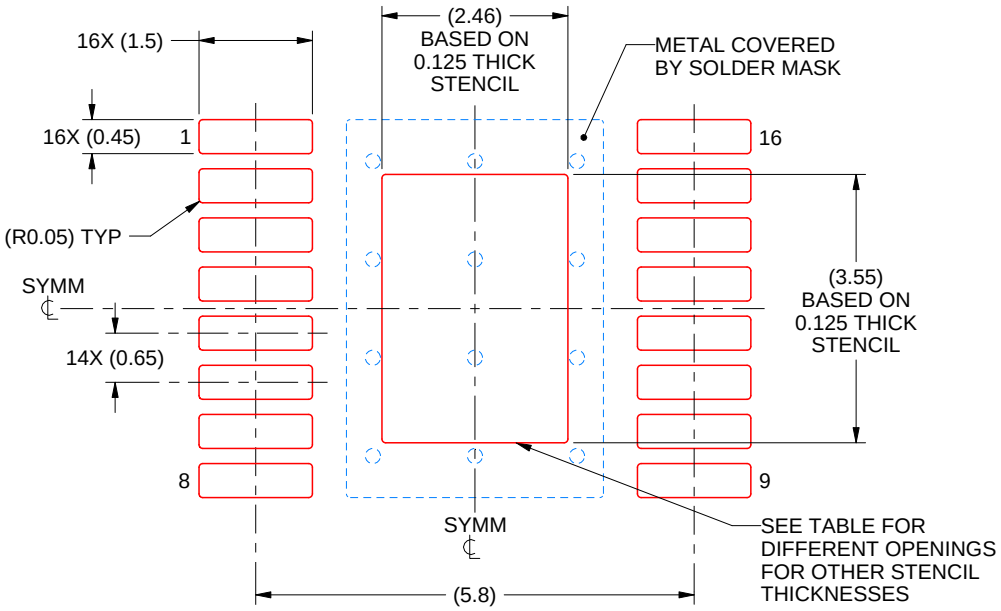


SOLDER MASK DETAILS

4223595/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

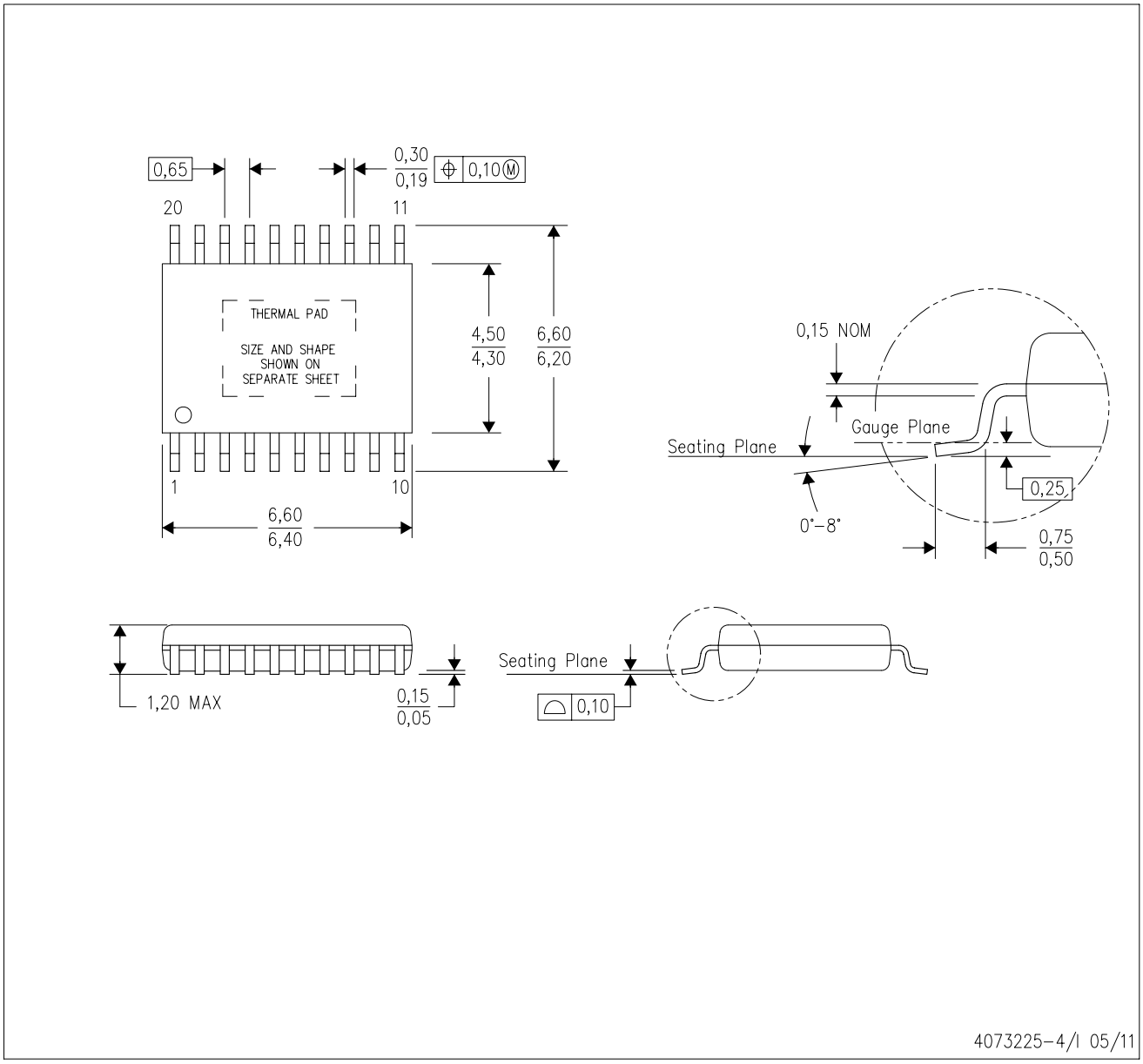
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 3.97
0.125	2.46 X 3.55 (SHOWN)
0.15	2.25 X 3.24
0.175	2.08 X 3.00

4223595/A 03/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

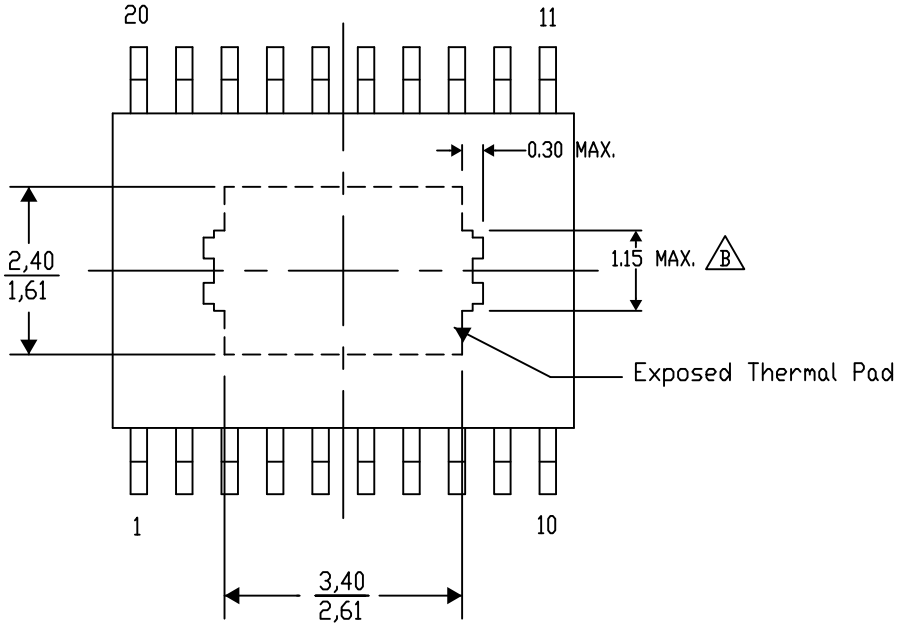
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

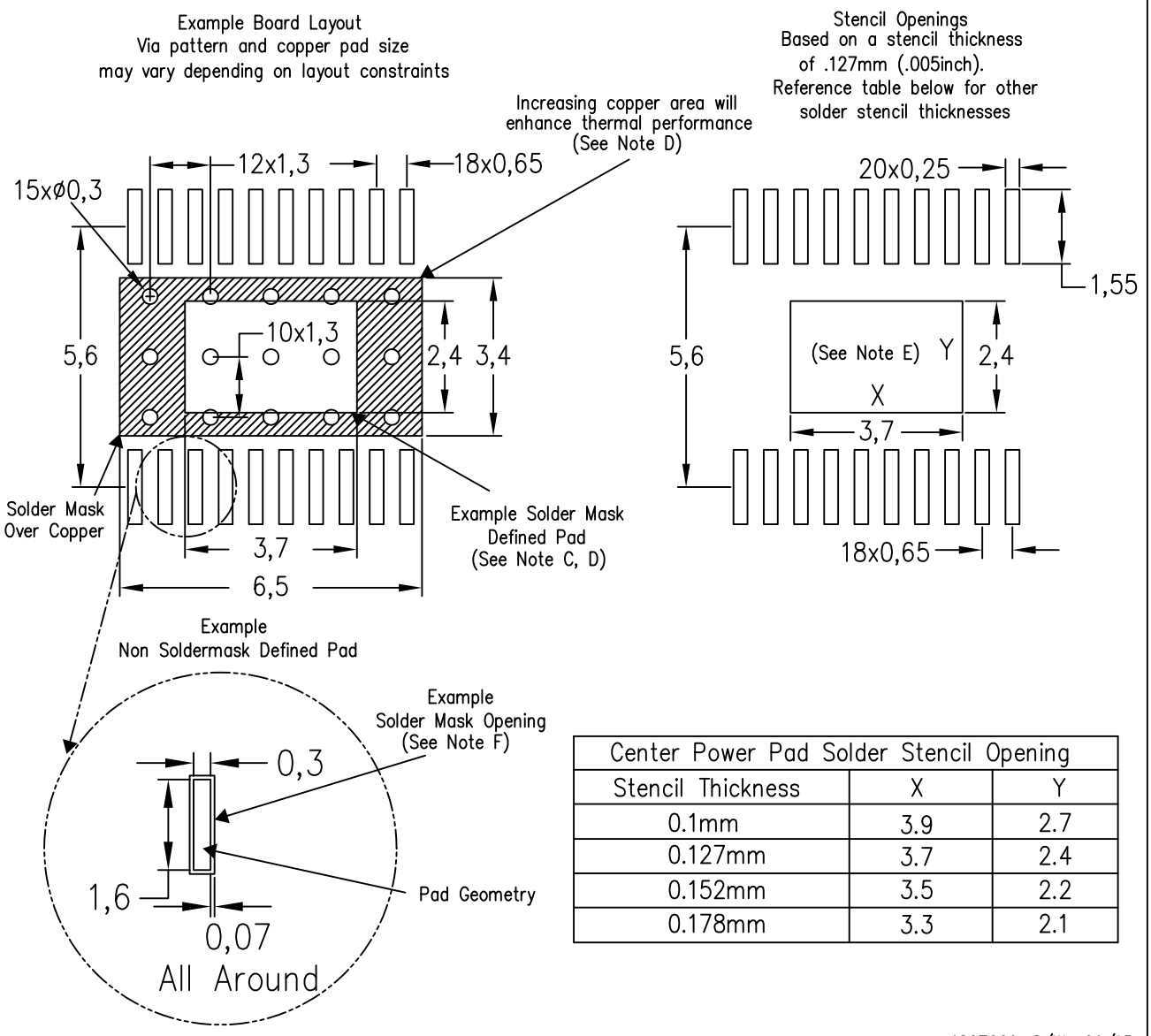
4206332–15/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609–8/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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