ADS54J60 双通道 16 位 1.0GSPS 模数转换器

1 特性

- 16 位分辨率、双通道、1GSPS ADC
- 本底噪声：–159dBFS/Hz
- 频谱性能（f_{IN} = 170MHz，–1dBFS）：
  - 信噪比 (SNR)：70dBFS
  - 噪声频谱密度 (NSD)：–157dBFS/Hz
  - SFDR：86dBc（包括交错音调）
  - SFDR：89dBc（不包括 HD2、HD3 和交错音调）
- 频谱性能（f_{IN} = 350MHz，–1dBFS）：
  - SNR：67.5dBFS
  - NSD：–154.5dBFS/Hz
  - SFDR：75dBc
  - SFDR：85dBc（不包括 HD2、HD3 和交错音调）
- 通道隔离：f_{IN} = 170MHz 时为 100dBc
- 输入满标度：1.9V_{PP}
- 输入带宽 (3dB)：1.2GHz
- 片上抖动
- 集成宽带 DDC 块
- 支持子类 1 的 JESD204B 接口：
  - 10.0Gbps 时每个 ADC 具有 2 条信道
  - 5.0Gbps 时每个 ADC 具有 4 条信道
  - 支持多芯片同步
- 功耗：1GSPS 时为 1.35W/通道
- 封装：72 引脚 VQFNP (10mm × 10mm)

2 应用

- 雷达和天线阵列
- 无线宽带
- 电缆 CMTS、DOCSIS 3.1 接收器
- 通信测试设备
- 微波接收器
- 软件定义无线电 (SDR)
- 数字转换器
- 医疗成像和诊断

3 说明

ADS54J60 是一款低功耗、高带宽 16 位、1.0GSPS 双通道模数转换器 (ADC)。该器件经设计具有高信噪比 (SNR)，可提供 -159dBFS/Hz 的噪底，从而 协助应用在宽瞬时带宽内 实现最高动态范围。该器件支持 JESD204B 串行接口，数据传输速率高达 10Gbps，每个 ADC 可支持 2 或 4 条通道。已缓冲模拟输入在大大减少采样保持毛刺脉冲能量的同时，在宽频率范围内提供统一的输入阻抗。可选择将每个 ADC 通道连接至数字下变频器 (DDC) 模块。ADS54J60 以超低功耗在宽输入频率范围内提供出色的无杂散动态范围 (SFDR)。

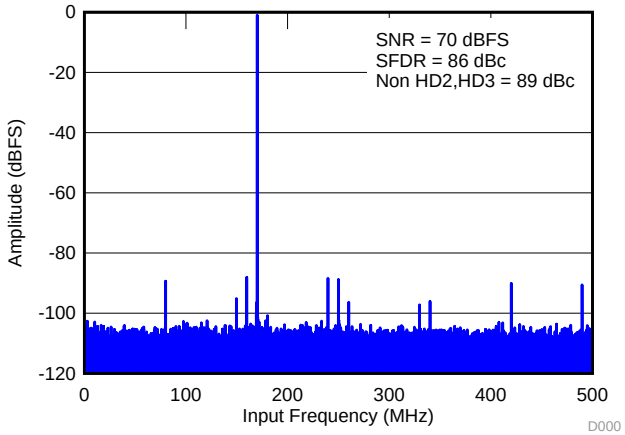
JESD204B 接口减少了接口线路数，从而实现高系统集成度。内部锁相环 (PLL) 会将 ADC 采样时钟加倍，以获得串行化各通道的 16 位数据时所使用的位时钟。

器件信息

器件型号	封装	封装尺寸（标称值）
ADS54J60	VQFNP (72)	10.00mm x 10.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

170MHz 输入信号的 FFT



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注：之前版本的页码可能与当前版本有所不同。

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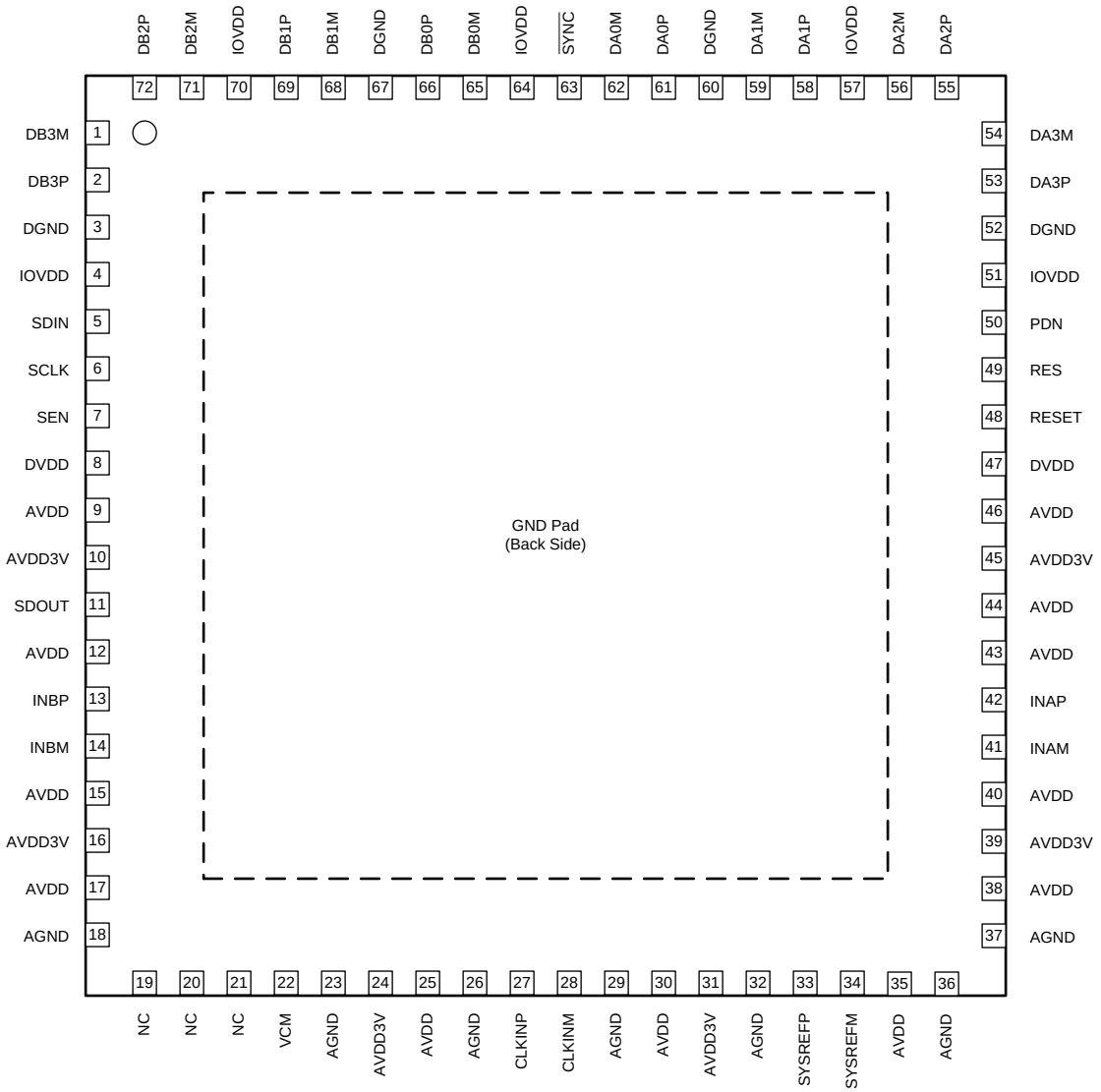
Changes from Revision A (May 2015) to Revision B **Page**

5 Device Comparison Table

PART NUMBER	SPEED GRADE (MSPS)	RESOLUTION (Bits)	CHANNEL
ADS54J20	1000	12	2
ADS54J42	625	14	2
ADS54J40	1000	14	2
ADS54J60	1000	16	2
ADS54J66	500	14	4
ADS54J69	500	16	2

6 Pin Configuration and Functions

RMP Package
72-Pin VQFNP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CLOCK, SYSREF			
CLKINM	28	I	Negative differential clock input for the ADC. The device has an internal 100-Ω termination resistor between the CLKINP and CLKINM pins.
CLKINP	27	I	Positive differential clock input for the ADC. The device has an internal 100-Ω termination resistor between the CLKINP and CLKINM pins.
SYSREFM	34	I	Negative external SYSREF input. Connect this pin to GND if not used.
SYSREFP	33	I	Positive external SYSREF input. Connect this pin to 1.8 V if not used.
CONTROL, SERIAL			
PDN	50	I/O	Power down, active low pin. Can be configured via an SPI register setting. Can be configured to fast overrange output for channel A via the SPI.
RESET	48	I	Hardware reset; active high. This pin has an internal 20-kΩ pulldown resistor.
SCLK	6	I	Serial interface clock input
SDIN	5	I	Serial interface data input
SDOUT	11	O	Serial interface data output. Can be configured to fast overrange output for channel B via the SPI.
SEN	7	I	Serial interface enable
DATA INTERFACE			
DA0M	62	O	JESD204B serial data negative outputs for channel A
DA1M	59		
DA2M	56		
DA3M	54		
DA0P	61	O	JESD204B serial data positive outputs for channel A
DA1P	58		
DA2P	55		
DA3P	53		
DB0M	65	O	JESD204B serial data negative outputs for channel B
DB1M	68		
DB2M	71		
DB3M	1		
DB0P	66	O	JESD204B serial data positive outputs for channel B
DB1P	69		
DB2P	72		
DB3P	2		
$\overline{\text{SYNC}}$	63	I	Synchronization input for JESD204B port
INPUT, COMMON MODE			
INAM	41	I	Differential analog negative input for channel A
INAP	42	I	Differential analog positive input for channel A
INBM	14	I	Differential analog negative input for channel B
INBP	13	I	Differential analog positive input for channel B
VCM	22	O	Common-mode voltage, 2.1 V. Note that analog inputs are internally biased to this pin through 600 Ω (effective), no external connection from the VCM pin to the INxP or INxM pin is required.
POWER SUPPLY			
AGND	18, 23, 26, 29, 32, 36, 37	I	Analog ground
AVDD	9, 12, 15, 17, 25, 30, 35, 38, 40, 43, 44, 46	I	Analog 1.9-V power supply
AVDD3V	10, 16, 24, 31, 39, 45	I	Analog 3.0-V power supply for the analog buffer
DGND	3, 52, 60, 67	I	Digital ground
DVDD	8, 47	I	Digital 1.9-V power supply
IOVDD	4, 51, 57, 64, 70	I	Digital 1.15-V power supply for the JESD204B transmitter
NC, RES			
NC	19-21	—	Unused pins, do not connect
RES	49	I	Reserved pin. Connect to DGND.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range	AVDD3V	–0.3	3.6	V
	AVDD	–0.3	2.1	
	DVDD	–0.3	2.1	
	IOVDD	–0.2	1.4	
Voltage between AGND and DGND		–0.3	0.3	V
Voltage applied to input pins	INAP, INBP, INAM, INBM	–0.3	3	V
	CLKINP, CLKINM	–0.3	AVDD + 0.3	
	SYSREFP, SYSREFM	–0.3	AVDD + 0.3	
	SCLK, SEN, SDIN, RESET, $\overline{\text{SYNC}}$, PDN	–0.2	2.1	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	NOM	MAX	UNIT
Supply voltage range	AVDD3V		2.85	3.0	3.6	V
	AVDD		1.8	1.9	2.0	
	DVDD		1.7	1.9	2.0	
	IOVDD		1.1	1.15	1.2	
Analog inputs	Differential input voltage range			1.9		V_{PP}
	Input common-mode voltage			2.0		V
	Maximum analog input frequency for 1.9-V_{PP} input amplitude(3)(4)			400		MHz
Clock inputs	Input clock frequency, device clock frequency		250(5)		1000	MHz
	Input clock amplitude differential ($V_{CLKP} - V_{CLKM}$)	Sine wave, ac-coupled	0.75	1.5		V_{PP}
		LVPECL, ac-coupled	0.8	1.6		
		LVDS, ac-coupled		0.7		
	Input device clock duty cycle		45%	50%	55%	
Temperature	Operating free-air, T_A		–40		85	°C
	Operating junction, T_J			105(6)	125	

(1) SYSREF must be applied for the device to initialize; see the *SYSREF Signal* section for details.
(2) After power-up, always use a hardware reset to reset the device for the first time; see Table 75 for details.
(3) Operating 0.5 dB below the maximum-supported amplitude is recommended to accommodate gain mismatch in interleaving ADCs.
(4) At high frequencies, the maximum supported input amplitude reduces; see Figure 37 for details.
(5) See Table 10.
(6) Prolonged use above the nominal junction temperature can increase the device failure-in-time (FIT) rate.

7.4 Thermal Information

THERMAL METRIC(1)		ADS54J60 RMP (VQFNP) 72 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	2.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	2.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, –1-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
	ADC sampling rate		250		1000	MSPS
	Resolution		16			Bits
POWER SUPPLIES						
AVDD3V	3.0-V analog supply		2.85	3.0	3.6	V
AVDD	1.9-V analog supply		1.8	1.9	2.0	V
DVDD	1.9-V digital supply		1.7	1.9	2.0	V
IOVDD	1.15-V SERDES supply		1.1	1.15	1.2	V
I_{AVDD3V}	3.0-V analog supply current	V_{IN} = full-scale on both channels		334	360	mA
I_{AVDD}	1.9-V analog supply current	V_{IN} = full-scale on both channels		359	510	mA
I_{DVDD}	1.9-V digital supply current	Eight lanes active (LMFS = 8224)		197	260	mA
I_{IOVDD}	1.15-V SERDES supply current	Eight lanes active (LMFS = 8224)		566	920	mA
P_{dis}	Total power dissipation	Eight lanes active (LMFS = 8224)		2.71	3.1	W
I_{DVDD}	1.9-V digital supply current	Four lanes active (LMFS = 4244)		211		mA
I_{IOVDD}	1.15-V SERDES supply current	Four lanes active (LMFS = 4244)		618		mA
P_{dis}	Total power dissipation	Four lanes active (LMFS = 4244)		2.80		W
I_{DVDD}	1.9-V digital supply current	Four lanes active (LMFS = 4222), 2X decimation		197		mA
I_{IOVDD}	1.15-V SERDES supply current	Four lanes active (LMFS = 4222), 2X decimation		593		mA
P_{dis}	Total power dissipation	Four lanes active (LMFS = 4222), 2X decimation		2.74		W
I_{DVDD}	1.9-V digital supply current	Two lanes active (LMFS = 2221), 4X decimation		176		mA
I_{IOVDD}	1.15-V SERDES supply current	Two lanes active (LMFS = 2221), 4X decimation		562		mA
P_{dis}(1)	Total power dissipation	Two lanes active (LMFS = 2221), 4X decimation		2.66		W
	Global power-down power dissipation			139	315	mW

(1) See the *Power-Down Mode* section for details.

Electrical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, –1-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS (INAP, INAM, INBP, INBM)						
	Differential input full-scale voltage			1.9		V_{PP}
V_{IC}	Common-mode input voltage			2.0		V
R_{IN}	Differential input resistance	At 170-MHz input frequency		0.6		kΩ
C_{IN}	Differential input capacitance	At 170-MHz input frequency		4.7		pF
	Analog input bandwidth (3 dB)	50-Ω source driving ADC inputs terminated with 50-Ω		1.2		GHz
CLOCK INPUT (CLKINP, CLKINM)						
	Internal clock biasing	CLKINP and CLKINM are connected to internal biasing voltage through 400-Ω		1.15		V

7.6 AC Characteristics

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, –1-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		70.9		dBFS
		f_{IN} = 100 MHz, A_{IN} = –1 dBFS		70.6		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS	67.2	70		
		f_{IN} = 230 MHz, A_{IN} = –1 dBFS		69.2		
		f_{IN} = 270 MHz, A_{IN} = –1 dBFS		68.7		
		f_{IN} = 300 MHz, A_{IN} = –1 dBFS		68.1		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS		67.1		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		67.6		
		f_{IN} = 720 MHz, A_{IN} = –6 dBFS		66		
		f_{IN} = 720 MHz, A_{IN} = –6 dBFS, gain = 5 dB		64.4		
NSD	Noise spectral density	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		157.9		dBFS/Hz
		f_{IN} = 100 MHz, A_{IN} = –1 dBFS		157.6		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS	154.2	157		
		f_{IN} = 230 MHz, A_{IN} = –1 dBFS		156.2		
		f_{IN} = 270 MHz, A_{IN} = –1 dBFS		155.7		
		f_{IN} = 300 MHz, A_{IN} = –1 dBFS		155.1		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS		154.1		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		154.6		
		f_{IN} = 720 MHz, A_{IN} = –6 dBFS		153		
		f_{IN} = 720 MHz, A_{IN} = –6 dBFS, gain = 5 dB		151.4		

AC Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, –1-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		70.7		dBFS
		f_{IN} = 100 MHz, A_{IN} = –1 dBFS		70.4		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS	67	69.8		
		f_{IN} = 230 MHz, A_{IN} = –1 dBFS		69.1		
		f_{IN} = 270 MHz, A_{IN} = –1 dBFS		68.3		
		f_{IN} = 300 MHz, A_{IN} = –1 dBFS		67.6		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS		66		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		66.8		
		f_{IN} = 720 MHz, A_{IN} = –6 dBFS		65.2		
		f_{IN} = 720 MHz, A_{IN} = –6 dBFS, gain = 5 dB		64.3		
SFDR	Spurious-free dynamic range (excluding IL spurs)	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		85		dBc
		f_{IN} = 100 MHz, A_{IN} = –1 dBFS		84		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS	78	88		
		f_{IN} = 230 MHz, A_{IN} = –1 dBFS		86		
		f_{IN} = 270 MHz, A_{IN} = –1 dBFS		81		
		f_{IN} = 300 MHz, A_{IN} = –1 dBFS		78		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS		73		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		72		
		f_{IN} = 720 MHz, A_{IN} = –6 dBFS		68		
		f_{IN} = 720 MHz, A_{IN} = –6 dBFS, gain = 5 dB		72		
HD2	Second-order harmonic distortion	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		85		dBc
		f_{IN} = 100 MHz, A_{IN} = –1 dBFS		92		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS	79	95		
		f_{IN} = 230 MHz, A_{IN} = –1 dBFS		86		
		f_{IN} = 270 MHz, A_{IN} = –1 dBFS		81		
		f_{IN} = 300 MHz, A_{IN} = –1 dBFS		81		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS		76		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		72		
		f_{IN} = 720 MHz, A_{IN} = –6 dBFS		68		
		f_{IN} = 720 MHz, A_{IN} = –6 dBFS, gain = 5 dB		72		
HD3	Third-order harmonic distortion	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		87		dBc
		f_{IN} = 100 MHz, A_{IN} = –1 dBFS		84		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS	82	89		
		f_{IN} = 230 MHz, A_{IN} = –1 dBFS		92		
		f_{IN} = 270 MHz, A_{IN} = –1 dBFS		82		
		f_{IN} = 300 MHz, A_{IN} = –1 dBFS		78		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS		73		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		70		
		f_{IN} = 720 MHz, A_{IN} = –6 dBFS		75		
		f_{IN} = 720 MHz, A_{IN} = –6 dBFS, gain = 5 dB		84		

AC Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, –1-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3, and IL spur)	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		94		dBFS
		f_{IN} = 100 MHz, A_{IN} = –1 dBFS		97		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS	79	93		
		f_{IN} = 230 MHz, A_{IN} = –1 dBFS		95		
		f_{IN} = 270 MHz, A_{IN} = –1 dBFS		95		
		f_{IN} = 300 MHz, A_{IN} = –1 dBFS		91		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS		85		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		90		
		f_{IN} = 720 MHz, A_{IN} = –6 dBFS		90		
		f_{IN} = 720 MHz, A_{IN} = –6 dBFS, gain = 5 dB		96		
THD	Total harmonic distortion	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		83		dBc
		f_{IN} = 100 MHz, A_{IN} = –1 dBFS		83		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS	74	87		
		f_{IN} = 230 MHz, A_{IN} = –1 dBFS		84		
		f_{IN} = 270 MHz, A_{IN} = –1 dBFS		78		
		f_{IN} = 300 MHz, A_{IN} = –1 dBFS		76		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS		71		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		71		
		f_{IN} = 720 MHz, A_{IN} = –6 dBFS		67		
		f_{IN} = 720 MHz, A_{IN} = –6 dBFS, gain = 5 dB		71		
ENOB	Effective number of bits	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		11.5		Bits
		f_{IN} = 100 MHz, A_{IN} = –1 dBFS		11.4		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS		11.3		
		f_{IN} = 230 MHz, A_{IN} = –1 dBFS		11.2		
		f_{IN} = 270 MHz, A_{IN} = –1 dBFS		11.0		
		f_{IN} = 300 MHz, A_{IN} = –1 dBFS		10.9		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS		10.7		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		10.8		
		f_{IN} = 720 MHz, A_{IN} = –6 dBFS		10.5		
		f_{IN} = 720 MHz, A_{IN} = –6 dBFS, gain = 5 dB		10.4		
SFDR_IL	Interleaving spur	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		88		dBc
		f_{IN} = 100 MHz, A_{IN} = –1 dBFS		90		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS	69	87		
		f_{IN} = 230 MHz, A_{IN} = –1 dBFS		85		
		f_{IN} = 270 MHz, A_{IN} = –1 dBFS		84		
		f_{IN} = 300 MHz, A_{IN} = –1 dBFS		82		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS		82		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		79		
		f_{IN} = 720 MHz, A_{IN} = –6 dBFS		79		
		f_{IN} = 720 MHz, A_{IN} = –6 dBFS, gain = 5 dB		75		

AC Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, –1-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IMD3	Two-tone, third-order intermodulation distortion	f_{IN1} = 185 MHz, f_{IN2} = 190 MHz, A_{IN} = –7 dBFS		–88		dBFS
		f_{IN1} = 365 MHz, f_{IN2} = 370 MHz, A_{IN} = –7 dBFS		–79		
		f_{IN1} = 465 MHz, f_{IN2} = 470 MHz, A_{IN} = –7 dBFS		–75		
	Crosstalk isolation between channel A and B	Full-scale, 170-MHz signal on aggressor; idle channel is victim		100		dB

7.7 Digital Characteristics

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, –1-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (RESET, SCLK, SEN, SDIN, $\overline{SYNC}$, PDN)(1)						
V_{IH}	High-level input voltage	All digital inputs support 1.2-V and 1.8-V logic levels	0.8			V
V_{IL}	Low-level input voltage	All digital inputs support 1.2-V and 1.8-V logic levels			0.4	V
I_{IH}	High-level input current	SEN		0		µA
		RESET, SCLK, SDIN, PDN, $\overline{SYNC}$		50		
I_{IL}	Low-level input current	SEN		50		µA
		RESET, SCLK, SDIN, PDN, $\overline{SYNC}$		0		
DIGITAL INPUTS (SYSREFP, SYSREFM)						
V_D	Differential input voltage		0.35	0.45	1.4	V
$V_{(CM\_DIG)}$	Common-mode voltage for SYSREF			1.3		V
DIGITAL OUTPUTS (SDOUT, PDN(2))						
V_{OH}	High-level output voltage		DVDD – 0.1	DVDD		V
V_{OL}	Low-level output voltage				0.1	V
DIGITAL OUTPUTS (JESD204B Interface: DxP, DxM)(3)						
V_{OD}	Output differential voltage	With default swing setting		700		mV_{PP}
V_{OC}	Output common-mode voltage			450		mV
	Transmitter short-circuit current	Transmitter pins shorted to any voltage between –0.25 V and 1.45 V	–100		100	mA
z_{os}	Single-ended output impedance			50		Ω
	Output capacitance	Output capacitance inside the device, from either output to ground		2		pF

(1) The RESET, SCLK, SDIN, and PDN pins have a 20-kΩ (typical) internal pulldown resistor to ground, and the SEN pin has a 20-kΩ (typical) pullup resistor to IOVDD.
(2) When functioning as an OVR pin for channel B.
(3) 100-Ω differential termination.

7.8 Timing Requirements

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input (unless otherwise noted)

		MIN	TYP	MAX	UNITS
SAMPLE TIMING					
	Aperture delay	0.75		1.6	ns
	Aperture delay matching between two channels on the same device		±70		ps
	Aperture delay matching between two devices at the same temperature and supply voltage		±270		ps
	Aperture jitter		120		f_S rms
WAKE-UP TIMING					
	Wake-up time to valid data after coming out of global power-down		150		µs
LATENCY (1)					
	Data latency: ADC sample to digital output		134		Input clock cycles
	OVR latency: ADC sample to OVR bit		62		Input clock cycles
	FOVR latency: ADC sample to FOVR signal on pin		18		Input clock cycles
t_{PDI}	Propagation delay: logic gates and output buffers delay (does not change with f_S)		4		ns
SYSREF TIMING					
t_{SU_SYSREF}	Setup time for SYSREF, referenced to the input clock falling edge	300		900	ps
t_{H_SYSREF}	Hold time for SYSREF, referenced to the input clock falling edge	100			ps
JESD OUTPUT INTERFACE TIMING CHARACTERISTICS					
	Unit interval	100		400	ps
	Serial output data rate	2.5		10	Gbps
	Total jitter for BER of 1E-15 and lane rate = 10 Gbps		26		ps
	Random jitter for BER of 1E-15 and lane rate = 10 Gbps		0.75		ps rms
	Deterministic jitter for BER of 1E-15 and lane rate = 10 Gbps		12		ps, pk-pk
t_R, t_F	Data rise time, data fall time: rise and fall times are measured from 20% to 80%, differential output waveform, 2.5 Gbps ≤ bit rate ≤ 10 Gbps		35		ps

(1) Overall latency = latency + t_{PDI}.

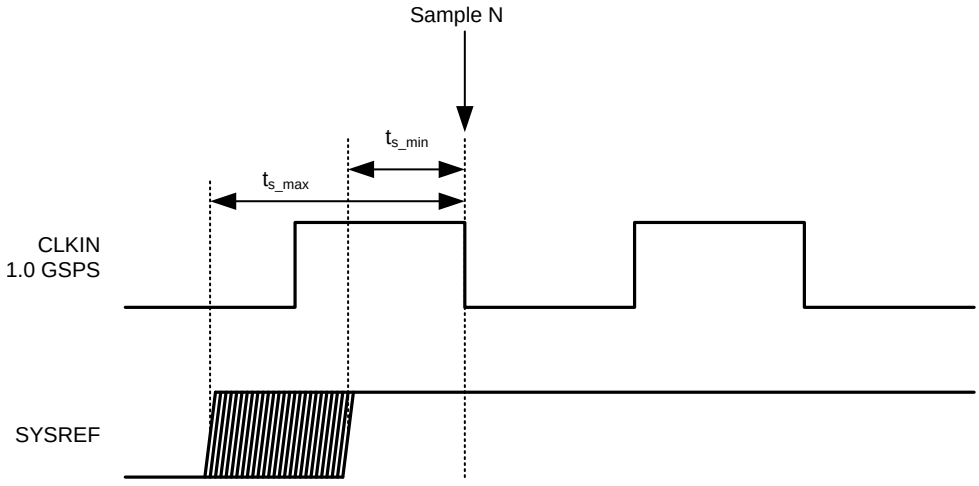


Figure 1. SYSREF Timing

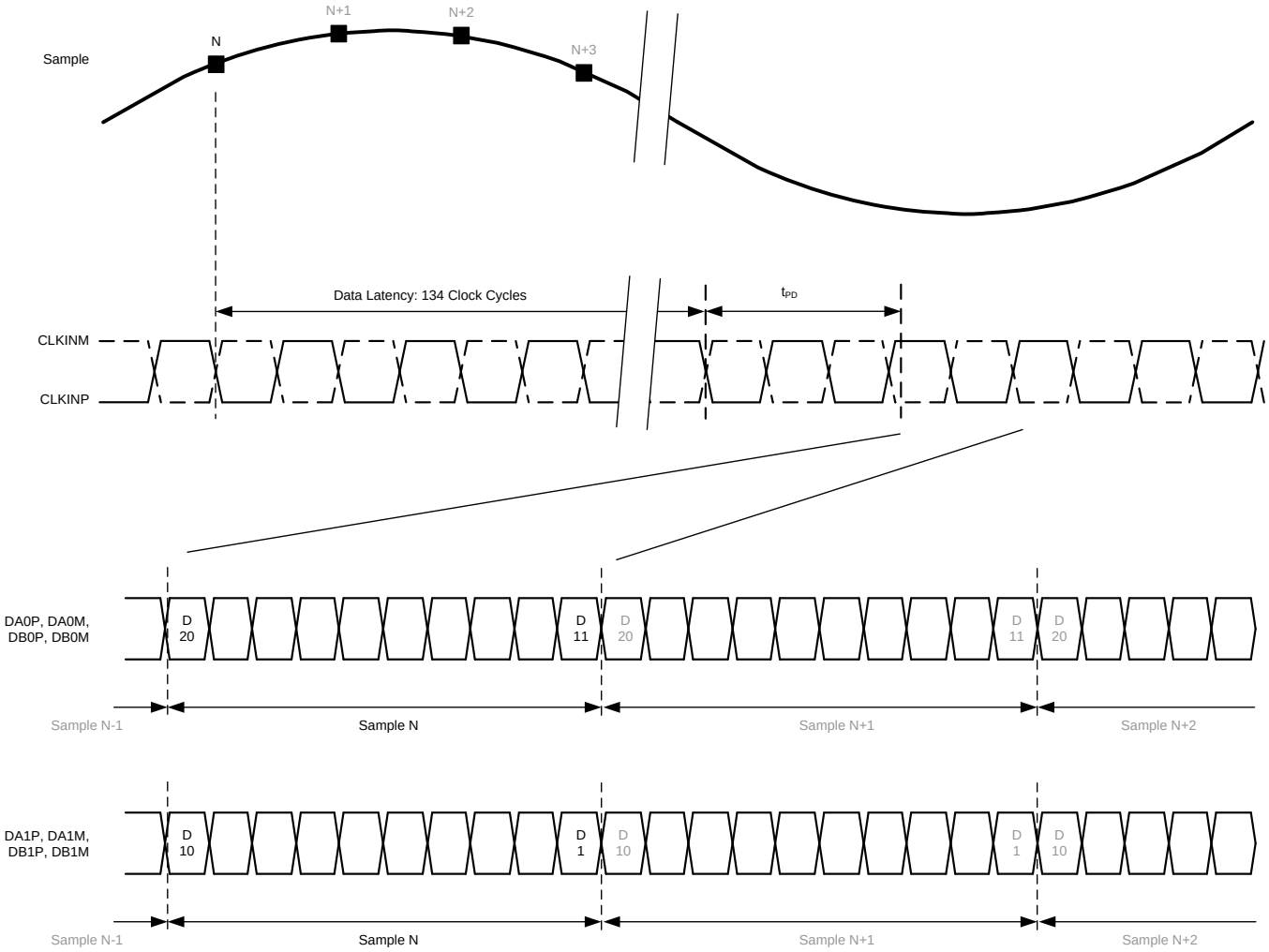
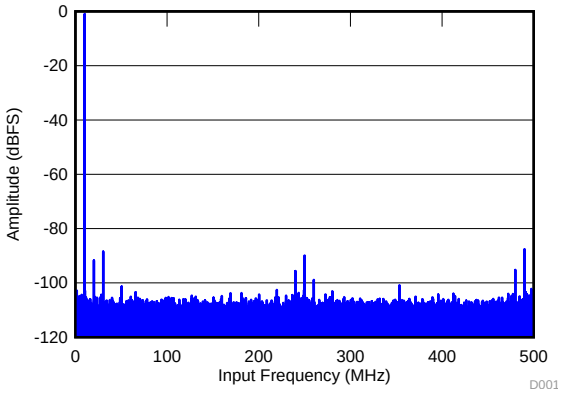


Figure 2. Sample Timing Requirements Diagram

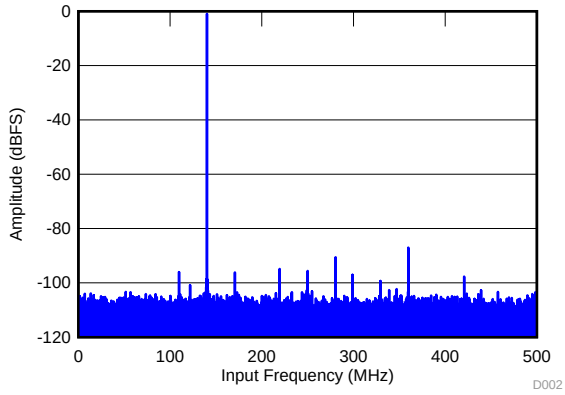
7.9 Typical Characteristics

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input (unless otherwise noted)



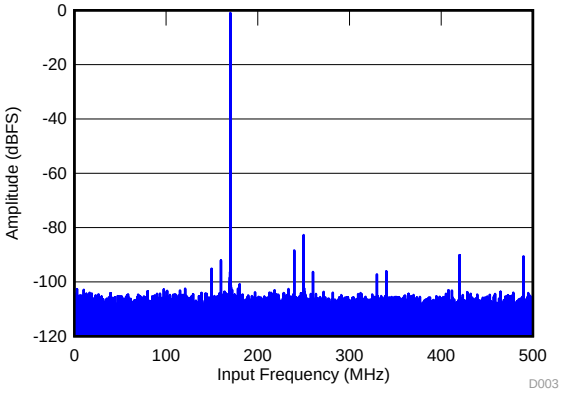
SNR = 71 dBFS; SFDR = 86 dBc;
IL spur = 94 dBc; non HD2, HD3 spur = 89 dBc

Figure 3. FFT for 10-MHz Input Signal



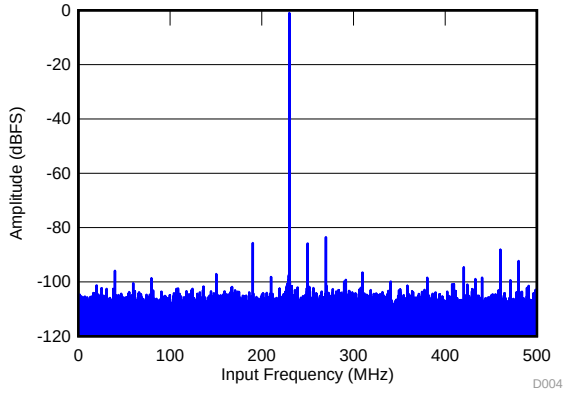
SNR = 70.3 dBFS; SFDR = 90 dBc;
IL spur = 95 dBc; non HD2, HD3 spur = 94 dBc

Figure 4. FFT for 140-MHz Input Signal



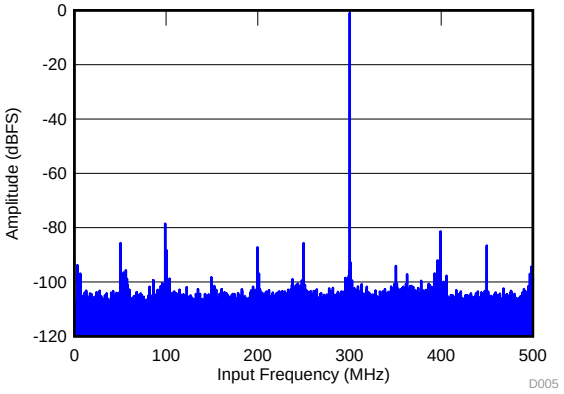
SNR = 69.8 dBFS; SFDR = 88 dBc;
IL spur = 86 dBc; non HD2, HD3 spur = 89 dBc

Figure 5. FFT for 170-MHz Input Signal



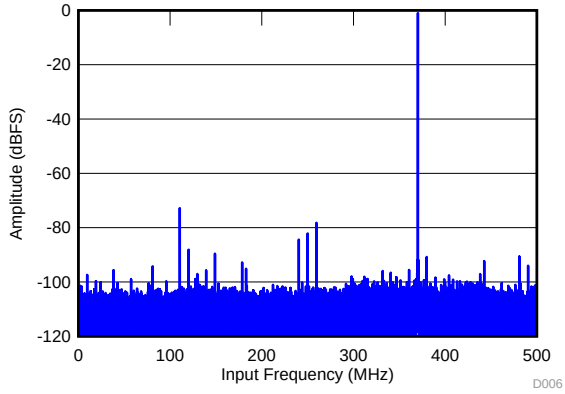
SNR = 68.9 dBFS; SFDR = 85 dBc;
IL spur = 85 dBc; non HD2, HD3 spur = 86 dBc

Figure 6. FFT for 230-MHz Input Signal



SNR = 68 dBFS; SFDR = 77 dBc;
IL spur = 84 dBc; non HD2, HD3 spur = 85 dBc

Figure 7. FFT for 300-MHz Input Signal

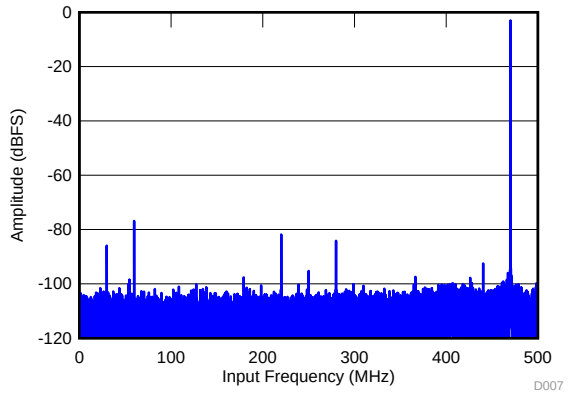


SNR = 66.7 dBFS; SFDR = 71 dBc;
IL spur = 87 dBc; non HD2, HD3 spur = 78 dBc

Figure 8. FFT for 370-MHz Input Signal

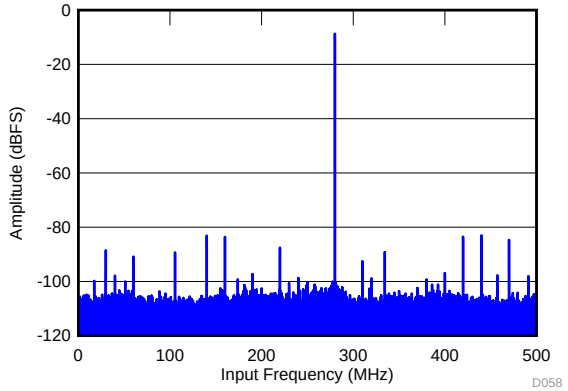
Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input (unless otherwise noted)



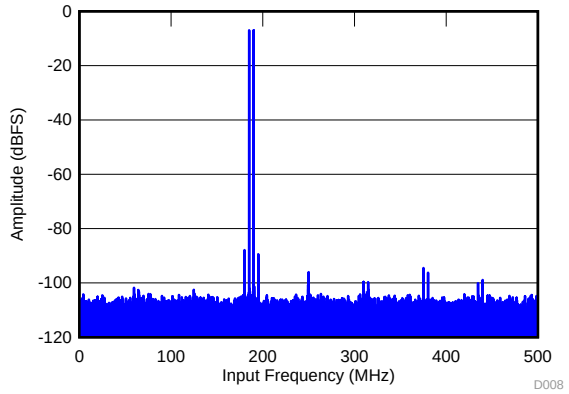
SNR = 67.9 dBFS; SFDR = 74 dBc;
IL spur = 82 dBc; non HD2, HD3 spur = 89 dBc

Figure 9. FFT for 470-MHz Input Signal at –3 dBFS



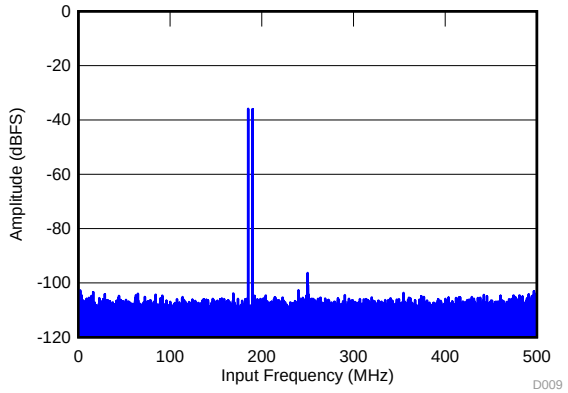
SNR = 66.3 dBFS, SINAD = 65.3 dBFS, THD = 70 dBc,
IL spur = 84 dBc, SFDR = 73 dBc, non HD2, HD3 spur = 90 dBFS

Figure 10. FFT for 720-MHz Input Signal at –6 dBFS



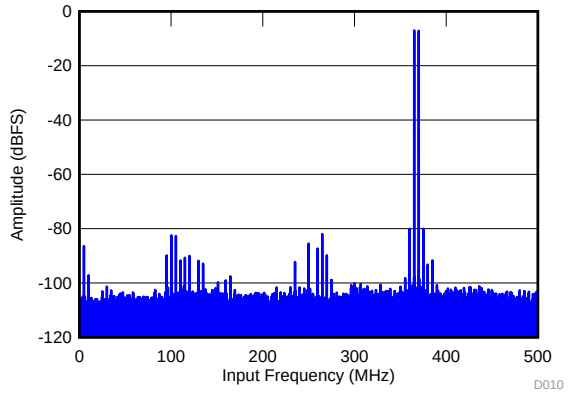
f_{IN1} = 185 MHz, f_{IN2} = 190 MHz, each tone at –7 dBFS,
IMD3 = 88 dBFS

Figure 11. FFT for Two-Tone Input Signal (–7 dBFS)



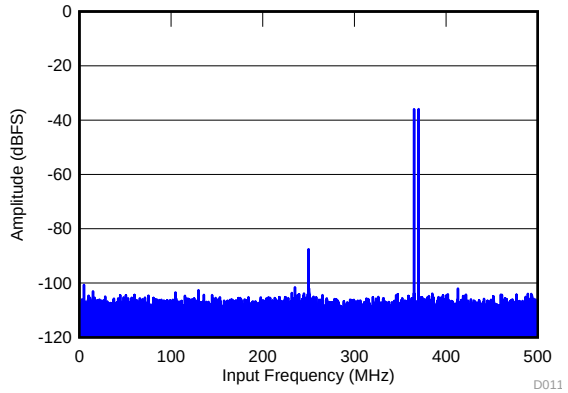
f_{IN1} = 185 MHz, f_{IN2} = 190 MHz, each tone at –36 dBFS,
IMD3 = 106 dBFS

Figure 12. FFT for Two-Tone Input Signal (–36 dBFS)



f_{IN1} = 365 MHz, f_{IN2} = 370 MHz, each tone at –7 dBFS,
IMD3 = 80 dBFS

Figure 13. FFT for Two-Tone Input Signal (–7 dBFS)

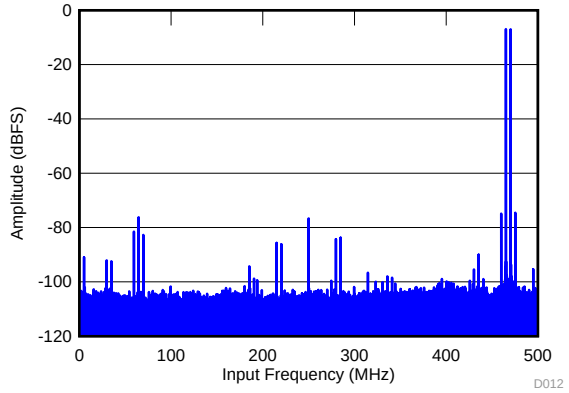


f_{IN1} = 365 MHz, f_{IN2} = 370 MHz, each tone at –36 dBFS,
IMD3 = 105 dBFS

Figure 14. FFT for Two-Tone Input Signal (–36 dBFS)

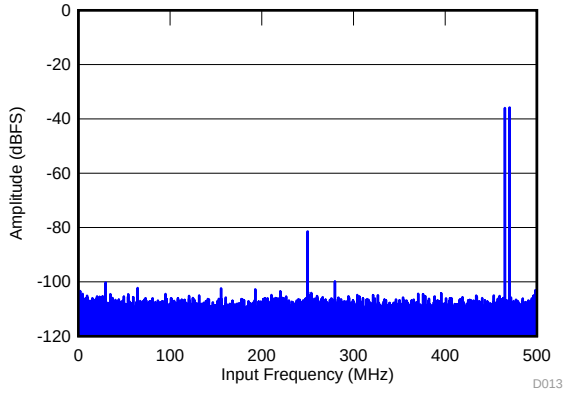
Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input (unless otherwise noted)



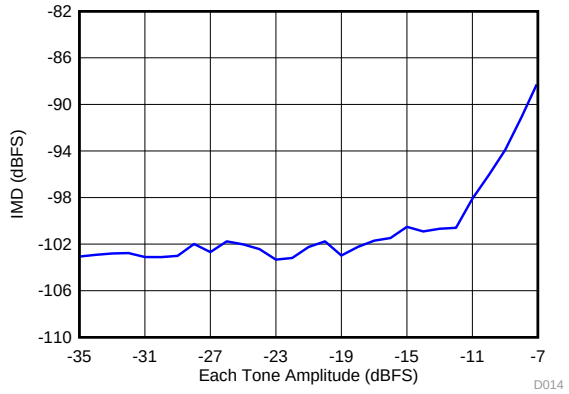
f_{IN1} = 465 MHz, f_{IN2} = 470 MHz, each tone at –7 dBFS, IMD3 = 75 dBFS

Figure 15. FFT for Two-Tone Input Signal (–7 dBFS)



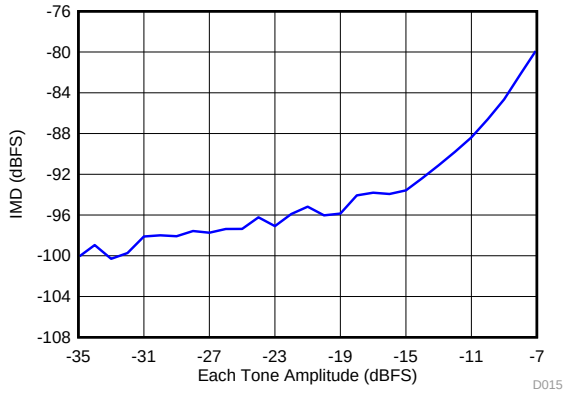
f_{IN1} = 465 MHz, f_{IN2} = 470 MHz, each tone at –36 dBFS, IMD3 = 106 dBFS

Figure 16. FFT for Two-Tone Input Signal (–36 dBFS)



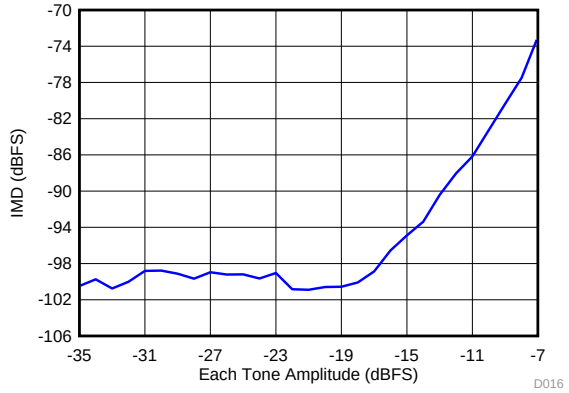
f_{IN1} = 185 MHz, f_{IN2} = 190 MHz

Figure 17. Intermodulation Distortion vs Input Tone Amplitude



f_{IN1} = 365 MHz, f_{IN2} = 370 MHz

Figure 18. Intermodulation Distortion vs Input Tone Amplitude



f_{IN1} = 465 MHz, f_{IN2} = 470 MHz

Figure 19. Intermodulation Distortion vs Input Tone Amplitude

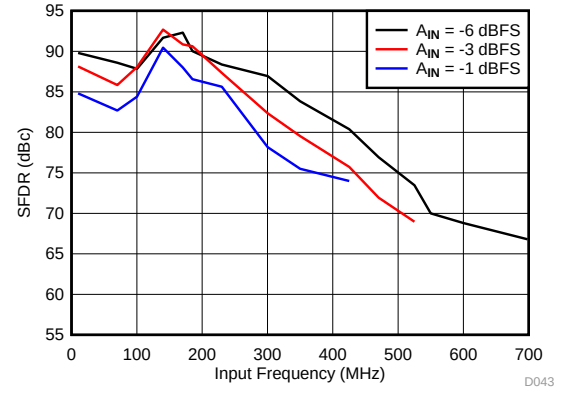


Figure 20. Spurious-Free Dynamic Range vs Input Frequency

Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input (unless otherwise noted)

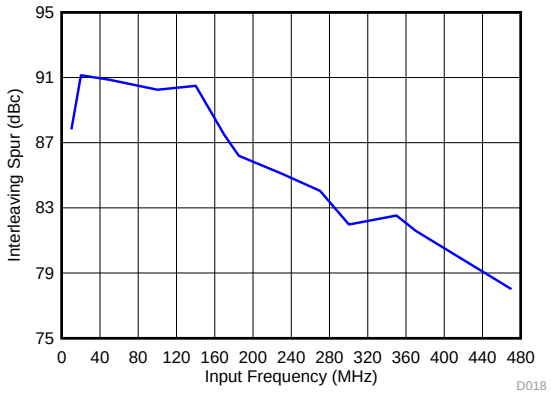


Figure 21. IL Spur vs Input Frequency

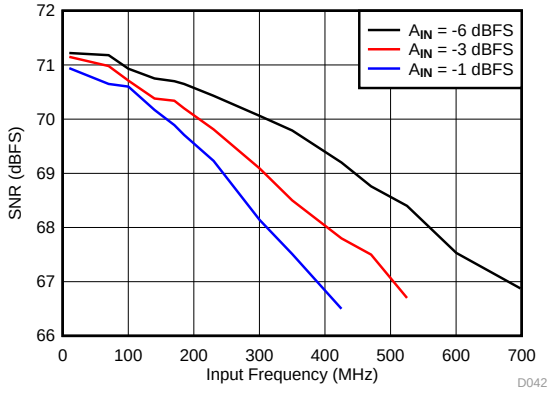
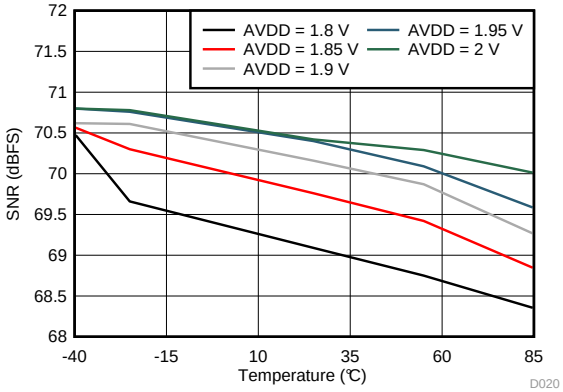
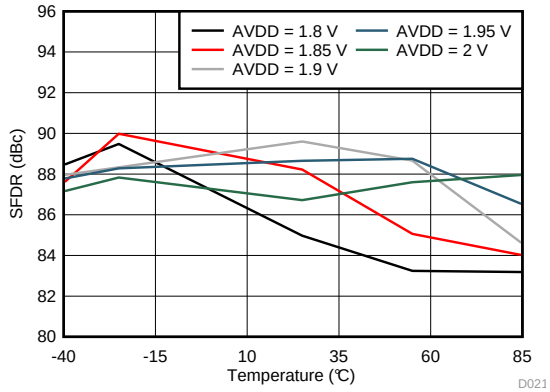


Figure 22. Signal-to-Noise Ratio vs Input Frequency



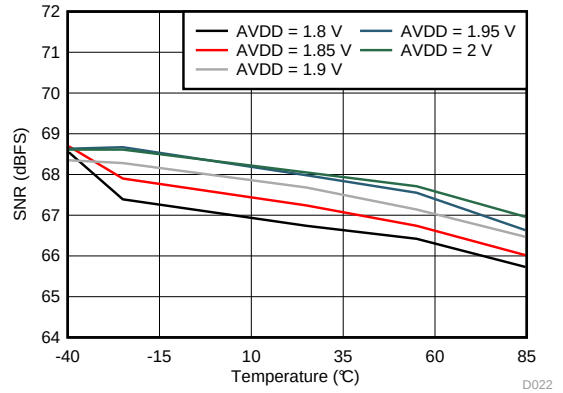
f_{IN} = 170 MHz

Figure 23. Signal-to-Noise Ratio vs AVDD Supply and Temperature



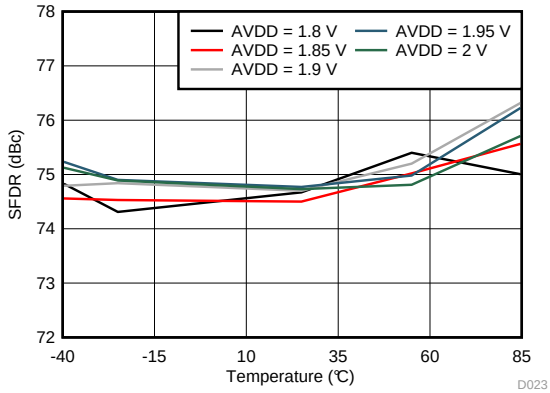
f_{IN} = 170 MHz

Figure 24. Spurious-Free Dynamic Range vs AVDD Supply and Temperature



f_{IN} = 350 MHz

Figure 25. Signal-to-Noise Ratio vs AVDD Supply and Temperature

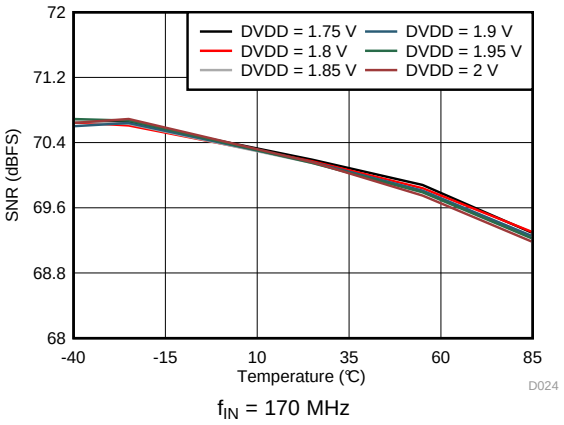


f_{IN} = 350 MHz

Figure 26. Spurious-Free Dynamic Range vs AVDD Supply and Temperature

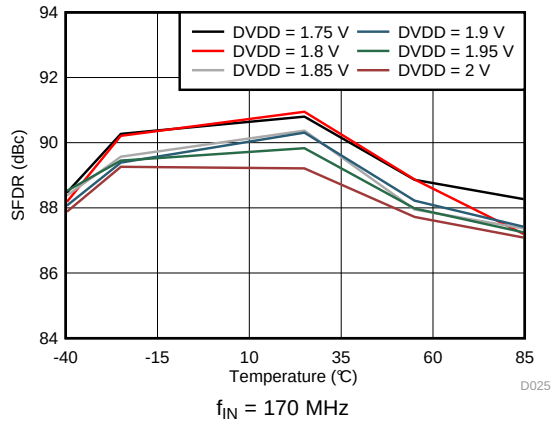
Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input (unless otherwise noted)



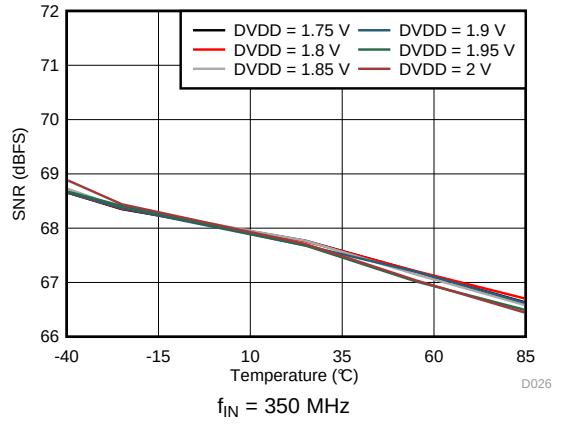
f_{IN} = 170 MHz

Figure 27. Signal-to-Noise Ratio vs DVDD Supply and Temperature



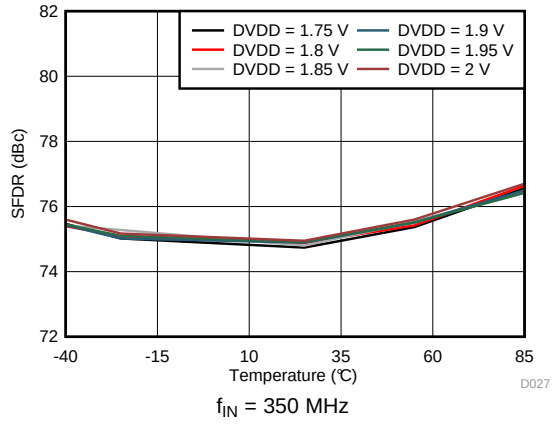
f_{IN} = 170 MHz

Figure 28. Spurious-Free Dynamic Range vs DVDD Supply and Temperature



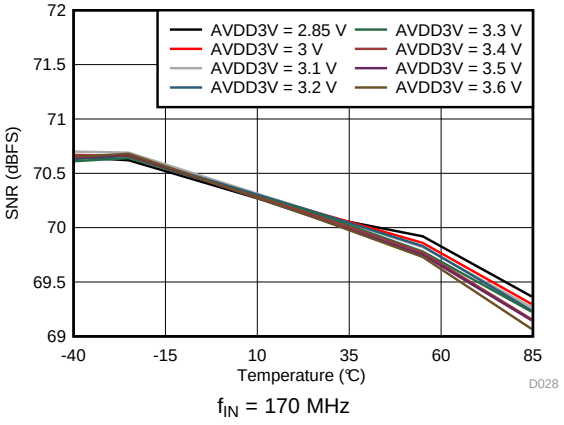
f_{IN} = 350 MHz

Figure 29. Signal-to-Noise Ratio vs DVDD Supply and Temperature



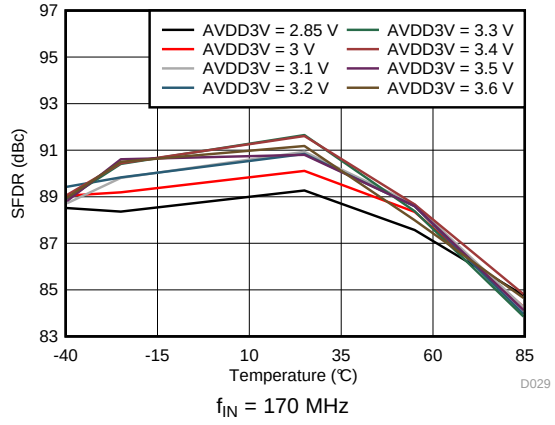
f_{IN} = 350 MHz

Figure 30. Spurious-Free Dynamic Range vs DVDD Supply and Temperature



f_{IN} = 170 MHz

Figure 31. Signal-to-Noise Ratio vs AVDD3V Supply and Temperature



f_{IN} = 170 MHz

Figure 32. Spurious-Free Dynamic Range vs AVDD3V Supply and Temperature

Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input (unless otherwise noted)

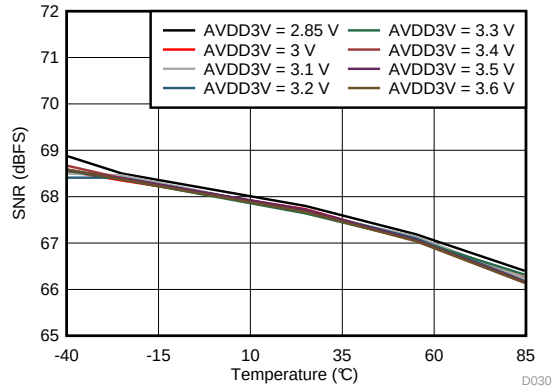


Figure 33. Signal-to-Noise Ratio vs AVDD3V Supply and Temperature

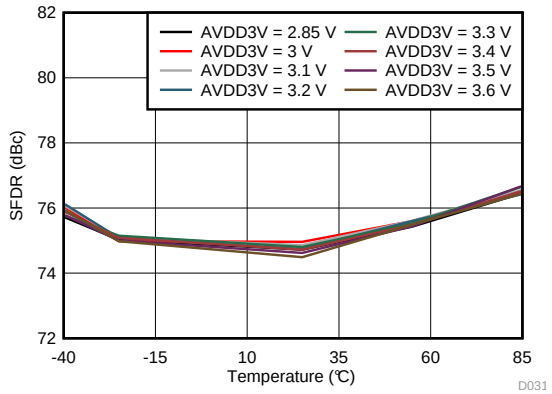


Figure 34. Spurious-Free Dynamic Range vs AVDD3V Supply and Temperature

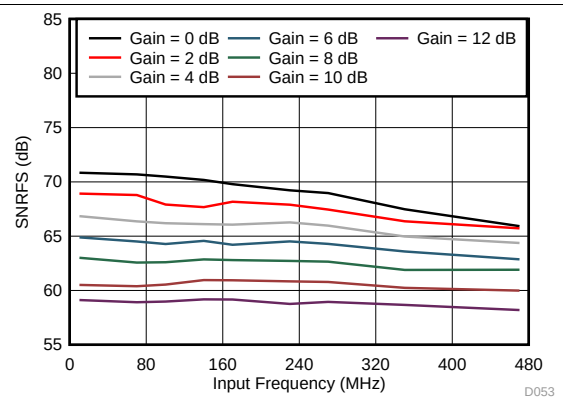


Figure 35. Signal-to-Noise Ratio vs Gain and Input Frequency

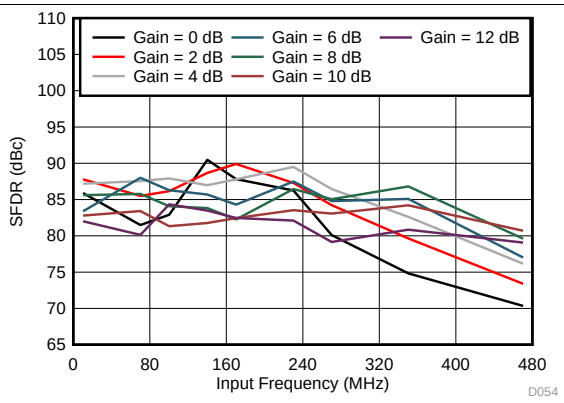


Figure 36. Spurious-Free Dynamic Range vs Gain and Input Frequency

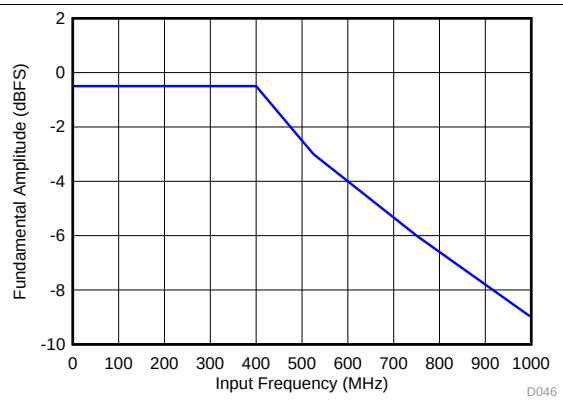


Figure 37. Maximum Supported Amplitude vs Frequency

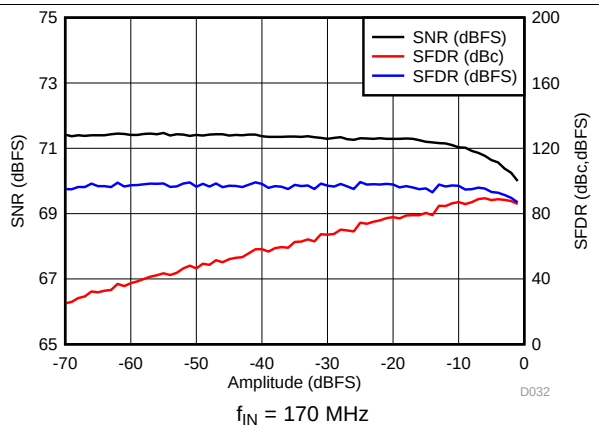
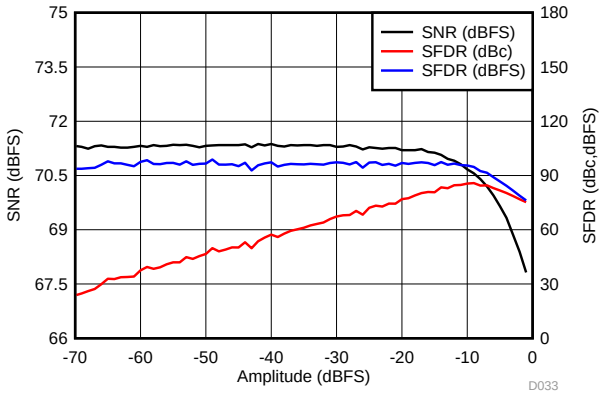


Figure 38. Performance vs Input Amplitude

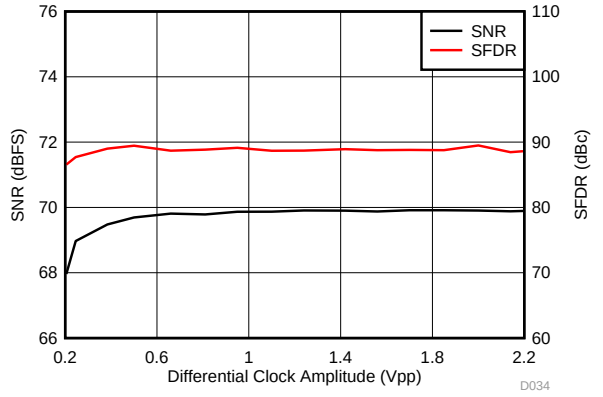
Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input (unless otherwise noted)



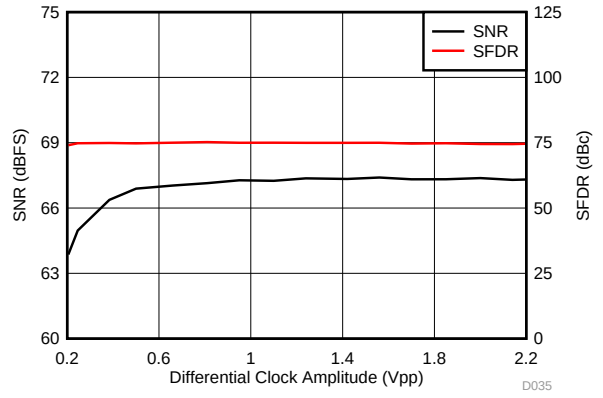
f_{IN} = 350 MHz

Figure 39. Performance vs Input Amplitude



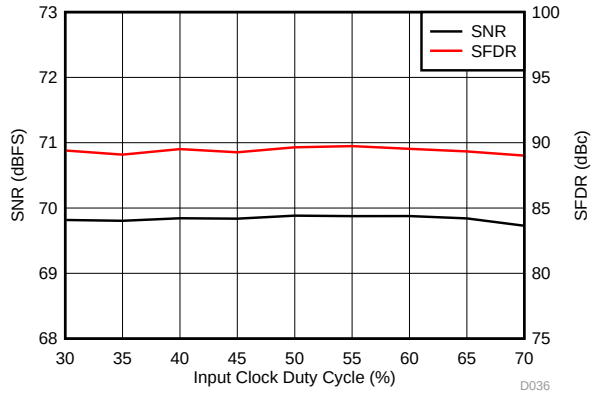
f_{IN} = 170 MHz

Figure 40. Performance vs Sampling Clock Amplitude



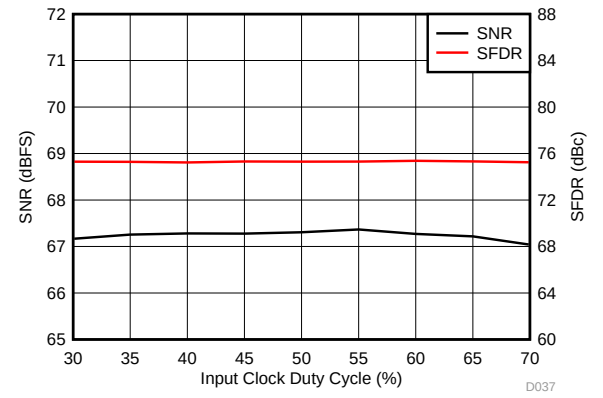
f_{IN} = 350 MHz

Figure 41. Performance vs Sampling Clock Amplitude



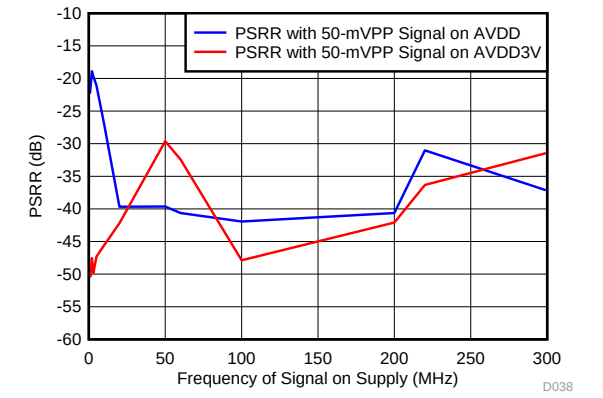
f_{IN} = 170 MHz

Figure 42. Performance vs Clock Duty Cycle



f_{IN} = 350 MHz

Figure 43. Performance vs Clock Duty Cycle

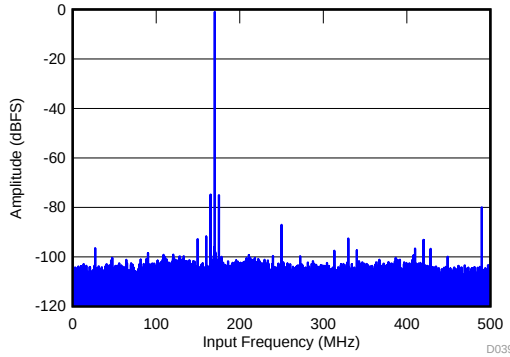


f_{IN} = 170 MHz

Figure 44. Power-Supply Rejection Ratio vs Test Signal Frequency

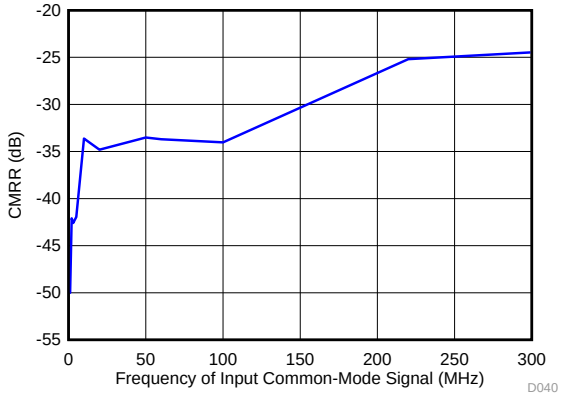
Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input (unless otherwise noted)



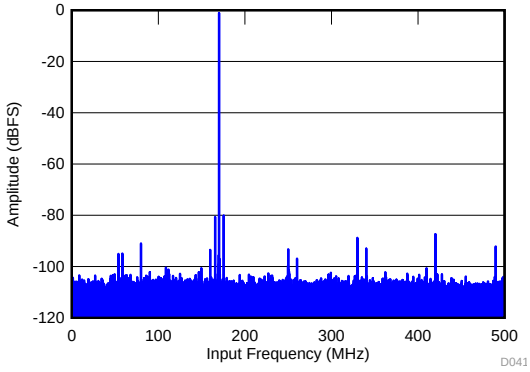
f_{IN} = 170 MHz , A_{IN} = –1 dBFS, SINAD = 67 dBFS, SFDR = 79 dBc, f_{PSRR} = 5 MHz, A_{PSRR} = 25 mV_{PP}, amplitude of $f_{IN} - f_{PSRR}$ = –74 dBFS, amplitude of $f_{IN} + f_{PSRR}$ = –76 dBFS

Figure 45. Power-Supply Rejection Ratio FFT for Test Signals on the AVDD Supply



f_{IN} = 170 MHz

Figure 46. Common-Mode Rejection Ratio vs Test Signal Frequency



f_{IN} = 170 MHz , A_{IN} = –1 dBFS, f_{CMRR} = 5 MHz, A_{CMRR} = 50 mV_{PP}, SINAD = 69.1 dBFS, SFDR = 86 dBc, amplitude of $f_{IN} \pm f_{CMRR}$= –80 dBFS

Figure 47. Common-Mode Rejection Ratio FFT

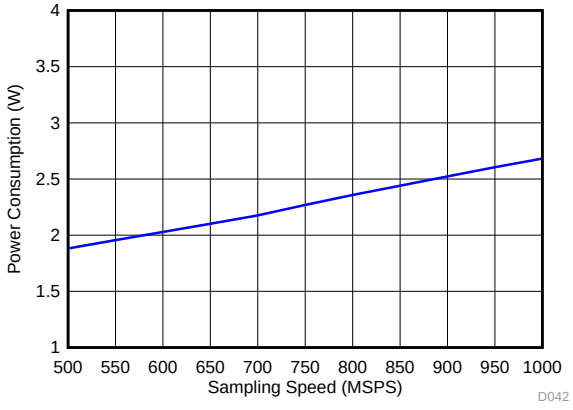


Figure 48. Power vs Sampling Speed

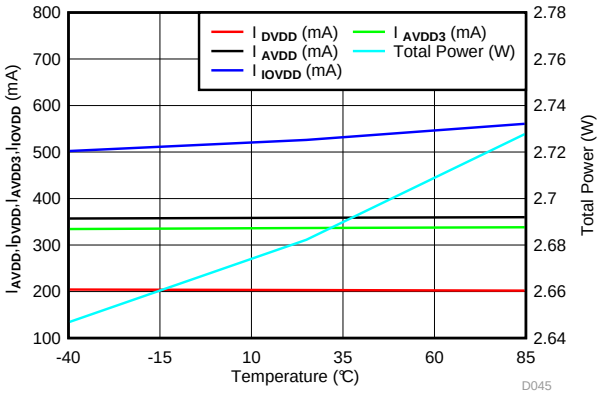
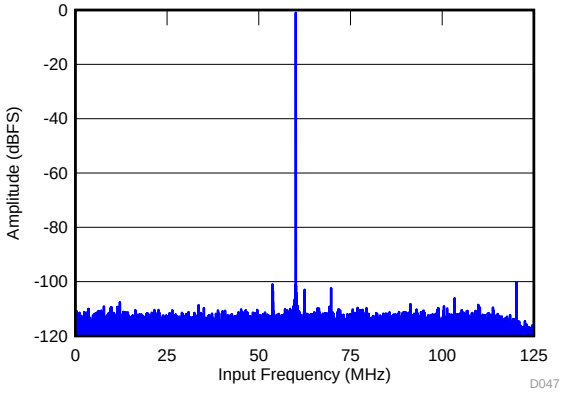


Figure 49. Power vs Temperature

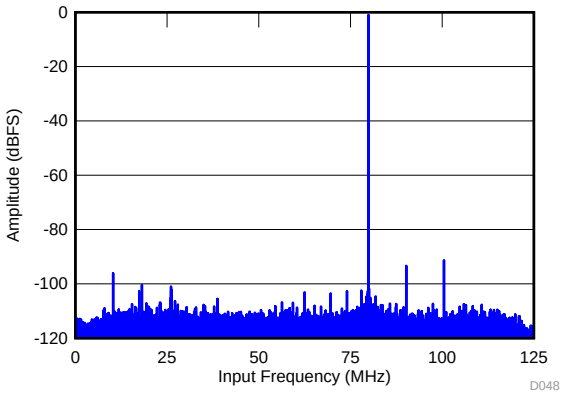


SNR = 76.4 dBFS, SFDR = 99 dBc

Figure 50. FFT for 60-MHz Input Signal in Decimate-by-4 Mode

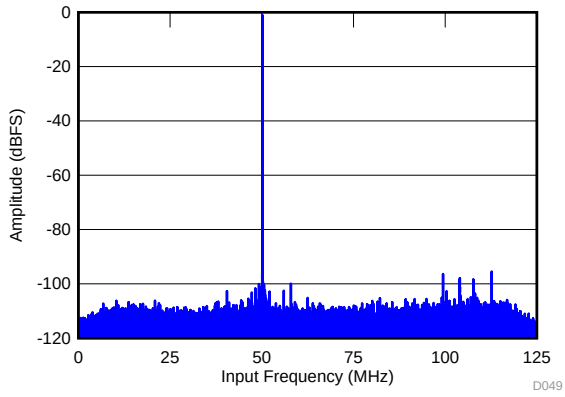
Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input (unless otherwise noted)



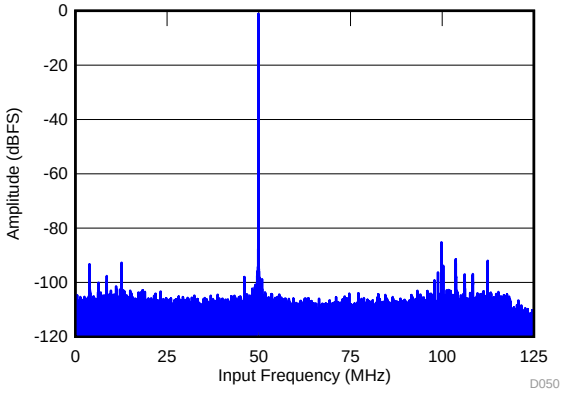
SNR = 75.2 dBFS, SFDR = 90 dBc

Figure 51. FFT for 170-MHz Input Signal in Decimate-by-4 Mode



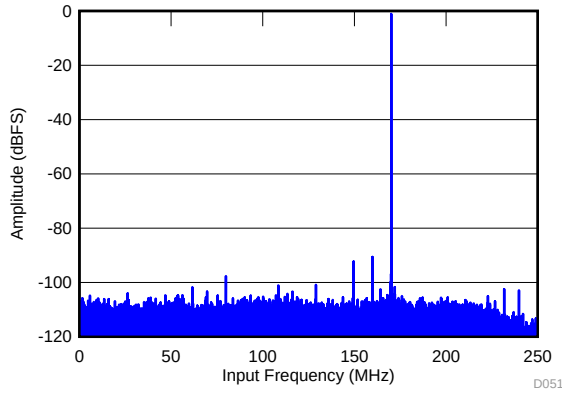
SNR = 72.8 dBFS, SFDR = 91 dBc

Figure 52. FFT for 300-MHz Input Signal in Decimate-by-4 Mode



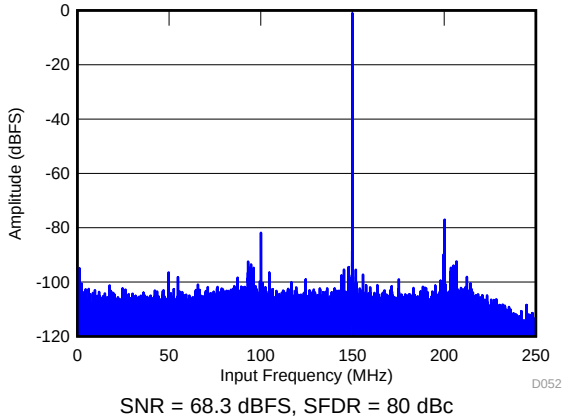
SNR = 69.6 dBFS, SFDR = 84 dBc

Figure 53. FFT for 450-MHz Input Signal in Decimate-by-4 Mode



SNR = 71.9 dBFS, SFDR = 89 dBc

Figure 54. FFT for 170-MHz Input Signal in Decimate-by-2 Mode



SNR = 68.3 dBFS, SFDR = 80 dBc

Figure 55. FFT for 350-MHz Input Signal in Decimate-by-2 Mode

7.10 Typical Characteristics: Contour

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, ADC sampling rate = 1.0 GSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, –1-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

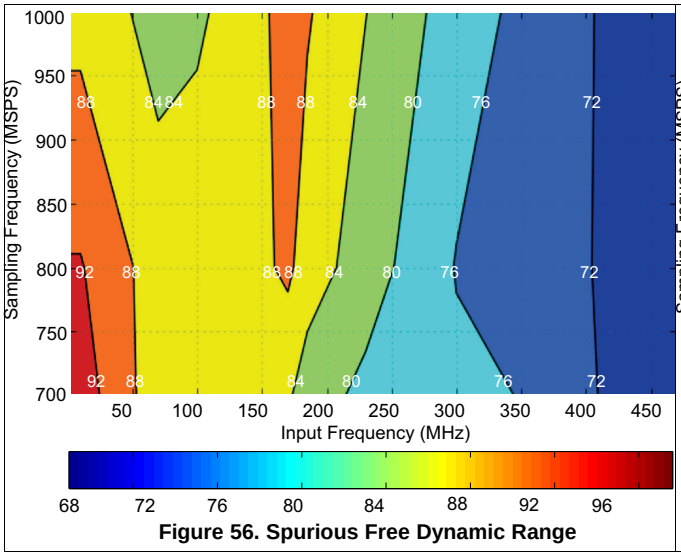


Figure 56. Spurious Free Dynamic Range

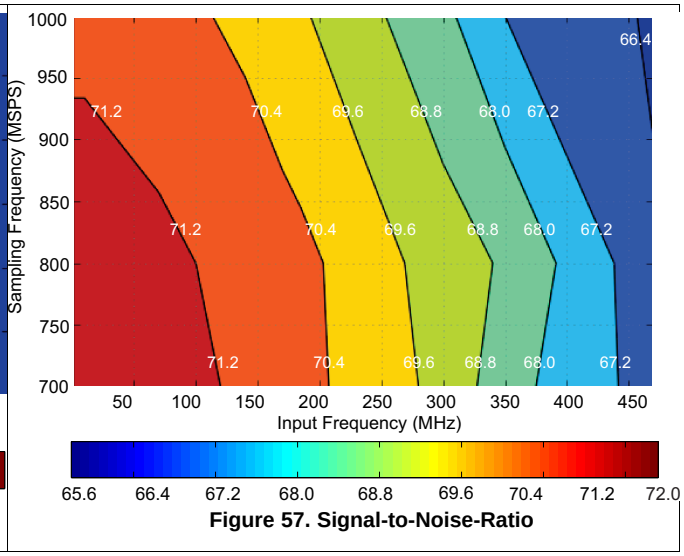


Figure 57. Signal-to-Noise-Ratio

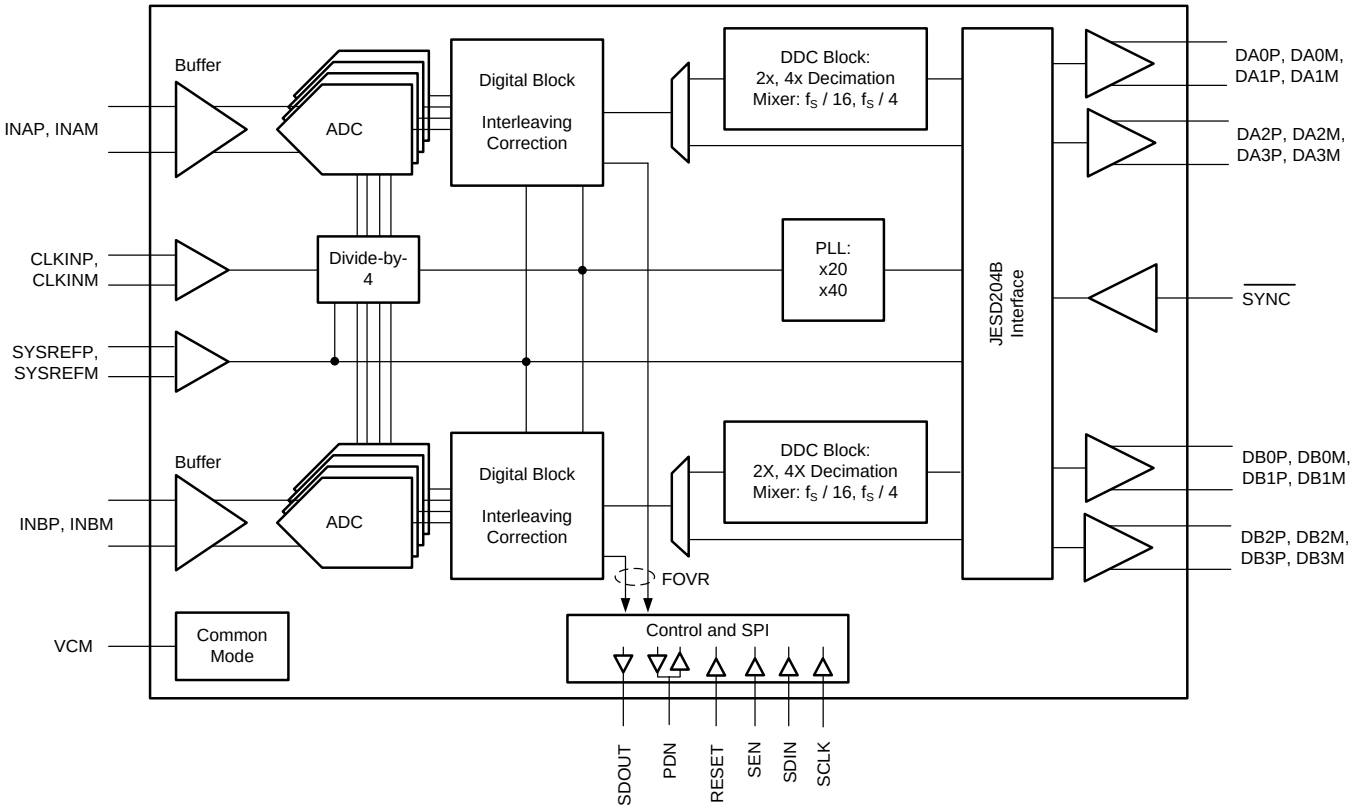
8 Detailed Description

8.1 Overview

The ADS54J60 is a low-power, wide-bandwidth, 16-bit, 1.0-GSPS, dual-channel, analog-to-digital converter (ADC). The ADS54J60 employs four interleaving ADCs for each channel to achieve a noise floor of –159 dBFS/Hz. The ADS54J60 uses TI's proprietary interleaving and dither algorithms to achieve a clean spectrum with a high spurious-free dynamic range (SFDR). The device also offers various programmable decimation filtering options for systems requiring higher signal-to-noise ratio (SNR) and SFDR over a wide range of frequencies.

Analog input buffers isolate the ADC driver from glitch energy generated from sampling process, thereby simplify the driving network on-board. The JESD204B interface reduces the number of interface lines with two-lane and four-lane options, allowing a high system integration density. The JESD204B interface operates in subclass 1, enabling multi-chip synchronization with the SYSREF input.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Analog Inputs

The ADS54J60 analog signal inputs are designed to be driven differentially. The analog input pins have internal analog buffers that drive the sampling circuit. As a result of the analog buffer, the input pins present a high impedance input across a very wide frequency range to the external driving source, which enables great flexibility in the external analog filter design as well as excellent 50-Ω matching for RF applications. The buffer also helps isolate the external driving circuit from the internal switching currents of the sampling circuit, resulting in a more constant SFDR performance across input frequencies.

The common-mode voltage of the signal inputs is internally biased to VCM using 600-Ω resistors, allowing for ac-coupling of the input drive network. Each input pin (INP, INM) must swing symmetrically between (VCM + 0.475 V) and (VCM – 0.475 V), resulting in a 1.9-V_{PP} (default) differential input swing. The input sampling circuit has a 3-dB bandwidth that extends up to 1.2 GHz. An equivalent analog input network diagram is shown in Figure 58.

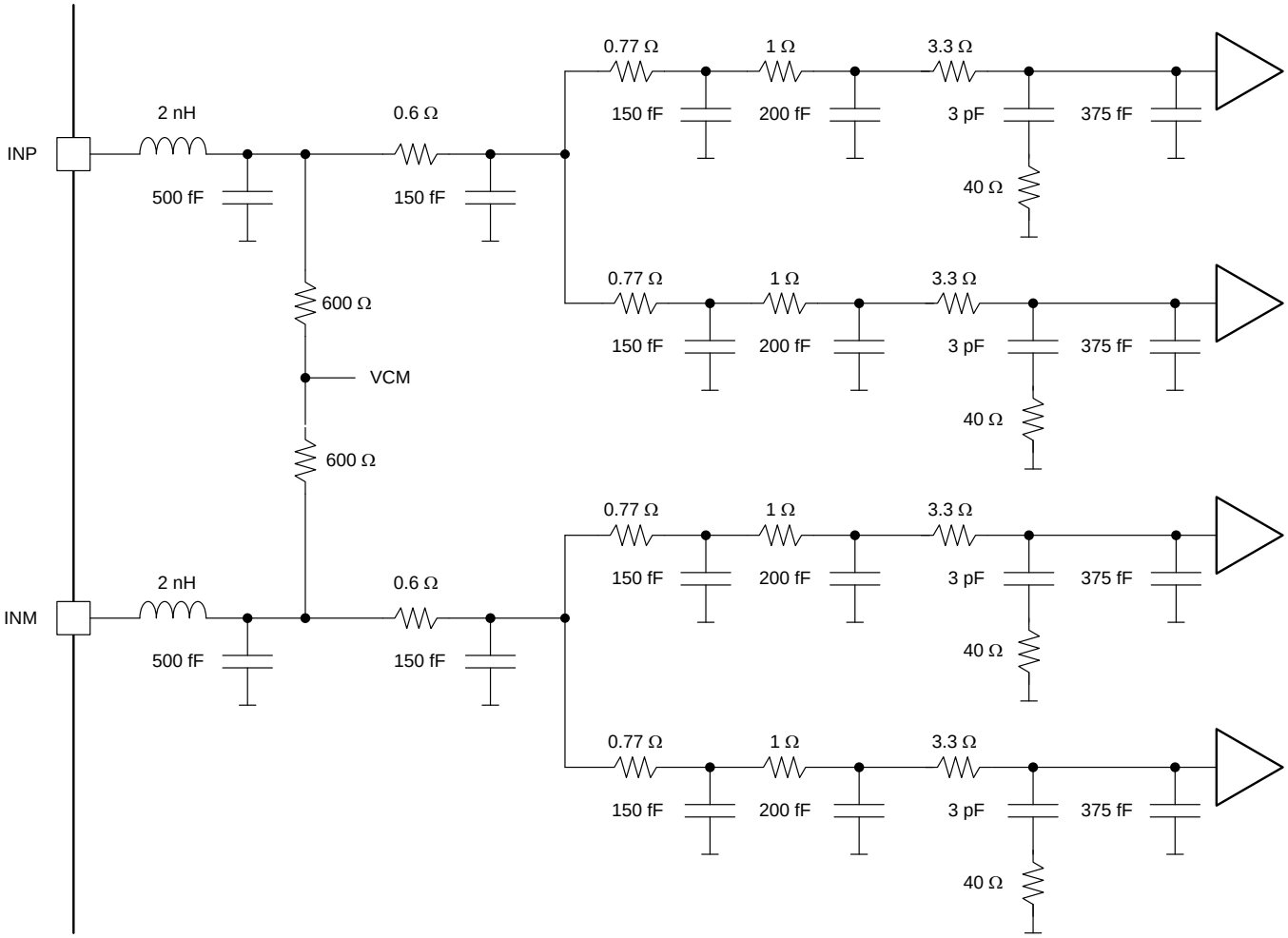


Figure 58. Analog Input Network

Feature Description (continued)

The input bandwidth shown in Figure 59 is measured with respect to a 50-Ω differential input termination at the ADC input pins. Figure 60 shows the signal processing done inside the DDC block of the ADS54J60.

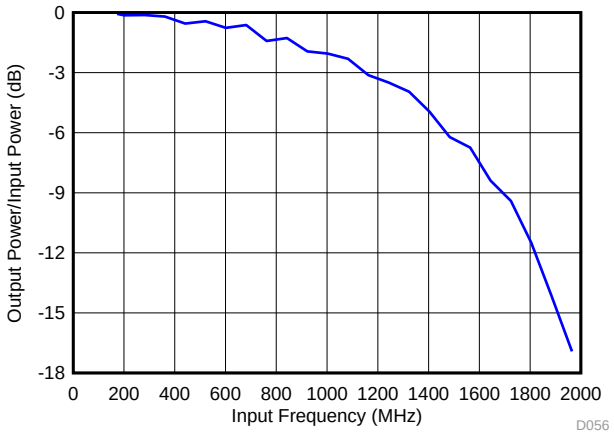
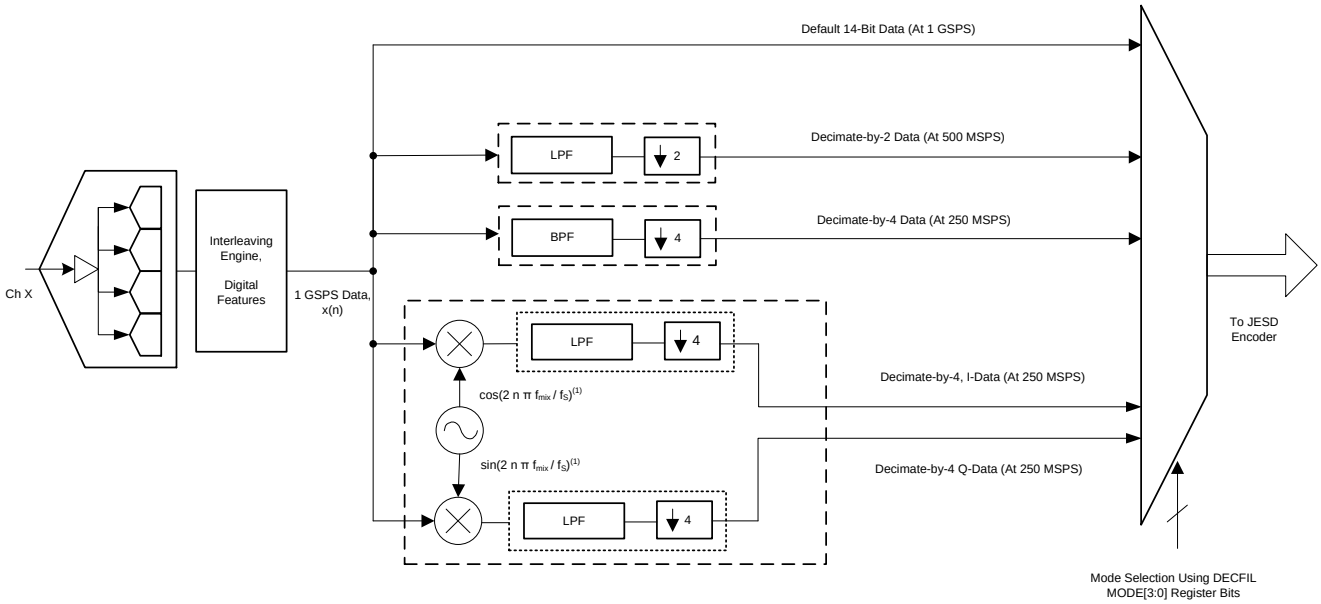


Figure 59. Transfer Function versus Frequency



(1) In IQ decimate-by-4 mode, the mixer frequency is fixed at $f_{mix} = f_S / 4$. For f_S = 1 GSPS and f_{mix} = 250 MHz.

Figure 60. DDC Block

Feature Description (continued)

8.3.2 DDC Block

The ADS54J60 has an optional DDC block that can be enabled via an SPI register write. Each ADC channel is followed by a DDC block consisting of three different decimate-by-2 and by-4 finite impulse response (FIR) half-band filter options. The different decimation filter options can be selected via SPI programming.

8.3.2.1 Decimate-by-2 Filter

This decimation filter has 41 taps. The stop-band attenuation is approximately 90 dB and the pass-band flatness is ±0.05 dB. Table 1 shows corner frequencies for low-pass and high-pass filter options.

Table 1. Corner Frequencies for the Decimate-by-2 Filter

CORNERS (dB)	LOW PASS	HIGH PASS
–0.1	0.202 × f_S	0.298 × f_S
–0.5	0.210 × f_S	0.290 × f_S
–1	0.215 × f_S	0.285 × f_S
–3	0.227 × f_S	0.273 × f_S

Figure 61 and Figure 62 show the frequency response of decimate-by-2 filter from dc to f_S / 2.

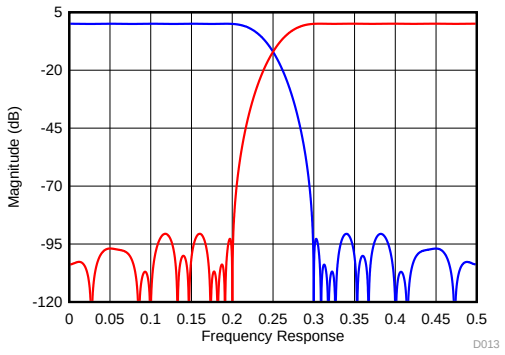


Figure 61. Decimate-by-2 Filter Response

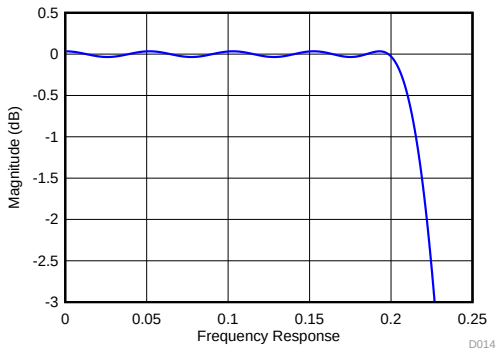


Figure 62. Decimate-by-2 Filter Response (Zoomed)

8.3.2.2 Decimate-by-4 Filter Using a Digital Mixer

This band-pass decimation filter consists of a digital mixer and three concatenated FIR filters with a combined latency of approximately 28 output clock cycles. The alias band attenuation is approximately 55 dB and the pass-band flatness is ±0.1 dB. By default after reset, the band-pass filter is centered at f_S / 16. Using the SPI, the center frequency can be programmed at N × f_S / 16 (where N = 1, 3, 5, or 7). Table 2 shows corner frequencies for two extreme options. Figure 63 and Figure 64 show frequency response of decimate-by-4 filter for center frequencies f_S/16 and 3 × f_S/16 (N =1 and 3).

Table 2. Corner frequencies for the Decimate-by-4 Filter

CORNERS (dB)	CORNER FREQUENCY AT LOWER SIDE (Center Frequency f_S / 16)	CORNER FREQUENCY AT HIGHER SIDE (Center Frequency f_S / 16)
–0.1	0.011 × f_S	0.114 × f_S
–0.5	0.010 × f_S	0.116 × f_S
–1	0.008 × f_S	0.117 × f_S
–3	0.006 × f_S	0.120 × f_S

Figure 63 and Figure 64 show the frequency response of a decimate-by-4 filter from dc to f_S / 2.

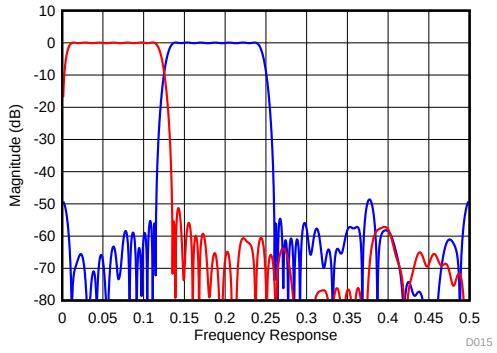


Figure 63. Decimate-by-4 Filter Response

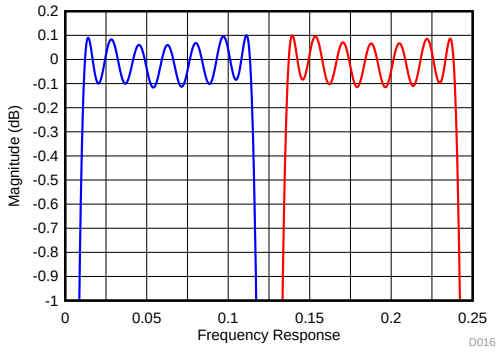


Figure 64. Decimate-by-4 Filter Response (Zoomed)

8.3.2.3 Decimate-by-4 Filter with IQ Outputs

In this configuration, the DDC block includes a fixed digital f_S / 4 mixer. Thus, the IQ pass band is approximately ±110 MHz, centered at f_S / 4. This decimation filter has 41 taps with a latency of approximately ten output clock cycles. The stop-band attenuation is approximately 90 dB and the pass-band flatness is ±0.05 dB. Table 3 shows the corner frequencies for a low-pass decimate-by-4 with IQ filter.

Table 3. Corner Frequencies for a Decimate-by-4 IQ Output Filter

CORNERS (dB)	LOW PASS
–0.1	0.107 × f_S
–0.5	0.112 × f_S
–1	0.115 × f_S
–3	0.120 × f_S

Figure 65 and Figure 66 show the frequency response of a decimate-by-4 IQ output filter from dc to f_S / 2.

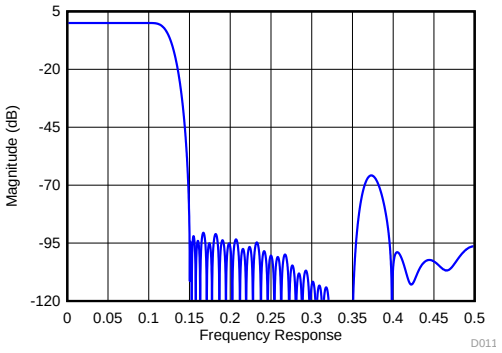


Figure 65. Decimate-by-4 with IQ Outputs Filter Response

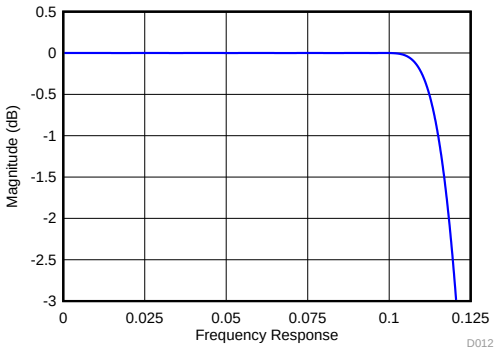


Figure 66. Decimate-by-4 with IQ Outputs Filter Response (Zoomed)

8.3.3 SYSREF Signal

The SYSREF signal is a periodic signal that is sampled by the ADS54J60 device clock and used to align the boundary of the local multi-frame clock inside the data converter. SYSREF is required to be a sub-harmonic of the local multiframe clock (LMFC) internal timing. To meet this requirement, the timing of SYSREF is dependent on the device clock frequency and the LMFC frequency, as determined by the selected DDC decimation and frames per multi-frame settings. TI recommends that the SYSREF signal be a low-frequency signal in the range of 1 MHz to 5 MHz in order to reduce coupling to the signal path both on the printed circuit board (PCB) as well as internal in the device.

The external SYSREF signal must be a sub-harmonic of the internal LMFC clock, as shown in Equation 1 and Table 4.

$$SYSREF = LMFC / 2^N \quad (1)$$

where

- N = 0, 1, 2, and so forth.

Table 4. Local Multi-Frame Clock Frequency

LMFS CONFIGURATION	DECIMATION	LMFC CLOCK(1)(2)
4211	—	f_S / K
4244	—	(f_S / 4) / K
8224	—	(f_S / 4) / K
4222	2X	(f_S / 4) / K
2242	2X	(f_S / 4) / K
2221	4X	(f_S / 4) / K
2441	4X (IQ)	(f_S / 4) / K
4421	4X (IQ)	(f_S / 4) / K
1241	4X	(f_S / 4) / K

(1) K = Number of frames per multi frame (JESD digital page 6900h, address 06h, bits 4-0).
(2) f_S = sampling (device) clock frequency.

For example, if LMFS = 8224 then the programmed value of K is 9 (the actual value is 9 + 1 = 10 because the actual value for K = the value set in the SPI register +1). If the device clock frequency is f_S = 1000 MSPS, then the local multi-frame clock frequency becomes (1000 / 4) / 10 = 25 MHz. The SYSREF signal frequency can be chosen as the LMFC frequency / 8 = 3.125 MHz.

8.3.3.1 SYSREF Not Present (Subclass 0, 2)

A SYSREF pulse is required by the ADS54J60 to reset internal counters. If SYSREF is not present, as can be the case in subclass 0 or 2, this pulse can be done by doing the following register writes shown in Table 5.

Table 5. Internally Pulsing SYSREF Twice Using Register Writes

ADDRESS (Hex)	DATA (Hex)	COMMENT
0-011h	80h	Set the master page
0-054h	80h	Enable manual SYSREF
0-053h	01h	Set SYSREF high
0-053h	00h	Set SYSREF low
0-053h	01h	Set SYSREF high
0-053h	00h	Set SYSREF low

8.3.4 Overrange Indication

The ADS54J60 provides a fast overrange indication that can be presented in the digital output data stream via SPI configuration. Alternatively, if not used, the SDOUT (pin 11) and PDN (pin 50) pins can be configured via the SPI to output the fast OVR indicator.

When the FOVR indication is embedded in the output data stream, it replaces the LSB of the 16-bit data stream going to the 8b/10b encoder, as shown in Figure 67.

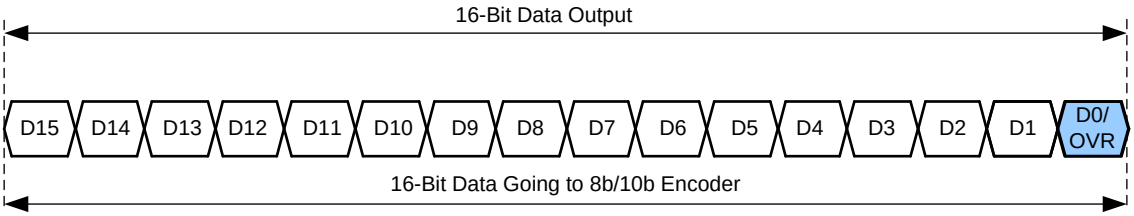


Figure 67. Overrange Indication in a Data Stream

8.3.4.1 Fast OVR

The fast OVR is triggered if the input voltage exceeds the programmable overrange threshold and is presented after only 18 clock cycles + t_{PD} (t_{PD} of the gates and buffers is approximately 4 ns), thus enabling a quicker reaction to an overrange event.

The input voltage level at which the overload is detected is referred to as the *threshold*. The threshold is programmable using the FOVR THRESHOLD bits, as shown in Figure 68. The FOVR is triggered 18 clock cycles + t_{PD} (t_{PD} of the gates and buffers is approximately 4 ns) after the overload condition occurs.

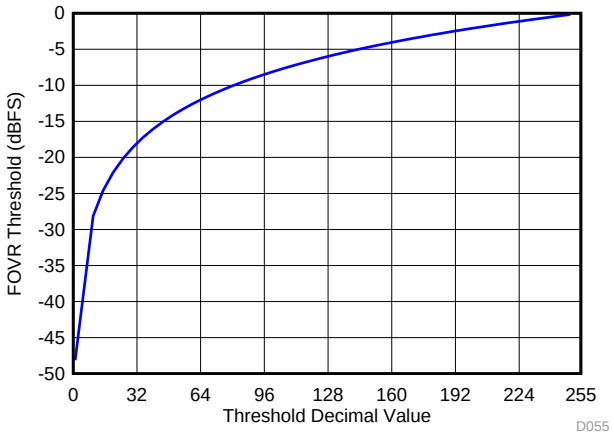


Figure 68. Programming Fast OVR Thresholds

The input voltage level at which the fast OVR is triggered is defined by Equation 2:

Full-Scale × [Decimal Value of the FOVR Threshold Bits] / 255) (2)

The default threshold is E3h (227d), corresponding to a threshold of –1 dBFS.

In terms of full-scale input, the fast OVR threshold can be calculated as Equation 3:

20log (FOVR Threshold / 255) (3)

8.3.5 Power-Down Mode

The ADS54J60 provides a highly-configurable power-down mode. Power-down can be enabled using the PDN pin or SPI register writes.

A power-down mask can be configured, which allows a trade-off between wake-up time and power consumption in power-down mode. Two independent power-down masks can be configured: MASK 1 and MASK 2 as shown in Table 6. See the master page registers in Table 15 for further details.

Table 6. Register Address for Power-Down Modes

REGISTER ADDRESS A[7:0] (Hex)	COMMENT	REGISTER DATA							
		7	6	5	4	3	2	1	0
MASTER PAGE (80h)									
20	MASK 1	PDN ADC CHA				PDN ADC CHB			
21		PDN BUFFER CHB		PDN BUFFER CHA		0	0	0	0
23	MASK 2	PDN ADC CHA				PDN ADC CHB			
24		PDN BUFFER CHB		PDN BUFFER CHA		0	0	0	0
26	CONFIG	GLOBAL PDN	OVERRIDE PDN PIN	PDN MASK SEL	0	0	0	0	0
55		0	0	0	PDN MASK	0	0	0	0

To save power, the device can be put in complete power down by using the GLOBAL PDN register bit. However, when JESD must remain linked up while putting the device in power down, the ADC and analog buffer can be powered down by using the PDN ADC CHx and PDN BUFFER CHx register bits after enabling the PDN MASK register bit. The PDN MASK SEL register bit can be used to select between MASK 1 or MASK 2. Table 7 shows power consumption for different combinations of the GLOBAL PDN, PDN ADC CHx, and PDN BUFF CHx register bits.

Table 7. Power Consumption in Different Power-Down Settings

REGISTER BIT	COMMENT	I_{AVDD3V} (mA)	I_{AVDD} (mA)	I_{DVDD} (mA)	I_{IOVDD} (mA)	TOTAL POWER (W)
Default	After reset, with a full-scale input signal to both channels	336	358	198	533	2.68
GBL PDN = 1	The device is in complete power-down state	2	6	22	199	0.29
GBL PDN = 0, PDN ADC CHx = 1 (x = A or B)	The ADC of one channel is powered down	274	223	135	512	2.09
GBL PDN = 0, PDN BUFF CHx = 1 (x = A or B)	The input buffer of one channel is powered down	262	352	194	545	2.45
GBL PDN = 0, PDN ADC CHx = 1, PDN BUFF CHx = 1 (x = A or B)	The ADC and input buffer of one channel is powered down	198	222	132	508	1.85
GBL PDN = 0, PDN ADC CHx = 1, PDN BUFF CHx = 1 (x = A and B)	The ADC and input buffer of both channels are powered down	60	85	66	484	1.02

8.4 Device Functional Modes

8.4.1 Device Configuration

The ADS54J60 can be configured by using a serial programming interface, as described in the *Serial Interface* section. In addition, the device has one dedicated parallel pin (PDN) for controlling the power-down mode.

The ADS54J60 supports a 24-bit (16-bit address, 8-bit data) SPI operation and uses paging (see the *Register Maps* section) to access all register bits.

8.4.1.1 Serial Interface

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), and SDIN (serial interface data) pins, as shown in Figure 69. Legends used in Figure 69 are explained in Table 8. Serially shifting bits into the device is enabled when SEN is low. Serial data on SDIN are latched at every SCLK rising edge when SEN is active (low). The interface can function with SCLK frequencies from 2 MHz down to very low speeds (of a few Hertz) and also with a non-50% SCLK duty cycle.

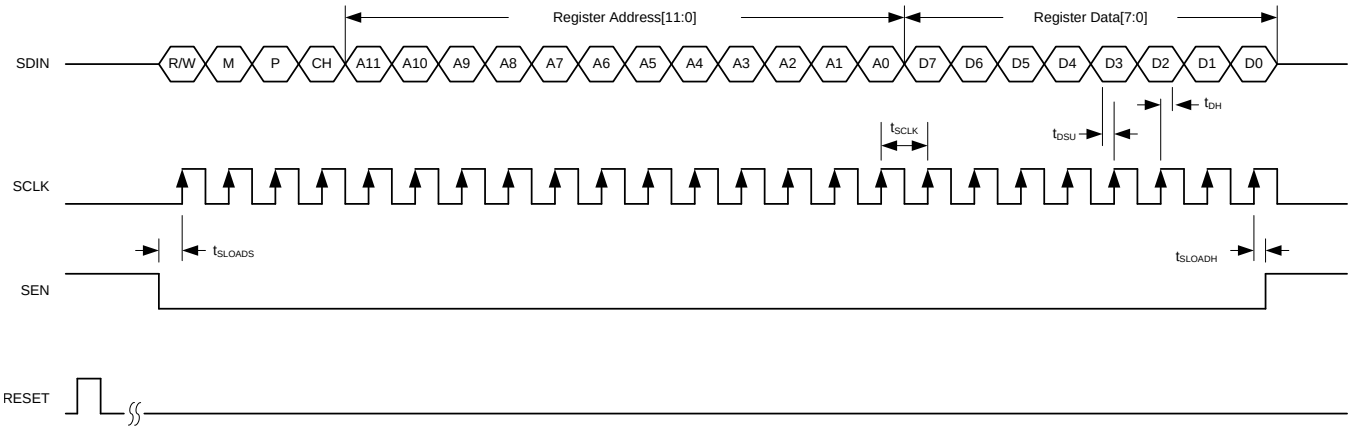


Figure 69. SPI Timing Diagram

Table 8. SPI Timing Diagram Legend

SPI BITS	DESCRIPTION	BIT SETTINGS
R/W	Read/write bit	0 = SPI write 1 = SPI read back
M	SPI bank access	0 = Analog SPI bank (master and ADC pages) 1 = JESD SPI bank (main digital, JESD analog, and JESD digital pages)
P	JESD page selection bit	0 = Page access 1 = Register access
CH	SPI access for a specific channel of the JESD SPI bank	0 = Channel A 1 = Channel B By default, both channels are being addressed.
A[11:0]	SPI address bits	—
D[7:0]	SPI data bits	—

Table 9 shows the timing requirements for the serial interface signals in Figure 69.

Table 9. SPI Timing Requirements

		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1 / t_{SCLK})	> dc		2	MHz
t_{SLOADS}	SEN to SCLK setup time	100			ns
t_{SLOADH}	SCLK to SEN hold time	100			ns
t_{DSU}	SDIN setup time	100			ns
t_{DH}	SDIN hold time	100			ns

8.4.1.2 Serial Register Write: Analog Bank

The analog SPI bank contains of two pages (the master and ADC page). The internal register of the ADS54J60 analog SPI bank can be programmed by:

1. Driving the SEN pin low.
2. Initiating a serial interface cycle specifying the page address of the register whose content must be written.
   - Master page: write address 0011h with 80h.
   - ADC page: write address 0011h with 0Fh.
3. Writing the register content as shown in Figure 70. When a page is selected, multiple writes into the same page can be done.

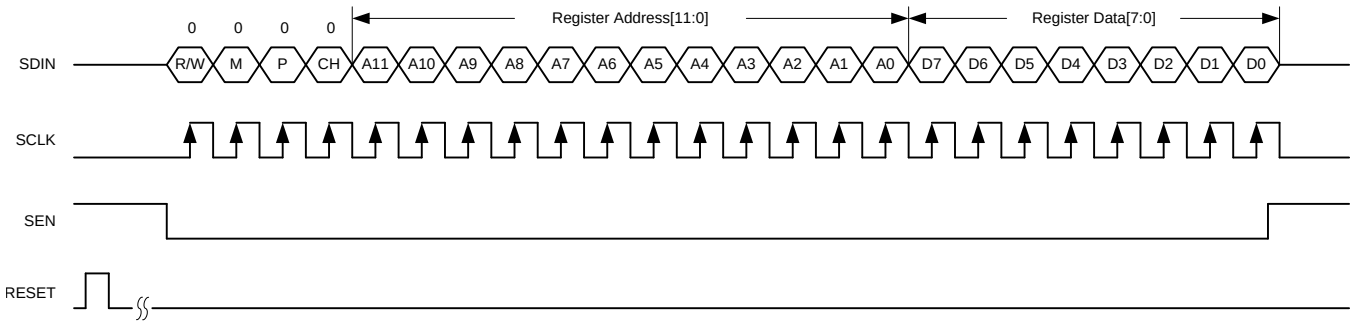


Figure 70. Serial Register Write Timing Diagram

8.4.1.3 Serial Register Readout: Analog Bank

The content from one of the two analog banks can be read out by:

1. Driving the SEN pin low.
2. Selecting the page address of the register whose content must be read.
   - Master page: write address 0011h with 80h.
   - ADC page: write address 0011h with 0Fh.
3. Setting the R/W bit to 1 and write the address to be read back.
4. Reading back the register content on the SDOUT pin, as shown in Figure 71. When a page is selected, multiple read backs from the same page can be done. SDOUT comes out at the SCLK falling edge with an approximate delay (t_{SD_DELAY}) of 68 ns; see Figure 75.

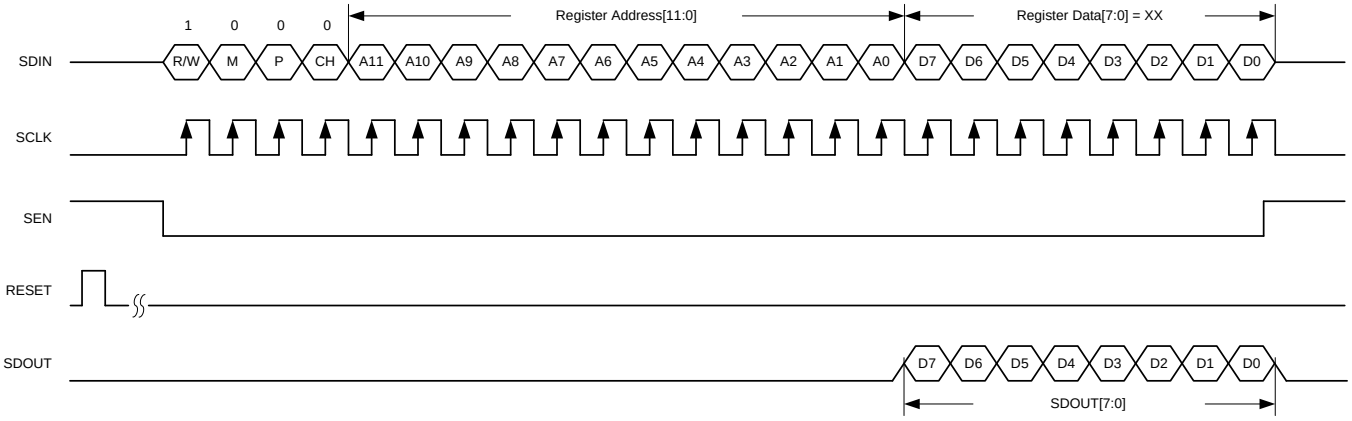


Figure 71. Serial Register Read Timing Diagram

8.4.1.4 JESD Bank SPI Page Selection

The JESD SPI bank contains four pages (main digital, JESD digital, and JESD analog pages). The individual pages can be selected by:

1. Driving the SEN pin low.
2. Setting the M bit to 1 and specifying the page with two register writes. Note that the P bit must be set to 0, as shown in Figure 72.
   - Write address 4003h with 00h (LSB byte of the page address).
   - Write address 4004h with the MSB byte of the page address.
     - For the main digital page: write address 4004h with 68h.
     - For the JESD digital page: write address 4004h with 69h.
     - For the JESD analog page: write address 4004h with 6Ah.

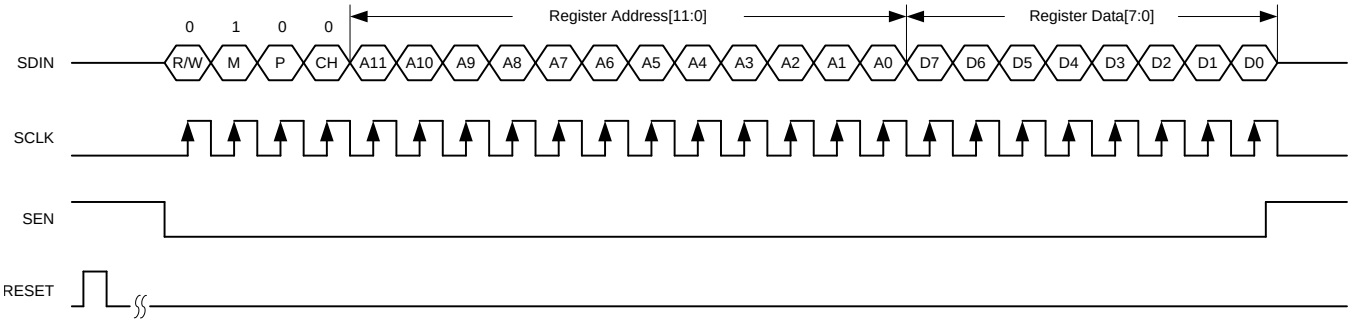


Figure 72. SPI Page Selection

8.4.1.5 Serial Register Write: JESD Bank

The ADS54J60 is a dual-channel device and the JESD204B portion is configured individually for each channel by using the CH bit. Note that the P bit must be set to 1 for register writes.

1. Drive the SEN pin low.
2. Select the JESD bank page. Note that the M bit = 1 and the P bit = 0.
   - Write address 4003h with 00h.
   - Write address 4005h with 01h to enable separate control for both channels.
     - For the main digital page: write address 4004h with 68h.
     - For the JESD digital page: write address 4004h with 69h.
     - For the JESD analog page: write address 4004h with 6Ah.
3. Set the M and P bits to 1, select channel A (CH = 0) or channel B (CH = 1), and write the register content as shown in Figure 73. When a page is selected, multiple writes into the same page can be done.

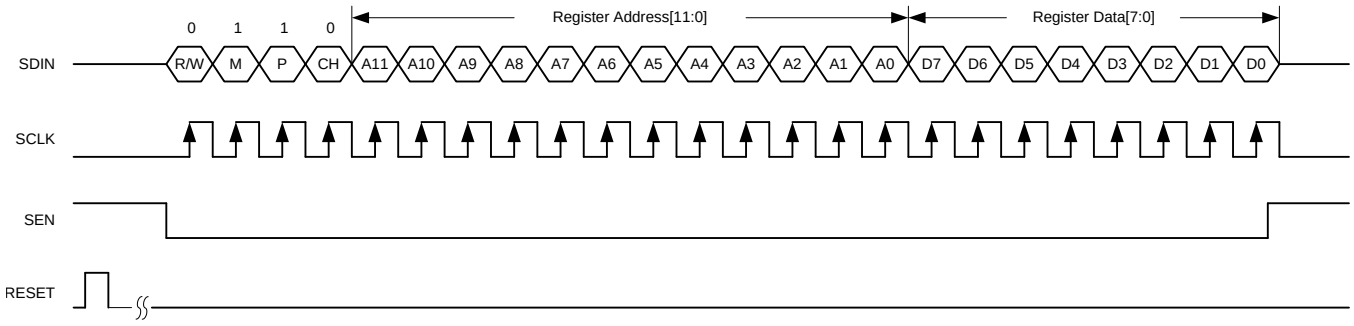


Figure 73. JESD Serial Register Write Timing Diagram

8.4.1.5.1 Individual Channel Programming

By default, register writes are applied to both channels. To enable individual channel writes, write address 4005h with 01h (default is 00h).

8.4.1.6 Serial Register Readout: JESD Bank

The content from one of the pages of the JESD bank can be read out by:

1. Driving the SEN pin low.
2. Selecting the JESD bank page. Note that the M bit = 1 and the P bit = 0.
   - Write address 4003h with 00h.
   - Write address 4005h with 01h to enable separate control for both channels.
     - For the main digital page: write address 4004h with 68h.
     - For the JESD digital page: write address 4004h with 69h.
     - For the JESD analog page: write address 4004h with 6Ah.
3. Setting the R/W, M, and P bits to 1, selecting channel A or channel B, and writing the address to be read back.
4. Reading back the register content on the SDOUT pin; see Figure 74. When a page is selected, multiple read backs from the same page can be done. SDOUT comes out at the SCLK falling edge with an approximate delay (t_{SD_DELAY}) of 68 ns; see Figure 75.

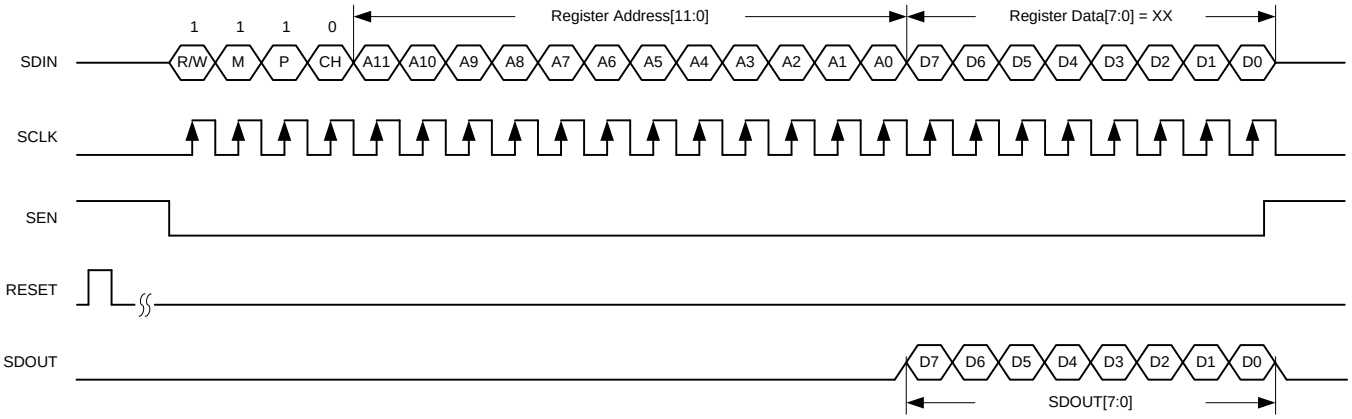


Figure 74. JESD Serial Register Read Timing Diagram

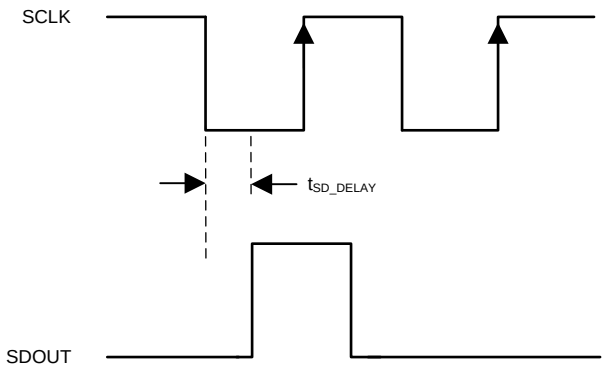


Figure 75. SDOUT Timing Diagram

8.4.2 JESD204B Interface

The ADS54J60 supports device subclass 1 with a maximum output data rate of 10.0 Gbps for each serial transmitter.

An external SYSREF signal is used to align all internal clock phases and the local multi-frame clock to a specific sampling clock edge, allowing synchronization of multiple devices in a system and minimizing timing and alignment uncertainty. The $\overline{\text{SYNC}}$ input is used to control the JESD204B SERDES blocks.

Depending on the ADC output data rate, the JESD204B output interface can be operated with either two or four lanes per single ADC; see Figure 76. The JESD204B setup and configuration of the frame assembly parameters is controlled via the SPI interface.

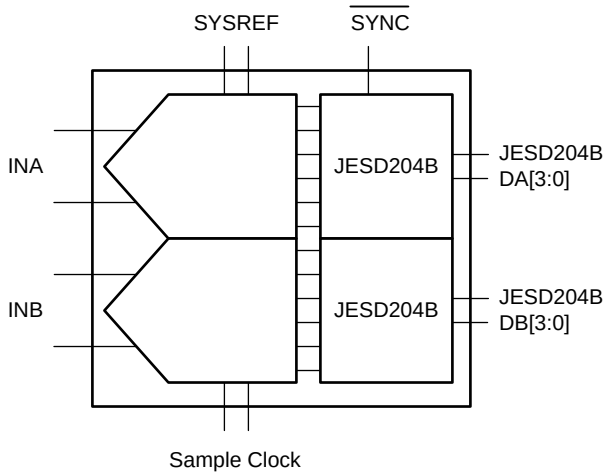


Figure 76. ADS54J60 Block Diagram

The JESD204B transmitter block shown in Figure 77 consists of the transport layer, the data scrambler, and the link layer. The transport layer maps the ADC output data into the selected JESD204B frame data format. The link layer performs the 8b/10b data encoding as well as the synchronization and initial lane alignment using the SYNC input signal. Optionally, data from the transport layer can be scrambled.

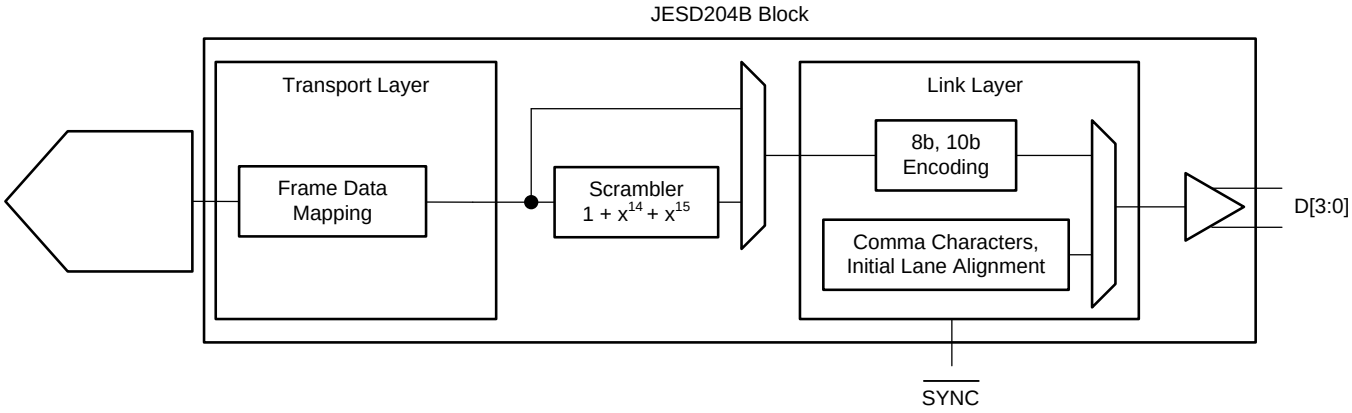


Figure 77. JESD204B Transmitter Block

8.4.2.1 JESD204B Initial Lane Alignment (ILA)

The initial lane alignment process is started when the receiving device de-asserts the $\overline{\text{SYNC}}$ signal, as shown in Figure 78. When a logic low is detected on the $\overline{\text{SYNC}}$ input pin, the ADS54J60 starts transmitting comma (K28.5) characters to establish a code group synchronization.

When synchronization is complete, the receiving device asserts the $\overline{\text{SYNC}}$ signal and the ADS54J60 starts the initial lane alignment sequence with the next local multi-frame clock boundary. The ADS54J60 transmits four multi-frames, each containing K frames (K is SPI programmable). Each of the multi-frames contains the frame start and end symbols and the second multi-frame also contains the JESD204 link configuration data.

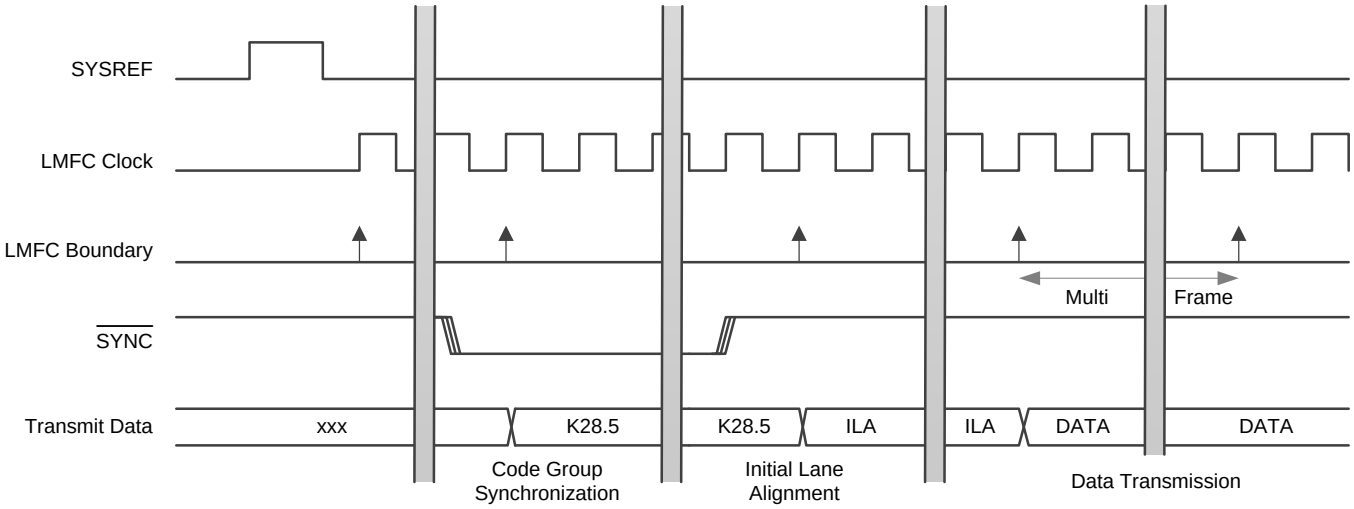


Figure 78. Lane Alignment Sequence

8.4.2.2 JESD204B Test Patterns

There are three different test patterns available in the transport layer of the JESD204B interface. The ADS54J60 supports a clock output, encoded test pattern, and an 12-octet RPAT pattern. These test patterns can be enabled via an SPI register write and are located in the JESD digital page of the JESD bank.

8.4.2.3 JESD204B Frame

The JESD204B standard defines the following parameters:

- L is the number of lanes per link.
- M is the number of converters per device.
- F is the number of octets per frame clock period, per lane.
- S is the number of samples per frame per converter.

8.4.2.4 JESD204B Frame

Table 10 lists the available JESD204B formats and valid ranges for the ADS54J60 when the decimation filter is not used. The ranges are limited by the SERDES lane rate and the maximum ADC sample frequency.

Table 10. Default Interface Rates

L	M	F	S	DECIMATION	MINIMUM RATES		MAXIMUM RATES	
					SAMPLING RATE (MSPS)	SERDES BIT RATE (Gbps)	SAMPLING RATE (MSPS)	SERDES BIT RATE (Gbps)
4	2	1	1	Not used	250	2.5	1000	10.0
4	2	4	4	Not used	250	2.5	1000	10.0
8	2	2	4	Not used	500	2.5	1000	5.0

NOTE

In the LMFS = 8224 row of Table 10, the sample order in lane DA2 and DA3 are swapped.

The detailed frame assembly is shown in Table 11.

Table 11. Default Frame Assembly

PIN	LMFS = 4211	LMFS = 4244				LMFS = 8224	
DA0						A_3[15:8]	A_3[7:0]
DA1	A_0[7:0]	A_2[15:8]	A_2[7:0]	A_3[15:8]	A_3[7:0]	A_2[15:8]	A_2[7:0]
DA2	A_0[15:8]	A_0[15:8]	A_0[7:0]	A_1[15:8]	A_1[7:0]	A_0[15:8]	A_0[7:0]
DA3						A_1[15:8]	A_1[7:0]
DB0						B_3[15:8]	B_3[7:0]
DB1	B_0[7:0]	B_2[15:8]	B_2[7:0]	B_3[15:8]	B_3[7:0]	B_2[15:8]	B_2[7:0]
DB2	B_0[15:8]	B_0[15:8]	B_0[7:0]	B_1[15:8]	B_1[7:0]	B_0[15:8]	B_0[7:0]
DB3						B_1[15:8]	B_1[7:0]

8.4.2.5 JESD204B Frame Assembly with Decimation

Table 12 lists the available JESD204B formats and valid ranges for the ADS54J60 when enabling the decimation filter. The ranges are limited by the SERDES line rate and the maximum ADC sample frequency.

Table 13 lists the detailed frame assembly with different decimation options.

Table 12. Interface Rates with Decimation Filter

L	M	F	S	DECIMATION	MINIMUM RATES			MAXIMUM RATES		
					DEVICE CLOCK FREQUENCY (MSPS)	OUTPUT SAMPLE RATE (MSPS)	SERDES BIT RATE (Gbps)	DEVICE CLOCK FREQUENCY (MSPS)	OUTPUT SAMPLE RATE (MSPS)	SERDES BIT RATE (Gbps)
4	4	2	1	4X (IQ)	500	125	2.5	1000	250	5.0
4	2	2	2	2X	500	250	2.5	1000	500	5.0
2	2	4	2	2X	300	150	3	1000	500	10.0
2	2	2	1	4X	500	125	2.5	1000	250	5.0
2	4	4	1	4X (IQ)	300	75	3	1000	250	10.0
1	2	4	1	4X	300	75	3	1000	250	10.0

Table 13. Frame Assembly with Decimation Filter

PIN	LMFS = 4222, 2X DECIMATION		LMFS = 2242, 2X DECIMATION				LMFS = 2221, 4X DECIMATION		LMFS = 2441, 4X DECIMATION (IQ)				LMFS = 4421, 4X DECIMATION (IQ)		LMFS = 1241, 4X DECIMATION			
DA0	A1 [15:8]	A1 [7:0]											AQ0 [15:8]	AQ0 [7:0]				
DA1	A0 [15:8]	A0 [7:0]	A0 [15:8]	A0 [7:0]	A1 [15:8]	A1 [7:0]	A0 [15:8]	A0 [7:0]	AI0 [15:8]	AI0 [7:0]	AQ0 [15:8]	AQ0 [7:0]	AI0 [15:8]	AI0 [7:0]	A0 [15:8]	A0 [7:0]	B0 [15:8]	B0 [7:0]
DA2																		
DA3																		
DB0	B1 [15:8]	B1 [7:0]											BQ0 [15:8]	BQ0 [7:0]				
DB1	B0 [15:8]	B0 [7:0]	B0 [15:8]	B0 [7:0]	B1 [15:8]	B1 [7:0]	B0 [15:8]	B0 [7:0]	BI0 [15:8]	BI0 [7:0]	BQ0 [15:8]	BQ0 [7:0]	BI0 [15:8]	BI0 [7:0]				
DB2																		
DB3																		

Table 14. Program Summary of DDC Modes and JESD Link Configuration(1)(2)

LMFS OPTIONS				DDC MODES PROGRAMMING				JESD LINK (LMFS) PROGRAMMING						
L	M	F	S	DECIMATION OPTIONS	DEC MODE EN, DECFIL EN(3)	DECFIL MODE[3:0](4)	JESD FILTER(5)	JESD MODE(6)	JESD PLL MODE(7)	LANE SHARE(8)	DA_BUS_REORDER(9)	DB_BUS_REORDER(10)	BUS_REORDER EN1(11)	BUS_REORDER EN2(12)
4	2	1	1	No decimation	00	00	000	100	10	0	00h	00h	0	0
4	2	4	4	No decimation	00	00	000	010	10	0	00h	00h	0	0
8	2	2	4	No decimation (default after reset)	00	00	000	001	00	0	00h	00h	0	0
4	4	2	1	4X (IQ)	11	0011 (LPF with f_S / 4 mixer)	111	001	00	0	0Ah	0Ah	1	1
4	2	2	2	2X	11	0010 (LPF) or 0110 (HPF)	110	001	00	0	0Ah	0Ah	1	1
2	2	4	2	2X	11	0010 (LPF) or 0110 (HPF)	110	010	10	0	0Ah	0Ah	1	1
2	2	2	1	4X	11	0000, 0100, 1000, or 1100 (all BPFs with different center frequencies).	100	001	00	0	0Ah	0Ah	1	1
2	4	4	1	4X (IQ)	11	0011 (LPF with an f_S / 4 mixer)	111	010	10	0	0Ah	0Ah	1	1
1	2	4	1	4X	11	0000, 0100, 1000, or 1100 (all BPFs with different center frequencies)	100	010	10	1	0Ah	0Ah	1	1

(1) Keeping the same LMFS settings for both channels is recommended.
(2) The PULSE RESET register bit must be pulsed after the registers in the main digital page are programmed.
(3) The DEC MODE EN and DECFIL EN register bits are located in the main digital page, register 04Dh (bit 3) and register 041h (bit 4).
(4) The DECFIL MODE[3:0] register bits are located in the main digital page, register 041h (bits 5 and 2-0).
(5) The JESD FILTER register bits are located in the JESD digital page, register 001h (bits 5-3).
(6) The JESD MODE register bits are located in the JESD digital page, register 001h (bits 2:0).
(7) The JESD PLL MODE register bits are located in the JESD analog page, register 016h (bits 1-0).
(8) The LANE SHARE register bit is located in the JESD digital page, register 016h (bit 4).
(9) The DA_BUS_REORDER register bits are located in the JESD digital page, register 031h (bits 7-0).
(10) The DB_BUS_REORDER register bits are located in the JESD digital page, register 032h (bits 7-0).
(11) The BUS_REORDER EN1 register bit is located in the main digital page, register 052h (bit 7).
(12) The BUS_REORDER EN2 register bit is located in the main digital page, register 072h (bit 3).

8.4.2.5.1 JESD Transmitter Interface

Each of the 10.0-Gbps SERDES JESD transmitter outputs requires ac coupling between the transmitter and receiver. The differential pair must be terminated with 100-Ω resistors as close to the receiving device as possible to avoid unwanted reflections and signal degradation, as shown in Figure 79.

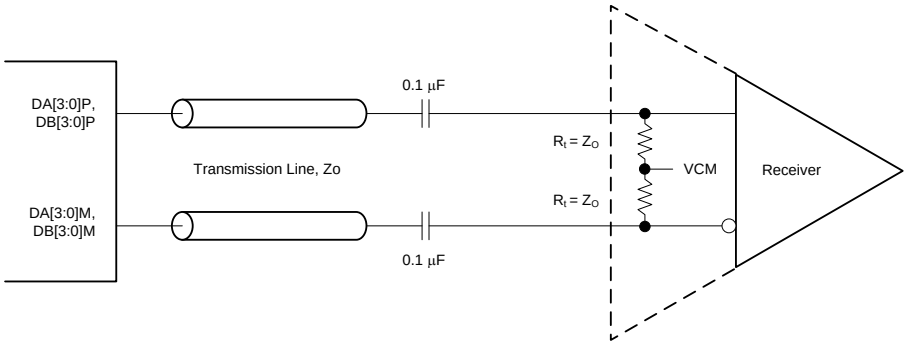


Figure 79. Output Connection to Receiver

8.4.2.5.2 Eye Diagram

Figure 80 to Figure 83 show the serial output eye diagrams of the ADS54J60 at 5.0 Gbps and 10 Gbps with default and increased output voltage swing against the JESD204B mask.

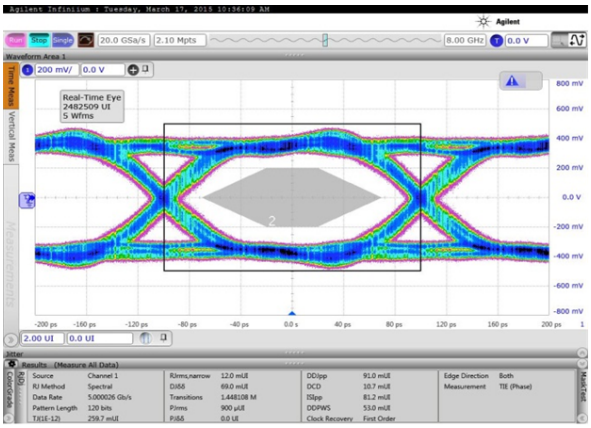


Figure 80. Eye at 5-Gbps Bit Rate with Default Output Swing

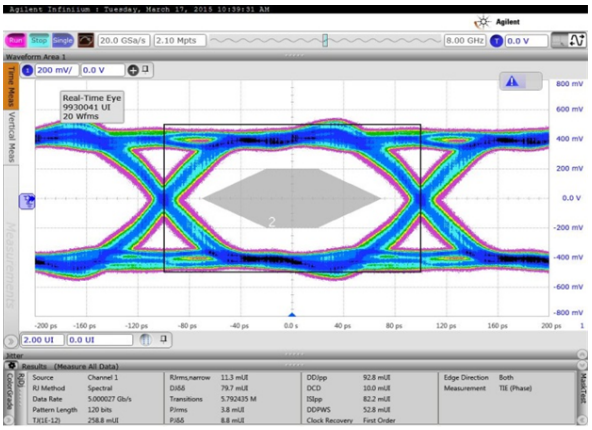


Figure 81. Eye at 5-Gbps Bit Rate with Increased Output Swing

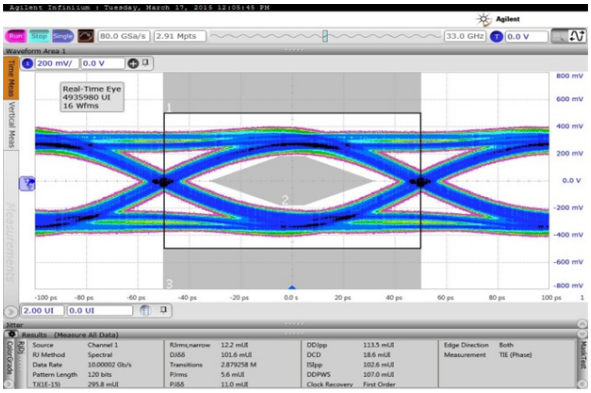


Figure 82. Eye at 10-Gbps Bit Rate with Default Output Swing

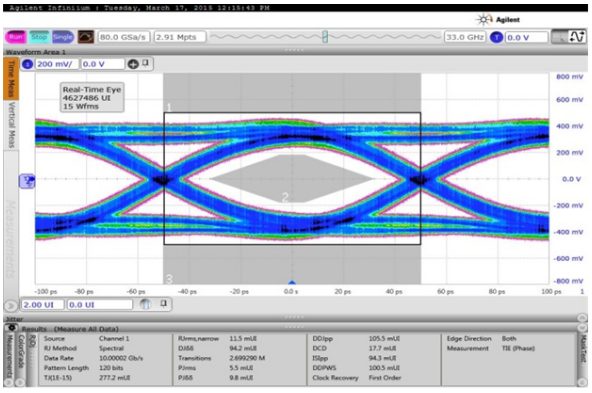
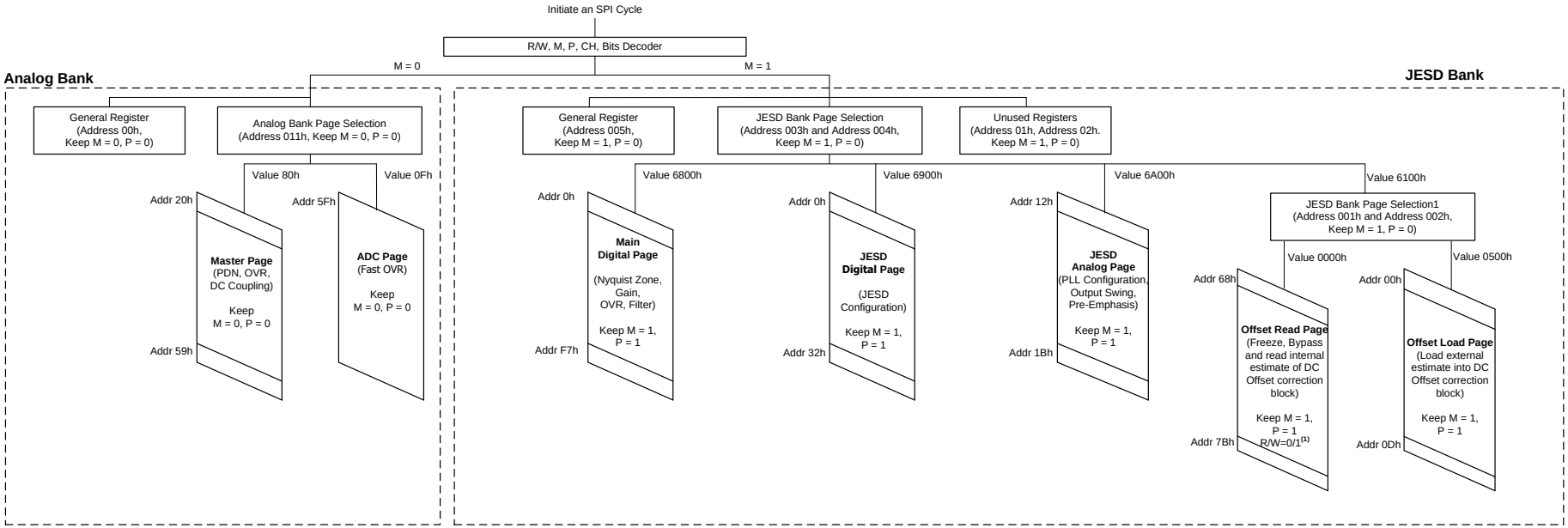


Figure 83. Eye at 10-Gbps Bit Rate with Increased Output Swing

8.5 Register Maps

Figure 84 shows a conceptual diagram of the serial registers.



(1) Set the R/W bit to 1 when reading an estimate of the dc offset correction block, otherwise keep this bit at 0.

Figure 84. Serial Interface Registers

The ADS54J60 contains two main SPI banks. The analog SPI bank gives access to the ADC analog blocks and the digital SPI bank controls the interleaving engine and anything related to the JESD204B serial interface. The analog SPI bank is divided into two pages (master and ADC) and the digital SPI bank is divided into three pages (main digital, JESD digital, and JESD analog). Table 15 lists a register map for the ADS54J60.

Register Maps (continued)

Table 15. Register Map

REGISTER ADDRESS	REGISTER DATA							
A[11:0] (Hex)	7	6	5	4	3	2	1	0
GENERAL REGISTERS								
0	RESET	0	0	0	0	0	0	RESET
1	JESD BANK PAGE SEL1[7:0]							
2	JESD BANK PAGE SEL1[15:8]							
3	JESD BANK PAGE SEL[7:0]							
4	JESD BANK PAGE SEL[15:8]							
5	0	0	0	0	0	0	0	DISABLE BROADCAST
11	ANALOG BANK PAGE SEL							
MASTER PAGE (ANALOG BANK PAGE SEL = 80h)								
20	PDN ADC CHA				PDN ADC CHB			
21	PDN BUFFER CHB		PDN BUFFER CHA		0	0	0	0
23	PDN ADC CHA				PDN ADC CHB			
24	PDN BUFFER CHB		PDN BUFFER CHA		0	0	0	0
26	GLOBAL PDN	OVERRIDE PDN PIN	PDN MASK SEL	0	0	0	0	0
4F	0	0	0	0	0	0	0	EN INPUT DC COUPLING
53	0	0	0	0	0	0	EN SYSREF DC COUPLING	MANUAL SYSREF
54	ENABLE MANUAL SYSREF	0	MASK SYSREF		0	0	0	0
55	0	0	0	PDN MASK	0	0	0	0
59	FOVR CHB	0	ALWAYS WRITE 1	0	0	0	0	0
ADC PAGE (ANALOG BANK PAGE SEL = 0Fh)								
5F	FOVR THRESHOLD PROG							
MAIN DIGITAL PAGE (JESD BANK PAGE SEL = 6800h)								
0	0	0	0	0	0	0	0	PULSE RESET
41	0	0	DECFIL MODE[3]	DECFIL EN	0	DECFIL MODE[2:0]		
42	0	0	0	0	0	NYQUIST ZONE		
43	0	0	0	0	0	0	0	FORMAT SEL
44	0	DIGITAL GAIN						
4B	0	0	FORMAT EN	0	0	0	0	0
4D	0	0	0	0	DEC MODE EN	0	0	0
4E	CTRL NYQUIST	0	IMPROVE IL PERF	0	0	0	0	0

Register Maps (continued)

Table 15. Register Map (continued)

REGISTER ADDRESS	REGISTER DATA							
A[11:0] (Hex)	7	6	5	4	3	2	1	0
52	BUS_ REORDER EN1	0	0	0	0	0	0	DIG GAIN EN
72	0	0	0	0	BUS_ REORDER EN2	0	0	0
AB	0	0	0	0	0	0	0	LSB SEL EN
AD	0	0	0	0	0	0	LSB SELECT	
F7	0	0	0	0	0	0	0	DIG RESET
JESD DIGITAL PAGE (JESD BANK PAGE SEL = 6900h)								
0	CTRL K	0	0	TESTMODE EN	FLIP ADC DATA	LANE ALIGN	FRAME ALIGN	TX LINK DIS
1	SYNC REG	SYNC REG EN	JESD FILTER			JESD MODE		
2	LINK LAYER TESTMODE			LINK LAYER RPAT	LMFC MASK RESET	0	0	0
3	FORCE LMFC COUNT	LMFC COUNT INIT					RELEASE ILANE SEQ	
5	SCRAMBLE EN	0	0	0	0	0	0	0
6	0	0	0	FRAMES PER MULTI FRAME (K)				
7	0	0	0	0	SUBCLASS	0	0	0
16	1	0	0	LANE SHARE	0	0	0	0
31	DA_BUS_REORDER[7:0]							
32	DB_BUS_REORDER[7:0]							
JESD ANALOG PAGE (JESD BANK PAGE SEL = 6A00h)								
12	SEL EMP LANE 1						ALWAYS WRITE 1	0
13	SEL EMP LANE 0						0	0
14	SEL EMP LANE 2						0	0
15	SEL EMP LANE 3						0	0
16	0	0	0	0	0	0	JESD PLL MODE	
17	0	PLL RESET	LANE PDN 1	0	LANE PDN 0	0	0	0
1A	0	0	0	0	0	0	FOVR CHA	0
1B	JESD SWING			0	FOVR CHA EN	0	0	0
OFFSET READ PAGE (JESD BANK PAGE SEL = 6100h, JESD BANK PAGE SEL1 = 0000h)								
68	FREEZE CORR	DC OFFSET CORR BW				BYPASS CORR	ALWAYS WRITE 1	0
69	0	0	0	0	0	0	0	EXT CORR EN
74	ADC0_CORR_INT_EST[7:0]							
75	0	0	0	0	0	ADC0_CORR_INT_EST[10:8]		
76	ADC1_CORR_INT_EST[7:0]							

Register Maps (continued)

Table 15. Register Map (continued)

REGISTER ADDRESS	REGISTER DATA							
A[11:0] (Hex)	7	6	5	4	3	2	1	0
77	0	0	0	0	0	ADC1_CORR_INT_EST[10:8]		
78	ADC2_CORR_INT_EST[7:0]							
79	0	0	0	0	0	ADC2_CORR_INT_EST[10:8]		
7A	ADC3_CORR_INT_EST[7:0]							
7B	0	0	0	0	0	ADC3_CORR_INT_EST[10:8]		
OFFSET LOAD PAGE (JESD BANK PAGE SEL = 6100h, JESD BANK PAGE SEL1 = 0500h)								
00	ADC0_LOAD_INT_EST[7:0]							
01	0	0	0	0	0	ADC0_CORR_INT_EST[10:8]		
04	ADC1_LOAD_INT_EST[7:0]							
05	0	0	0	0	0	ADC1_CORR_INT_EST[10:8]		
08	ADC2_LOAD_INT_EST[7:0]							
09	0	0	0	0	0	ADC2_CORR_INT_EST[10:8]		
0C	ADC3_LOAD_INT_EST[7:0]							
0D	0	0	0	0	0	ADC3_CORR_INT_EST[10:8]		

8.5.1 Example Register Writes

This section provides three different example register writes. Table 16 describes a global power-down register write, Table 17 describes the register writes when the default lane setting (eight active lanes per device) is changed to four active lanes (LMFS = 4211), and Table 18 describes the register writes for 2X decimation with four active lanes (LMFS = 4222).

Table 16. Global Power Down

ADDRESS (Hex)	DATA (Hex)	COMMENT
0-011h	80h	Set the master page
0-026h	C0h	Set the global power-down

Table 17. Two Lanes per Channel Mode (LMFS = 4211)

ADDRESS (Hex)	DATA (Hex)	COMMENT
4-004h	69h	Select the JESD digital page
4-003h	00h	Select the JESD digital page
6-001h	02h	Select the digital to 40X mode
4-004h	6Ah	Select the JESD analog page
6-016h	02h	Set the SERDES PLL to 40X mode

Table 18. 2X Decimation (LPF for Both Channels) with Four Active Lanes (LMFS = 4222)

ADDRESS (Hex)	DATA (Hex)	COMMENT
4-004h	68h	Select the main digital page (6800h)
4-003h	00h	Select the main digital page (6800h)
6-041h	12h	Set decimate-by-2 (low-pass filter)
6-04Dh	08h	Enable decimation filter control
6-072h	08h	BUS_REORDER EN2
6-052h	80h	BUS_REORDER EN1
6-000h	01h	Pulse the PULSE RESET bit (so that register writes to the main digital page go into effect).
6-000h	00h	
4-004h	69h	Select the JESD digital page (6900h)
4-003h	00h	Select the JESD digital page (6900h)
6-031h	0Ah	Output bus reorder for channel A
6-032h	0Ah	Output bus reorder for channel B
6-001h	31h	Program the JESD MODE and JESD FILTER register bits for LMFS = 4222.

Table 19 lists the access codes for the ADS54J60 registers.

Table 19. ADS54J60 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R/W	R-W	Read or write
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.5.2 Register Descriptions

8.5.2.1 General Registers

8.5.2.1.1 Register 0h (address = 0h)

Figure 85. Register 0h

7	6	5	4	3	2	1	0
RESET	0	0	0	0	0	0	RESET
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 20. Register 0h Field Descriptions

Bit	Field	Type	Reset	Description
7	RESET	W	0h	0 = Normal operation 1 = Internal software reset, clears back to 0
6-1	0	W	0h	Must write 0
0	RESET	W	0h	0 = Normal operation 1 = Internal software reset, clears back to 0

8.5.2.1.2 Register 1h (address = 1h)

Figure 86. Register 1h

7	6	5	4	3	2	1	0
JESD BANK PAGE SEL1[7:0]							
R/W-0h							

Table 21. Register 1h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	JESD BANK PAGE SEL1[7:0]	R/W	0h	Program these bits to access the desired page in the JESD bank. 0000h = OFFSET READ Page 0500h = OFFSET LOAD Page

8.5.2.1.3 Register 2h (address = 2h)

Figure 87. Register 2h

7	6	5	4	3	2	1	0
JESD BANK PAGE SEL1[15:8]							
R/W-0h							

Table 22. Register 2h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	JESD BANK PAGE SEL1[15:8]	R/W	0h	Program these bits to access the desired page in the JESD bank. 0000h = OFFSET READ Page 0500h = OFFSET LOAD Page

8.5.2.1.4 Register 3h (address = 3h)

Figure 88. Register 3h

7	6	5	4	3	2	1	0
JESD BANK PAGE SEL[7:0]							
R/W-0h							

Table 23. Register 3h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	JESD BANK PAGE SEL[7:0]	R/W	0h	Program these bits to access the desired page in the JESD bank. 6800h = Main digital page selected 6900h = JESD digital page selected 6A00h = JESD analog page selected 6100h = OFFSET READ or LOAD Page

8.5.2.1.5 Register 4h (address = 4h)

Figure 89. Register 4h

7	6	5	4	3	2	1	0
JESD BANK PAGE SEL[15:8]							
R/W-0h							

Table 24. Register 4h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	JESD BANK PAGE SEL[15:8]	R/W	0h	Program these bits to access the desired page in the JESD bank. 6800h = Main digital page selected 6900h = JESD digital page selected 6A00h = JESD analog page selected 6100h = OFFSET READ or LOAD Page

8.5.2.1.6 Register 5h (address = 5h)

Figure 90. Register 5h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DISABLE BROADCAST
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 25. Register 5h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	DISABLE BROADCAST	R/W	0h	0 = Normal operation. Channel A and B are programmed as a pair. 1 = Channel A and B can be individually programmed based on the CH bit.

8.5.2.1.7 Register 11h (address = 11h)

Figure 91. Register 11h

7	6	5	4	3	2	1	0
ANALOG PAGE SEL							
R/W-0h							

Table 26. Register 11h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ANALOG BANK PAGE SEL	R/W	0h	Program these bits to access the desired page in the analog bank. Master page = 80h ADC page = 0Fh

8.5.2.2 Master Page (080h) Registers

8.5.2.2.1 Register 20h (address = 20h), Master Page (080h)

Figure 92. Register 20h

7	6	5	4	3	2	1	0
PDN ADC CHA				PDN ADC CHB			
R/W-0h				R/W-0h			

Table 27. Registers 20h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PDN ADC CHA	R/W	0h	There are two power-down masks that are controlled via the PDN mask register bit in address 55h. The power-down mask 1 or mask 2 are selected via register bit 5 in address 26h. Power-down mask 1: addresses 20h and 21h. Power-down mask 2: addresses 23h and 24h. 0Fh = Power-down CHB only. F0h = Power-down CHA only. FFh = Power-down both.
3-0	PDN ADC CHB	R/W	0h	

8.5.2.2.2 Register 21h (address = 21h), Master Page (080h)

Figure 93. Register 21h

7	6	5	4	3	2	1	0
PDN BUFFER CHB		PDN BUFFER CHA		0	0	0	0
R/W-0h		R/W-0h		W-0h	W-0h	W-0h	W-0h

Table 28. Register 21h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PDN BUFFER CHB	R/W	0h	There are two power-down masks that are controlled via the PDN mask register bit in address 55h. The power-down mask 1 or mask 2 are selected via register address 26h, bit 5. Power-down mask 1: addresses 20h and 21h. Power-down mask 2: addresses 23h and 24h. There are two buffers per channel. One buffer drives two ADC cores. PDN BUFFER CHx: 00 = Both buffers of a channel are active. 11 = Both buffers are powered down. 01–10 = Do not use.
5-4	PDN BUFFER CHA	R/W	0h	
3-0	0	W	0h	Must write 0.

8.5.2.2.3 Register 23h (address = 23h), Master Page (080h)

Figure 94. Register 23h

7	6	5	4	3	2	1	0
PDN ADC CHA				PDN ADC CHB			
R/W-0h				R/W-0h			

Table 29. Register 23h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PDN ADC CHA	R/W	0h	There are two power-down masks that are controlled via the PDN mask register bit in address 55h. The power-down mask 1 or mask 2 are selected via register address 26h, bit 5. Power-down mask 1: addresses 20h and 21h. Power-down mask 2: addresses 23h and 24h. 0Fh = Power-down CHB only. F0h = Power-down CHA only. FFh = Power-down both.
3-0	PDN ADC CHB	R/W	0h	

8.5.2.2.4 Register 24h (address = 24h), Master Page (080h)

Figure 95. Register 24h

7	6	5	4	3	2	1	0
PDN BUFFER CHB		PDN BUFFER CHA		0	0	0	0
R/W-0h		R/W-0h		W-0h	W-0h	W-0h	W-0h

Table 30. Register 24h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PDN BUFFER CHB	R/W	0h	There are two power-down masks that are controlled via the PDN mask register bit in address 55h. The power-down mask 1 or mask 2 are selected via register address 26h, bit 5. Power-down mask 1: addresses 20h and 21h. Power-down mask 2: addresses 23h and 24h. Power-down mask 2: addresses 23h and 24h. There are two buffers per channel. One buffer drives two ADC cores. PDN BUFFER CHx: 00 = Both buffers of a channel are active. 11 = Both buffers are powered down. 01–10 = Do not use.
5-4	PDN BUFFER CHA	R/W	0h	
3-0	0	W	0h	Must write 0.

8.5.2.2.5 Register 26h (address = 26h), Master Page (080h)

Figure 96. Register 26h

7	6	5	4	3	2	1	0
GLOBAL PDN	OVERRIDE PDN PIN	PDN MASK SEL	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 31. Register 26h Field Descriptions

Bit	Field	Type	Reset	Description
7	GLOBAL PDN	R/W	0h	Bit 6 (OVERRIDE PDN PIN) must be set before this bit can be programmed. 0 = Normal operation 1 = Global power-down via the SPI
6	OVERRIDE PDN PIN	R/W	0h	This bit ignores the power-down pin control. 0 = Normal operation 1 = Ignores inputs on the power-down pin
5	PDN MASK SEL	R/W	0h	This bit selects power-down mask 1 or mask 2. 0 = Power-down mask 1 1 = Power-down mask 2
4-0	0	W	0h	Must write 0

8.5.2.2.6 Register 4Fh (address = 4Fh), Master Page (080h)

Figure 97. Register 4Fh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	EN INPUT DC COUPLING
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 32. Register 4Fh Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	EN INPUT DC COUPLING	R/W	0h	The device has an internal biasing resistor of 600 Ω from VCM to the INP and INM pins. A small common-mode current flows through these resistors causing approximately a 100-mV drop. To compensate for the drop, the device raises the VCM voltage by 100 mV by default. This compensation is particularly helpful in AC-coupling applications where the common-mode voltage on the INP and INM pins is established by internal biasing resistors. In DC-coupling applications, because the common-mode voltage is established by external circuit, there is no need to raise VCM by 100 mV. 0 = Device raises VCM voltage by 100 mV, useful in AC-coupling applications 1 = Device does not raise the VCM voltage, useful in DC-coupling applications

8.5.2.2.7 Register 53h (address = 53h), Master Page (080h)

Figure 98. Register 53h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	EN SYSREF DC COUPLING	MANUAL SYSREF
W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h

Table 33. Register 53h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1	EN SYSREF DC COUPLING	R/W	0h	Enables a higher common-mode voltage input on the SYSREF signal (up to 1.6 V). 0 = Normal operation 1 = Enables a higher SYSREF common-mode voltage support
0	MANUAL SYSREF	R/W	0h	The device has a feature to apply the SYSREF signal manually through the serial interface instead of the SYREFP, SYREFM pins. This application can be done by first setting the ENABLE MANUAL SYSREF register bit, then using the MANUAL SYSREF bit to set the SYSREF signal high or low. 0 = Set SYSREF low 1 = Set SYSREF high

8.5.2.2.8 Register 54h (address = 54h), Master Page (080h)

Figure 99. Register 54h

7	6	5	4	3	2	1	0
ENABLE MANUAL SYSREF	0	MASK SYSREF		0	0	0	0
R/W-0h	W-0h	R/W-0h		W-0h	W-0h	W-0h	W-0h

Table 34. Register 54h Field Descriptions

Bit	Field	Type	Reset	Description
7	ENABLE MANUAL SYSREF	R/W	0h	Enables the SYSREF input from the serial interface, thus disabling pin control. Use the MANUAL SYSREF register bit to apply SYSREF manually.
6	0	W	0h	Must write 0
5-4	MASK SYSREF	R/W	0h	00 = Normal operation 11 = The SYSREF signal is ignored by the device irrespective of how the signal was applied (through a pin or manually by the serial interface)
3-0	0	W	0h	Must write 0

8.5.2.2.9 Register 55h (address = 55h), Master Page (080h)

Figure 100. Register 55h

7	6	5	4	3	2	1	0
0	0	0	PDN MASK	0	0	0	0
W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h

Table 35. Register 55h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	W	0h	Must write 0
4	PDN MASK	R/W	0h	This bit enables power-down via a register bit. 0 = Normal operation 1 = Power-down is enabled by powering down internal blocks as specified in the selected power-down mask
3-0	0	W	0h	Must write 0

8.5.2.2.10 Register 59h (address = 59h), Master Page (080h)

Figure 101. Register 59h

7	6	5	4	3	2	1	0
FOVR CHB	0	ALWAYS WRITE 1	0	0	0	0	0
W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 36. Register 59h Field Descriptions

Bit	Field	Type	Reset	Description
7	FOVR CHB	W	0h	Outputs FOVR signal for channel B on the SDOUT pin. 0 = normal operation 1 = FOVR on SDOUT pin
6	0	W	0h	Must write 0
5	ALWAYS WRITE 1	R/W	0h	Must write 1
4-0	0	W	0h	Must write 0

8.5.2.3 ADC Page (0Fh) Register

8.5.2.3.1 Register 5F (address = 5F), ADC Page (0Fh)

Figure 102. Register 5F

7	6	5	4	3	2	1	0
FOVR THRESHOLD PROG							
R/W-E3h							

Table 37. Register 5F Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOVR THRESHOLD PROG	R/W	E3h	Program the fast OVR thresholds together for channel A and B, as described in the *Overrange Indication* section.

8.5.2.4 Main Digital Page (6800h) Registers

8.5.2.4.1 Register 0h (address = 0h), Main Digital Page (6800h)

Figure 103. Register 0h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	PULSE RESET
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 38. Register 0h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	PULSE RESET	R/W	0h	Must be pulsed after power-up or after configuring registers in the main digital page of the JESD bank. Any register bits in the main digital page (6800h) take effect only after this bit is pulsed; see the *Start-Up Sequence* section for the correct sequence. 0 = Normal operation 0 → 1 → 0 = Bit is pulsed

8.5.2.4.2 Register 41h (address = 41h), Main Digital Page (6800h)

Figure 104. Register 41h

7	6	5	4	3	2	1	0
0	0	DECFIL MODE[3]	DECFIL EN	0	DECFIL MODE[2:0]		
W-0h	W-0h	R/W-0h	R/W-0h	W-0h	R/W-0h		

Table 39. Register 41h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0
5	DECFIL MODE[3]	R/W	0h	This bit selects the decimation filter mode. Table 40 lists the bit settings. The decimation filter control (DEC MODE EN, register 4Dh, bit 3) and decimation filter enable (DECFIL EN, register 41h, bit 4) must be enabled.
4	DECFIL EN	R/W	0h	Enables the digital decimation filter 0 = Normal operation, full rate output 1 = Digital decimation enabled
3	0	W	0h	Must write 0
2-0	DECFIL MODE[2:0]	R/W	0h	These bits select the decimation filter mode. Table 40 lists the bit settings. The decimation filter control (DEC MODE EN, register 4Dh, bit 3) and decimation filter enable (DECFIL EN, register 41h, bit 4) must be enabled.

Table 40. DECFIL MODE Bit Settings

BITS (5, 2-0)	FILTER MODE	DECIMATION
0000	Band-pass filter centered on 3 × f_S / 16	4X
0100	Band-pass filter centered on 5 × f_S / 16	4X
1000	Band-pass filter centered on 1 × f_S / 16	4X
1100	Band-pass filter centered on 7 × f_S / 16	4X
0010	Low-pass filter	2X
0110	High-pass filter	2X
0011	Low-pass filter with f_S / 4 mixer	4X (IQ)

8.5.2.4.3 Register 42h (address = 42h), Main Digital Page (6800h)

Figure 105. Register 42h

7	6	5	4	3	2	1	0
0	0	0	0	0	NYQUIST ZONE		
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h		

Table 41. Register 42h Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	W	0h	Must write 0
2-0	NYQUIST ZONE	R/W	0h	The Nyquist zone must be selected for proper interleaving correction. Control must be enabled (register 4Eh, bit 7). 000 = 1st Nyquist zone (0 MHz to 500 MHz) 001 = 2nd Nyquist zone (500 MHz to 1000 MHz) 010 = 3rd Nyquist zone (1000 MHz to 1500 MHz) All others = Not used

8.5.2.4.4 Register 43h (address = 43h), Main Digital Page (6800h)

Figure 106. Register 43h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	FORMAT SEL
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 42. Register 43h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	FORMAT SEL	R/W	0h	Changes the output format. Set the FORMAT EN bit to enable control using this bit. 0 = Twos complement 1 = Offset binary

8.5.2.4.5 Register 44h (address = 44h), Main Digital Page (6800h)

Figure 107. Register 44h

7	6	5	4	3	2	1	0
0	DIGITAL GAIN						
R/W-0h	R/W-0h						

Table 43. Register 44h Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0h	Must write 0
6-0	DIGITAL GAIN	R/W	0h	Digital gain setting. Digital gain must be enabled (register 52h, bit 0). Gain in dB = 20log (digital gain / 32) 7Fh = 127 which equals digital gain of 12 dB

8.5.2.4.6 Register 4Bh (address = 4Bh), Main Digital Page (6800h)

Figure 108. Register 4Bh

7	6	5	4	3	2	1	0
0	0	FORMAT EN	0	0	0	0	0
W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 44. Register 4Bh Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0
5	FORMAT EN	R/W	0h	This bit enables control for data format selection using the FORMAT SEL register bit. 0 = Default, output is in twos complement format 1 = Output is in offset binary format after FORMAT SEL bit is also set
4-0	0	W	0h	Must write 0

8.5.2.4.7 Register 4Dh (address = 4Dh), Main Digital Page (6800h)

Figure 109. Register 4Dh

7	6	5	4	3	2	1	0
0	0	0	0	DEC MOD EN	0	0	0
W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

Table 45. Register 4Dh Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0
3	DEC MOD EN	R/W	0h	This bit enables control of decimation filter mode via the DECFIL MODE[3:0] register bits. 0 = Default 1 = Decimation modes control is enabled
2-0	0	W	0h	Must write 0

8.5.2.4.8 Register 4Eh (address = 4Eh), Main Digital Page (6800h)

Figure 110. Register 4Eh

7	6	5	4	3	2	1	0
CTRL NYQUIST	0	IMPROVE IL PERF	0	0	0	0	0
R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 46. Register 4Eh Field Descriptions

Bit	Field	Type	Reset	Description
7	CTRL NYQUIST	R/W	0h	This bit enables selecting the Nyquist zone using register 42h, bits 2-0. 0 = Selection disabled 1 = Selection enabled
6	0	W	0h	Must write 0
5	IMPROVE IL PERF	R/W	0h	Improves interleaving performance. Effective only for input frequencies that are within ± f_S / 64 band centered at n × f_S / 8 (n = 1, 2, 3, or 4). For example, at a 1-Gsps sampling rate, this bit may improve IL performance when input frequencies fall within the ±15.625-MHz band located at 125 MHz, 250 MHz, 375 MHz, and 500 MHz. 0 = Default 1 = Improves IL performance for certain input frequencies
4-0	0	W	0h	Must write 0

8.5.2.4.9 Register 52h (address = 52h), Main Digital Page (6800h)

Figure 111. Register 52h

7	6	5	4	3	2	1	0
BUS_REORDER_EN1	0	0	0	0	0	0	DIG GAIN EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 47. Register 52h Field Descriptions

Bit	Field	Type	Reset	Description
7	BUS_REORDER_EN1	R/W	0h	Must write 1 in DDC mode only
6-1	0	W	0h	Must write 0
0	DIG GAIN EN	R/W	0h	Enables selecting the digital gain for register 44h. 0 = Digital gain disabled 1 = Digital gain enabled

8.5.2.4.10 Register 72h (address = 72h), Main Digital Page (6800h)

Figure 112. Register 72h

7	6	5	4	3	2	1	0
0	0	0	0	BUS_REORDER_EN2	0	0	0
W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

Table 48. Register 72h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0
3	BUS_REORDER_EN2	R/W	0h	Must write a 1 in DDC mode only
2-0	0	W	0h	Must write 0

8.5.2.4.11 Register ABh (address = ABh), Main Digital Page (6800h)

Figure 113. Register ABh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	LSB SEL EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 49. Register ABh Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	LSB SEL EN	R/W	0h	Enable control for the LSB SELECT register bit. 0 = Default 1 = The LSB of 16-bit ADC data can be programmed as fast OVR using the LSB SELECT bit.

8.5.2.4.12 Register ADh (address = ADh), Main Digital Page (6800h)

Figure 114. Register ADh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LSB SELECT	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	

Table 50. Register ADh Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1-0	LSB SELECT	R/W	0h	Enables output of the FOVR flag instead of the output data LSB. 00 = Output is 16-bit data 11 = Output data LSB is replaced by the FOVR information for each channel

8.5.2.4.13 Register F7h (address = F7h), Main Digital Page (6800h)

Figure 115. Register F7h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DIG RESET
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 51. Register F7h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	DIG RESET	W	0h	Self-clearing reset for the digital block. Does not include the interleaving correction. 0 = Normal operation 1 = Digital reset

8.5.2.5 JESD Digital Page (6900h) Registers

8.5.2.5.1 Register 0h (address = 0h), JESD Digital Page (6900h)

Figure 116. Register 0h

7	6	5	4	3	2	1	0
CTRL K	0	0	TESTMODE EN	FLIP ADC DATA	LANE ALIGN	FRAME ALIGN	TX LINK DIS
R/W-0h	W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 52. Register 0h Field Descriptions

Bit	Field	Type	Reset	Description
7	CTRL K	R/W	0h	Enable bit for a number of frames per multi frame. 0 = Default is five frames per multi frame 1 = Frames per multi frame can be set in register 06h
6-5	0	W	0h	Must write 0
4	TESTMODE EN	R/W	0h	This bit generates the long transport layer test pattern mode, as per section 5.1.6.3 of the JESD204B specification. 0 = Test mode disabled 1 = Test mode enabled
3	FLIP ADC DATA	R/W	0h	0 = Normal operation 1 = Output data order is reversed: MSB to LSB.
2	LANE ALIGN	R/W	0h	This bit inserts the lane alignment character (K28.3) for the receiver to align to lane boundary, as per section 5.3.3.5 of the JESD204B specification. 0 = Normal operation 1 = Inserts lane alignment characters
1	FRAME ALIGN	R/W	0h	This bit inserts the lane alignment character (K28.7) for the receiver to align to lane boundary, as per section 5.3.3.5 of the JESD204B specification. 0 = Normal operation 1 = Inserts frame alignment characters
0	TX LINK DIS	R/W	0h	This bit disables sending the initial link alignment (ILA) sequence when $\overline{\text{SYNC}}$ is de-asserted. 0 = Normal operation 1 = ILA disabled

8.5.2.5.2 Register 1h (address = 1h), JESD Digital Page (6900h)

Figure 117. Register 1h

7	6	5	4	3	2	1	0
SYNC REG	SYNC REG EN	JESD FILTER			JESD MODE		
R/W-0h	R/W-0h	R/W-0h			R/W-01h		

Table 53. Register 1h Field Descriptions

Bit	Field	Type	Reset	Description
7	SYNC REG	R/W	0h	Register control for sync request. 0 = Normal operation 1 = ADC output data are replaced with K28.5 characters. Register bit SYNC REG EN must also be set to 1.
6	SYNC REG EN	R/W	0h	Enables register control for sync request. 0 = Use the $\overline{\text{SYNC}}$ pin for sync requests 1 = Use the SYNC REG register bit for sync requests
5-3	JESD FILTER	R/W	0h	These bits and the JESD MODE bits set the correct LMFS configuration for the JESD interface. The JESD FILTER setting must match the configuration in the decimation filter page. 000 = Filter bypass mode See Table 54 for valid combinations for register bits JESD FILTER along with JESD MODE.
2-0	JESD MODE	R/W	01h	These bits select the number of serial JESD output lanes per ADC. The JESD PLL MODE register bit located in the JESD analog page must also be set accordingly. 001 = Default after reset(Eight active lanes) See Table 54 for valid combinations for register bits JESD FILTER along with JESD MODE.

Table 54. Valid Combinations for JESD FILTER and JESD MODE Bits

REGISTER BIT JESD FILTER	REGISTER BIT JESD MODE	DECIMATION FACTOR	NUMBER OF ACTIVE LANES PER DEVICE
000	100	No decimation	Four lanes are active
000	010	No decimation	Four lanes are active
000	001	No decimation (default after reset)	Eight lanes are active
111	001	4X (IQ)	Four lanes are active
110	001	2X	Four lanes are active
110	010	2X	Two lanes are active
100	001	4X	Two lanes are active
111	010	4X (IQ)	Two lanes are active
100	010	4X	One lane is active

8.5.2.5.3 Register 2h (address = 2h), JESD Digital Page (6900h)

Figure 118. Register 2h

7	6	5	4	3	2	1	0
LINK LAYER TESTMODE			LINK LAYER RPAT	LMFC MASK RESET	0	0	0
R/W-0h			R/W-0h	R/W-0h	W-0h	W-0h	W-0h

Table 55. Register 2h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	LINK LAYER TESTMODE	R/W	0h	These bits generate a pattern according to clause 5.3.3.8.2 of the JESD204B document. 000 = Normal ADC data 001 = D21.5 (high-frequency jitter pattern) 010 = K28.5 (mixed-frequency jitter pattern) 011 = Repeat initial lane alignment (generates a K28.5 character and continuously repeats lane alignment sequences) 100 = 12 octet RPAT jitter pattern All others = Not used
4	LINK LAYER RPAT	R/W	0h	This bit changes the running disparity in the modified RPAT pattern test mode (only when the link layer test mode = 100). 0 = Normal operation 1 = Changes disparity
3	LMFC MASK RESET	R/W	0h	Mask LMFC reset coming to digital block. 0 = LMFC reset is not masked 1 = Ignore LMFC reset request
2-0	0	W	0h	Must write 0

8.5.2.5.4 Register 3h (address = 3h), JESD Digital Page (6900h)

Figure 119. Register 3h

7	6	5	4	3	2	1	0
FORCE LMFC COUNT	LMFC COUNT INIT					RELEASE ILANE SEQ	
R/W-0h	R/W-0h					R/W-0h	

Table 56. Register 3h Field Descriptions

Bit	Field	Type	Reset	Description
7	FORCE LMFC COUNT	R/W	0h	This bit forces the LMFC count. 0 = Normal operation 1 = Enables using a different starting value for the LMFC counter
6-2	LMFC COUNT INIT	R/W	0h	When SYSREF transmits to the digital block, the LMFC count resets to 0 and K28.5 stops transmitting when the LMFC count reaches 31. The initial value that the LMFC count resets to can be set using LMFC COUNT INIT. In this manner, the receiver can be synchronized early because it receives the LANE ALIGNMENT SEQUENCE early. The FORCE LMFC COUNT register bit must be enabled.
1-0	RELEASE ILANE SEQ	R/W	0h	These bits delay the generation of the lane alignment sequence by 0, 1, 2 or 3 multi frames after the code group synchronization. 00 = 0 01 = 1 10 = 2 11 = 3

8.5.2.5.5 Register 5h (address = 5h), JESD Digital Page (6900h)

Figure 120. Register 5h

7	6	5	4	3	2	1	0
SCRAMBLE EN	0	0	0	0	0	0	0
R/W-Undefined	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 57. Register 5h Field Descriptions

Bit	Field	Type	Reset	Description
7	SCRAMBLE EN	R/W	Undefined	Scramble enable bit in the JESD204B interface. 0 = Scrambling disabled 1 = Scrambling enabled
6-0	0	W	0h	Must write 0

8.5.2.5.6 Register 6h (address = 6h), JESD Digital Page (6900h)

Figure 121. Register 6h

7	6	5	4	3	2	1	0
0	0	0	FRAMES PER MULTI FRAME (K)				
W-0h	W-0h	W-0h	R/W-8h				

Table 58. Register 6h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	W	0h	Must write 0
4-0	FRAMES PER MULTI FRAME (K)	R/W	8h	These bits set the number of multi frames. Actual K is the value in hex + 1 (that is, 0Fh is K = 16).

8.5.2.5.7 Register 7h (address = 7h), JESD Digital Page (6900h)

Figure 122. Register 7h

7	6	5	4	3	2	1	0
0	0	0	0	SUBCLASS	0	0	0
W-0h	W-0h	W-0h	W-0h	R/W-1h	W-0h	W-0h	W-0h

Table 59. Register 7h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0
3	SUBCLASS	R/W	1h	This bit sets the JESD204B subclass. 000 = Subclass 0 backward compatible with JESD204A 001 = Subclass 1 deterministic latency using the SYSREF signal
2-0	0	W	0h	Must write 0

8.5.2.5.8 Register 16h (address = 16h), JESD Digital Page (6900h)

Figure 123. Register 16h

7	6	5	4	3	2	1	0
1	0	0	LANE SHARE	0	0	0	0
W-1h	W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 60. Register 16h Field Descriptions

Bit	Field	Type	Reset	Description
7	1	W	1h	Must write 1
6-5	0	W	0h	Must write 0
4	LANE SHARE	R/W	0h	When using decimate-by-4, the data of both channels are output over one lane (LMFS = 1241). 0 = Normal operation (each channel uses one lane) 1 = Lane sharing is enabled, both channels share one lane (LMFS = 1241)
3-0	0	W	0h	Must write 0

8.5.2.5.9 Register 31h (address = 31h), JESD Digital Page (6900h)

Figure 124. Register 31h

7	6	5	4	3	2	1	0
DA_BUS_REORDER[7:0]							
R/W-0h							

Table 61. Register 31h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DA_BUS_REORDER[7:0]	R/W	0h	Use these bits to program output connections between data streams and output lanes in decimate-by-2 and decimate-by-4 mode. Table 14 lists the supported combinations of these bits.

8.5.2.5.10 Register 32h (address = 32h), JESD Digital Page (6900h)

Figure 125. Register 32h

7	6	5	4	3	2	1	0
DB_BUS_REORDER[7:0]							
R/W-0h							

Table 62. Register 32h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DB_BUS_REORDER[7:0]	R/W	0h	Use these bits to program output connections between data streams and output lanes in decimate-by-2 and decimate-by-4 mode. Table 14 lists the supported combinations of these bits.

8.5.2.6 JESD Analog Page (6A00h) Registers

8.5.2.6.1 Register 12h (address = 12h), JESD Analog Page (6A00h)

Figure 126. Register 12h

7	6	5	4	3	2	1	0
SEL EMP LANE 1						ALWAYS WRITE 1	0
R/W-0h						W-0h	W-0h

Table 63. Register 12h-15h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	SEL EMP LANE 1	R/W	0h	Selects the amount of de-emphasis for the JESD output transmitter. The de-emphasis value in dB is measured as the ratio between the peak value after the signal transition to the settled value of the voltage in one bit period. 000000 = 0 dB 000001 = –1 dB 000011 = –2 dB 000111 = –4.1 dB 001111 = –6.2 dB 011111 = –8.2 dB 111111 = –11.5 dB
1	ALWAYS WRITE 1	W	0h	1 = Always write 1
0	0	W	0h	0 = Must write 0

8.5.2.6.2 Registers 13h-15h (address = 13h-15h), JESD Analog Page (6A00h)

Figure 127. Register 13h

7	6	5	4	3	2	1	0
SEL EMP LANE 0						0	0
R/W-0h						W-0h	W-0h

Figure 128. Register 14h

7	6	5	4	3	2	1	0
SEL EMP LANE 2						0	0
R/W-0h						W-0h	W-0h

Figure 129. Register 15h

7	6	5	4	3	2	1	0
SEL EMP LANE 3						0	0
R/W-0h						W-0h	W-0h

Table 64. Register 13h-15h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	SEL EMP LANE x (where x = 0, 2, or 3)	R/W	0h	Selects the amount of de-emphasis for the JESD output transmitter. The de-emphasis value in dB is measured as the ratio between the peak value after the signal transition to the settled value of the voltage in one bit period. 000000 = 0 dB 000001 = –1 dB 000011 = –2 dB 000111 = –4.1 dB 001111 = –6.2 dB 011111 = –8.2 dB 111111 = –11.5 dB
1-0	0	W	0h	0 = Must write 0

8.5.2.6.3 Register 16h (address = 16h), JESD Analog Page (6A00h)

Figure 130. Register 16h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	JESD PLL MODE	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	

Table 65. Register 16h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1-0	JESD PLL MODE	R/W	0h	These bits select the JESD PLL multiplication factor and must match the JESD MODE setting. 00 = 20X mode, four lanes per ADC 01 = Not used 10 = 40X mode 11 = Not used Table 14 lists a programming summary of the DDC modes and JESD link configuration.

8.5.2.6.4 Register 17h (address = 17h), JESD Analog Page (6A00h)

Figure 131. Register 17h

7	6	5	4	3	2	1	0
0	PLL RESET	LANE PDN 1	0	LANE PDN 0	0	0	0
W-0h	R/W-0h	R/W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

Table 66. Register 17h Field Descriptions

Bit	Field	Type	Reset	Description
7	0	W	0h	Must write 0
6	PLL RESET	R/W	0h	Pulse this bit after powering up the device; see Table 75. 0 = Default 0 → 1 → 0 = The PLL RESET bit is pulsed.
5	LANE PDN 1	R/W	0h	This bit powers down unused SERDES lanes DA0, DA3, DB0, and DB3 in certain LMFS settings (applicable for LMFS = 4244, 2242, 2441, 4211, and 2221). Powering down unused lanes puts the SERDES buffers in tri-state mode and saves approximately 15-mA current on the IOVDD supply. 00 : Default 11 : DA0, DB0, DA3, and DB3 are powered down Others: Do not use
4	0	W	0h	Must write 0
3	LANE PDN 0	R/W	0h	This bit powers down unused SERDES lanes DA0, DA3, DB0, and DB3 in certain LMFS settings (applicable for LMFS = 4244, 2242, 2441, 4211, and 2221). Powering down unused lanes puts the SERDES buffers in tri-state mode and saves approximately 15-mA current on the IOVDD supply. 00 : Default 11 : DA0, DB0, DA3, and DB3 are powered down Others: Do not use
2-0	0	W	0h	Must write 0

8.5.2.6.5 Register 1Ah (address = 1Ah), JESD Analog Page (6A00h)

Figure 132. Register 1Ah

7	6	5	4	3	2	1	0
0	0	0	0	0	0	FOVR CHA	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

Table 67. Register 1Ah Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1	FOVR CHA	R/W	0h	Outputs FOVR signal for channel A on the PDN pin. FOVR CHA EN (register 1Bh, bit 3) must be enabled. 0 = Normal operation 1 = FOVR on the PDN pin
0	0	W	0h	Must write 0

8.5.2.6.6 Register 1Bh (address = 1Bh), JESD Analog Page (6A00h)

Figure 133. Register 1Bh

7	6	5	4	3	2	1	0
JESD SWING			0	FOVR CHA EN	0	0	0
R/W-0h			W-0h	R/W-0h	W-0h	W-0h	W-0h

Table 68. Register 1Bh Field Descriptions

Bit	Field	Type	Reset	Description
7-5	JESD SWING	R/W	0h	Selects output amplitude VOD (mVpp) of the JESD transmitter (for all lanes) 0 = 860 mVpp 1 = 810 mVpp 2 = 770 mVpp 3 = 745 mVpp 4 = 960 mVpp 5 = 930 mVpp 6 = 905 mVpp 7 = 880 mVpp
4	0	W	0h	Must write 0
3	FOVR CHA EN	R/W	0h	Enables overwrite of PDN pin with the FOVR signal from ChA. 0 = Normal operation 1 = PDN is being overwritten
2-0	0	R/W	0h	Must write 0

8.5.2.7 Offset Read Page (JESD BANK PAGE SEL = 6100h, JESD BANK PAGE SEL1 = 0000h) Registers

8.5.2.7.1 Register 068h (address = 068h), Offset Read Page

Figure 134. Register 068h

7	6	5	4	3	2	1	0
FREEZE CORR	DC OFFSET CORR BW				BYPASS CORR	ALWAYS WRITE 1	0
R/W-0h	R/W-0h				R/W-0h	R/W-0h	W-0h

Table 69. Register 068h Field Descriptions

Bit	Field	Type	Reset	Description
7	FREEZE CORR	R/W	0h	Offset correction block is enabled by default. Set this bit to freeze the block. 0 = Default after reset 1 = Offset correction block is frozen See the *DC Offset Correction Block in the ADS54J60* section for details.
6-3	DC OFFSET CORR BW	R/W	0h	These bits allow the user to program the 3-dB bandwidth of the notch filter centered around k × f_S / 4 (k = 0, 1, 2). The notch filter is a first-order digital filter with 3-dB bandwidth: 3-dB bandwidth normalized to f_S 0 = 2.99479E-07 1 = 1.4974E-07 2 = 7.48698E-08 3 = 3.74349E-08 4 = 1.87174E-08 5 = 9.35872E-09 6 = 4.67936E-09 7 = 2.33968E-09 8 = 1.16984E-09 9 = 5.8492E-10 10 = 2.9246E-10 11 = 1.4623E-10 For example, at f_S = 1 GSPS, if DC OFFSET CORR BW is set to 1, the notch filter has a 3-dB bandwidth of 149.74 Hz.
2	BYPASS CORR	R/W	0h	0 = Default after reset 1 = Offset correction block is bypassed See the *DC Offset Correction Block in the ADS54J60* section for details.
1	ALWAYS WRITE 1	R/W	0h	Always write 1
0	0	W	0h	Must write 0

8.5.2.7.2 Register 069h (address = 069h), Offset Read Page

Figure 135. Register 069h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	EXT CORR EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

Table 70. Register 069h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	EXT CORR EN	R/W	0h	Enables loading of external estimate into offset correction block. 0 = Default after reset (device uses internal estimate for offset correction) 1 = External estimate can be loaded by using the ADCx_LOAD_EXT_EST register bits See the *DC Offset Correction Block in the ADS54J60* section for details.

8.5.2.7.3 Registers 074h, 076h, 078h, 7Ah (address = 074h, 076h, 078h, 7Ah), Offset Read Page

Figure 136. Registers 074h, 076h, 078h, 7Ah

7	6	5	4	3	2	1	0
ADCx_CORR_INT_EST[7:0]							
R/W-0h							

Table 71. Registers 074h, 076h, 078h, 7Ah Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ADCx_CORR_INT_EST[7:0]	R/W	0h	Internal estimate for all four interleaving ADC cores of the dc offset corrector block can be read from these bits. Keep the R/W bit set to 1 when reading from these registers. See the *DC Offset Correction Block in the ADS54J60* section for details.

8.5.2.7.4 Registers 075h, 077h, 079h, 7Bh (address = 075h, 077h, 079h, 7Bh), Offset Read Page

Figure 137. Registers 075h, 077h, 079h, 7Bh

7	6	5	4	3	2	1	0
0	0	0	0	0	ADCx_CORR_INT_EST[10:8]		
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h		

Table 72. Registers 075h, 077h, 079h, 7Bh Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	W	0h	Must write 0
2-0	ADCx_CORR_INT_EST[10:8]	R/W	0h	Internal estimate for all four interleaving ADC cores of the dc offset corrector block can be read from these bits. Keep the R/W bit set to 1 when reading from these registers. See the *DC Offset Correction Block in the ADS54J60* section for details.

8.5.2.8 Offset Load Page (JESD BANK PAGE SEL= 6100h, JESD BANK PAGE SEL1 = 0500h) Registers

8.5.2.8.1 Registers 00h, 04h, 08h, 0Ch (address = 00h, 04h, 08h, 0Ch), Offset Load Page

Figure 138. Registers 00h, 04h, 08h, 0Ch

7	6	5	4	3	2	1	0
ADCx_LOAD_EXT_EST[7:0]							
R/W-0h							

Table 73. Registers 00h, 04h, 08h, 0Ch Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ADCx_LOAD_EXT_EST[7:0]	R/W	0h	External estimate can be loaded into the dc offset corrector blocks for all four interleaving ADC cores. See the *DC Offset Correction Block in the ADS54J60* section for details.

8.5.2.8.2 Registers 01h, 05h, 09h, 0Dh (address = 01h, 05h, 09h, 0Dh), Offset Load Page

Figure 139. Registers 01h, 05h, 09h, 0Dh

7	6	5	4	3	2	1	0
0	0	0	0	0	ADCx_LOAD_EXT_EST[10:8]		
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h		

Table 74. Registers 01h, 05h, 09h, 0Dh Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	W	0h	Must write 0
2-0	ADCx_CORR_INT_EST[10:8]	R/W	0h	External estimate can be loaded into the dc offset corrector blocks for all four interleaving ADC cores. See the *DC Offset Correction Block in the ADS54J60* section for details.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Start-Up Sequence

The steps described in Table 75 are recommended as the power-up sequence with the ADS54J60 in 20X mode (LMFS = 8224).

Table 75. Initialization Sequence

STEP	SEQUENCE	DESCRIPTION	PAGE BEING PROGRAMMED	COMMENT
1	Power-up the device	Bring up IOVDD to 1.15 V before applying power to DVDD. Bring up DVDD to 1.9 V, AVDD to 1.9 V, and AVDD3V to 3.0 V.	—	See the *Power Sequencing and Initialization* section for power sequence requirements.
2	Reset the device	**Hardware reset**		
		Apply a hardware reset by pulsing pin 48 (low → high → low).	—	A hardware reset clears all registers to their default values.
		Register writes are equivalent to a hardware reset.		
		Write address 0-000h with 81h.	General register	Reset registers in the ADC and master pages of the analog bank.
				This bit is a self-clearing bit.
		Write address 4-001h with 00h and address 4-002h with 00h.	Unused page	Clear any unwanted content from the unused pages of the JESD bank.
		Write address 4-003h with 00h and address 4-004h with 68h.	—	Select the main digital page of the JESD bank.
		Write address 6-0F7h with 01h for channel A.	Main digital page (JESD bank)	Use the DIG RESET register bit to reset all pages in the JESD bank.
				This bit is a self-clearing bit.
		Write address 6-000h with 01h, then address 6-000h with 00h.		Pulse the PULSE RESET register bit for channel A.
3	Performance modes	Write address 0-011h with 80h.	—	Select the master page of the analog bank.
		Write address 0-059h with 20h.	Master page (analog bank)	Set the ALWAYS WRITE 1 bit.
4	Program desired registers for decimation options and JESD link configuration	**Default register writes for DDC modes and JESD link configuration (LMFS 8224).**		
		Write address 4-003h with 00h and address 4-004h with 69h.	—	Select the JESD digital page.
		Write address 6-000h with 80h.	JESD digital page (JESD bank)	Set the CTRL K bit for both channels by programming K according to the SYSREF signal later on in the sequence.
		JESD link is configured with LMFS = 8224 by default with no decimation.		See Table 14 for configuring the JESD digital page registers for the desired LMFS and programming appropriate DDC mode.
		Write address 4-003h with 00h and address 4-004h with 6Ah.	—	Select the JESD analog page.
		JESD link is configured with LMFS = 8224 by default with no decimation.	JESD analog page (JESD bank)	See Table 14 for configuring the JESD analog page registers for the desired LMFS and programming appropriate DDC mode.
		Write address 6-017h with 40h.		PLL reset.
		Write address 6-017h with 00h.		PLL reset clear.
		Write address 4-003h with 00h and address 4-004h with 68h.	—	Select the main digital page.
		JESD link is configured with LMFS = 8224 by default with no decimation.	Main digital page (JESD bank)	See Table 14 for configuring the main digital page registers for the desired LMFS and programming appropriate DDC mode.
		Write address 6-000h with 01h and address 6-000h with 00h.		Pulse the PULSE RESET register bit. All settings programmed in the main digital page take effect only after this bit is pulsed.

Table 75. Initialization Sequence (continued)

STEP	SEQUENCE	DESCRIPTION	PAGE BEING PROGRAMMED	COMMENT
5	Set the value of K and the SYSREF signal frequency accordingly	Write address 4-003h with 00h and address 4-004h with 69h.	—	Select the JESD digital page.
		Write address 6-006h with XXh (choose the value of K).	JESD digital page (JESD bank)	See the *SYSREF Signal* section to choose the correct frequency for SYSREF.
6	JESD lane alignment	Pull the SYNCB pin (pin 63) low.	—	Transmit K28.5 characters.
		Pull the SYNCB pin high.		After the receiver is synchronized, initiate an ILA phase and subsequent transmissions of ADC data.

9.1.2 Hardware Reset

Figure 140 and Table 76 show the timing for a hardware reset.

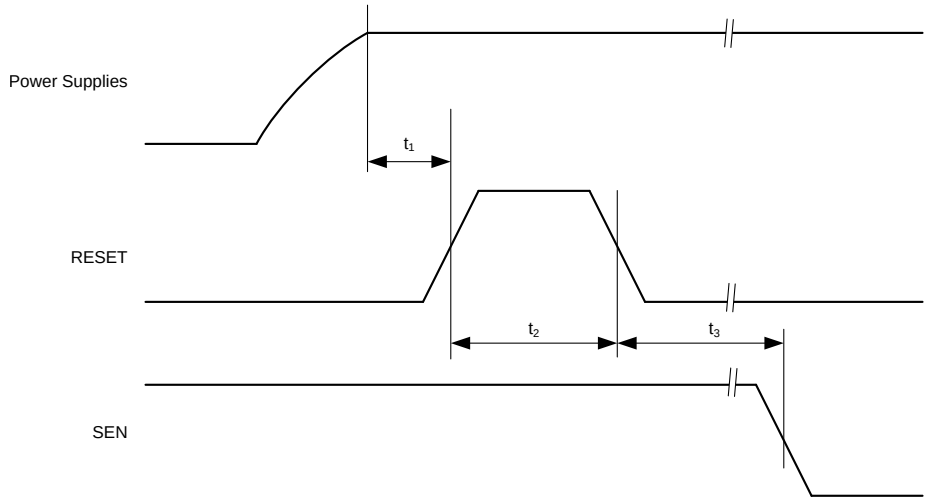


Figure 140. Hardware Reset Timing Diagram

Table 76. Timing Requirements for Figure 140

		MIN	TYP	MAX	UNIT
t_1	Power-on delay: delay from power up to active high RESET pulse	1			ms
t_2	Reset pulse duration: active high RESET pulse duration	10			ns
t_3	Register write delay: delay from RESET disable to SEN active	100			ns

9.1.3 SNR and Clock Jitter

The signal-to-noise ratio (SNR) of the ADC is limited by three different factors: quantization noise, thermal noise, and jitter, as shown in Equation 4. The quantization noise is typically not noticeable in pipeline converters and is 98 dB for a 16-bit ADC. The thermal noise limits the SNR at low input frequencies and the clock jitter sets the SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20log\sqrt{\left(10^{-\frac{SNR_{Quantization\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Thermal\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2} \quad (4)$$

The SNR limitation resulting from sample clock jitter can be calculated by Equation 5:

$$SNR_{Jitter}[dBc] = -20log(2\pi \times f_{in} \times T_{Jitter}) \quad (5)$$

The total clock jitter (T_{Jitter}) has two components: the internal aperture jitter (130 fs) is set by the noise of the clock input buffer and the external clock jitter. T_{Jitter} can be calculated by Equation 6:

$$T_{Jitter} = \sqrt{\left(T_{Jitter,\ Ext\_Clock\_Input}\right)^2 + \left(T_{Aperture\_ADC}\right)^2} \quad (6)$$

External clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as band-pass filters at the clock input. A faster clock slew rate also improves the ADC aperture jitter.

The ADS54J60 has a thermal noise of approximately 71.1 dBFS and an internal aperture jitter of 120 fs. The SNR, depending on the amount of external jitter for different input frequencies, is shown in Figure 141.

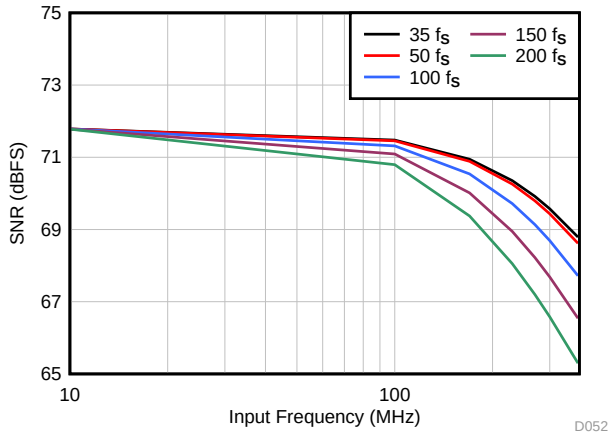


Figure 141. SNR versus Input Frequency and External Clock Jitter

9.1.4 DC Offset Correction Block in the ADS54J60

The ADS54J60 employs eight dc offset correction blocks (four per channel, one per interleaving core). Figure 142 shows a dc correction block diagram.

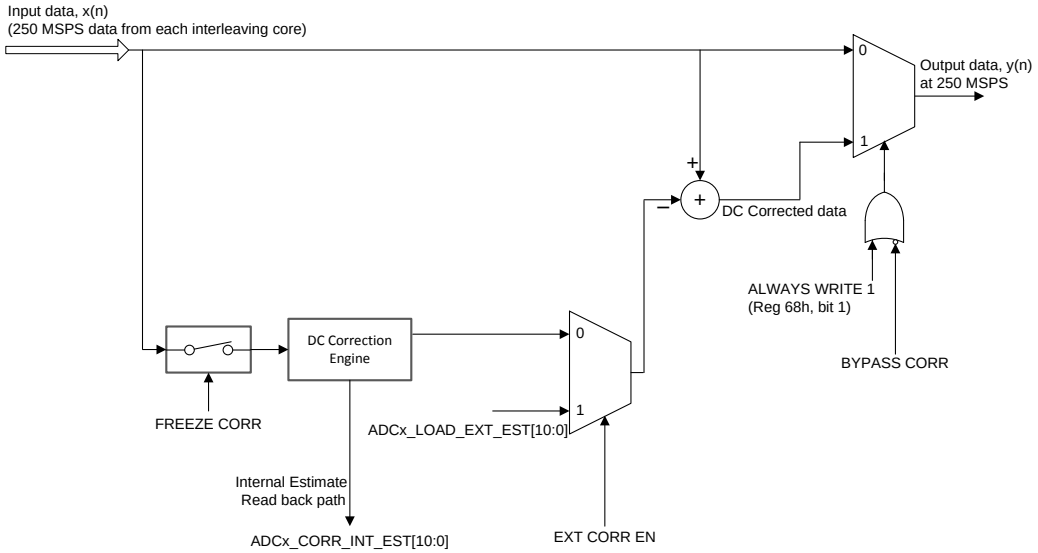


Figure 142. DC Offset Correction Block Diagram

The purpose of the dc offset correction block is to correct the dc offset of interleaving cores that mainly arise from the amplifier in the first pipeline stage. Any mismatch in dc offset among interleaving cores results in spurs at f_S / 4 and f_S / 2. The dc offset correction blocks estimate and correct the dc offset of an individual core, to the ideal mid-code value, and thereby remove the effect of offset mismatch.

The dc offset correction block can correct the dc offset of an individual core up to ±1024 codes.

In applications involving dc-coupling between the ADC and the driver, the dc offset correction block can either be *bypassed* or *frozen* because the block cannot distinguish the external dc signal from the internal dc offset. Figure 143 shows that when bypassed, the internal dc mismatch appears at dc, f_S / 4, and f_S / 2 frequency points and can be as big as –40 dBFS.

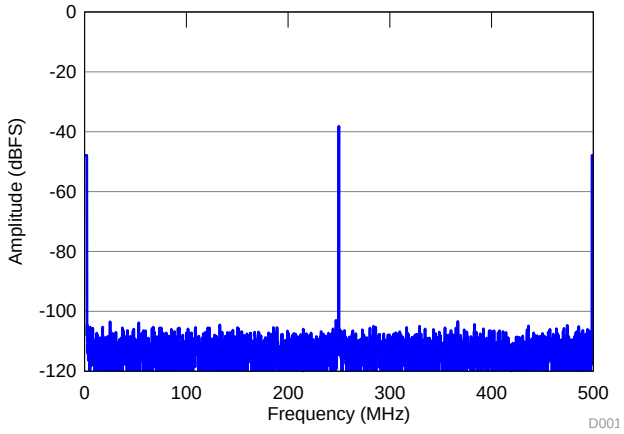


Figure 143. FFT After Bypassing the DC Offset Correction Block

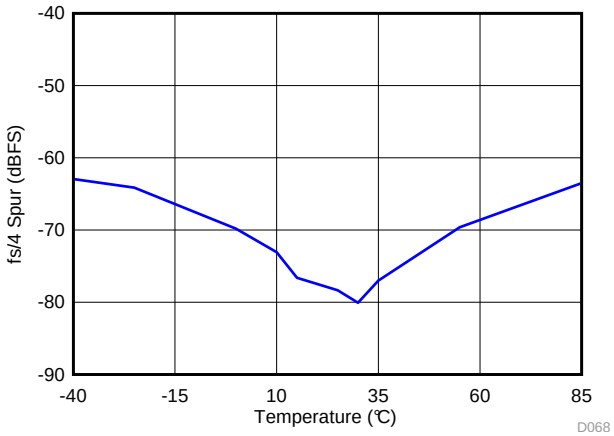
9.1.4.1 Freezing the DC Offset Correction Block

After device is powered up, the dc offset correction block estimates the internal dc offset with the idle channel input before the block is frozen. When frozen, the correction block holds the last estimated value that belongs to the internal dc offset. After the correction block is frozen, an external signal can be applied.

9.1.4.2 Effect of Temperature

The internal dc offset of the individual cores changes with temperature, resulting in f_S / 4 and f_S / 2 spurs appearing again in the spectrum at a different temperature.

Figure 144 shows a variation of the f_S / 4 spur over temperature for a typical device.



NOTE: The offset correction block was frozen at room temperature, then the temperature was varied from –40°C to +85°C.

Figure 144. Variation of the f_S / 4 Spur Over Temperature

Although some systems can accept such a variation in the f_S / 4 and f_S / 2 spurs across temperature, other systems may require the internal dc offset profile to be calibrated with temperature. To achieve this calibration, the device provides an option to read the internal estimate values from the correction block for each of the interleaving cores and also to load the values back to the correction block. For calibration, after power up, a temperature sweep can be performed with the idle channel input and the internal dc offset can be read back using the ADCx_CORR_INT_EST register bits for salient temperature points. Then during operation, when temperature changes, the corresponding estimates can be externally loaded to the correction block using the ADCx_LOAD_EXT_EST register bits.

The dc offset corrector block is enabled by default. For a given channel, the device can disable and freeze the block, read the estimate of the block, and load the external estimate.

Table 77 lists an example of required SPI writes for reading an internal estimate of the dc offset correction block, and then loading the estimate back to the corrector.

Table 77. Format (16-Bit Address, 8-Bit Data)

STEP	ADDRESS (Hex)(1)	DATA (Hex)	COMMENT
Reading an internal estimate from both channels	4-005	01	This setting disables broadcast mode (channel A and B can be individually programmed)
	4-004	61	Selects offset read page (61000000h)
	4-003	00	
	4-002	00	
	4-001	00	
	Data from the offset read page can be read as below (keep the R/W bit = 1)		
	E-074	xx	Reading the internal estimate [7:0] for core 0, channel A on the SDOUT pin
	E-075	xx	Reading the internal estimate [10:8] for core 0, channel A on the SDOUT pin
	E-076	xx	Reading the internal estimate [7:0] for core 1, channel A on the SDOUT pin
	E-077	xx	Reading the internal estimate [10:8] for core 1, channel A on the SDOUT pin
	E-078	xx	Reading the internal estimate [7:0] for core 2, channel A on the SDOUT pin
	E-079	xx	Reading the internal estimate [10:8] for core 2, channel A on the SDOUT pin
	E-07A	xx	Reading the internal estimate [7:0] for core 3, channel A on the SDOUT pin
	E-07B	xx	Reading the internal estimate [10:8] for core 3, channel A on the SDOUT pin
	F-074	xx	Reading the internal estimate [7:0] for core 0, channel B on the SDOUT pin
	F-075	xx	Reading the internal estimate [10:8] for core 0, channel B on the SDOUT pin
	F-076	xx	Reading the internal estimate [7:0] for core 1, channel B on the SDOUT pin
	F-077	xx	Reading the internal estimate [10:8] for core 1, channel B on the SDOUT pin
	F-078	xx	Reading the internal estimate [7:0] for core 2, channel B on the SDOUT pin
	F-079	xx	Reading the internal estimate [10:8] for core 2, channel B on the SDOUT pin
	F-07A	xx	Reading the internal estimate [7:0] for core 3, channel B on the SDOUT pin
	F-07B	xx	Reading the internal estimate [10:8] for core 3, channel B on the SDOUT pin

(1) The address field is represented in four hex bits in a-bcd format, where *a* contains information about the R/W, M, P, and CH bits, and *bcd* contain the actual address of the register.

Table 77. Format (16-Bit Address, 8-Bit Data) (continued)

STEP	ADDRESS (Hex)(1)	DATA (Hex)	COMMENT
Loading an external estimate to both channels	6-069	01	Enables the external correction bit located in the offset read page for channel A
	7-069	01	Enables the external correction bit located in the offset read page for channel B
	4-004	61	Change page to offset load page (61000500h)
	4-003	00	
	4-002	05	
	4-001	00	
	6-000	xx	Loading the external estimate [7:0] for core 0, channel A through SPI writes
	6-001	xx	Loading the external estimate [10:8] for core 0, channel A through SPI writes
	6-004	xx	Loading the external estimate [7:0] for core 1, channel A through SPI writes
	6-005	xx	Loading the external estimate [10:8] for core 1, channel A through SPI writes
	6-008	xx	Loading the external estimate [7:0] for core 2, channel A through SPI writes
	6-009	xx	Loading the external estimate [10:8] for core 2, channel A through SPI writes
	6-00C	xx	Loading the external estimate [7:0] for core 3, channel A through SPI writes
	6-00D	xx	Loading the external estimate [10:8] for core 3, channel A through SPI writes
	7-000	xx	Loading the external estimate [7:0] for core 0, channel B through SPI writes
	7-001	xx	Loading the external estimate [10:8] for core 0, channel B through SPI writes
	7-004	xx	Loading the external estimate [7:0] for core 1, channel B through SPI writes
	7-005	xx	Loading the external estimate [10:8] for core 1, channel B through SPI writes
	7-008	xx	Loading the external estimate [7:0] for core 2, channel B through SPI writes
	7-009	xx	Loading the external estimate [10:8] for core 2, channel B through SPI writes
	7-00C	xx	Loading the external estimate [7:0] for core 3, channel B through SPI writes
	7-00D	xx	Loading the external estimate [10:8] for core 3, channel B through SPI writes

9.1.5 Idle Channel Histogram

Figure 145 shows a histogram of output codes when no signal is applied at the analog inputs of the ADS54J60. When the dc offset correction block of the device is bypassed, Figure 146 shows that the output code histogram becomes multi-modal with as many as four peaks because the ADS54J60 is a 4-way interleaved ADC with each ADC core having a different internal dc offset.

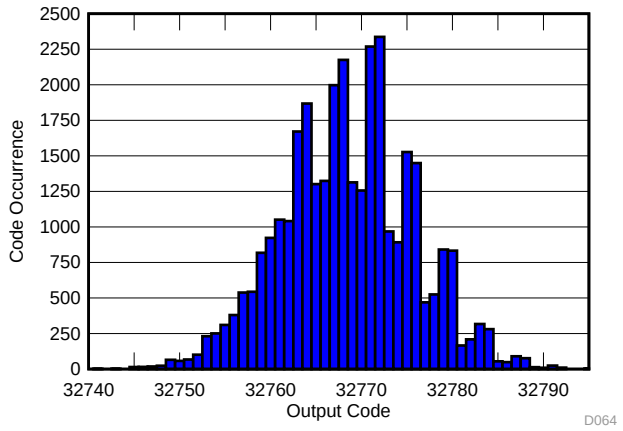


Figure 145. Idle Channel Histogram
(No Signal at Analog Inputs, DC Offset Correction is On)

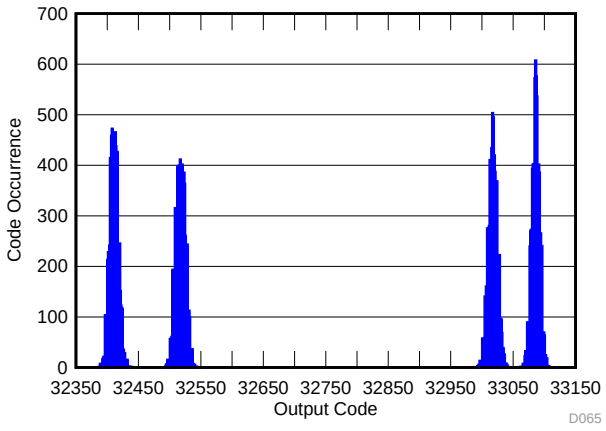


Figure 146. Idle Channel Histogram
(No Signal at Analog Inputs, DC Offset Correction is Off)

When the dc offset correction block is frozen (instead of being bypassed), as shown in Figure 147, the output code histogram improves (compared to when bypassed). However, when temperature changes, the dc offset difference among interleaving cores may increase, resulting in increased spacing between peaks in the histogram.

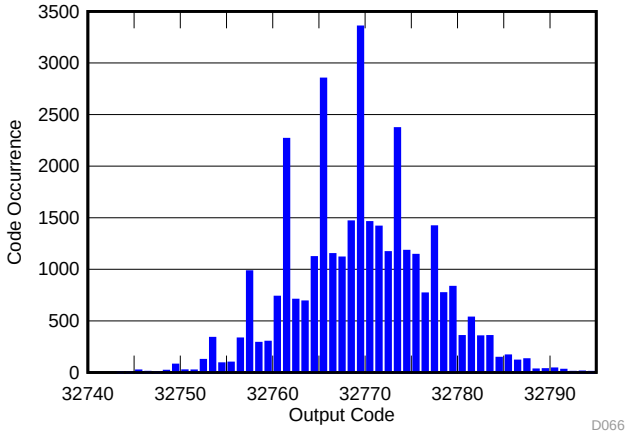
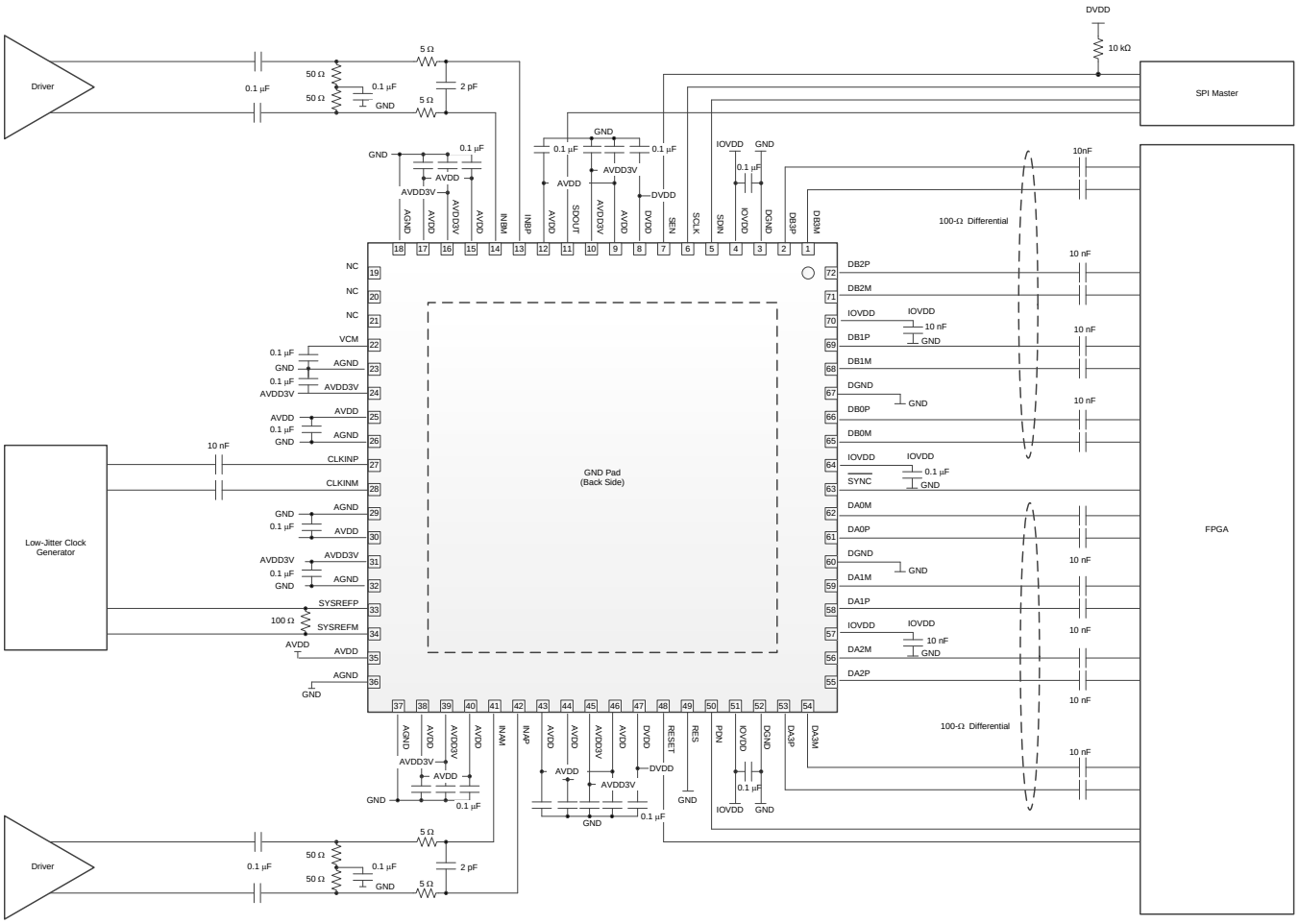


Figure 147. Idle Channel Histogram
(No Signal at Analog Inputs, DC Offset Correction is Frozen)

9.2 Typical Application

The ADS54J60 is designed for wideband receiver applications demanding excellent dynamic range over a large input frequency range. A typical schematic for an ac-coupled receiver is shown in Figure 148.



NOTE: GND = AGND and DGND connected in the PCB layout.

Figure 148. AC-Coupled Receiver

Typical Application (continued)

9.2.1 Design Requirements

9.2.1.1 Transformer-Coupled Circuits

Typical applications involving transformer-coupled circuits are discussed in this section. To achieve good phase and amplitude balances at the ADC inputs, surface-mount transformers can be used (for example, for frequencies up to 300 MHz, ADT1-1WT or WBC1-1 can be used and for higher input frequencies TC1-1-13M+ can be used). When designing dc driving circuits, the ADC input impedance must be considered. Figure 149 and Figure 150 show the impedance ($Z_{IN} = R_{IN} \parallel C_{IN}$) across the ADC input pins.

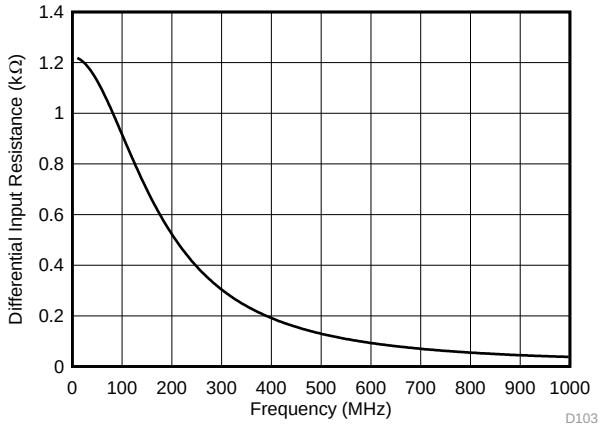


Figure 149. R_{IN} vs Input Frequency

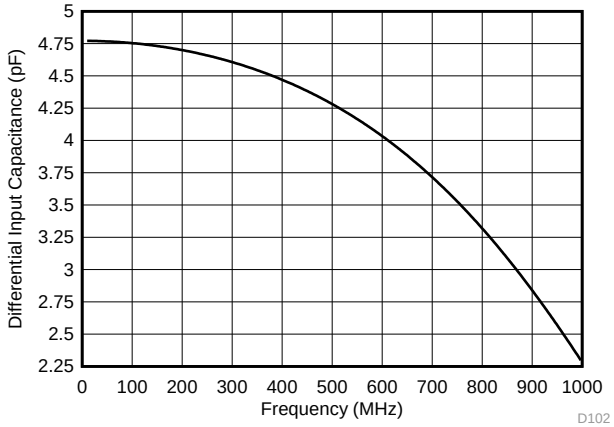


Figure 150. C_{IN} vs Input Frequency

By using the simple drive circuit of Figure 151, uniform performance can be obtained over a wide frequency range. The buffers present at the analog inputs of the device help isolate the external drive source from the switching currents of the sampling circuit.

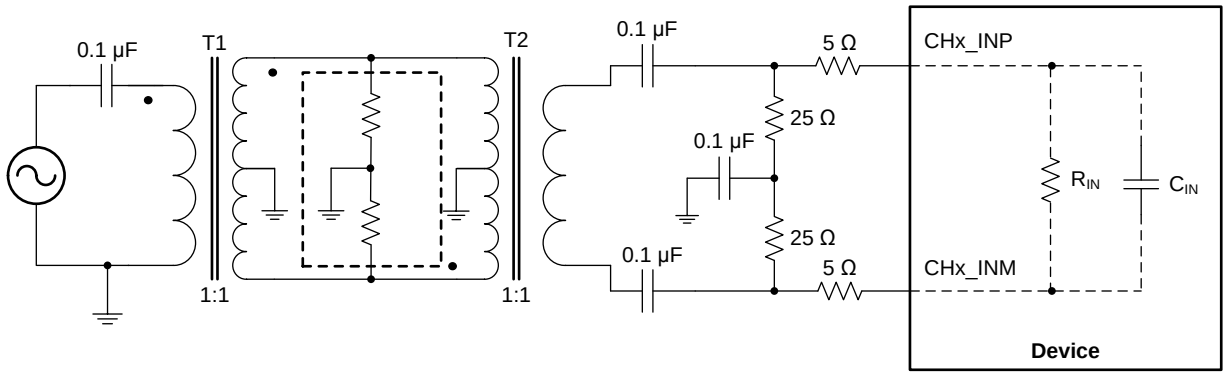


Figure 151. Input Drive Circuit

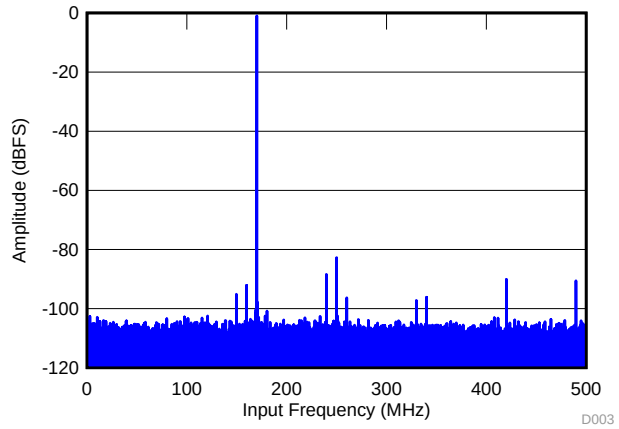
9.2.2 Detailed Design Procedure

For optimum performance, the analog inputs must be driven differentially. This architecture improves common-mode noise immunity and even-order harmonic rejection. A small resistor (5 Ω to 10 Ω) in series with each input pin is recommended to damp out ringing caused by package parasitics, as shown in Figure 151.

Typical Application (continued)

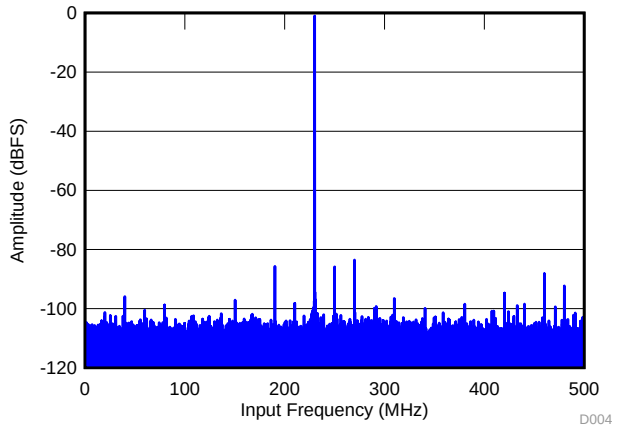
9.2.3 Application Curves

Figure 152 and Figure 153 show the typical performance at 170 MHz and 230 MHz, respectively.



SNR = 69.8 dBFS; SFDR = 88 dBc;
IL spur = 86 dBc; non HD2, HD3 spur = 89 dBc

Figure 152. FFT for 170-MHz Input Signal



SNR = 68.9 dBFS; SFDR = 85 dBc;
IL spur = 85 dBc; non HD2, HD3 spur = 86 dBc

Figure 153. FFT for 230-MHz Input Signal

10 Power Supply Recommendations

The device requires a 1.15-V nominal supply for IOVDD, a 1.9-V nominal supply for DVDD, a 1.9-V nominal supply for AVDD, and a 3.0-V nominal supply for AVDD3V. For detailed information regarding the operating voltage minimum and maximum specifications of different supplies, see the *Recommended Operating Conditions* table.

10.1 Power Sequencing and Initialization

Figure 154 shows the suggested power-up sequencing for the device. Note that the 1.15-V IOVDD supply must rise before the 1.9-V DVDD supply. If the 1.9-V DVDD supply rises before the 1.15-V IOVDD supply, then the internal default register settings may not load properly. The other supplies (the 3-V AVDD3V and the 1.9-V AVDD), can come up in any order during the power sequence. The power supplies can ramp up at any rate and there is no hard requirement for the time delay between IOVDD ramp up to DVDD ramp-up (can be in orders of microseconds but is recommend to be a few milliseconds).

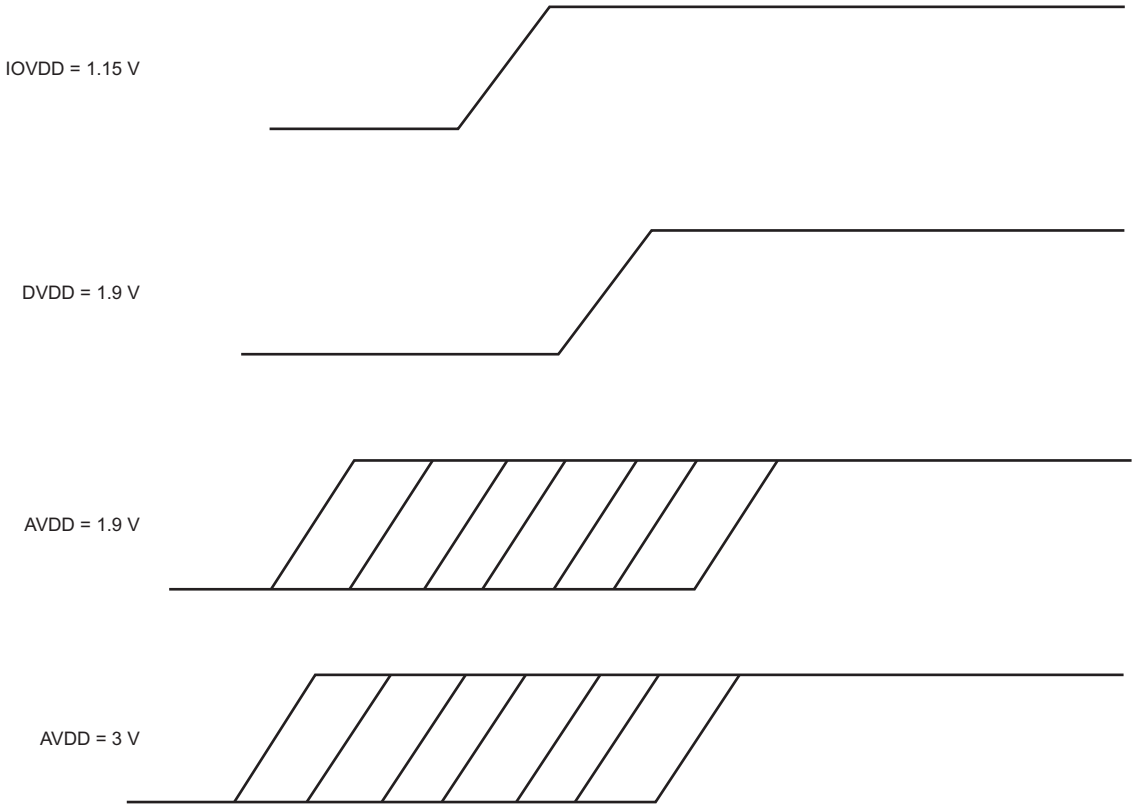


Figure 154. Power Sequencing for the ADS54Jxx Family of Devices

11 Layout

11.1 Layout Guidelines

The device evaluation module (EVM) layout can be used as a reference layout to obtain the best performance. A layout diagram of the EVM top layer is provided in Figure 155. A complete layout of the EVM is available at the ADS54J60 EVM folder. Some important points to remember during board layout are:

- Analog inputs are located on opposite sides of the device pinout to ensure minimum crosstalk on the package level. To minimize crosstalk onboard, the analog inputs must exit the pinout in opposite directions, as illustrated in the reference layout of Figure 155 as much as possible.
- In the device pinout, the sampling clock is located on a side perpendicular to the analog inputs in order to minimize coupling between them. This configuration is also maintained on the reference layout of Figure 155 as much as possible.
- Keep digital outputs away from the analog inputs. When these digital outputs exit the pinout, the digital output traces must not be kept parallel to the analog input traces because this configuration can result in coupling from the digital outputs to the analog inputs and degrade performance. All digital output traces to the receiver [such as a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC)] must be matched in length to avoid skew among outputs.
- At each power-supply pin (AVDD, DVDD, or AVDDD3V), keep a 0.1-µF decoupling capacitor close to the device. A separate decoupling capacitor group consisting of a parallel combination of 10-µF, 1-µF, and 0.1-µF capacitors can be kept close to the supply source.

NOTE

The PDN and SDOUT traces must be routed away from the analog input traces. When the PDN and SDOUT pins are programmed to carry OVR information, the proximity of these pins to the analog input traces may result in degradation of ADC performance because of coupling. For best performance, the PDN and SDOUT traces must not overlap or cross the path of the analog input traces even if routed on different layers of the PCB.

11.2 Layout Example

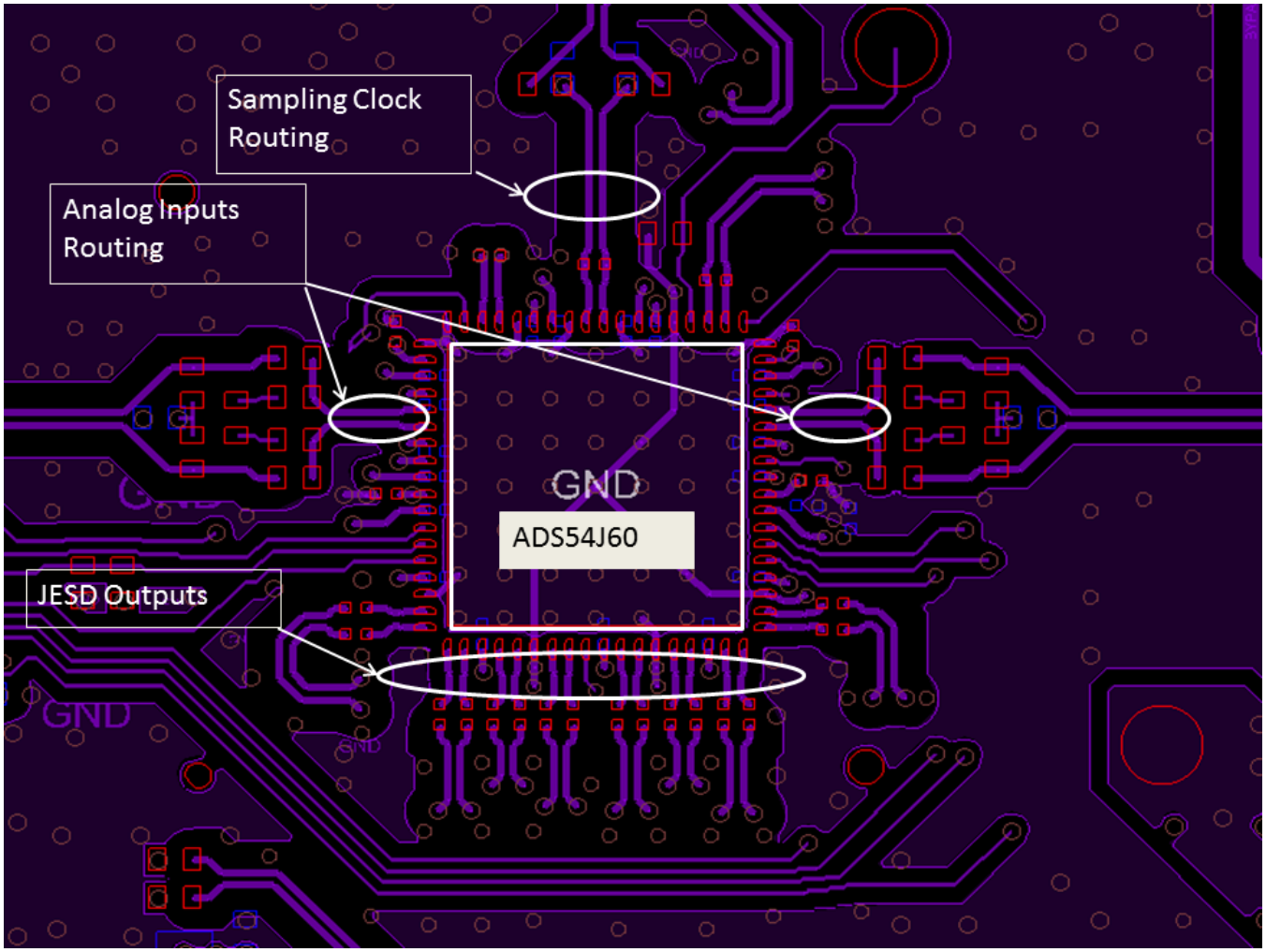


Figure 155. ADS54J60 EVM layout

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，《*ADS54J20 双通道 12 位 1.0GSPS 模数转换器*》数据表
- 德州仪器 (TI)，《*ADS54J40 双通道 14 位 1.0GSPS 模数转换器*》数据表
- 德州仪器 (TI)，《*ADS54J42 双通道 14 位 625MSPS 模数转换器*》数据表
- 德州仪器 (TI)，《*具有集成 DDC 的 ADS54J66 四通道 14 位 500MSPS ADC*》数据表
- 德州仪器 (TI)，《*ADS54J69 双通道 16 位 500MSPS 模数转换器*》数据表
- 德州仪器 (TI)，《*ADS54J60EVM 用户指南*》

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商标

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ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS54J60IRMP	ACTIVE	VQFN	RMP	72	168	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ54J60	Samples
ADS54J60IRMPT	ACTIVE	VQFN	RMP	72	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ54J60	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

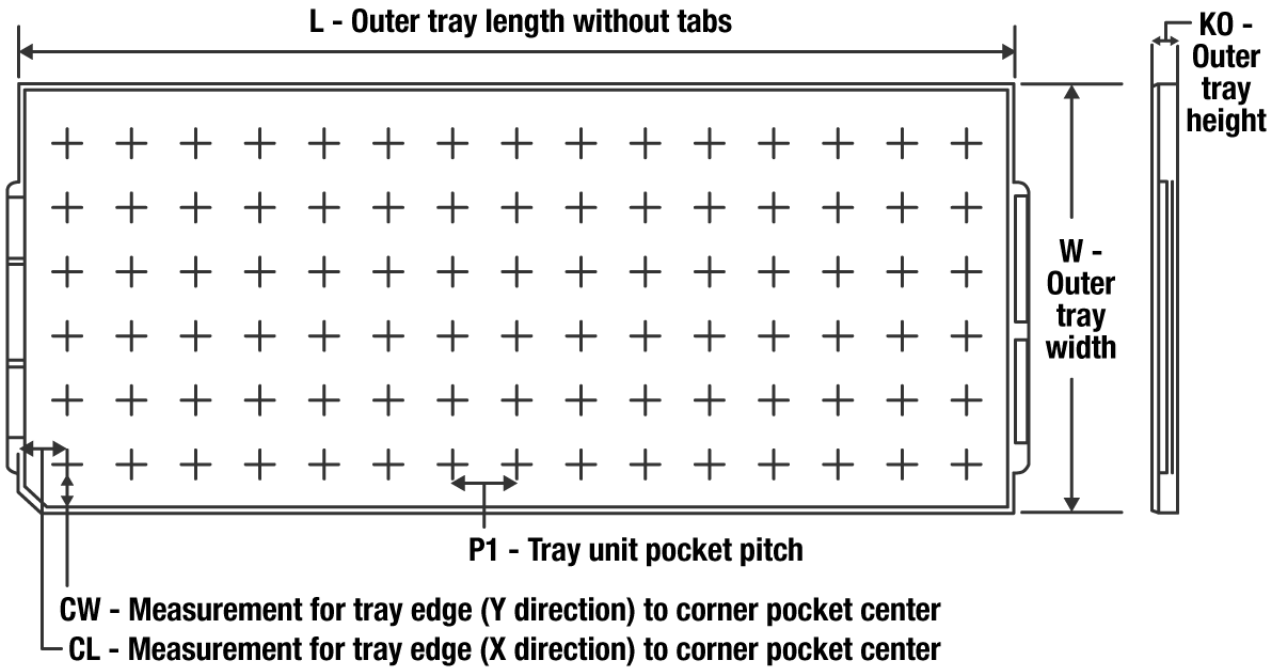
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

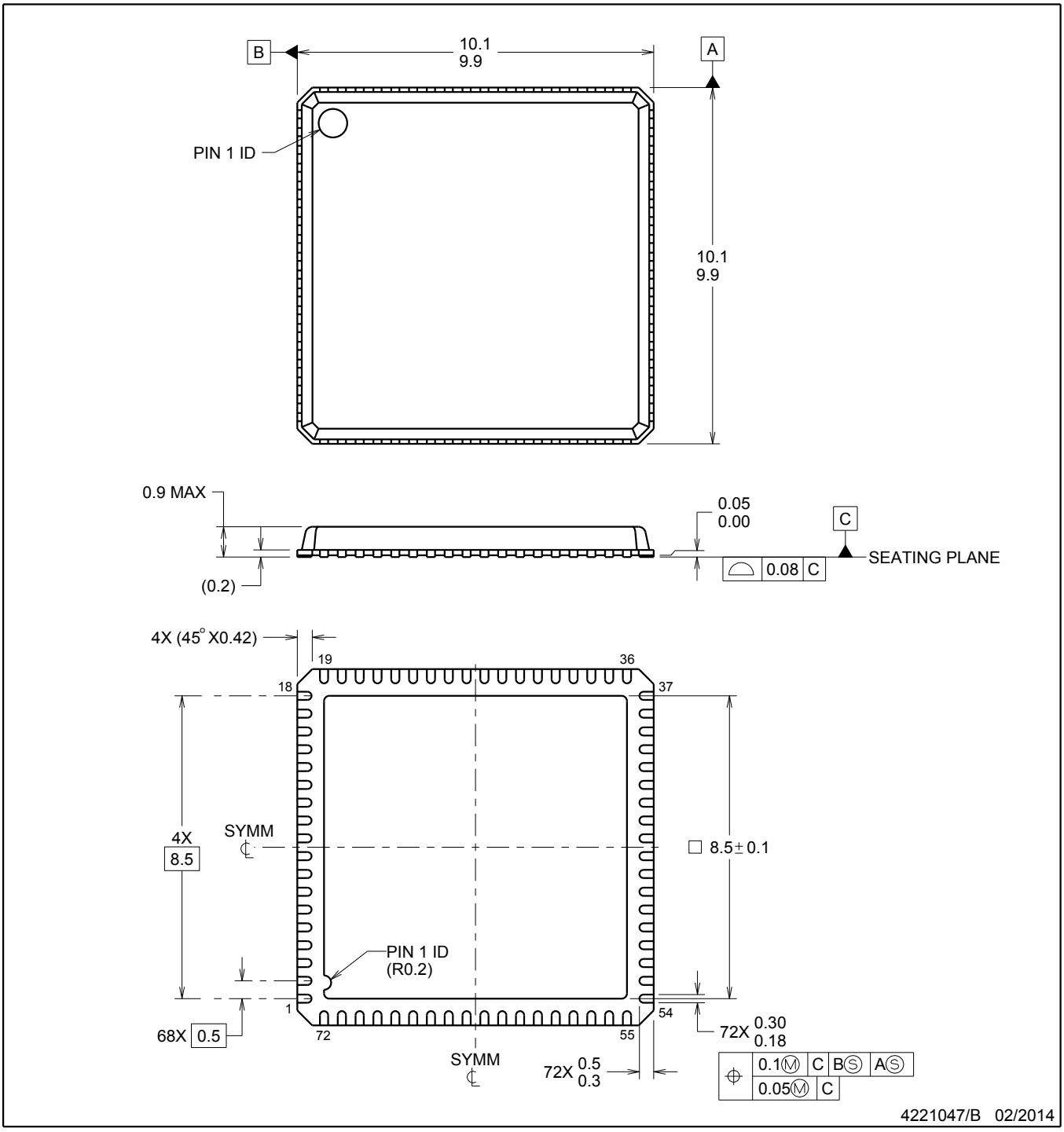
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADS54J60IRMP	RMP	VQFNP	72	168	8 X 21	150	315	135.9	7620	14.65	11	11.95

PACKAGE OUTLINE

RMP0072A

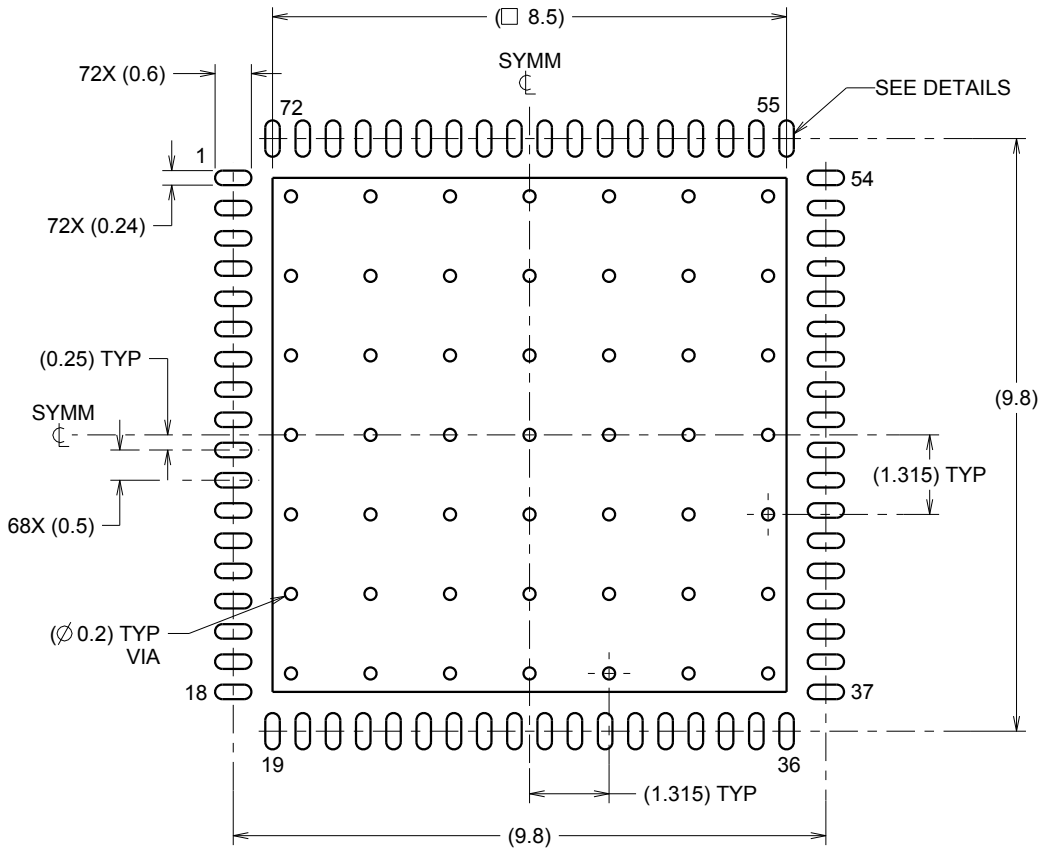
VQFN - 0.9 mm max height

VQFN

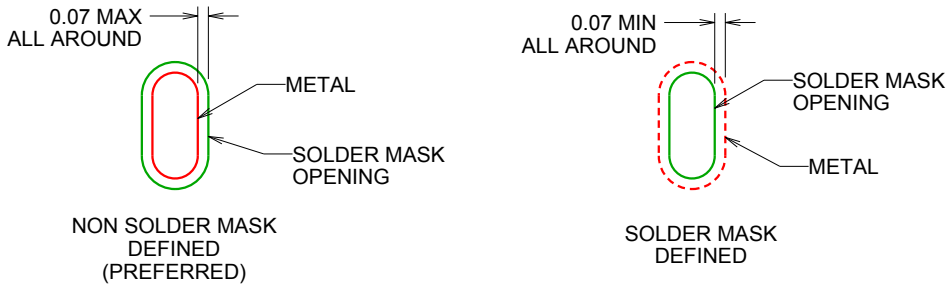


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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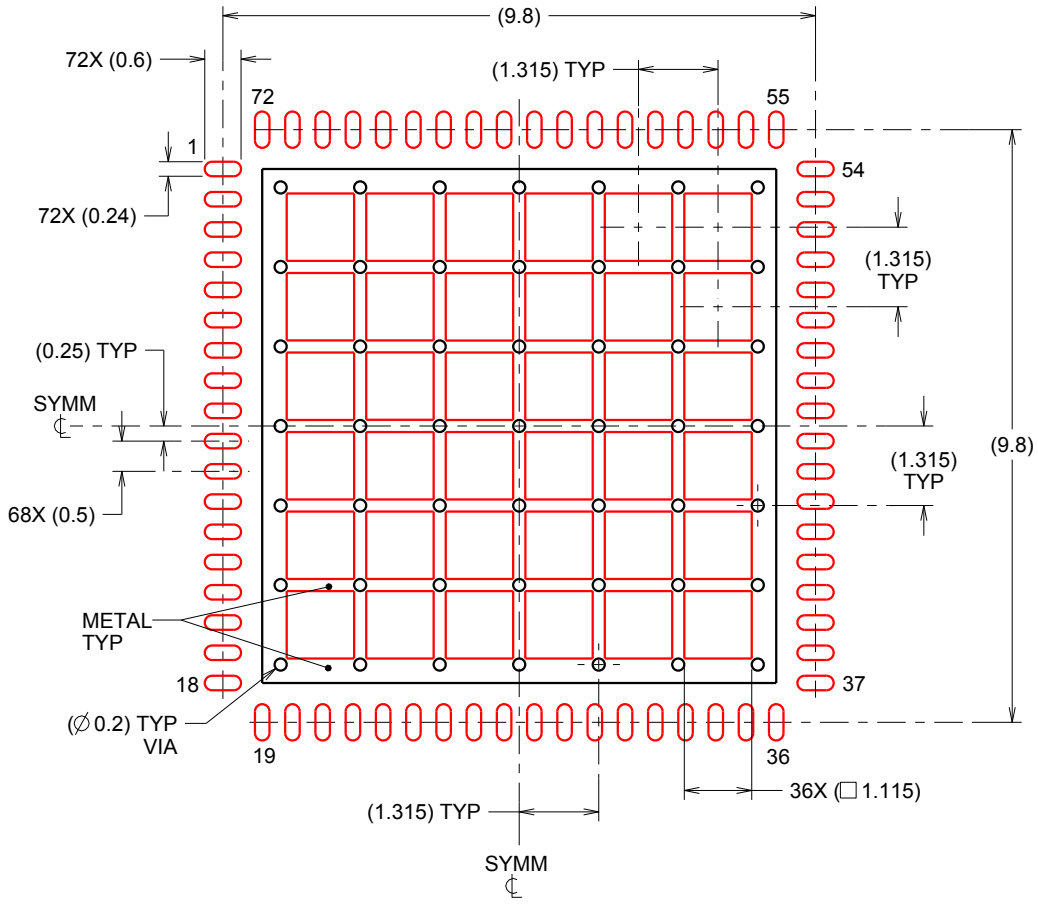
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
62% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

4221047/B 02/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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