# 用于汽车的 UCC21520-Q1、UCC21520A-Q1 4A、6A、5.7kV$_{RMS}$ 隔离式双通道栅极驱动器

## 1 特性

- 符合汽车应用 要求
- 具有符合 AEC-Q100 标准的下列结果
  - 器件温度 1 级
  - 器件 HBM ESD 分类等级 H2
  - 器件 CDM ESD 分类等级 C6
- 通用：双路低侧、双路高侧或半桥驱动器
- 工作温度范围：–40 至 +125°C
- 开关参数：
  - 19ns 典型传播延迟
  - 10ns 最小脉冲宽度
  - 5ns 最大延迟匹配度
  - 6ns 最大脉宽失真度
- 共模瞬态抗扰度 (CMTI) 大于 100 V/ns
- 浪涌抗扰度高达 12.8kV
- 隔离栅寿命 > 40 年
- 4A 峰值拉电流，6A 峰值灌电流输出
- TTL 和 CMOS 兼容输入
- 3V 至 18V 输入 VCCI 范围，可连接数字和模拟控制器
- 高达 25V 的 VDD 输出驱动电源
  - 5V 和 8V VDD UVLO 选项
- 可通过编程的重叠和死区时间
- 抑制短于 5ns 的输入脉冲和噪声瞬态
- 可针对电源排序快速禁用
- 安全相关认证：
  - 8000V$_{PK}$ 增强型隔离，符合 DIN V VDE V 0884-11:2017-01 标准
  - 符合 UL 1577 标准且长达 1 分钟的 5.7kV$_{RMS}$ 隔离
  - 获得 CSA 认证，符合 IEC 60950-1、IEC 62368-1、IEC 61010-1 和 IEC 60601-1 终端设备标准
  - 获得 GB4943.1-2011 CQC 认证

## 2 应用

- HEV 和 BEV 电池充电器
- 直流/直流和交流/直流电源中的隔离式转换器
- 电机驱动和直流-交流太阳能逆变器
- 不间断电源 (UPS)

## 3 说明

UCC21520-Q1 是隔离式双通道栅极驱动器，具有 4A 峰值拉电流和 6A 峰值灌电流。该器件设计用于驱动高达 5MHz 的功率 MOSFET、IGBT 和 SiC MOSFET，具有一流的传播延迟和脉宽失真度。

输入侧通过一个 5.7kV$_{RMS}$ 增强型隔离层与两个输出驱动器隔离，共模瞬态抗扰度 (CMTI) 的最小值为 100V/ns。两个二次侧驱动器之间采用内部功能隔离，支持高达 1500 V$_{DC}$ 的工作电压。

每个驱动器可配置为两个低侧驱动器、两个高侧驱动器或一个死区时间 (DT) 可编程的半桥驱动器。禁用引脚可同时关断两个输出，在保持开路或接地时允许器件正常运行。作为一种失效防护机制，初级侧逻辑故障会强制两个输出为低电平。

每个器件接受高达 25V 的 VDD 电源电压。凭借 3V 至 18V 的宽输入电压 VCCI 范围，该驱动器非常适合连接模拟和数字控制器。所有电源电压引脚都具有欠压锁定 (UVLO) 保护功能。

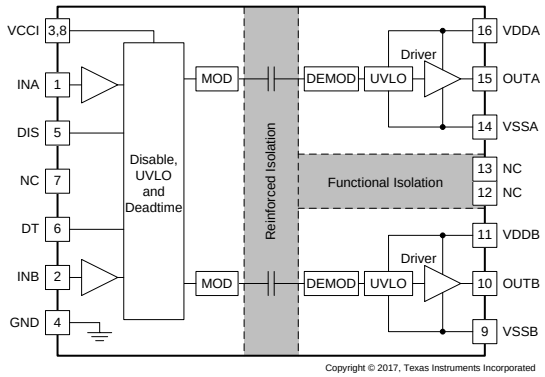
凭借上述所有高级 功能，UCC21520-Q1 可以实现高效率、高功率密度和稳健性。

器件比较(1)

| 器件编号 | 封装 | UVLO 级别 |
|---|---|---|
| UCC21520-Q1 | DW SOIC (16) | 8V |
| UCC21520A-Q1 | DW SOIC (16) | 5V |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

功能方框图



# 目录



## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

**Changes from Revision A (May 2018) to Revision B** **Page**

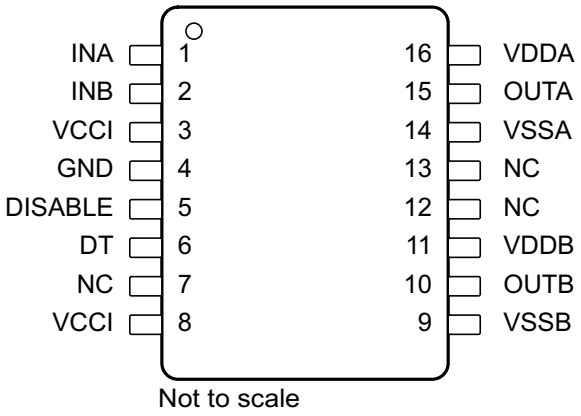
- 已更改 将 UCC21520A-Q1“预告信息”销售状态更改成了“初始发行版”。 ... 1
- Added detailed description for DISABLE Pin and DT Pin ... 3
- Changed $t_{PWD}$ in the switching characteristic section. ... 9
- 已添加 feature descriptions for UVLO delay to OUTPUT ... 16
- 已添加 bullet "It is recommended..." bullet to the component placement in the Layout Guidelines. ... 38

**Changes from Original (October 2017) to Revision A** **Page**

- 已添加 在该数据表中添加了 UCC21520A-Q1 器件（5V UVLO 选项） ... 1
- 已添加 添加了 UCC21520A-Q1 预告信息。 ... 1
- Changed $t_{PWD}$ in the switching characteristic section. ... 9
- 已添加 typical curves of 5-V UVLO hysteresis and ON-OFF thresholds ... 12

# 5 Pin Configuration and Functions

**DW Package**
**16-Pin SOIC**
**Top View**




Not to scale

**Pin Functions**

| PIN | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| DISABLE | 5 | I | Disables both driver outputs if asserted high, enables if set low or left open. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity. Bypass using a ≈1nF low ESR/ESL capacitor close to DIS pin when connecting to a micro controller with distance. |
| DT | 6 | I | Programmable dead time function.<br>Tying DT to VCCI allows the outputs to overlap. Leaving DT open sets the dead time to <15 ns. Placing a 500-Ω to 500-kΩ resistor (RDT) between DT and GND adjusts dead time according to: DT (in ns) = 10 x $R_{DT}$ (in kΩ). It is recommended to parallel a ceramic capacitor, 2.2 nF or above, close to the DT pin with $R_{DT}$ to achieve better noise immunity. |
| GND | 4 | P | Primary-side ground reference. All signals in the primary side are referenced to this ground. |
| INA | 1 | I | Input signal for A channel. INA input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity. |
| INB | 2 | I | Input signal for B channel. INB input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity. |
| NC | 7 | – | No Internal connection. |
| NC | 12 | – | No internal connection. |
| NC | 13 | – | No internal connection. |
| OUTA | 15 | O | Output of driver A. Connect to the gate of the A channel FET or IGBT. |
| OUTB | 10 | O | Output of driver B. Connect to the gate of the B channel FET or IGBT. |
| VCCI | 3 | P | Primary-side supply voltage. Locally decoupled to GND using a low ESR/ESL capacitor located as close to the device as possible. |
| VCCI | 8 | P | Primary-side supply voltage. This pin is internally shorted to pin 3. |
| VDDA | 16 | P | Secondary-side power for driver A. Locally decoupled to VSSA using a low ESR/ESL capacitor located as close to the device as possible. |
| VDDB | 11 | P | Secondary-side power for driver B. Locally decoupled to VSSB using low ESR/ESL capacitor located as close to the device as possible. |
| VSSA | 14 | P | Ground for secondary-side driver A. Ground reference for secondary side A channel. |
| VSSB | 9 | P | Ground for secondary-side driver B. Ground reference for secondary side B channel. |

(1) P =Power, G= Ground, I= Input, O= Output

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input bias pin supply voltage | VCCI to GND | –0.3 | 20 | V |
| Driver bias supply | VDDA-VSSA, VDDB-VSSB | –0.3 | 30 | V |
| Output signal voltage | OUTA to VSSA, OUTB to VSSB | –0.3 | $V_{VDDA}$+0.3, $V_{VDDB}$+0.3 | V |
| | OUTA to VSSA, OUTB to VSSB, Transient for 200 ns | –2 | $V_{VDDA}$+0.3, $V_{VDDB}$+0.3 | V |
| Input signal voltage | INA, INB, DIS, DT to GND | –0.3 | $V_{VCCI}$+0.3 | V |
| | INA, INB Transient for 50ns | –5 | $V_{VCCI}$+0.3 | V |
| Channel to channel voltage | VSSA-VSSB, VSSB-VSSA | | 1500 | V |
| Junction temperature, $T_J$ (2) | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) To maintain the recommended operating conditions for $T_J$, see the Thermal Information.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | ±4000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | ±1500 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| VCCI | VCCI Input supply voltage | | 3 | 18 | V |
| VDDA, VDDB | Driver output bias supply | UCC21520A-Q1 5-V UVLO version | 6.5 | 25 | V |
| VDDA, VDDB | Driver output bias supply | UCC21520-Q1 8-V UVLO version | 9.2 | 25 | V |
| $T_A$ | Ambient Temperature | | –40 | 125 | °C |
| $T_J$ | Junction Temperature | | –40 | 130 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | UCC21520-Q1 DW-16 (SOIC) | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 67.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 34.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 32.1 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 18.0 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 31.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Power Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $P_D$ | Power dissipation by UCC21520-Q1 | VCCI = 18 V, VDDA/B = 12 V, INA/B = 3.3 V, 3 MHz 50% duty cycle square wave 1-nF load | 1.05 | W |
| $P_{DI}$ | Power dissipation by transmitter side of UCC21520-Q1 | | 0.05 | W |
| $P_{DA}$, $P_{DB}$ | Power dissipation by each driver side of UCC21520-Q1 | | 0.5 | W |

## 6.6 Insulation Specifications

| PARAMETER | | TEST CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| CLR | External clearance(1) | Shortest pin-to-pin distance through air | > 8 | mm |
| CPG | External creepage(1) | Shortest pin-to-pin distance across the package surface | > 8 | mm |
| DTI | Distance through insulation | Minimum internal gap (internal clearance) of the double insulation (2 × 10.5 µm) | >21 | µm |
| CTI | Comparative tracking index | DIN EN 60112 (VDE 0303-11); IEC 60112 | > 600 | V |
| | Material group | According to IEC 60664-1 | I | |
| | Overvoltage category per IEC 60664-1 | Rated mains voltage ≤ 600 $V_{RMS}$ | I-IV | |
| | | Rated mains voltage ≤ 1000 $V_{RMS}$ | I-III | |
| **DIN V VDE V 0884-11 (VDE V 0884-11): 2017-01(2)** | | | | |
| $V_{IORM}$ | Maximum repetitive peak isolation voltage | AC voltage (bipolar) | 2121 | $V_{PK}$ |
| $V_{IOWM}$ | Maximum working isolation voltage | AC voltage (sine wave); time dependent dielectric breakdown (TDDB), test (See 图 1) | 1500 | $V_{RMS}$ |
| | | DC voltage | 2121 | $V_{DC}$ |
| $V_{IOTM}$ | Maximum transient isolation voltage | $V_{TEST} = V_{IOTM}$, t = 60 sec (qualification)<br>$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production) | 8000 | $V_{PK}$ |
| $V_{IOSM}$ | Maximum surge isolation voltage(3) | Test method per IEC 62368-1, 1.2/50 µs waveform,<br>$V_{TEST} = 1.6 \times V_{IOSM} = 12800\ V_{PK}$ (qualification) | 8000 | $V_{PK}$ |
| $q_{pd}$ | Apparent charge(4) | Method a, After Input/Output safety test subgroup 2/3.<br>$V_{ini} = V_{IOTM}$, $t_{ini}$ = 60s;<br>$V_{pd(m)} = 1.2\ X\ V_{IORM} = 2545\ V_{PK}$, $t_m$ = 10s | <5 | pC |
| | | Method a, After environmental tests subgroup 1.<br>$V_{ini} = V_{IOTM}$, $t_{ini}$ = 60s;<br>$V_{pd(m)} = 1.6\ X\ V_{IORM} = 3394\ V_{PK}$, $t_m$ = 10s | <5 | |
| | | Method b1; At routine test (100% production) and preconditioning (type test)<br>$V_{ini} = 1.2 \times V_{IOTM}$; $t_{ini}$ = 1s;<br>$V_{pd(m)} = 1.875 * V_{IORM} = 3977\ V_{PK}$ , $t_m$ = 1s | <5 | |
| $C_{IO}$ | Barrier capacitance, input to output(5) | $V_{IO}$ = 0.4 sin (2πft), f =1 MHz | 1.2 | pF |
| $R_{IO}$ | Isolation resistance, input to output(5) | $V_{IO}$ = 500 V at $T_A$ = 25°C | $> 10^{12}$ | Ω |
| | | $V_{IO}$ = 500 V at 100°C ≤ $T_A$ ≤ 125°C | $> 10^{11}$ | |
| | | $V_{IO}$ = 500 V at $T_S$ =150°C | $> 10^{9}$ | |
| | Pollution degree | | 2 | |
| | Climatic category | | 40/125/21 | |
| **UL 1577** | | | | |
| $V_{ISO}$ | Withstand isolation voltage | $V_{TEST} = V_{ISO}$ = 5700 $V_{RMS}$, t = 60 sec. (qualification),<br>$V_{TEST} = 1.2 \times V_{ISO}$ = 6840$V_{RMS}$, t = 1 sec (100% production) | 5700 | $V_{RMS}$ |

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

## 6.7 Safety-Related Certifications

| VDE | CSA | UL | CQC |
|---|---|---|---|
| Certified according to DIN V VDE V 0884-11:2017-01, and DIN EN 60950-1 (VDE 0805 Teil 1):2014-08 | Certified according to IEC 60950-1, IEC 62368-1, IEC 61010-1 and IEC 60601-1 | Recognized under UL 1577 Component Recognition Program | Certified according to GB 4943.1-2011 |
| Reinforced Insulation Maximum Transient Isolation voltage, 8000 $V_{PK}$; Maximum Repetitive Peak Isolation Voltage, 2121 $V_{PK}$; Maximum Surge Isolation Voltage, 8000 $V_{PK}$ | Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed.+A1+A2, 800 $V_{RMS}$ maximum working voltage (pollution degree 2, material group I) Reinforced insulation per CSA 62368-1-14 and IEC 62368-1 2nd Ed., 800 $V_{RMS}$ maximum working voltage (pollution degree 2, material group I); Basic insulation per CSA 61010-1-12+A1 and IEC 61010-1 3rd Ed., 600 $V_{RMS}$ maximum working voltage (pollution degree 2, material group III); 2 MOPP (Means of Patient Protection) per CSA 60601- 1:14 and IEC 60601-1 Ed.3+A1, 250 $V_{RMS}$ maximum working voltage | Single protection, 5700 $V_{RMS}$ | Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate 660 $V_{RMS}$ maximum working voltage |
| Certification number: 40040142 | Master contract number : 220991 | File number: E181974 | Certificate number: CQC16001155011 |

## 6.8 Safety-Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

| PARAMETER | | TEST CONDITIONS | SIDE | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_S$ | Safety output supply current | $R_{\theta JA}$ = 67.3ºC/W, VDDA/B = 12 V, $T_A$ = 25°C, $T_J$ = 150°C<br>See 图 2 | DRIVER A, DRIVER B | | | 75 | mA |
| | | $R_{\theta JA}$ = 67.3ºC/W, VDDA/B = 25 V, $T_A$ = 25°C, $T_J$ = 150°C<br>See 图 2 | DRIVER A, DRIVER B | | | 36 | mA |
| $P_S$ | Safety supply power | $R_{\theta JA}$ = 67.3ºC/W, $T_A$ = 25°C, $T_J$ = 150°C<br>See 图 3 | INPUT | | | 50 | mW |
| | | | DRIVER A | | | 900 | |
| | | | DRIVER B | | | 900 | |
| | | | TOTAL | | | 1850 | |
| $T_S$ | Safety temperature(1) | | | | | 150 | °C |

(1) The maximum safety temperature, $T_S$, has the same value as the maximum junction temperature, $T_J$, specified for the device. The $I_S$ and $P_S$ parameters represent the safety current and safety power respectively. The maximum limits of $I_S$ and $P_S$ should not be exceeded. These limits vary with the ambient temperature, $T_A$.

The junction-to-air thermal resistance, $R_{\theta JA}$, in the ***Thermal Information*** table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.

$P_S = I_S \times V_I$, where $V_I$ is the maximum input voltage.

## 6.9 Electrical Characteristics

$V_{VCCI}$ = 3.3 V or 5 V, 0.1-µF capacitor from VCCI to GND, $V_{VDDA}$ = $V_{VDDB}$ = 12 V, 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, $T_A$ = –40°C to +125°C, (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENTS** | | | | | | |
| $I_{VCCI}$ | VCCI quiescent current | $V_{INA}$ = 0 V, $V_{INB}$ = 0 V | | 1.5 | 2.0 | mA |
| $I_{VDDA}$, $I_{VDDB}$ | VDDA and VDDB quiescent current | $V_{INA}$ = 0 V, $V_{INB}$ = 0 V | | 1.0 | 1.8 | mA |
| $I_{VCCI}$ | VCCI operating current | (f = 500 kHz) current per channel, $C_{OUT}$ = 100 pF | | 2.0 | | mA |
| $I_{VDDA}$, $I_{VDDB}$ | VDDA and VDDB operating current | (f = 500 kHz) current per channel, $C_{OUT}$ = 100 pF | | 2.5 | | mA |
| **VCCI UVLO THRESHOLDS** | | | | | | |
| $V_{VCCI\_ON}$ | Rising threshold | | 2.55 | 2.7 | 2.85 | V |
| $V_{VCCI\_OFF}$ | Falling threshold VCCI_OFF | | 2.35 | 2.5 | 2.65 | V |
| $V_{VCCI\_HYS}$ | Threshold hysteresis | | | 0.2 | | V |
| **UCC21520A-Q1 VDD UVLO THRESHOLDS (5-V UVLO Version)** | | | | | | |
| $V_{VDDA\_ON}$, $V_{VDDB\_ON}$ | Rising threshold VDDA_ON, VDDB_ON | | 5.7 | 6.0 | 6.3 | V |
| $V_{VDDA\_OFF}$, $V_{VDDB\_OFF}$ | Falling threshold VDDA_OFF, VDDB_OFF | | 5.4 | 5.7 | 6 | V |
| $V_{VDDA\_HYS}$, $V_{VDDB\_HYS}$ | Threshold hysteresis | | | 0.3 | | V |
| **UCC21520-Q1 VDD UVLO THRESHOLDS (8-V UVLO Version)** | | | | | | |
| $V_{VDDA\_ON}$, $V_{VDDB\_ON}$ | Rising threshold VDDA_ON, VDDB_ON | | 8.3 | 8.7 | 9.2 | V |
| $V_{VDDA\_OFF}$, $V_{VDDB\_OFF}$ | Falling threshold VDDA_OFF, VDDB_OFF | | 7.8 | 8.2 | 8.7 | V |
| $V_{VDDA\_HYS}$, $V_{VDDB\_HYS}$ | Threshold hysteresis | | | 0.5 | | V |
| **INA, INB AND DISABLE** | | | | | | |
| $V_{INAH}$, $V_{INBH}$, $V_{DISH}$ | Input high voltage | | 1.6 | 1.8 | 2 | V |
| $V_{INAL}$, $V_{INBL}$, $V_{DISL}$ | Input low voltage | | 0.8 | 1 | 1.2 | V |
| $V_{INA\_HYS}$, $V_{INB\_HYS}$, $V_{DIS\_HYS}$ | Input hysteresis | | | 0.8 | | V |
| $V_{INA}$, $V_{INB}$ | Negative transient, ref to GND, 50 ns pulse | Not production tested, bench test only | –5 | | | V |

## Electrical Characteristics (continued)

$V_{VCCI}$ = 3.3 V or 5 V, 0.1-µF capacitor from VCCI to GND, $V_{VDDA}$ = $V_{VDDB}$ = 12 V, 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, $T_A$ = –40°C to +125°C, (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | |
| $I_{OA+}$, $I_{OB+}$ | Peak output source current | $C_{VDD}$ = 10 µF, $C_{LOAD}$ = 0.18 µF, f = 1 kHz, bench measurement | | 4 | | A |
| $I_{OA-}$, $I_{OB-}$ | Peak output sink current | $C_{VDD}$ = 10 µF, $C_{LOAD}$ = 0.18 µF, f = 1 kHz, bench measurement | | 6 | | A |
| $R_{OHA}$, $R_{OHB}$ | Output resistance at high state | $I_{OUT}$ = –10 mA, $T_A$ = 25°C, $R_{OHA}$, $R_{OHB}$ do not represent drive pull-up performance. See $t_{RISE}$ in Switching Characteristics and Output Stage for details. | | 5 | | Ω |
| $R_{OLA}$, $R_{OLB}$ | Output resistance at low state | $I_{OUT}$ = 10 mA, $T_A$ = 25°C | | 0.55 | | Ω |
| $V_{OHA}$, $V_{OHB}$ | Output voltage at high state | $V_{VDDA}$, $V_{VDDB}$ = 12 V, $I_{OUT}$ = –10 mA, $T_A$ = 25°C | | 11.95 | | V |
| $V_{OLA}$, $V_{OLB}$ | Output voltage at low state | $V_{VDDA}$, $V_{VDDB}$ = 12 V, $I_{OUT}$ = 10 mA, $T_A$ = 25°C | | 5.5 | | mV |
| **DEADTIME AND OVERLAP PROGRAMMING** | | | | | | |
| Dead time | | Pull DT pin to VCCI | Overlap determined by INA INB | | | - |
| | | DT pin is left open, min spec characterized only, tested for outliers | 0 | 8 | 15 | ns |
| | | $R_{DT}$ = 20 kΩ | 160 | 200 | 240 | ns |

## 6.10 Switching Characteristics

$V_{VCCI}$ = 3.3 V or 5 V, 0.1-µF capacitor from VCCI to GND, $V_{VDDA}$ = $V_{VDDB}$ = 12 V, 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, $T_A$ = –40°C to +125°C, (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{RISE}$ | Output rise time, 20% to 80% measured points | $C_{OUT}$ = 1.8 nF | | 6 | 16 | ns |
| $t_{FALL}$ | Output fall time, 90% to 10% measured points | $C_{OUT}$ = 1.8 nF | | 7 | 12 | ns |
| $t_{PWmin}$ | Minimum pulse width | Output off for less than minimum, $C_{OUT}$ = 0 pF | | | 20 | ns |
| $t_{PDHL}$ | Propagation delay from INx to OUTx falling edges | | | 19 | 30 | ns |
| $t_{PDLH}$ | Propagation delay from INx to OUTx rising edges | | | 19 | 30 | ns |
| $t_{PWD}$ | Pulse width distortion $\lvert t_{PDLH} - t_{PDHL} \rvert$ | | | | 6 | ns |
| $t_{DM}$ | Propagation delays matching between VOUTA, VOUTB | f = 100 kHz | | | 5 | ns |
| $\lvert CM_H \rvert$ | High-level common-mode transient immunity | INA and INB both are tied to VCCI; $V_{CM}$=1500V; (See CMTI Testing) | 100 | | | V/ns |
| $\lvert CM_L \rvert$ | Low-level common-mode transient immunity | INA and INB both are tied to GND; $V_{CM}$=1500V; (See CMTI Testing) | 100 | | | |

## 6.11 Insulation Characteristics Curves

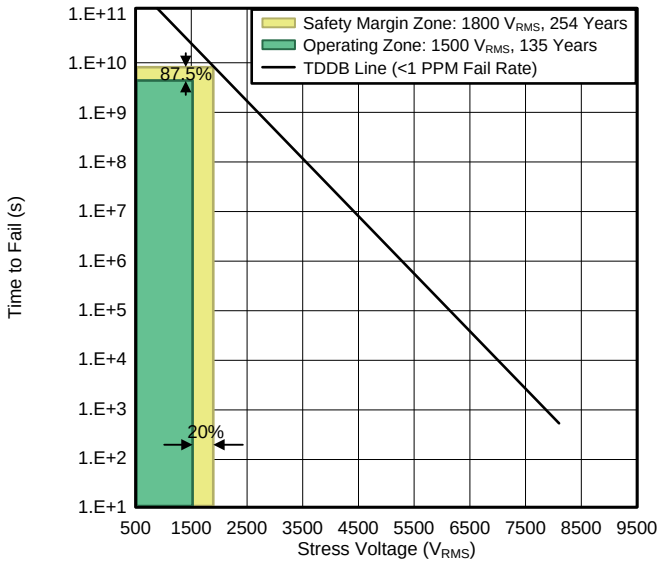



**图 1. Reinforced Isolation Capacitor Life Time Projection**

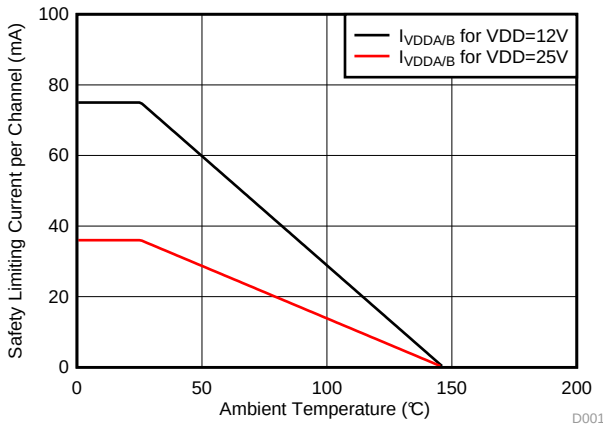



**图 2. Thermal Derating Curve for Safety-Related Limiting Current (Current in Each Channel with Both Channels Running Simultaneously)**

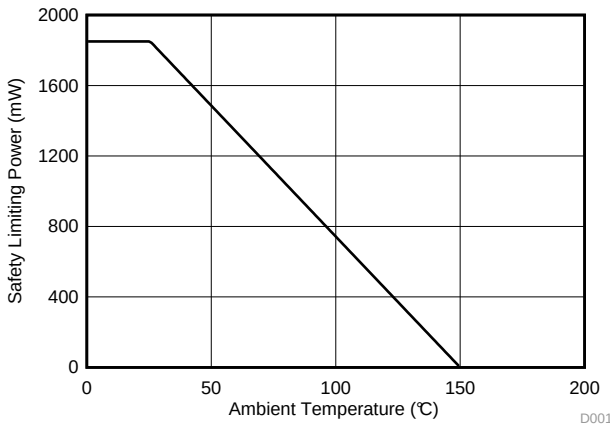



**图 3. Thermal Derating Curve for Safety-Related Limiting Power**

## 6.12 Typical Characteristics

VDDA = VDDB= 12 V, VCCI = 3.3 V, $T_A$ = 25°C, No load unless otherwise noted.

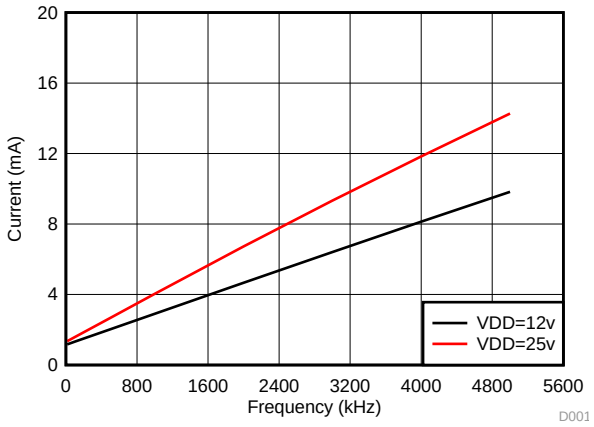



**图 4. Per Channel Current Consumption vs. Frequency (No Load, VDD = 12 V or 25 V)**

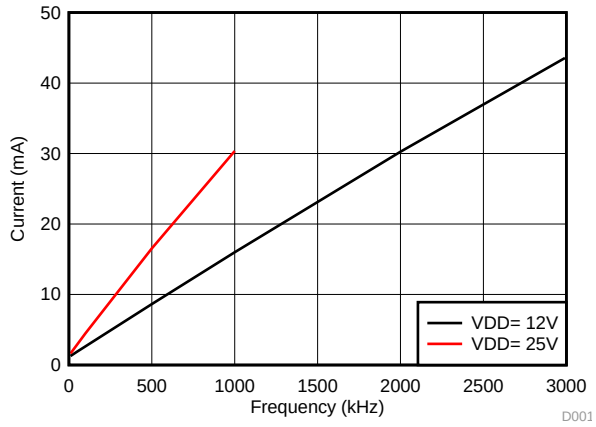



**图 5. Per Channel Current Consumption ($I_{VDDA/B}$) vs. Frequency (1-nF Load, VDD = 12 V or 25 V)**

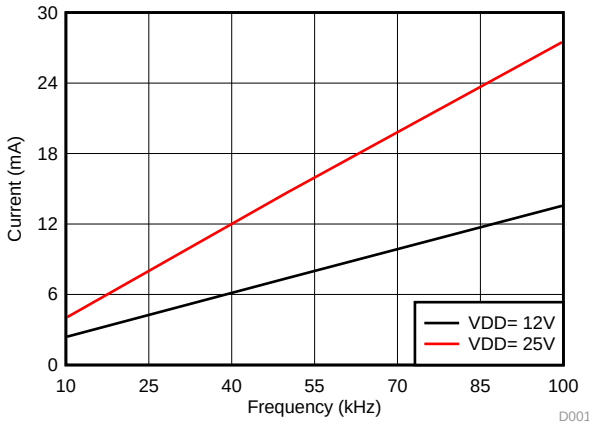



**图 6. Per Channel Current Consumption ($I_{VDDA/B}$) vs. Frequency (10-nF Load, VDD = 12 V or 25 V)**

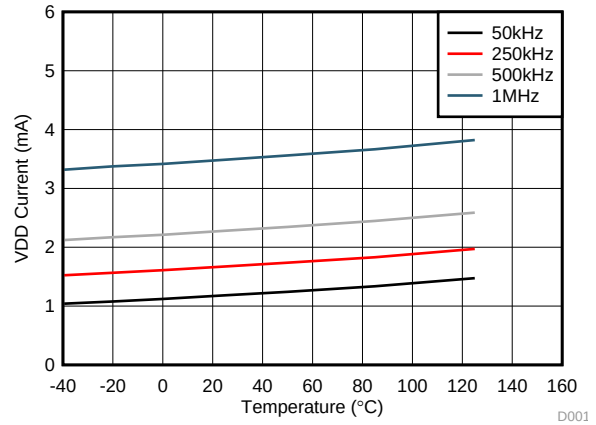



**图 7. Per Channel ($I_{VDDA/B}$) Supply Current Vs. Temperature (No Load, Different Switching Frequencies)**

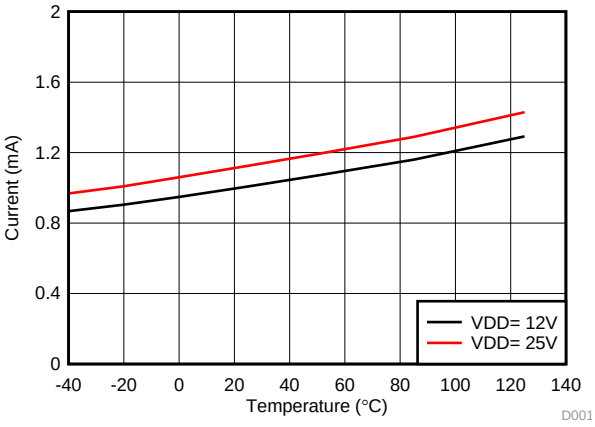



**图 8. Per Channel ($I_{VDDA/B}$) Quiescent Supply Current vs Temperature (No Load, Input Low, No Switching)**

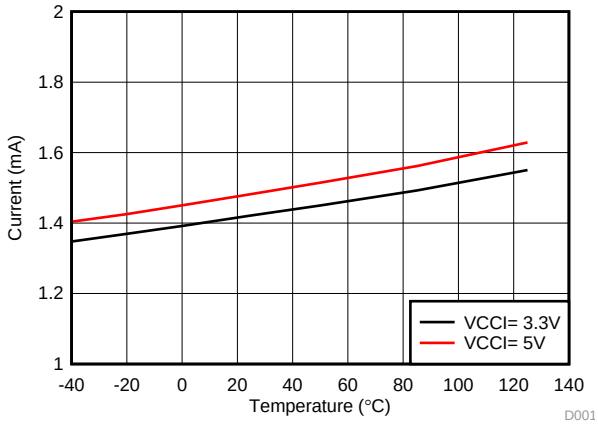



**图 9. $I_{VCCI}$ Quiescent Supply Current vs Temperature (No Load, Input Low, No Switching)**

## Typical Characteristics (接下页)

VDDA = VDDB= 12 V, VCCI = 3.3 V, $T_A$ = 25°C, No load unless otherwise noted.

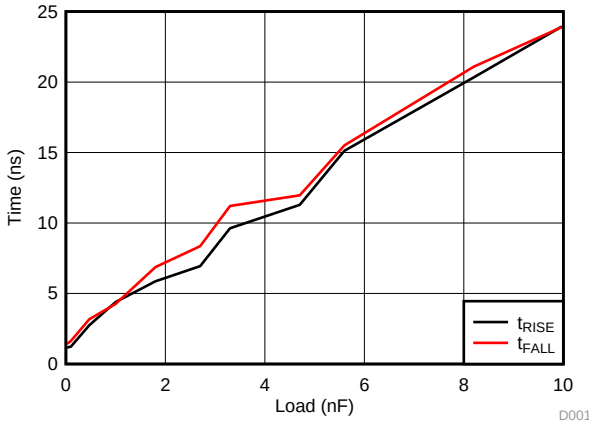



图 10. Rising and Falling Times vs. Load (VDD = 12 V)

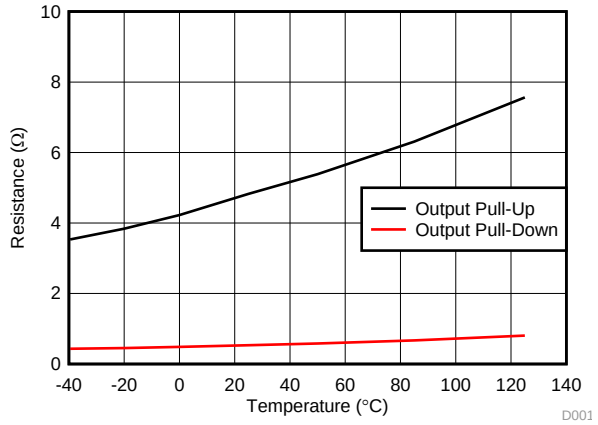



图 11. Output Resistance vs. Temperature

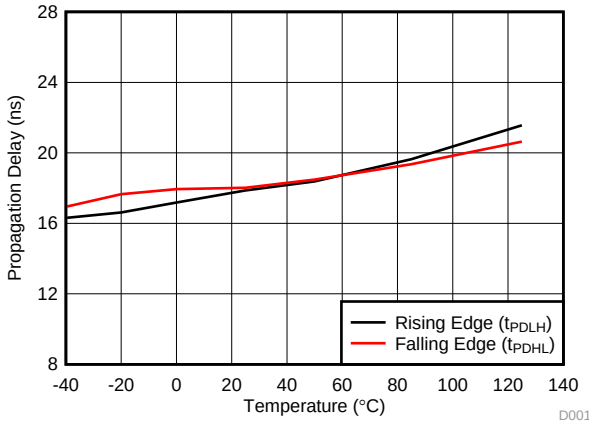



图 12. Propagation Delay vs. Temperature

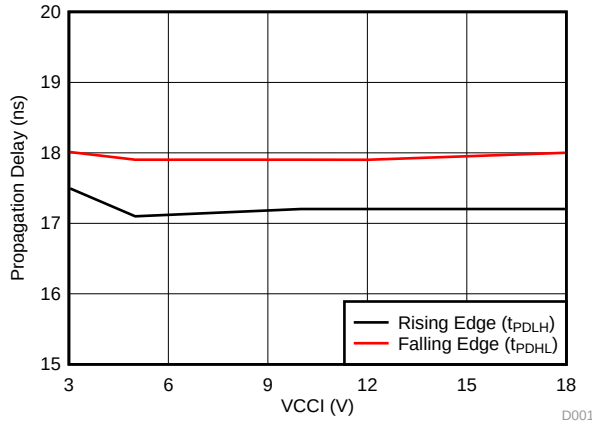



图 13. Propagation Delay vs. VCCI

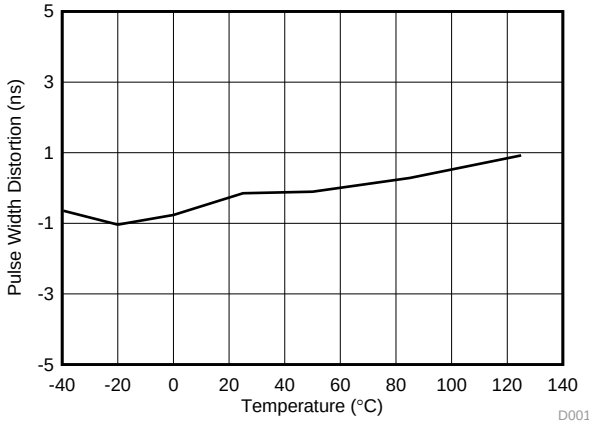



图 14. Pulse Width Distortion vs. Temperature

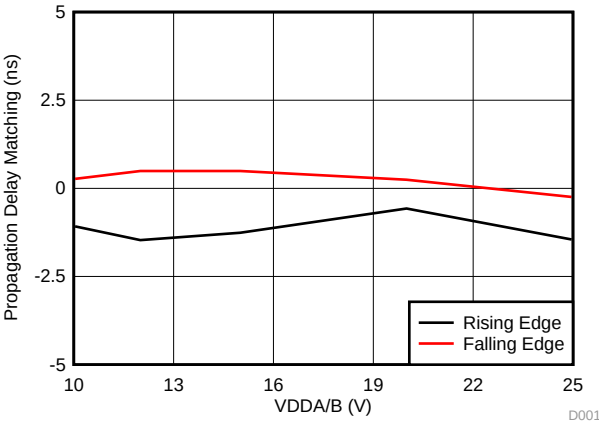



图 15. Propagation Delay Matching ($t_{DM}$) vs. VDD

## Typical Characteristics (接下页)

VDDA = VDDB= 12 V, VCCI = 3.3 V, $T_A$ = 25°C, No load unless otherwise noted.

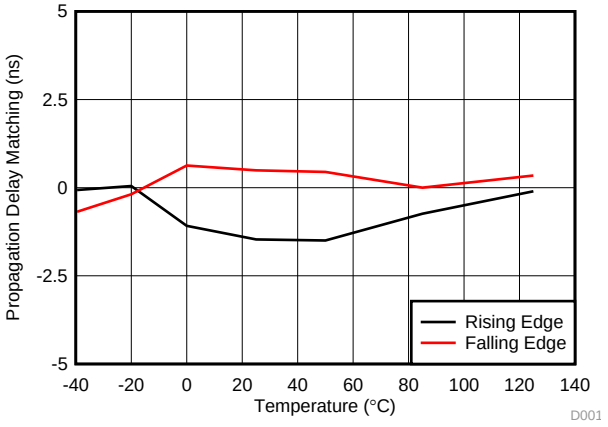



图 16. Propagation Delay Matching ($t_{DM}$) vs. Temperature

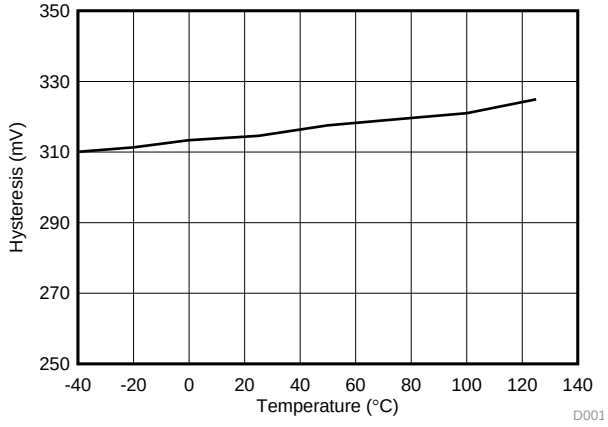



图 17. VDD 5-V UVLO Hysteresis vs. Temperature

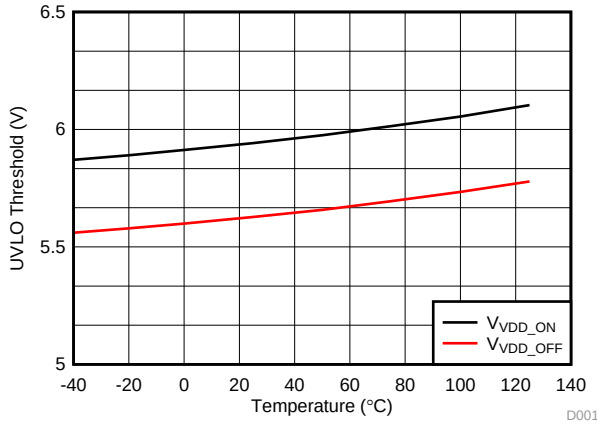



图 18. VDD 5-V UVLO Threshold vs. Temperature

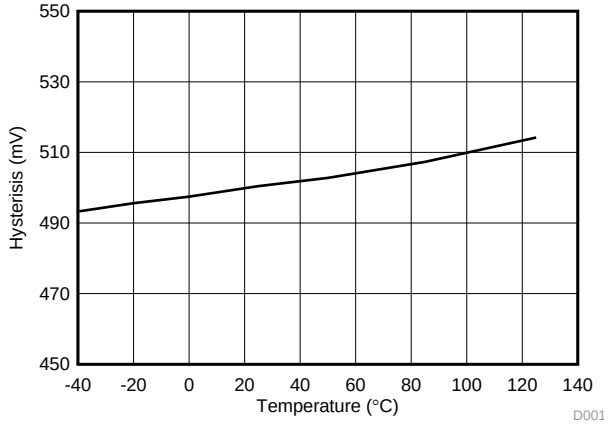



图 19. VDD 8-V UVLO Hysteresis vs. Temperature

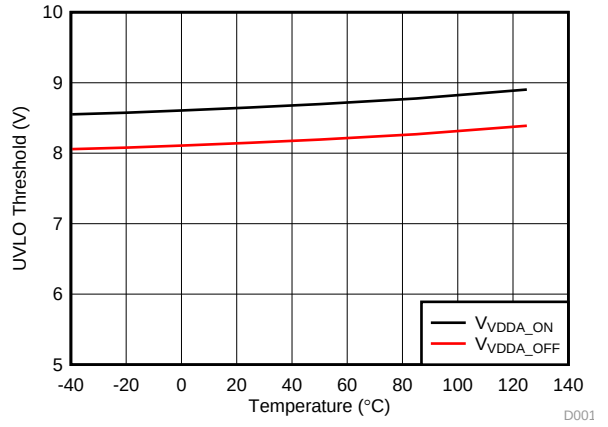



图 20. VDD 8-V UVLO Threshold vs. Temperature

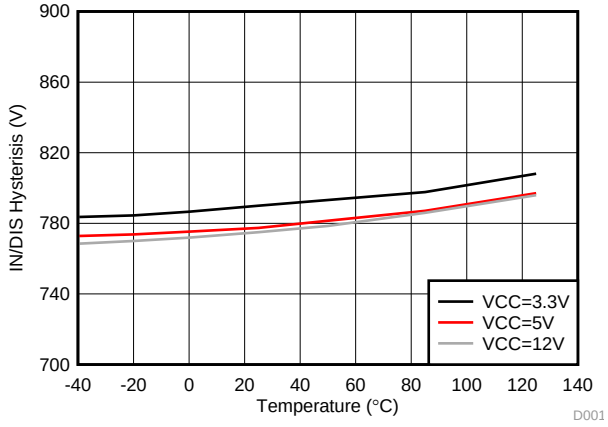



图 21. IN/DIS Hysteresis vs. Temperature

## Typical Characteristics (接下页)

VDDA = VDDB= 12 V, VCCI = 3.3 V, $T_A$ = 25°C, No load unless otherwise noted.

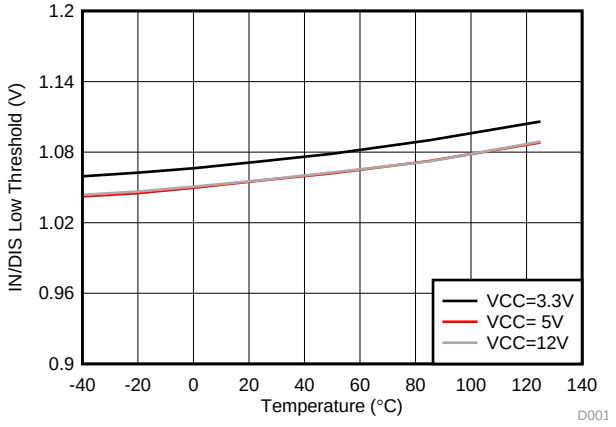



图 22. IN/DIS Low Threshold

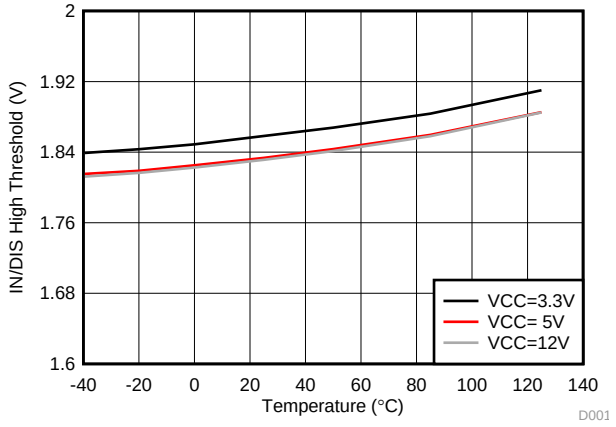



图 23. IN/DIS High Threshold

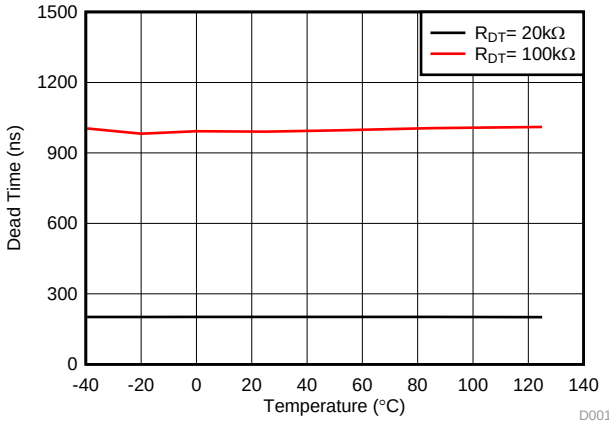



图 24. Dead Time vs. Temperature (with $R_{DT}$ = 20 kΩ and 100 kΩ)

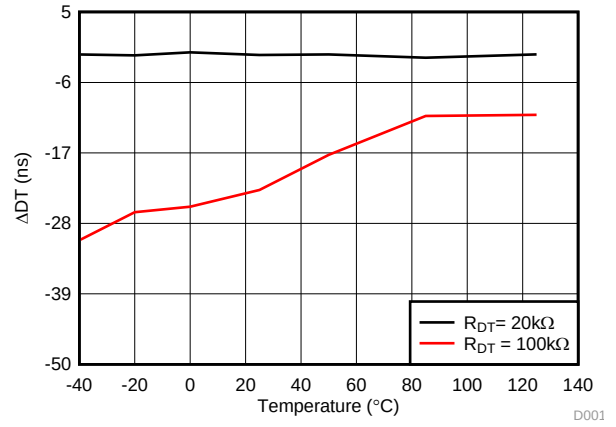



图 25. Dead Time Matching vs. Temperature (with $R_{DT}$ = 20 kΩ and 100 kΩ)

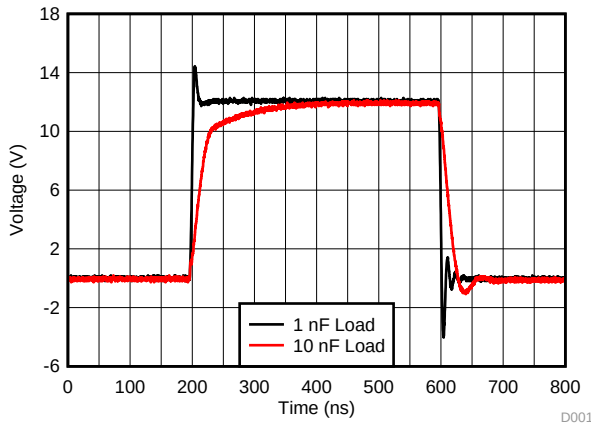



图 26. Typical Output Waveforms

# 7 Parameter Measurement Information

## 7.1 Propagation Delay and Pulse Width Distortion

图 27 shows how one calculates pulse width distortion ($t_{PWD}$) and delay matching ($t_{DM}$) from the propagation delays of channels A and B. It can be measured by ensuring that both inputs are in phase and disabling the dead time function by shorting the DT Pin to VCC.

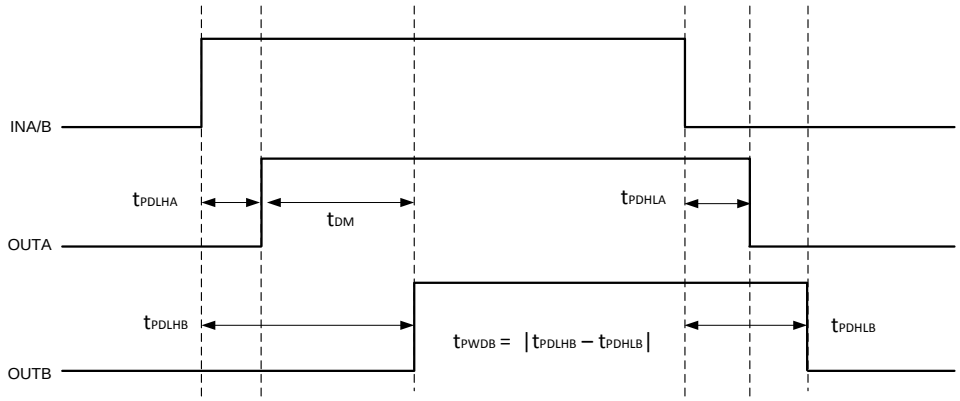



**图 27. Overlapping Inputs, Dead Time Disabled**

## 7.2 Rising and Falling Time

图 28 shows the criteria for measuring rising ($t_{RISE}$) and falling ($t_{FALL}$) times. For more information on how short rising and falling times are achieved see Output Stage

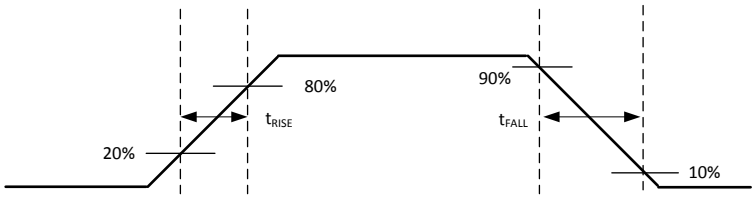



**图 28. Rising and Falling Time Criteria**

## 7.3 Input and Disable Response Time

图 29 shows the response time of the disable function. It is recommended to bypass using a ≈1nF low ESR/ESL capacitor close to DIS pin when connecting DIS pin to a micro controller with distance. For more information, see Disable Pin .

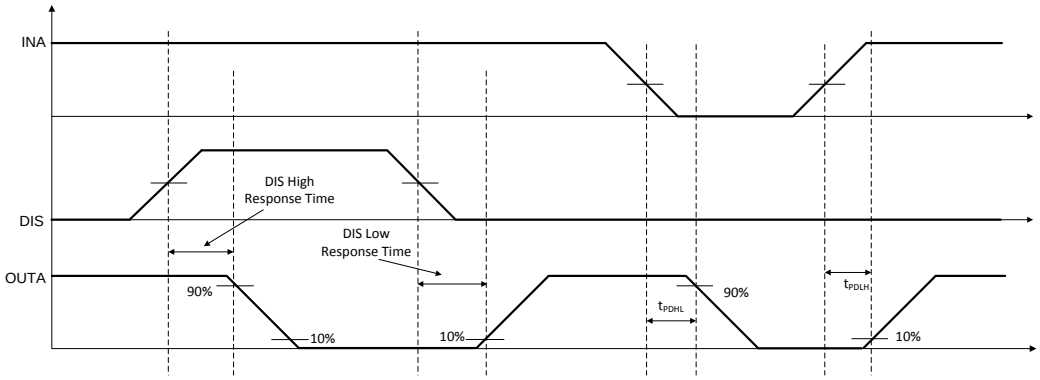



**图 29. Disable Pin Timing**

## 7.4 Programable Dead Time

Leaving the DT pin open or tying it to GND through an appropriate resistor ($R_{DT}$) sets a dead-time interval. For more details on dead time, refer to Programmable Dead Time (DT) Pin.

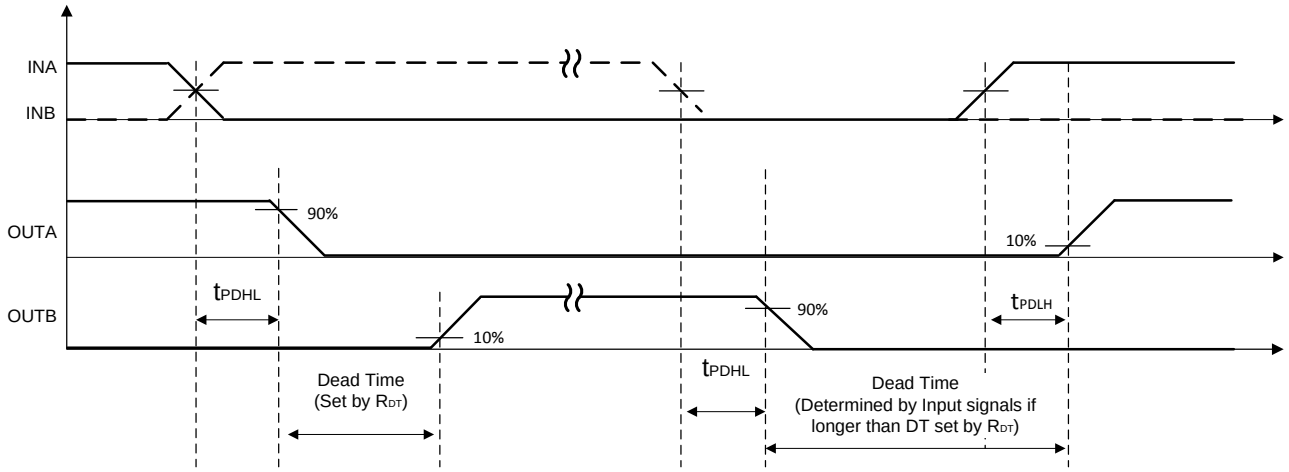



**图 30. Dead-Time Switching Parameters**

## 7.5 Power-up UVLO Delay to OUTPUT

Before the driver is ready to deliver a proper output state, there is a power-up delay from the UVLO rising edge to output and it is defined as $t_{VCCI+\ to\ OUT}$ for VCCI UVLO (typically 40us) and $t_{VDD+\ to\ OUT}$ for VDD UVLO (typically 50us). It is recommended to consider proper margin before launching PWM signal after the driver's VCCI and VDD bias supply is ready. 图 31 and 图 32 show the power-up UVLO delay timing diagram for VCCI and VDD.

If INA or INB are active before VCCI or VDD have crossed above their respective on thresholds, the output will not update until $t_{VCCI+\ to\ OUT}$ or $t_{VDD+\ to\ OUT}$ after VCCI or VDD crossing its UVLO rising threshold. However, when either VCCI or VDD receive a voltage less than their respective off thresholds, there is <1µs delay, depending on the voltage slew rate on the supply pins, before the outputs are held low. This asymmetric delay is designed to ensure safe operation during VCCI or VDD brownouts.

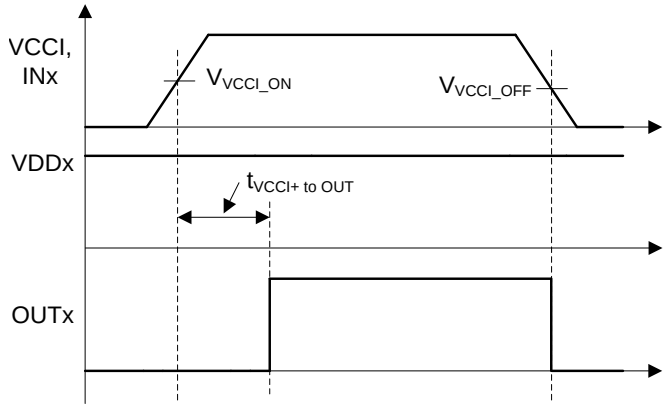



**图 31. VCCI Power-up UVLO Delay**

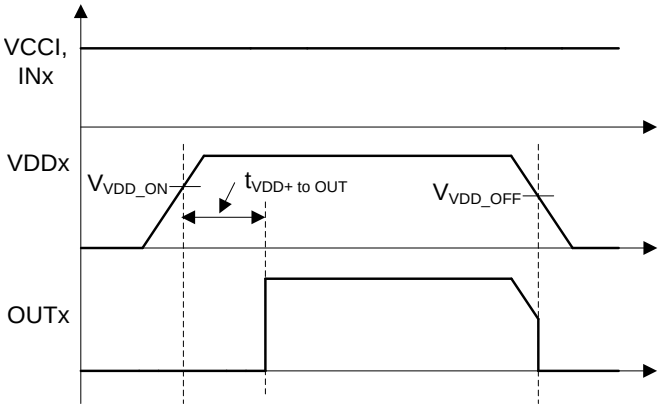



**图 32. VDDA/B Power-up UVLO Delay**

## 7.6 CMTI Testing

图 33 is a simplified diagram of the CMTI testing configuration.

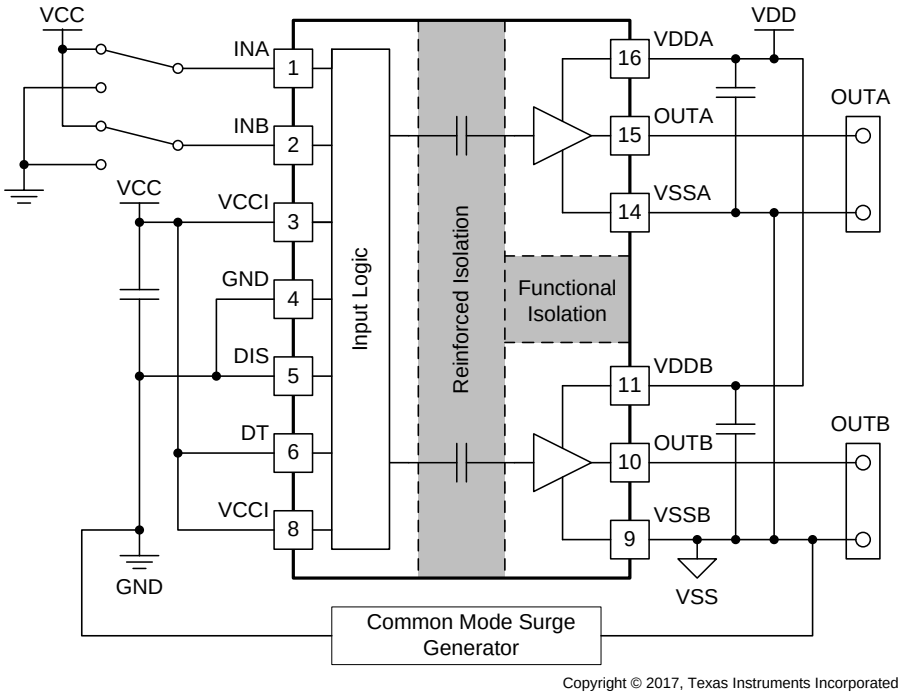



**图 33. Simplified CMTI Testing Setup**

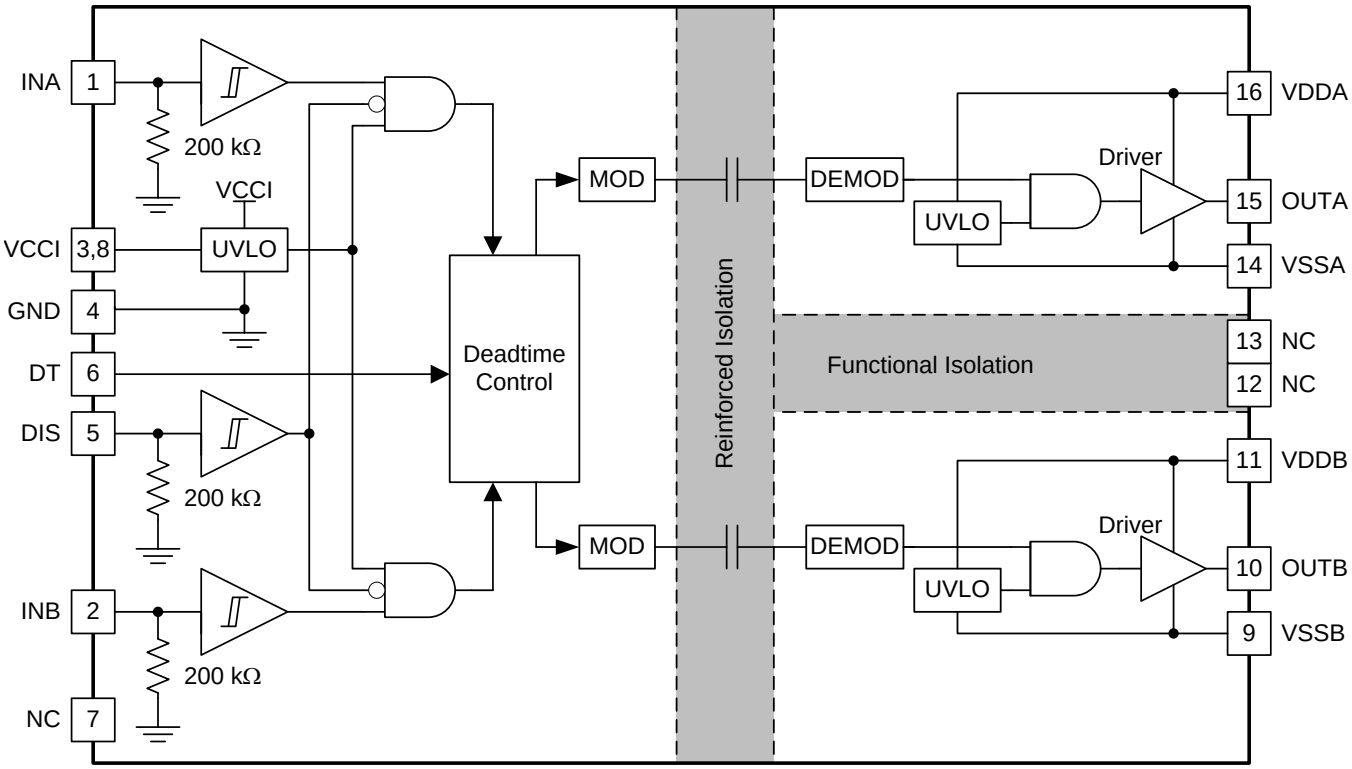
# 8 Detailed Description

## 8.1 Overview

In order to switch power transistors rapidly and reduce switching power losses, high-current gate drivers are often placed between the output of control devices and the gates of power transistors. There are several instances where controllers are not capable of delivering sufficient current to drive the gates of power transistors. This is especially the case with digital controllers, since the input signal from the digital controller is often a 3.3-V logic signal capable of only delivering a few mA.

The UCC21520-Q1 is a flexible dual gate driver which can be configured to fit a variety of power supply and motor drive topologies, as well as drive several types of transistors, including SiC MOSFETs. The UCC21520-Q1 has many features that allow it to integrate well with control circuitry and protect the gates it drives such as: resistor-programmable dead time (DT) control, a DISABLE pin, and under voltage lock out (UVLO) for both input and output voltages. The UCC21520-Q1 also holds its outputs low when the inputs are left open or when the input pulse is not wide enough. The driver inputs are CMOS and TTL compatible for interfacing to digital and analog power controllers alike. Each channel is controlled by its respective input pins (INA and INB), allowing full and independent control of each of the outputs.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 VDD, VCCI, and Under Voltage Lock Out (UVLO)

The UCC21520-Q1 has an internal under voltage lock out (UVLO) protection feature on the supply circuit blocks between the VDD and VSS pins for both outputs. When the VDD bias voltage is lower than $V_{VDD\_ON}$ at device start-up or lower than $V_{VDD\_OFF}$ after start-up, the VDD UVLO feature holds the effected output low, regardless of the status of the input pins (INA and INB).

When the output stages of the driver are in an unbiased or UVLO condition, the driver outputs are held low by an active clamp circuit that limits the voltage rise on the driver outputs (Illustrated in 图 34 ). In this condition, the upper PMOS is resistively held off by $R_{Hi-Z}$ while the lower NMOS gate is tied to the driver output through $R_{CLAMP}$. In this configuration, the output is effectively clamped to the threshold voltage of the lower NMOS device, typically around 1.5 V, when no bias power is available.

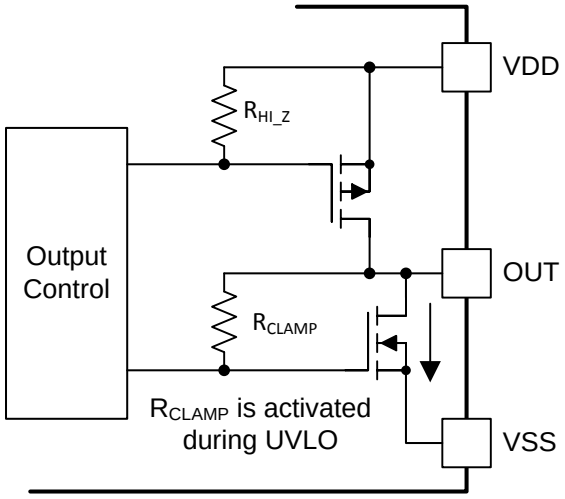



**图 34. Simplified Representation of Active Pull Down Feature**

The VDD UVLO protection has a hysteresis feature ($V_{VDD\_HYS}$). This hysteresis prevents chatter when there is ground noise from the power supply. Also this allows the device to accept small drops in bias voltage, which is bound to happen when the device starts switching and operating current consumption increases suddenly.

The input side of the UCC21520-Q1 also has an internal under voltage lock out (UVLO) protection feature. The device isn't active unless the voltage, VCCI, is going to exceed $V_{VCCI\_ON}$ on start up. And a signal will cease to be delivered when that pin receives a voltage less than $V_{VCCI\_OFF}$. And, just like the UVLO for VDD, there is hystersis ($V_{VCCI\_HYS}$) to ensure stable operation.

## Feature Description (接下页)

All versions of the UCC21520-Q1 can withstand an absolute maximum of 30 V for VDD, and 20 V for VCCI.

**表 1. UCC21520-Q1 VCCI UVLO Feature Logic**

| CONDITION | INPUTS | | OUTPUTS | |
|---|---|---|---|---|
| | INA | INB | OUTA | OUTB |
| VCCI-GND < $V_{VCCI\_ON}$ during device start up | H | L | L | L |
| VCCI-GND < $V_{VCCI\_ON}$ during device start up | L | H | L | L |
| VCCI-GND < $V_{VCCI\_ON}$ during device start up | H | H | L | L |
| VCCI-GND < $V_{VCCI\_ON}$ during device start up | L | L | L | L |
| VCCI-GND < $V_{VCCI\_OFF}$ after device start up | H | L | L | L |
| VCCI-GND < $V_{VCCI\_OFF}$ after device start up | L | H | L | L |
| VCCI-GND < $V_{VCCI\_OFF}$ after device start up | H | H | L | L |
| VCCI-GND < $V_{VCCI\_OFF}$ after device start up | L | L | L | L |

**表 2. UCC21520-Q1 VDD UVLO Feature Logic**

| CONDITION | INPUTS | | OUTPUTS | |
|---|---|---|---|---|
| | INA | INB | OUTA | OUTB |
| VDD-VSS < $V_{VDD\_ON}$ during device start up | H | L | L | L |
| VDD-VSS < $V_{VDD\_ON}$ during device start up | L | H | L | L |
| VDD-VSS < $V_{VDD\_ON}$ during device start up | H | H | L | L |
| VDD-VSS < $V_{VDD\_ON}$ during device start up | L | L | L | L |
| VDD-VSS < $V_{VDD\_OFF}$ after device start up | H | L | L | L |
| VDD-VSS < $V_{VDD\_OFF}$ after device start up | L | H | L | L |
| VDD-VSS < $V_{VDD\_OFF}$ after device start up | H | H | L | L |
| VDD-VSS < $V_{VDD\_OFF}$ after device start up | L | L | L | L |

### 8.3.2 Input and Output Logic Table

Assume VCCI, VDDA, VDDB are powered up. See VDD, VCCI, and Under Voltage Lock Out (UVLO) for more information on UVLO operation modes.

**表 3. INPUT/OUTPUT Logic Table(1)**

| INPUTS | | DISABLE | OUTPUTS | | NOTE |
|---|---|---|---|---|---|
| INA | INB | | OUTA | OUTB | |
| L | L | L or Left Open | L | L | If Dead Time function is used, output transitions occur after the dead time expires. See Programmable Dead Time (DT) Pin |
| L | H | L or Left Open | L | H | |
| H | L | L or Left Open | H | L | |
| H | H | L or Left Open | L | L | DT is left open or programmed with $R_{DT}$ |
| H | H | L or Left Open | H | H | DT pin pulled to VCCI |
| Left Open | Left Open | L or Left Open | L | L | - |
| X | X | H | L | L | - |

(1) "X" means L, H or left open.

### 8.3.3 Input Stage

The input pins (INA, INB, and DIS) of the UCC21520-Q1 are based on a TTL and CMOS compatible input-threshold logic that is totally isolated from the VDD supply voltage. The input pins are easy to drive with logic-level control signals (Such as those from 3.3-V micro-controllers), since the UCC21520-Q1 has a typical high threshold ($V_{INAH}$) of 1.8 V and a typical low threshold of 1 V, which vary little with temperature (see 图 22,图 23). A wide hysterisis ($V_{INA\_HYS}$) of 0.8 V makes for good noise immunity and stable operation. If any of the inputs are ever left open, internal pull-down resistors force the pin low. These resistors are typically 200 kΩ (See Functional Block Diagram). However, it is still recommended to ground an input if it is not being used.

Since the input side of the UCC21520-Q1 is isolated from the output drivers, the input signal amplitude can be larger or smaller than VDD, provided that it doesn't exceed the recommended limit. This allows greater flexibility when integrating with control signal sources, and allows the user to choose the most efficient VDD for their chosen gate. That said, the amplitude of any signal applied to INA or INB must *never* be at a voltage higher than VCCI.

### 8.3.4 Output Stage

The UCC21520-Q1 output stages feature a pull-up structure which delivers the highest peak-source current when it is most needed, during the Miller plateau region of the power-switch turn on transition (when the power switch drain or collector voltage experiences dV/dt). The output stage pull-up structure features a P-channel MOSFET and an additional *Pull-Up* N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a brief boost in the peak-sourcing current, enabling fast turn on. This is accomplished by briefly turning on the N-channel MOSFET during a narrow instant when the output is changing states from low to high. The on-resistance of this N-channel MOSFET ($R_{NMOS}$) is approximately 1.47 Ω when activated.

The $R_{OH}$ parameter is a DC measurement and it is representative of the on-resistance of the P-channel device only. This is because the *Pull-Up* N-channel device is held in the off state in DC condition and is turned on only for a brief instant when the output is changing states from low to high. Therefore the effective resistance of the UCC21520-Q1 pull-up stage during this brief turn-on phase is much lower than what is represented by the $R_{OH}$ parameter. Therefore, the value of $R_{OH}$ belies the fast nature of the UCC21520-Q1's turn-on time.

The pull-down structure in the UCC21520-Q1 is simply composed of an N-channel MOSFET. The $R_{OL}$ parameter, which is also a DC measurement, is representative of the impedance of the pull-down state in the device. Both outputs of the UCC21520-Q1 are capable of delivering 4-A peak source and 6-A peak sink current pulses. The output voltage swings between VDD and VSS provides rail-to-rail operation, thanks to the MOS-out stage which delivers very low drop-out.

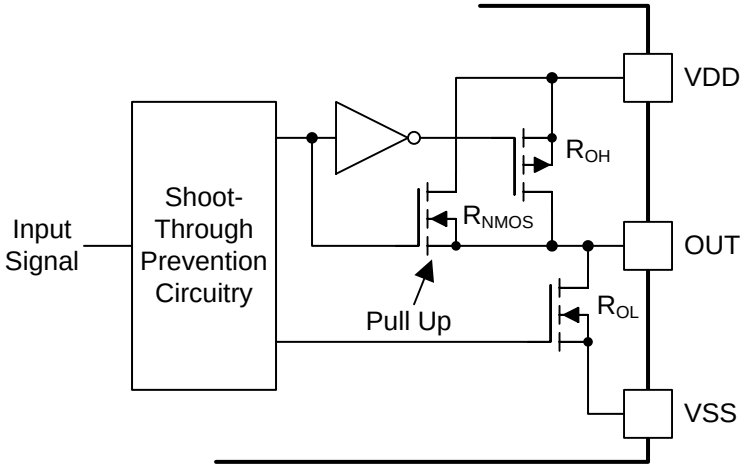



**图 35. Output Stage**

### 8.3.5 Diode Structure in the UCC21520-Q1

图 36 illustrates the multiple diodes involved in the ESD protection components of the UCC21520-Q1. This provides a pictorial representation of the absolute maximum rating for the device.

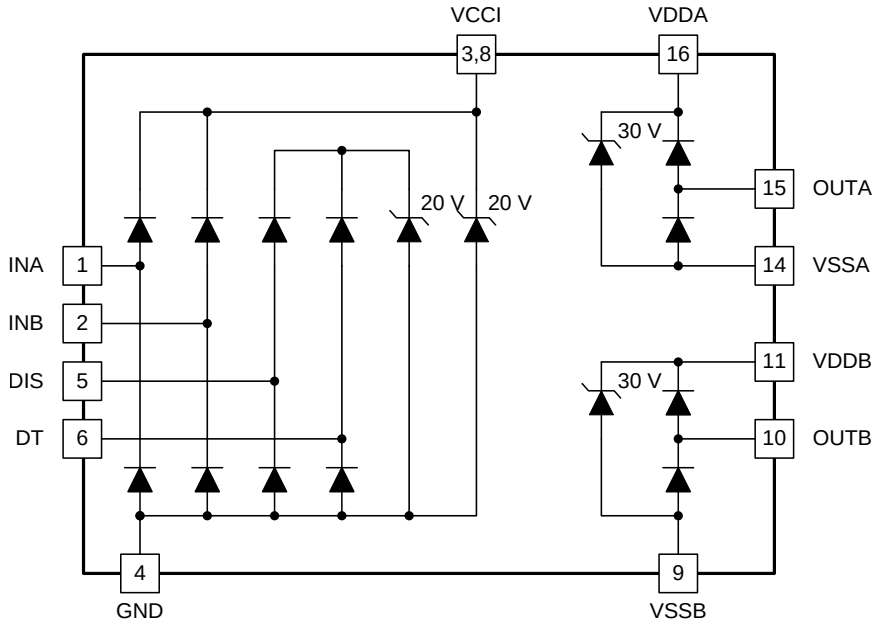



**图 36. ESD Structure**

## 8.4 Device Functional Modes

### 8.4.1 Disable Pin

Setting the DISABLE pin high shuts down both outputs simultaneously. Grounding (or left open) the DISABLE pin allows the UCC21520-Q1 to operate normally. The DISABLE response time is in the range of 20ns and quite responsive , which is as fast as propagation delay. The DISABLE pin is only functional (and necessary) when VCCI stays above the UVLO threshold. It is recommended to tie this pin to ground if the DISABLE pin is not used to achieve better noise immunity, and it is recommended to bypass using a ≈1nF low ESR/ESL capacitor close to DIS pin when connecting DIS pin to a micro controller with distance.

## Device Functional Modes (接下页)

### 8.4.2 Programmable Dead Time (DT) Pin

The UCC21520-Q1 allows the user to adjust dead time (DT) in the following ways:

#### *8.4.2.1 Tying the DT Pin to VCC*

Outputs completely match inputs, so no dead time is asserted. This allows outputs to overlap.

#### *8.4.2.2 DT Pin Left Open or Connected to a Programming Resistor between DT and GND Pins*

If the DT pin is left open, the dead time duration ($t_{DT}$) is set to <15 ns. One can program $t_{DT}$ by placing a resistor, $R_{DT}$, between the DT pin and GND. The appropriate $R_{DT}$ value can be determined from from 公式 1, where $R_{DT}$ is in kΩ and $t_{DT}$ is in ns:

$$t_{DT} \approx 10 \times R_{DT} \quad (1)$$

The steady state voltage at DT pin is around 0.8 V, and the DT pin current will be less than 10uA when $R_{DT}$=100kΩ. Therefore, It is recommended to parallel a ceramic capacitor, 2.2nF or above, close to the chip with $R_{DT}$ to achieve better noise immunity and better deadtime matching between two channels, especially when the dead time is larger than 300ns. The major consideration is that the current through the $R_{DT}$ is used to set the dead time, and this current decreases as $R_{DT}$ increases.

An input signal's falling edge activates the programmed dead time for the other signal. The output signals' dead time is always set to the longer of either the driver's programmed dead time or the input signal's own dead time. If both inputs are high simultaneously, both outputs will immediately be set low. This feature is used to prevent shoot-through, and it doesn't affect the programmed dead time setting for normal operation. Various driver dead time logic operating conditions are illustrated and explained in 图 37:

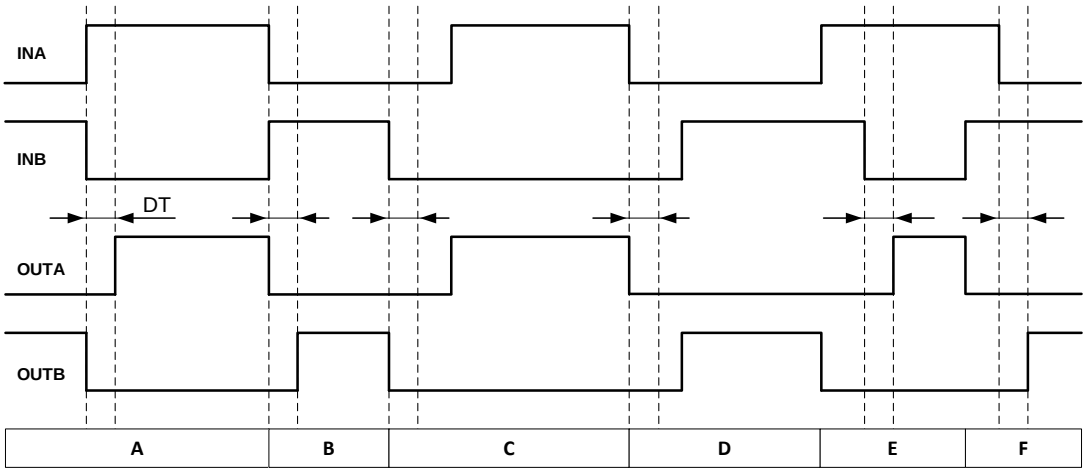



**图 37. Input and Output Logic Relationship With Input Signals**

**Condition A:** INB goes low, INA goes high. INB sets OUTB low immediately and assigns the programmed dead time to OUTA. OUTA is allowed to go high after the programmed dead time.

**Condition B:** INB goes high, INA goes low. Now INA sets OUTA low immediately and assigns the programmed dead time to OUTB. OUTB is allowed to go high after the programmed dead time.

**Condition C:** INB goes low, INA is still low. INB sets OUTB low immediately and assigns the programmed dead time for OUTA. In this case, the input signal's *own* dead time is longer than the programmed dead time. Thus, when INA goes high, it immediately sets OUTA high.

**Condition D:** INA goes low, INB is still low. INA sets OUTA low immediately and assigns the programmed dead time to OUTB. INB's *own* dead time is longer than the programmed dead time. Thus, when INB goes high, it immediately sets OUTB high.

## Device Functional Modes (接下页)

**Condition E:** INA goes high, while INB and OUTB are still high. To avoid overshoot, INA immediately pulls OUTB low and keeps OUTA low. After some time OUTB goes low and assigns the programmed dead time to OUTA. OUTB is already low. After the programmed dead time, OUTA is allowed to go high.

**Condition F:** INB goes high, while INA and OUTA are still high. To avoid overshoot, INB immediately pulls OUTA low and keeps OUTB low. After some time OUTA goes low and assigns the programmed dead time to OUTB. OUTA is already low. After the programmed dead time, OUTB is allowed to go high.

# 9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The UCC21520-Q1 effectively combines both isolation and buffer-drive functions. The flexible, universal capability of the UCC21520-Q1 (with up to 18-V VCCI and 25-V VDDA/VDDB) allows the device to be used as a low-side, high-side, high-side/low-side or half-bridge driver for MOSFETs, IGBTs or SiC MOSFETs. With integrated components, advanced protection features (UVLO, dead time, and disable) and optimized switching performance; the UCC21520-Q1 enables designers to build smaller, more robust designs for enterprise, telecom, automotive, and industrial applications with a faster time to market.

## 9.2 Typical Application

The circuit in 图 38 shows a reference design with the UCC21520-Q1 driving a typical half-bridge configuration which could be used in several popular power converter topologies such as synchronous buck, synchronous boost, half-bridge/full bridge isolated topologies, and 3-phase motor drive applications.

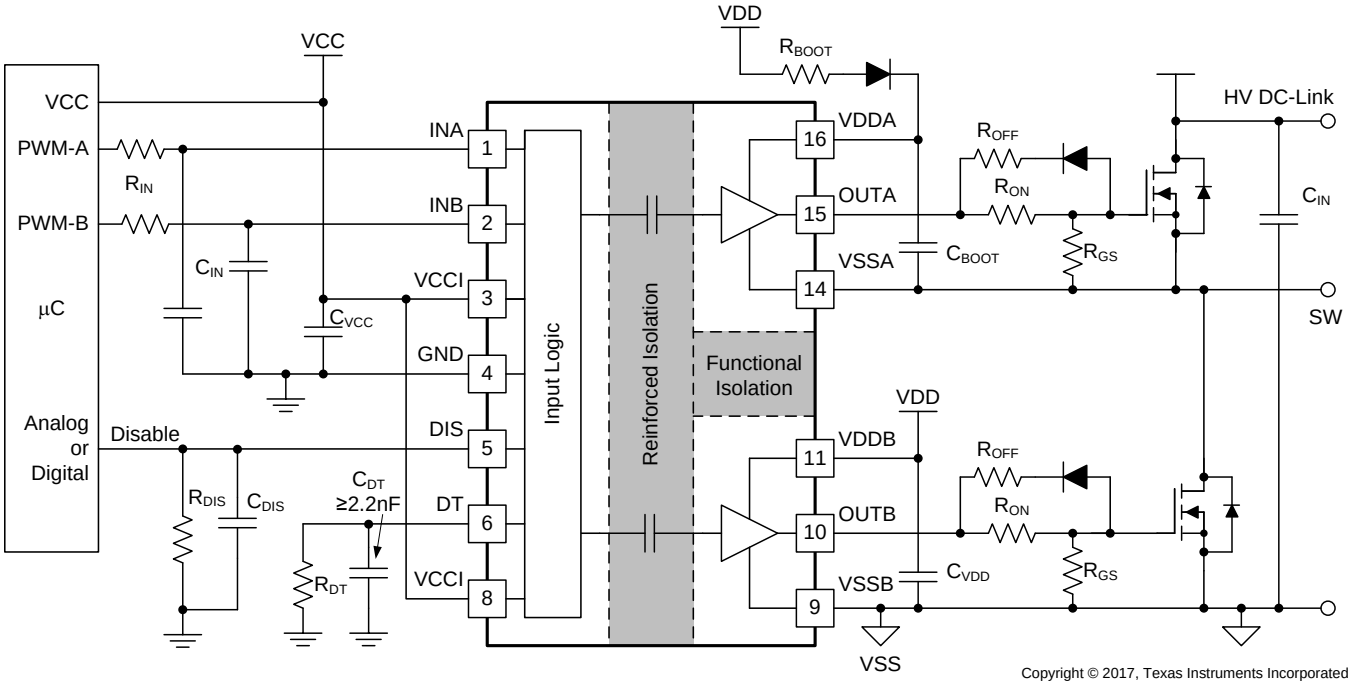



图 38. Typical Application Schematic

## Typical Application (接下页)

### 9.2.1 Design Requirements

表 4 lists reference design parameters for the example application: UCC21520-Q1 driving 1200-V SiC-MOSFETs in a high side-low side configuration.

**表 4. UCC21520-Q1 Design Requirements**

| PARAMETER | VALUE | UNITS |
|---|---|---|
| Power transistor | C2M0080120D | - |
| VCC | 5.0 | V |
| VDD | 20 | V |
| Input signal amplitude | 3.3 | V |
| Switching frequency ($f_s$) | 100 | kHz |
| DC link voltage | 800 | V |

### 9.2.2 Detailed Design Procedure

#### *9.2.2.1 Designing INA/INB Input Filter*

It is recommended that users avoid shaping the signals to the gate driver in an attempt to slow down (or delay) the signal at the output. However, a small input $R_{IN}$-$C_{IN}$ filter can be used to filter out the ringing introduced by non-ideal layout or long PCB traces.

Such a filter should use an $R_{IN}$ in the range of 0 Ω to100 Ω and a $C_{IN}$ between 10 pF and 100 pF. In the example, an $R_{IN}$ = 51 Ω and a $C_{IN}$ = 33 pF are selected, with a corner frequency of approximately 100 MHz.

When selecting these components, it is important to pay attention to the trade-off between good noise immunity and propagation delay.

#### *9.2.2.2 Select External Bootstrap Diode and its Series Resistor*

The bootstrap capacitor is charged by VDD through an external bootstrap diode every cycle when the low side transistor turns on. Charging the capacitor involves high-peak currents, and therefore transient power dissipation in the bootstrap diode may be significant. Conduction loss also depends on the diode's forward voltage drop. Both the diode conduction losses and reverse recovery losses contribute to the total losses in the gate driver circuit.

When selecting external bootstrap diodes, it is recommended that one chose high voltage, fast recovery diodes or SiC Schottky diodes with a low forward voltage drop and low junction capacitance in order to minimize the loss introduced by reverse recovery and related grounding noise bouncing. In the example, the DC-link voltage is 800 $V_{DC}$. The voltage rating of the bootstrap diode should be higher than the DC-link voltage with a good margin. Therefore, a 1200-V SiC diode, C4D02120E, is chosen in this example.

A bootstrap resistor, $R_{BOOT}$, is used to reduce the inrush current in $D_{BOOT}$ and limit the ramp up slew rate of voltage of VDDA-VSSA during each switching cycle, especially when the VSSA(SW) pin has an excessive negative transient voltage. The recommended value for $R_{BOOT}$ is between 1 Ω and 20 Ω depending on the diode used. In the example, a current limiting resistor of 2.2 Ω is selected to limit the inrush current of bootstrap diode. The estimated worst case peak current through $D_{Boot}$ is,

$$I_{DBoot(pk)} = \frac{V_{DD} - V_{BDF}}{R_{Boot}} = \frac{20V - 2.5V}{2.2\Omega} \approx 8A \quad (2)$$

where

- $V_{BDF}$ is the estimated bootstrap diode forward voltage drop at 8 A.

#### 9.2.2.3 Gate Driver Output Resistor

The external gate driver resistors, $R_{ON}/R_{OFF}$, are used to:

1. Limit ringing caused by parasitic inductances/capacitances.
2. Limit ringing caused by high voltage/current switching dv/dt, di/dt, and body-diode reverse recovery.
3. Fine-tune gate drive strength, i.e. peak sink and source current to optimize the switching loss.
4. Reduce electromagnetic interference (EMI).

As mentioned in *Output Stage*, the UCC21520-Q1 has a pull-up structure with a P-channel MOSFET and an additional *pull-up* N-channel MOSFET in parallel. The combined peak source current is 4 A. Therefore, the peak source current can be predicted with:

$$I_{OA+} = \min\left(4A, \frac{V_{DD} - V_{BDF}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}}\right)$$
$$I_{OB+} = \min\left(4A, \frac{V_{DD}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}}\right) \quad (3)$$

where

- $R_{ON}$: External turn-on resistance.
- $R_{GFET\_INT}$: Power transistor internal gate resistance, found in the power transistor datasheet.
- $I_{O+}$ = Peak source current – The minimum value between 4 A, the gate driver peak source current, and the calculated value based on the gate drive loop resistance. (4)

In this example:

$$I_{OA+} = \frac{V_{DD} - V_{BDF}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}} = \frac{20V - 0.8V}{1.47\Omega \,||\, 5\Omega + 2.2\Omega + 4.6\Omega} \approx 2.4A \quad (5)$$

$$I_{OB+} = \frac{V_{DD}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}} = \frac{20V}{1.47\Omega \,||\, 5\Omega + 2.2\Omega + 4.6\Omega} \approx 2.5A \quad (6)$$

Therefore, the high-side and low-side peak source current is 2.4 A and 2.5 A respectively. Similarly, the peak sink current can be calculated with:

$$I_{OA-} = \min\left(6A, \frac{V_{DD} - V_{BDF} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}}\right)$$
$$I_{OB-} = \min\left(6A, \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}}\right) \quad (7)$$

where

- $R_{OFF}$: External turn-off resistance;
- $V_{GDF}$: The anti-parallel diode forward voltage drop which is in series with $R_{OFF}$. The diode in this example is an MSS1P4.
- $I_{O-}$: Peak sink current – the minimum value between 6 A, the gate driver peak sink current, and the calculated value based on the gate drive loop resistance. (8)

In this example,

$$I_{OA-} = \frac{V_{DD} - V_{BDF} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}} = \frac{20V - 0.8V - 0.75V}{0.55\Omega + 0\Omega + 4.6\Omega} \approx 3.6A \quad (9)$$

$$I_{OB--} \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}} = \frac{20V\text{-}0.75V}{0.55\Omega + 0\Omega + 4.6\Omega} \approx 3.7A \quad (10)$$

Therefore, the high-side and low-side peak sink current is 3.6 A and 3.7 A respectively.

Importantly, the estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate driver loop can slow down the peak gate drive current and introduce overshoot and undershoot. Therefore, it is strongly recommended that the gate driver loop should be minimized. On the other hand, the peak source/sink current is dominated by loop parasitics when the load capacitance ($C_{ISS}$) of the power transistor is very small (typically less than 1 nF), because the rising and falling time is too small and close to the parasitic ringing period.

#### *9.2.2.4 Estimate Gate Driver Power Loss*

The total loss, $P_G$, in the gate driver subsystem includes the power losses of the UCC21520 -Q1 ($P_{GD}$) and the power losses in the peripheral circuitry, such as the external gate drive resistor. Bootstrap diode loss is not included in $P_G$ and not discussed in this section.

$P_{GD}$ is the key power loss which determines the thermal safety-related limits of the UCC21520-Q1, and it can be estimated by calculating losses from several components.

The first component is the static power loss, $P_{GDQ}$, which includes quiescent power loss on the driver as well as driver self-power consumption when operating with a certain switching frequency. $P_{GDQ}$ is measured on the bench with no load connected to OUTA and OUTB at a given VCCI, VDDA/VDDB, switching frequency and ambient temperature. 图 4 shows the per output channel current consumption vs. operating frequency with no load. In this example, $V_{VCCI}$ = 5 V and $V_{VDD}$ = 20 V. The current on each power supply, with INA/INB switching from 0 V to 3.3 V at 100 kHz is measured to be $I_{VCCI}$ = 2.5 mA, and $I_{VDDA}$ = $I_{VDDB}$ = 1.5 mA. Therefore, the $P_{GDQ}$ can be calculated with

$$P_{GDO} = V_{VCCI} \times I_{VCCI} + V_{VDDA} \times I_{DDA} + V_{VDDB} \times I_{DDB} \approx 72mW \quad (11)$$

The second component is switching operation loss, $P_{GDO}$, with a given load capacitance which the driver charges and discharges the load during each switching cycle. Total dynamic loss due to load switching, $P_{GSW}$, can be estimated with

$$P_{GSW} = 2 \times V_{DD} \times Q_G \times f_{SW}$$

where

- $Q_G$ is the gate charge of the power transistor. (12)

If a split rail is used to turn on and turn off, then VDD is going to be equal to difference between the positive rail to the negative rail.

So, for this example application:

$$P_{GSW} = 2 \times 20V \times 60nC \times 100kHz = 240mW \quad (13)$$

$Q_G$ represents the total gate charge of the power transistor switching 800 V at 20 A, and is subject to change with different testing conditions. The UCC21520-Q1 gate driver loss on the output stage, $P_{GDO}$, is part of $P_{GSW}$. $P_{GDO}$ will be equal to $P_{GSW}$ if the external gate driver resistances are zero, and all the gate driver loss is dissipated inside the UCC21520-Q1. If there are external turn-on and turn-off resistances, the total loss will be distributed between the gate driver pull-up/down resistances and external gate resistances. Importantly, the pull-up/down resistance is a linear and fixed resistance if the source/sink current is not saturated to 4 A/6 A, however, it will be non-linear if the source/sink current is saturated. Therefore, $P_{GDO}$ is different in these two scenarios.

**Case 1 - Linear Pull-Up/Down Resistor:**

$$P_{GDO} = \frac{P_{GSW}}{2} \times \left( \frac{R_{OH} \,||\, R_{NMOS}}{R_{OH} \,||\, R_{NMOS} + R_{ON} + R_{GFET\_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}} \right) \tag{14}$$

In this design example, all the predicted source/sink currents are less than 4 A/6 A, therefore, the UCC21520-Q1 gate driver loss can be estimated with:

$$P_{GDO} = \frac{240\text{mW}}{2} \times \left( \frac{5\Omega \,||\, 1.47\Omega}{5\Omega \,||\, 1.47\Omega + 2.2\Omega + 4.6\Omega} + \frac{0.55\Omega}{0.55\Omega + 0\Omega + 4.6\Omega} \right) \approx 30\text{mW} \tag{15}$$

**Case 2 - Nonlinear Pull-Up/Down Resistor:**

$$P_{GDO} = 2 \times f_{SW} \times \left[ 4\text{A} \times \int_0^{T_{R\_Sys}} \left( V_{DD} - V_{OUTA/B}(t) \right) dt + 6\text{A} \times \int_0^{T_{F\_Sys}} V_{OUTA/B}(t)\, dt \right]$$

where

- $V_{OUTA/B}(t)$ is the gate driver OUTA and OUTB pin voltage during the turn on and off transient, and it can be simplified that a constant current source (4 A at turn-on and 6 A at turn-off) is charging/discharging a load capacitor. Then, the $V_{OUTA/B}(t)$ waveform will be linear and the $T_{R\_Sys}$ and $T_{F\_Sys}$ can be easily predicted. (16)

For some scenarios, if only one of the pull-up or pull-down circuits is saturated and another one is not, the $P_{GDO}$ will be a combination of Case 1 and Case 2, and the equations can be easily identified for the pull-up and pull-down based on the above discussion. Therefore, total gate driver loss dissipated in the gate driver UCC21520-Q1, $P_{GD}$, is:

$$P_{GD} = P_{GDQ} + P_{GDO} \tag{17}$$

which is equal to 102 mW in the design example.

#### *9.2.2.5 Estimating Junction Temperature*

The junction temperature ($T_J$) of the UCC21520-Q1 can be estimated with:

$$T_J = T_C + \Psi_{JT} \times P_{GD}$$

where

- $T_C$ is the UCC21520-Q1 case-top temperature measured with a thermocouple or some other instrument, and
- $\Psi_{JT}$ is the Junction-to-top characterization parameter from the Thermal Information table. (18)

Using the junction-to-top characterization parameter ($\Psi_{JT}$) instead of the junction-to-case thermal resistance ($R_{\Theta JC}$) can greatly improve the accuracy of the junction temperature estimation. The majority of the thermal energy of most ICs is released into the PCB through the package leads, whereas only a small percentage of the total energy is released through the top of the case (where thermocouple measurements are usually conducted). $R_{\Theta JC}$ can only be used effectively when most of the thermal energy is released through the case, such as with metal packages or when a heatsink is applied to an IC package. In all other cases, use of $R_{\Theta JC}$ will inaccurately estimate the true junction temperature. $\Psi_{JT}$ is experimentally derived by assuming that the amount of energy leaving through the top of the IC will be similar in both the testing environment and the application environment. As long as the recommended layout guidelines are observed, junction temperature estimates can be made accurately to within a few degrees Celsius. For more information, see the Semiconductor and IC Package Thermal Metrics application report.

#### 9.2.2.6 Selecting VCCI, VDDA/B Capacitor

Bypass capacitors for VCCI, VDDA, and VDDB are essential for achieving reliable performance. It is recommended that one choose low ESR and low ESL surface-mount multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients and capacitance tolerances. Importantly, DC bias on an MLCC will impact the actual capacitance value. For example, a 25-V, 1-µF X7R capacitor is measured to be only 500 nF when a DC bias of 15 $V_{DC}$ is applied.

##### 9.2.2.6.1 Selecting a VCCI Capacitor

A bypass capacitor connected to VCCI supports the transient current needed for the primary logic and the total current consumption, which is only a few mA. Therefore, a 50-V MLCC with over 100 nF is recommended for this application. If the bias power supply output is a relatively long distance from the VCCI pin, a tantalum or electrolytic capacitor, with a value over 1 µF, should be placed in parallel with the MLCC.

##### 9.2.2.6.2 Selecting a VDDA (Bootstrap) Capacitor

A VDDA capacitor, also referred to as a *bootstrap capacitor* in bootstrap power supply configurations, allows for gate drive current transients up to 6 A, and needs to maintain a stable gate drive voltage for the power transistor.

The total charge needed per switching cycle can be estimated with

$$Q_{Total} = Q_G + \frac{I_{VDD}@100kHz(\text{No Load})}{f_{SW}} = 60nC + \frac{1.5mA}{100kHz} = 75nC \quad (19)$$

where

- $Q_G$: Gate charge of the power transistor.
- $I_{VDD}$: The channel self-current consumption with no load at 100kHz.

Therefore, the absolute minimum $C_{Boot}$ requirement is:

$$C_{Boot} = \frac{Q_{Total}}{\Delta V_{VDDA}} = \frac{75nC}{0.5V} = 150nF \quad (20)$$

where

- $\Delta V_{VDDA}$ is the voltage ripple at VDDA, which is 0.5 V in this example.

In practice, the value of $C_{Boot}$ is greater than the calculated value. This allows for the capacitance shift caused by the DC bias voltage and for situations where the power stage would otherwise skip pulses due to load transients. Therefore, it is recommended to include a safety-related margin in the $C_{Boot}$ value and place it as close to the VDD and VSS pins as possible. A 50-V 1-µF capacitor is chosen in this example.

$$C_{Boot} = 1\mu F \quad (21)$$

To further lower the AC impedance for a wide frequency range, it is recommended to have bypass capacitor with a low capacitance value, in this example a 100 nF, in parallel with $C_{Boot}$ to optimize the transient performance.

> **注**
>
> Too large $C_{BOOT}$ is not good. $C_{BOOT}$ may not be charged within the first few cycles and $V_{BOOT}$ could stay below UVLO. As a result, the high-side FET does not follow input signal command. Also during initial $C_{BOOT}$ charging cycles, the bootstrap diode has highest reverse recovery current and losses.

#### 9.2.2.6.3 Select a VDDB Capacitor

Chanel B has the same current requirements as Channel A, Therefore, a VDDB capacitor (Shown as $C_{VDD}$ in 图 38) is needed. In this example with a bootstrap configuration, the VDDB capacitor will also supply current for VDDA through the bootstrap diode. A 50-V, 10-µF MLCC and a 50-V, 220-nF MLCC are chosen for $C_{VDD}$. If the bias power supply output is a relatively long distance from the VDDB pin, a tantalum or electrolytic capacitor, with a value over 10 µF, should be used in parallel with CVDD.

### *9.2.2.7 Dead Time Setting Guidelines*

For power converter topologies utilizing half-bridges, the dead time setting between the top and bottom transistor is important for preventing shoot-through during dynamic switching.

The UCC21520-Q1 dead time specification in the electrical table is defined as the time interval from 90% of one channel's falling edge to 10% of the other channel's rising edge (see

*图 30*). This definition ensures that the dead time setting is independent of the load condition, and guarantees linearity through manufacture testing. However, this dead time setting may not reflect the dead time in the power converter system, since the dead time setting is dependent on the external gate drive turn-on/off resistor, DC-Link switching voltage/current, as well as the input capacitance of the load transistor.

Here is a suggestion on how to select an appropriate dead time for UCC21520-Q1:

$$DT_{Setting} = DT_{Req} + T_{F\_Sys} + T_{R\_Sys} - T_{D(on)} \quad (22)$$

where

- $DT_{setting}$: UCC21520-Q1 dead time setting in ns, $DT_{Setting}$ = 10 × RDT(in kΩ).
- $DT_{Req}$: System required dead time between the real $V_{GS}$ signal of the top and bottom switch with enough margin, or ZVS requirement.
- $T_{F\_Sys}$: In-system gate turn-off falling time at worst case of load, voltage/current conditions.
- $T_{R\_Sys}$: In-system gate turn-on rising time at worst case of load, voltage/current conditions.
- $T_{D(on)}$: Turn-on delay time, from 10% of the transistor gate signal to power transistor gate threshold.

In the example, $DT_{Setting}$ is set to 250 ns.

It should be noted that the UCC21520-Q1 dead time setting is decided by the DT pin configuration (See Programmable Dead Time (DT) Pin), and it cannot automatically fine-tune the dead time based on system conditions. It is recommended to parallel a ceramic capacitor, 2.2 nF or above, close to the DT pin with $R_{DT}$ to achieve better noise immunity.

### 9.2.2.8 Application Circuits with Output Stage Negative Bias

When parasitic inductances are introduced by non-ideal PCB layout and long package leads (e.g. TO-220 and TO-247 type packages), there could be ringing in the gate-source drive voltage of the power transistor during high di/dt and dv/dt switching. If the ringing is over the threshold voltage, there is the risk of unintended turn-on and even shoot-through. Applying a negative bias on the gate drive is a popular way to keep such ringing below the threshold. Below are a few examples of implementing negative gate drive bias.

*图 39* shows the first example with negative bias turn-off on the channel-A driver using a Zener diode on the isolated power supply output stage. The negative bias is set by the Zener diode voltage. If the isolated power supply, $V_A$, is equal to 25 V, the turn-off voltage will be –5.1 V and turn-on voltage will be 25 V – 5.1 V ≈ 20 V. The channel-B driver circuit is the same as channel-A, therefore, this configuration needs two power supplies for a half-bridge configuration, and there will be steady state power consumption from $R_Z$.

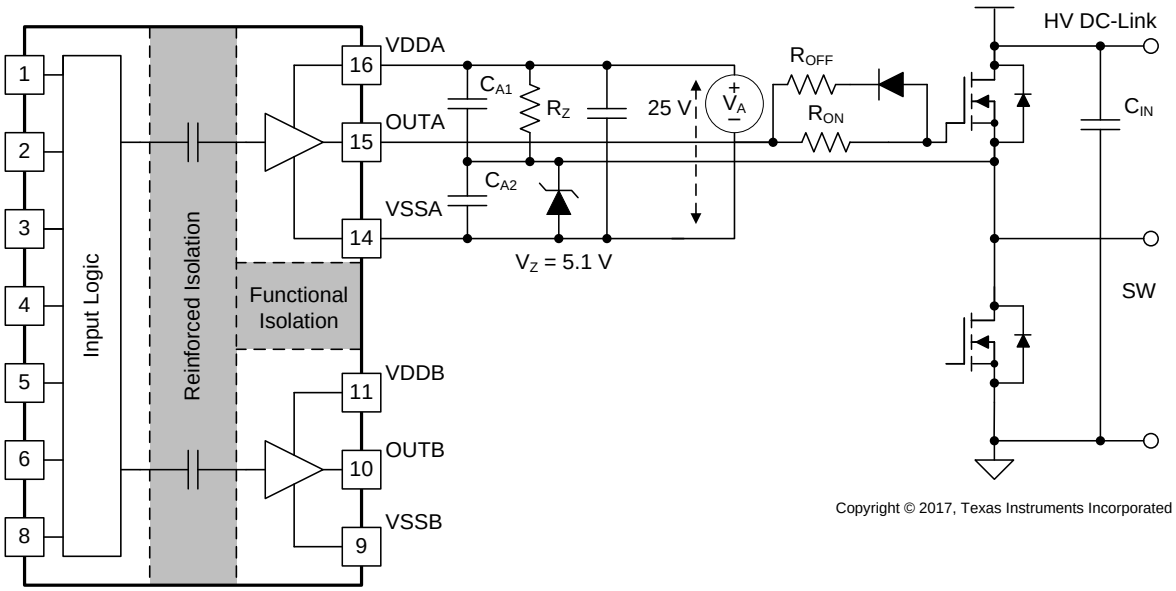



**图 39. Negative Bias with Zener Diode on Iso-Bias Power Supply Output**

*图 40* shows another example which uses two supplies (or single-input-double-output power supply). Power supply $V_{A+}$ determines the positive drive output voltage and $V_{A–}$ determines the negative turn-off voltage. The configuration for channel B is the same as channel A. This solution requires more power supplies than the first example, however, it provides more flexibility when setting the positive and negative rail voltages.

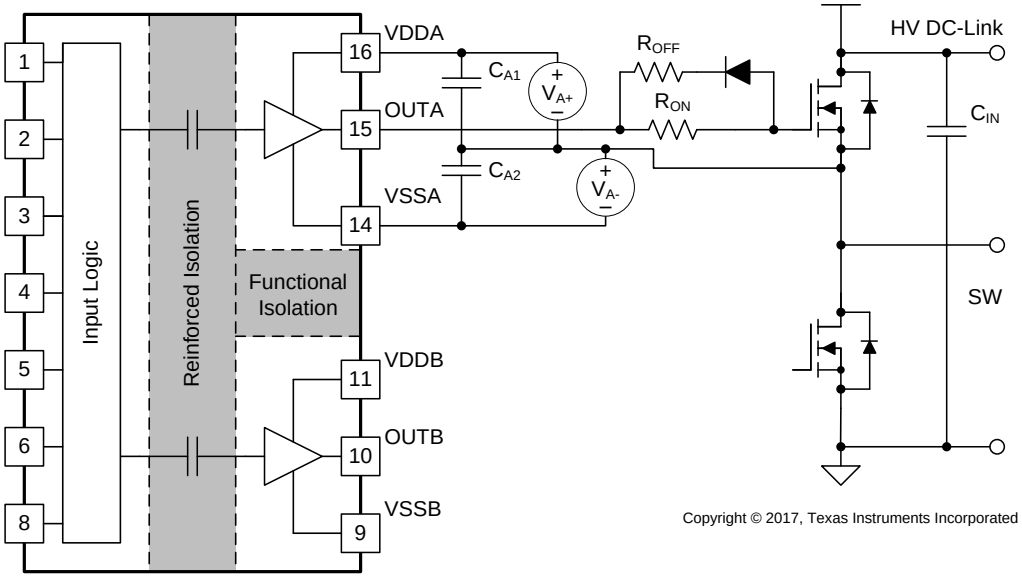



**图 40. Negative Bias with Two Iso-Bias Power Supplies**

The last example, shown in 图 41, is a single power supply configuration and generates negative bias through a Zener diode in the gate drive loop. The benefit of this solution is that it only uses one power supply and the bootstrap power supply can be used for the high side drive. This design requires the least cost and design effort among the three solutions. However, this solution has limitations:

1. The negative gate drive bias is not only determined by the Zener diode, but also by the duty cycle, which means the negative bias voltage will change when the duty cycle changes. Therefore, converters with a fixed duty cycle (~50%) such as variable frequency resonant convertors or phase shift convertors favor this solution.
2. The high side VDDA-VSSA must maintain enough voltage to stay in the recommended power supply range, which means the low side switch must turn-on or have free-wheeling current on the body (or anti-parallel) diode for a certain period during each switching cycle to refresh the bootstrap capacitor. Therefore, a 100% duty cycle for the high side is not possible unless there is a dedicated power supply for the high side, like in the other two example circuits.

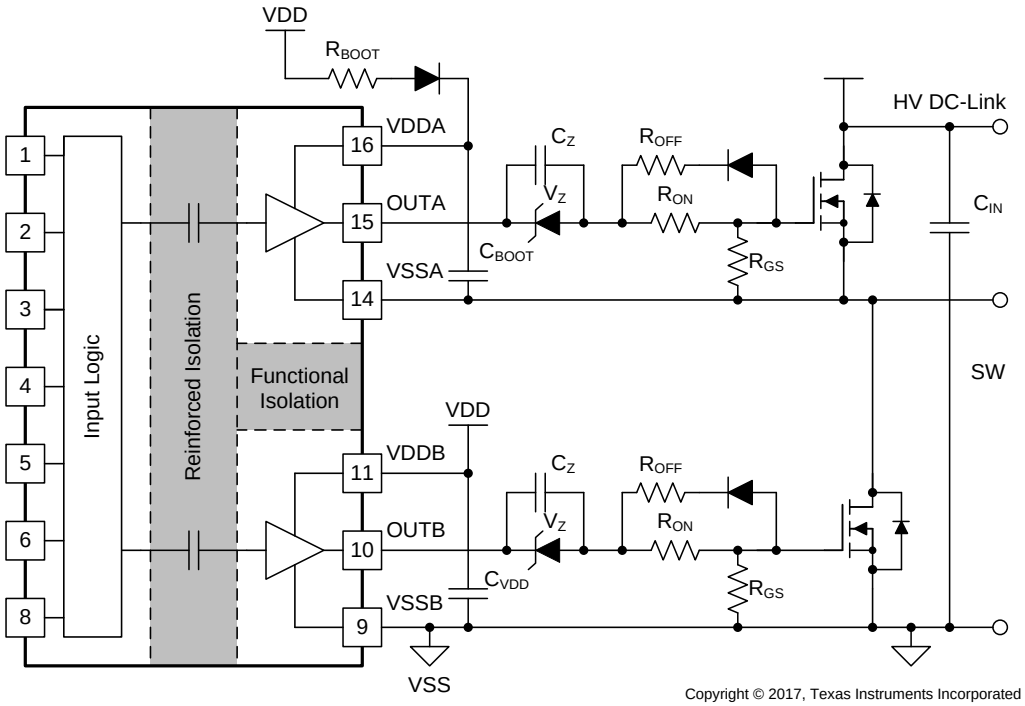



**图 41. Negative Bias with Single Power Supply and Zener Diode in Gate Drive Path**

### 9.2.3 Application Curves

图 42 and 图 43 shows the bench test waveforms for the design example shown in 图 38 under these conditions: VCC = 5 V, VDD = 20 V, $f_{SW}$ = 100 kHz, $V_{DC-Link}$ = 0 V.

**Channel 1 (Yellow):** UCC21520-Q1 INA pin signal.

**Channel 2 (Blue):** UCC21520-Q1 INB pin signal.

**Channel 3 (Pink):** Gate-source signal on the high side power transistor.

**Channel 4 (Green):** Gate-source signal on the low side power transistor.

In 图 42, INA and INB are sent complimentary 3.3-V, 50% duty-cycle signals. The gate drive signals on the power transistor have a 250-ns dead time, shown in the measurement section of 图 42. The dead-time matching is less than 1 ns with the 250-ns dead-time setting.

图 43 shows a zoomed-in version of the waveform of 图 42, with measurements for propagation delay and rising/falling time. Cursors are also used to measure dead time. Importantly, the output waveform is measured between the power transistors' gate and source pins, and is not measured directly from the driver OUTA and OUTB pins. Due to the split on and off resistors ($R_{on}$,$R_{off}$) and different sink and source currents, different rising (16 ns) and falling time (9 ns) are observed in 图 43.


图 42. Bench Test Waveform for INA/B and OUTA/B

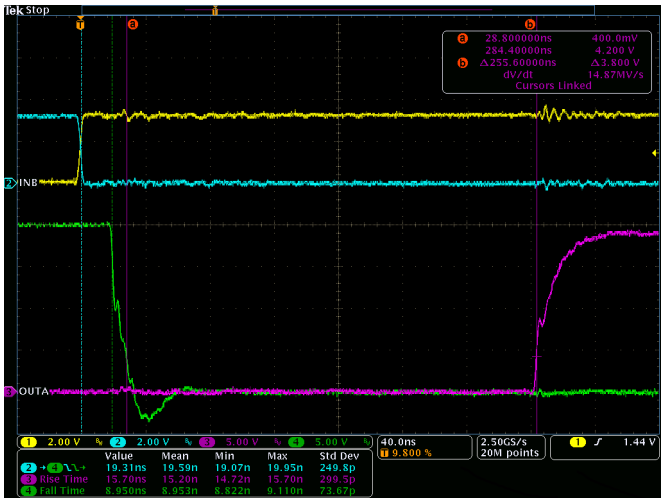



图 43. Zoomed-In bench-test waveform

## 10 Power Supply Recommendations

The recommended input supply voltage (VCCI) for the UCC21520-Q1 is between 3 V and 18 V. The output bias supply voltage (VDDA/VDDB) range depends on which version of UCC21520-Q1 one is using. The lower end of this bias supply range is governed by the internal under voltage lockout (UVLO) protection feature of each device. One mustn't let VDD or VCCI fall below their respective UVLO thresholds (For more information on UVLO see VDD, VCCI, and Under Voltage Lock Out (UVLO)). The upper end of the VDDA/VDDB range depends on the maximum gate voltage of the power device being driven by the UCC21520-Q1. The UCC21520-Q1 have a recommended maximum VDDA/VDDB of 25 V.

A local bypass capacitor should be placed between the VDD and VSS pins. This capacitor should be positioned as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. It is further suggested that one place two such capacitors: one with a value of ≈10-µF for device biasing, and an additional ≤100-nF capacitor in parallel for high frequency filtering.

Similarly, a bypass capacitor should also be placed between the VCCI and GND pins. Given the small amount of current drawn by the logic circuitry within the input side of the UCC21520-Q1, this bypass capacitor has a minimum recommended value of 100 nF.

# 11 Layout

## 11.1 Layout Guidelines

One must pay close attention to PCB layout in order to achieve optimum performance for the UCC21520-Q1. Below are some key points.

**Component Placement:**

- Low-ESR and low-ESL capacitors must be connected close to the device between the VCCI and GND pins and between the VDD and VSS pins to support high peak currents when turning on the external power transistor.
- To avoid large negative transients on the switch node VSSA (HS) pin, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.
- It is recommended to place the dead-time setting resistor, $R_{DT}$, and its bypassing capacitor close to DT pin of the UCC21520-Q1.
- It is recommended to bypass using a ≈1nF low ESR/ESL capacitor, $C_{DIS}$, close to DIS pin when connecting to a µC with distance.

**Grounding Considerations:**

- It is essential to confine the high peak currents that charge and discharge the transistor gates to a minimal physical area. This will decrease the loop inductance and minimize noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- Pay attention to high current path that includes the bootstrap capacitor, bootstrap diode, local VSSB-referenced bypass capacitor, and the low-side transistor body/anti-parallel diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode by the VDD bypass capacitor. This recharging occurs in a short time interval and involves a high peak current. Minimizing this loop length and area on the circuit board is important for ensuring reliable operation.

**High-Voltage Considerations:**

- To ensure isolation performance between the primary and secondary side, one should avoid placing any PCB traces or copper below the driver device. A PCB cutout is recommended in order to prevent contamination that may compromise the UCC21520-Q1's isolation performance.
- For half-bridge, or high-side/low-side configurations, where the channel A and channel B drivers could operate with a DC-link voltage up to 1500 $V_{DC}$, one should try to increase the creepage distance of the PCB layout between the high and low-side PCB traces.

**Thermal Considerations:**

- A large amount of power may be dissipated by the UCC21520-Q1 if the driving voltage is high, the load is heavy, or the switching frequency is high (refer to Estimate Gate Driver Power Loss for more details). Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction to board thermal impedance ($\theta_{JB}$).
- Increasing the PCB copper connecting to VDDA, VDDB, VSSA and VSSB pins is recommended, with priority on maximizing the connection to VSSA and VSSB (see 图 45 and 图 46). However, high voltage PCB considerations mentioned above must be maintained.
- If there are multiple layers in the system, it is also recommended to connect the VDDA, VDDB, VSSA and VSSB pins to internal ground or power planes through multiple vias of adequate size. However, keep in mind that there shouldn't be any traces/coppers from different high voltage planes overlapping.

## 11.2 Layout Example

图 44 shows a 2-layer PCB layout example with the signals and key components labeled.

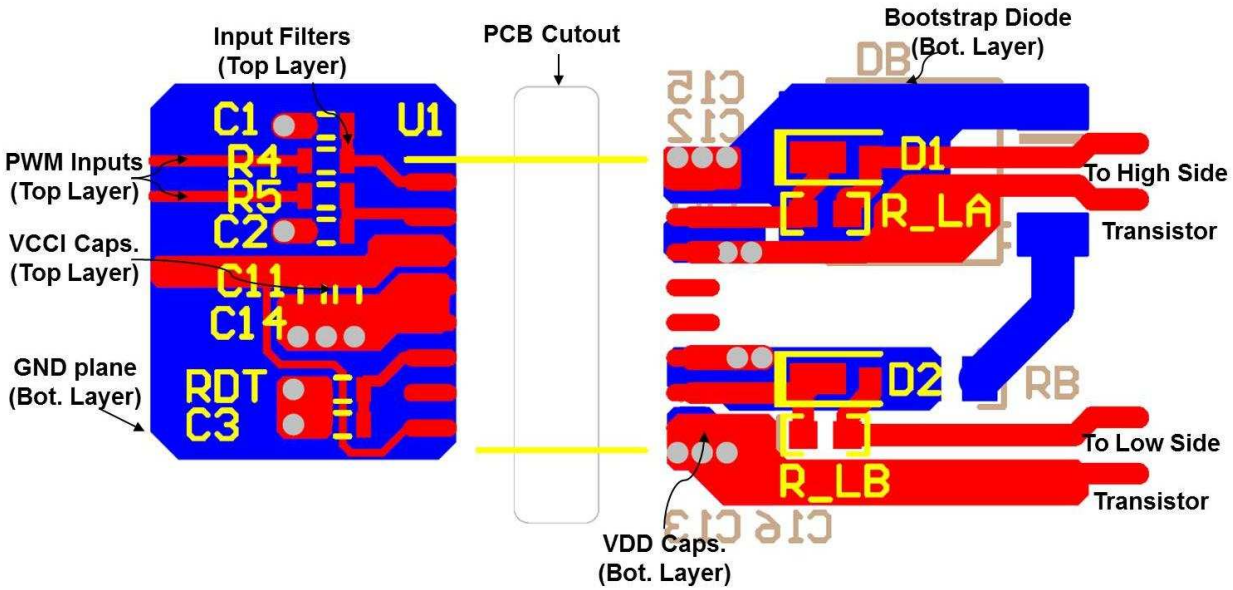



**图 44. Layout Example**

图 45 and 图 46 shows top and bottom layer traces and copper.

**注**

There are no PCB traces or copper between the primary and secondary side, which ensures isolation performance.

## Layout Example (接下页)

PCB traces between the high-side and low-side gate drivers in the output stage are increased to maximize the creepage distance for high-voltage operation, which will also minimize cross-talk between the switching node VSSA (SW), where high dv/dt may exist, and the low-side gate drive due to the parasitic capacitance coupling.

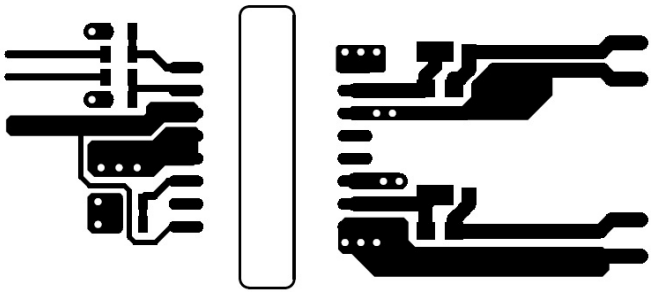


图 45. Top Layer Traces and Copper

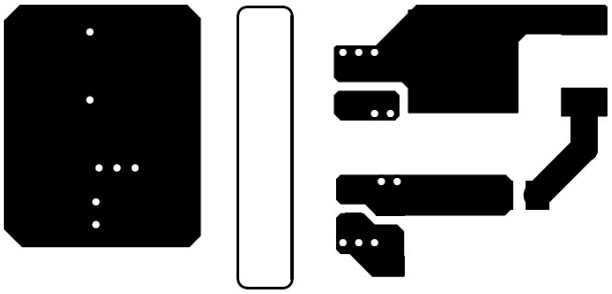


图 46. Bottom Layer Traces and Copper

图 47 and 图 48 are 3D layout pictures with top view and bottom views.

**注**

The location of the PCB cutout between the primary side and secondary sides, which ensures isolation performance.

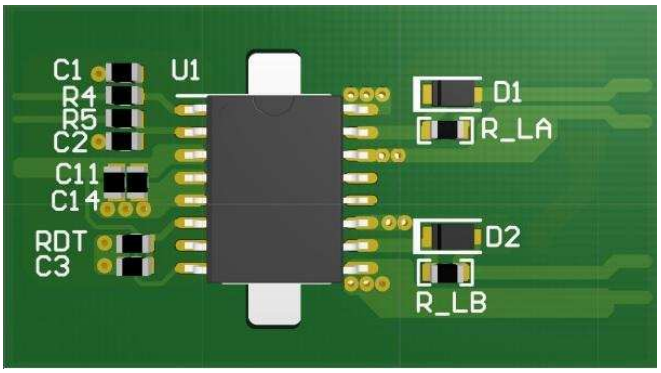



图 47. 3-D PCB Top View

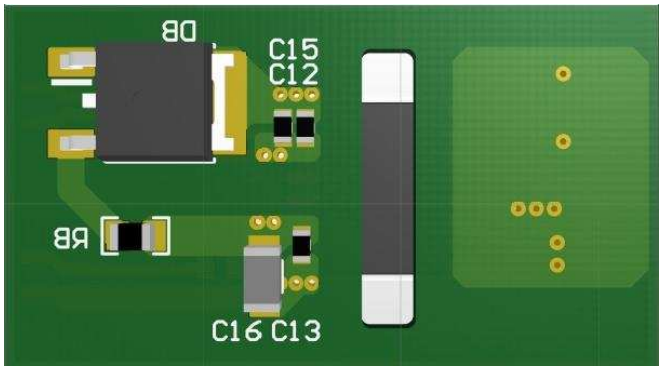



图 48. 3-D PCB Bottom View

# 12 器件和文档支持

## 12.1 文档支持

### 12.1.1 相关文档

请参阅如下相关文档：

- 隔离相关术语

## 12.2 认证

UL 在线认证目录，*"FPPT2.E181974 非光学隔离器件 - 组件"*证书编号：20160516-E181974,

VDE Pruf- und Zertifizierungsinstitut 认证，工厂监督合格证书

CQC 在线认证目录，"GB4943.1-2011，数字隔离器证书"证书编号：CQC16001155011

CSA 在线认证目录，"CSA 合格证书"证书编号：70097761，主合同编号：220991

## 12.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 12.4 社区资源

**下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。**

**TI E2E™ 在线社区** ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

**设计支持** ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

## 12.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

## 12.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

# 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| UCC21520AQDWQ1 | LIFEBUY | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | UCC21520AQ | |
| UCC21520AQDWRQ1 | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | UCC21520AQ | Samples |
| UCC21520QDWQ1 | LIFEBUY | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | UCC21520Q | |
| UCC21520QDWRQ1 | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | UCC21520Q | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF UCC21520-Q1 :**

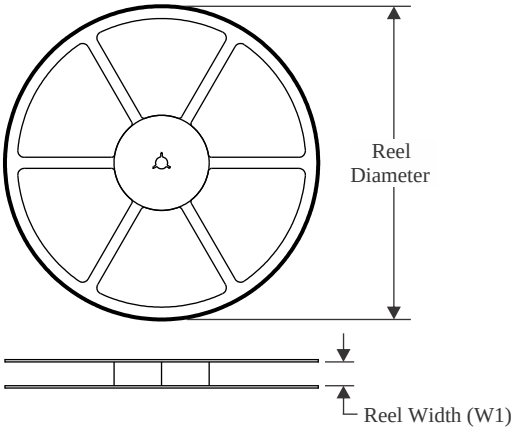
- Catalog : UCC21520

NOTE: Qualified Version Definitions:

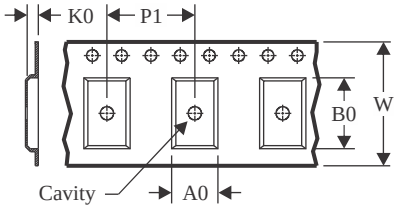
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

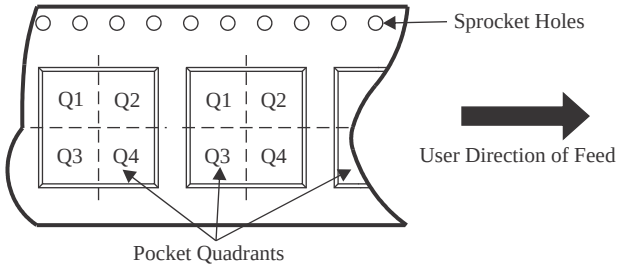



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

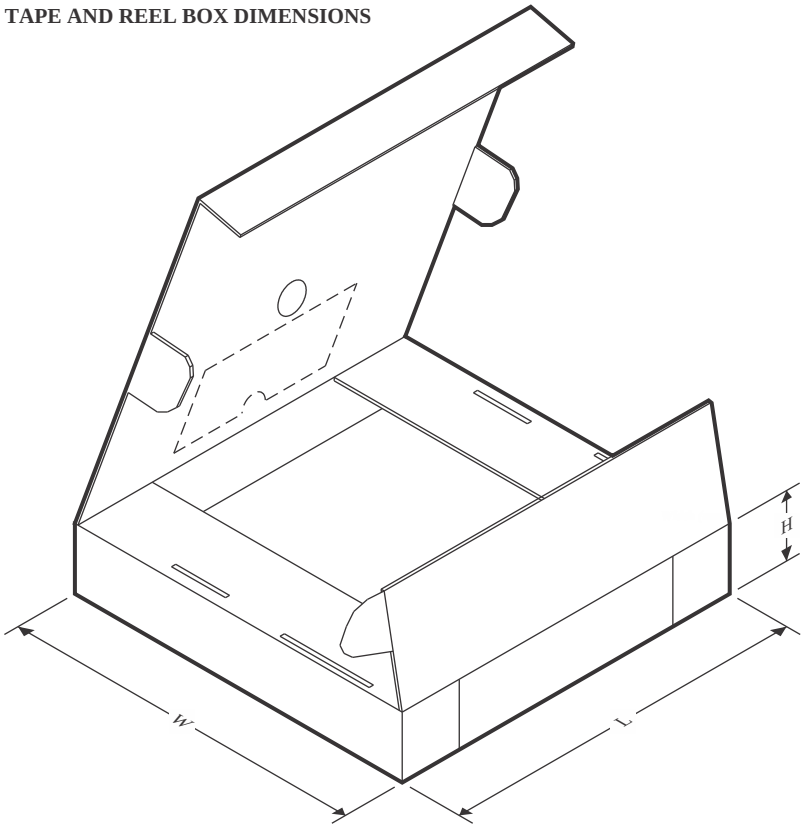
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UCC21520AQDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| UCC21520AQDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| UCC21520QDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| UCC21520QDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| UCC21520QDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

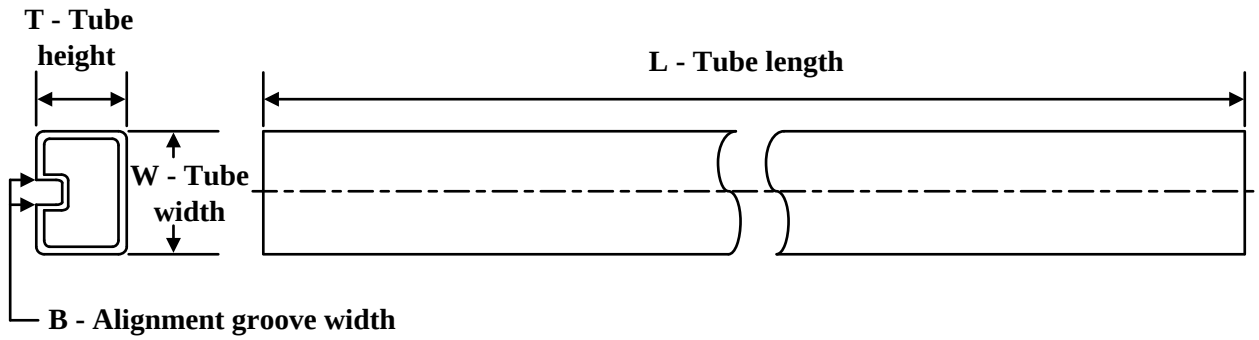
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| UCC21520AQDWRQ1 | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| UCC21520AQDWRQ1 | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| UCC21520QDWRQ1 | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| UCC21520QDWRQ1 | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| UCC21520QDWRQ1 | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| UCC21520AQDWQ1 | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| UCC21520AQDWQ1 | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| UCC21520QDWQ1 | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| UCC21520QDWQ1 | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |

# GENERIC PACKAGE VIEW

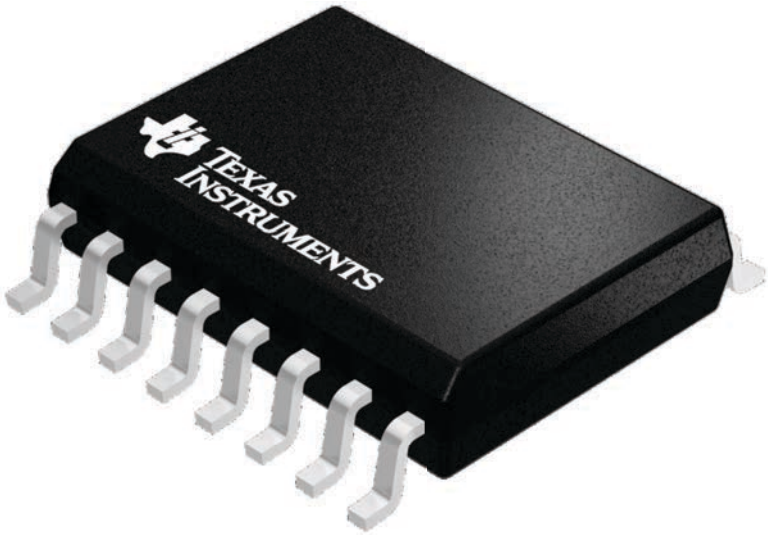
## DW 16

## SOIC - 2.65 mm max height

**7.5 x 10.3, 1.27 mm pitch**

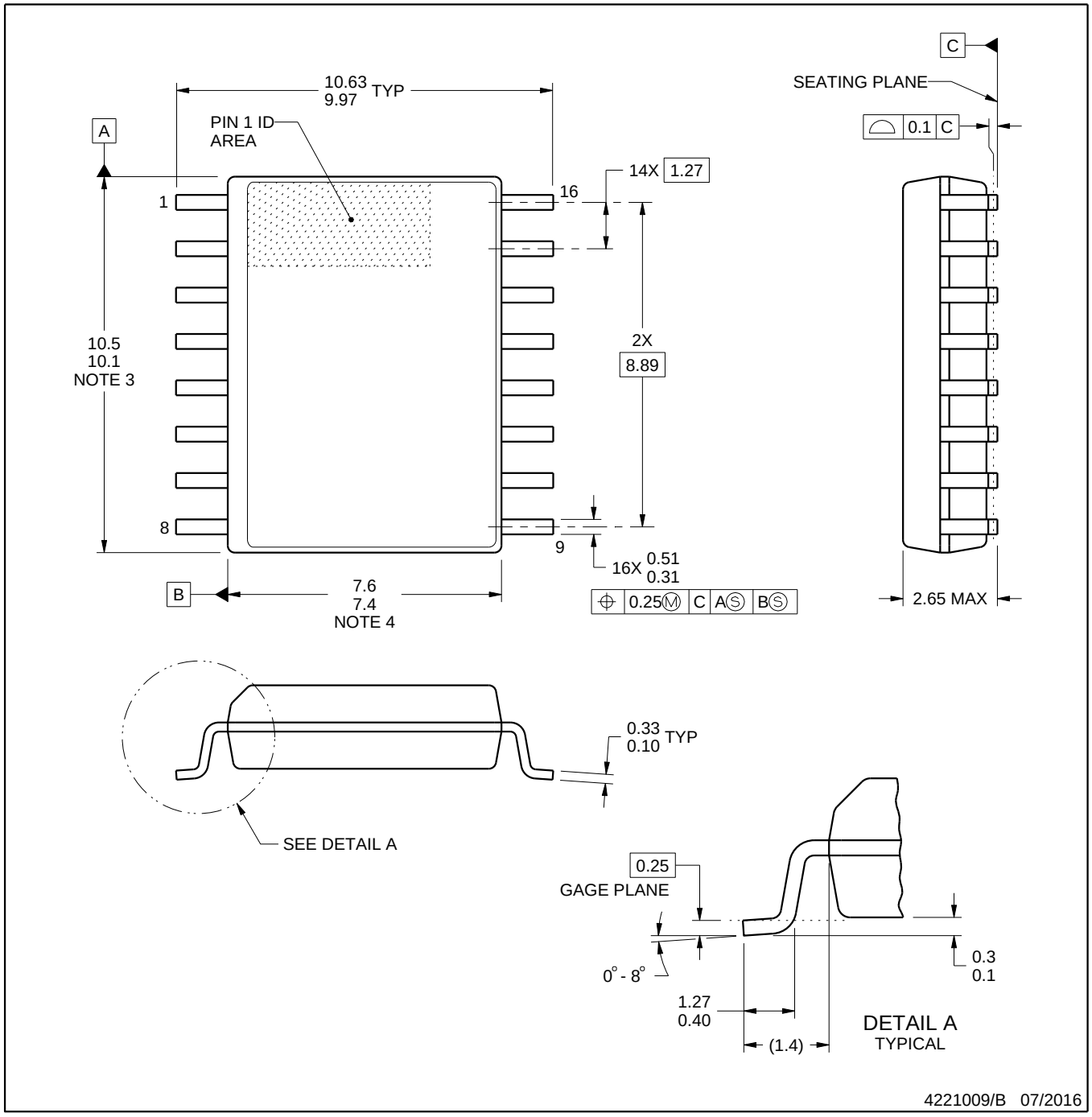
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



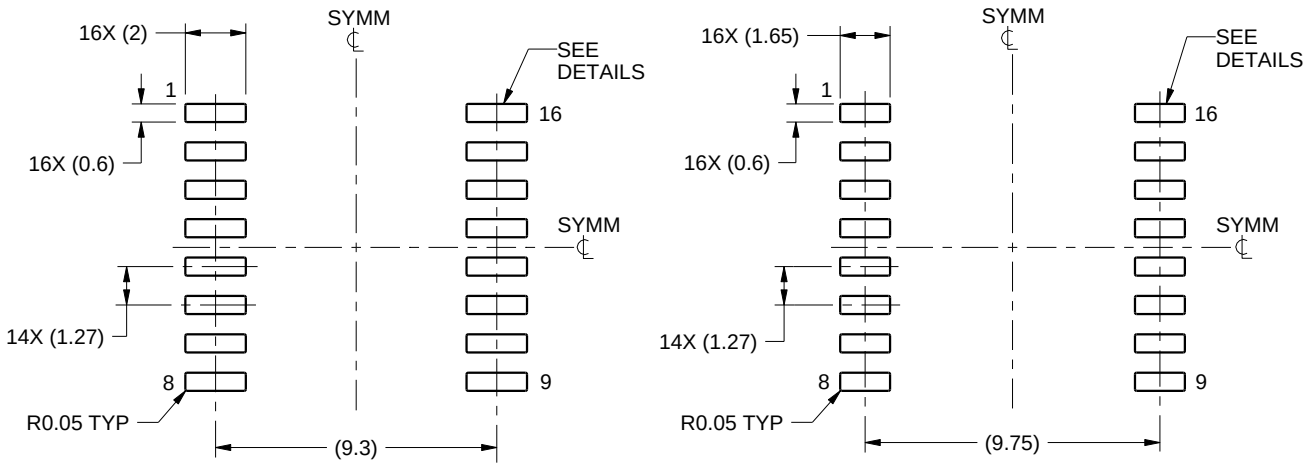

4224780/A

SOIC




NOTES:

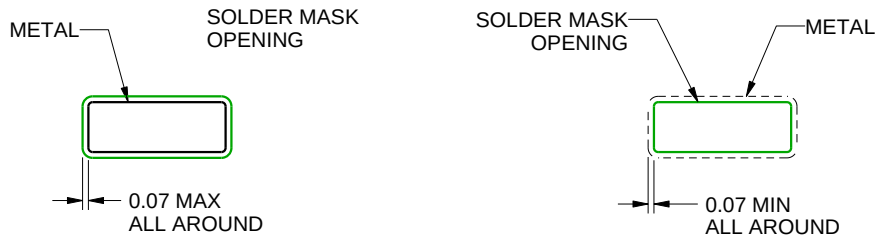
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.




IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X




NON SOLDER MASK DEFINED

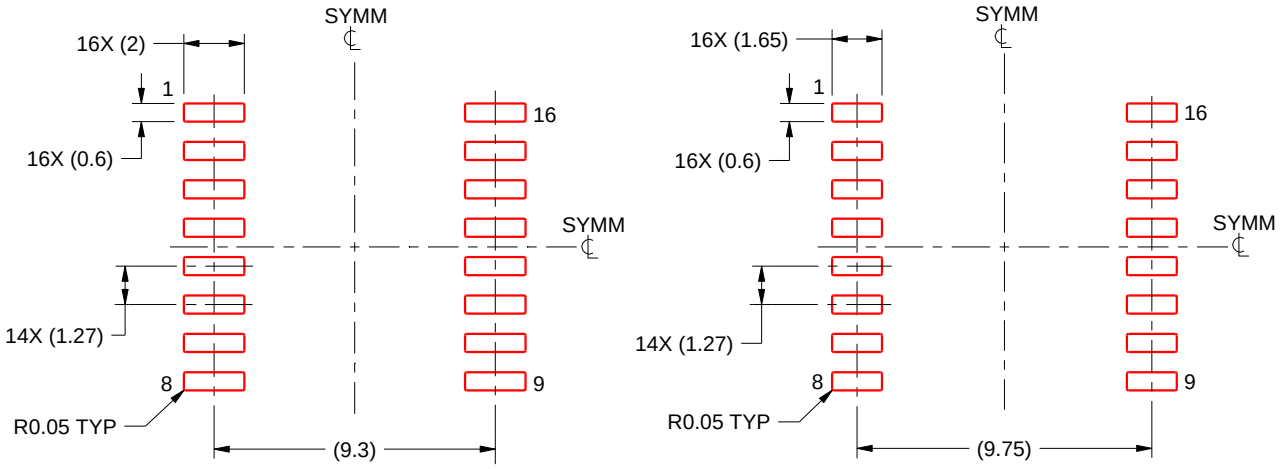
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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