TPS25820、TPS25821 USB Type-C™ 1.5A 源控制器和电源开关

1 特性

- USB Type-C™ Rel. 1.3 兼容源控制器
- CC 线路上 STD/1.5A 电流通告性能
- 连接器连接/断开的检测
- 超高速极性确定
- V_{BUS} 和 V_{CONN} (TPS25820) 应用以及用内部固定电流限制放电
- Type-C 连接器不附加任何器件时的工作电流为 1.0μA（典型值）
- 64mΩ（典型值）高侧输出 MOSFET
- 满足 USB 限流要求
  - 输出电流限制为 1.7A，精度为 ±7%
  - 快速过流响应 - 1.5μs（典型值）
- CC1 和 CC2 ±8kV 接触放电以及 ± 15kV 空气放电 ESD 额定值 (IEC-61000-4-2)
- IEC/UL 证书
  - US-33101-UL: IEC 60950-1:2005; AMD1:2009, AMD2:2013
  - US-33102-UL: IEC 62368-1:2014

2 应用

- USB 2.0 或 3.x Type-C 主机和集线器端口
- 笔记本/台式计算机和平板电脑
- LCD 监视器/扩展坞和充电托板
- Type-C USB 墙壁充电器、移动电源和 CLA
- 机顶盒和音频/视频系统

3 说明

TPS25820/21 是一款 USB Type-C 电源控制器，集成了一个额定电流为 1.5A 的 USB 电源开关。TPS25820/21 通过监测 Type-C 配置通道 (CC) 线路来确定 USB 接收装置是否连接。如果连接了接收装置，TPS25820/21 会向 V_{BUS} 供电，并将可选的 V_{BUS} 拉电流能力通过直通 CC 线路传达给接收器。如果使用电子标记电缆连接了接收装置，TPS25820 还会将 V_{CONN} 电源施加于电缆 V_{CONN} 引脚。TPS25821 不会施加 V_{CONN} 电源，并在 USB 2.0 以及实施无数据充电等不需要 V_{CONN} 的情况下发挥作用。

在不附加任何器件时，TPS25820/21 消耗的电流为 1.0μA（典型值）。$\overline{FAULT}$ 输出在开关处于过流和过热条件时发出信号。$\overline{SINK}$ 输出在连接了接收装置时发出信号，$\overline{POL}$ 输出将以信号形式发出电缆超速线路的极性。

器件信息(1)

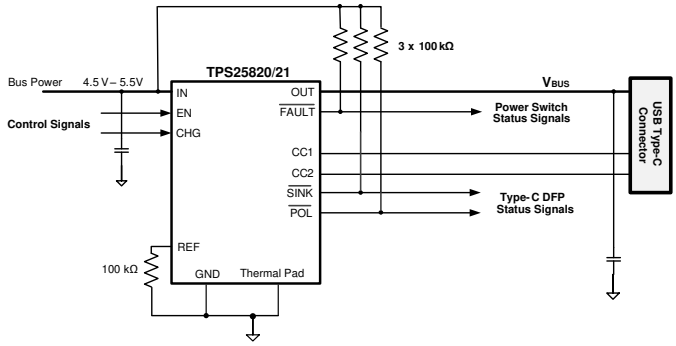
器件型号	封装	封装尺寸（标称值）
TPS25820	WSON (12)	3.00mm x 2.00mm
TPS25821	WSON (12)	3.00mm x 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

器件比较

器件型号	VCONN
TPS25820	是
TPS25821	否

简化原理图



目录

4 修订历史记录

Changes from Revision B (February 2019) to Revision C **Page**

- 已添加 向特性部分添加了 US-33102-UL: IEC 62368-1:2014 ... 1

Changes from Revision A (December 2017) to Revision B **Page**

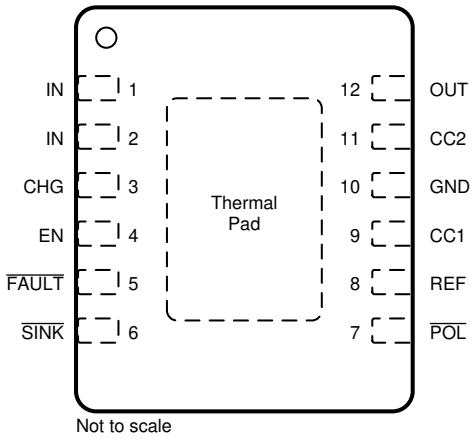
- 已添加 添加了 IEC/UL 证书编号（目标位置：特性部分） ... 1

Changes from Original (November 2017) to Revision A **Page**

- 已更改 将 TPS25821 从产品预览更改为生产数据 ... 1

5 Pin Configuration and Functions

DSS Package
12-Pin WSON
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
IN	1, 2	I	Device input supply. V_{BUS} internal power switch input supply. V_{CONN} internal power switch input supply for the TPS25820.
CHG	3	I	Charge logic input to select between standard USB or 1.5-A Type-C current sourcing ability.
EN	4	I	Logic input to turn the device on and off.
$\overline{\text{FAULT}}$	5	O	Open-drain logic output that asserts when the device is in overtemperature and/or V_{BUS} is in current limit condition.
$\overline{\text{SINK}}$	6	O	Open-drain logic output that asserts when a Type-C Sink is identified on the CC lines.
$\overline{\text{POL}}$	7	O	Open-drain logic output that signals which Type-C CC pin is connected to the cable CC line. This gives the information needed to mux the super speed lines. Asserted when the CC2 pin is connected to the cable CC line.
REF	8	I	Analog input used to make a current reference. Connect a 0.5%, 100-ppm, 100-kΩ resistor between this pin and GND.
CC1	9	I/O	Analog input/output that connects to the Type-C receptacle CC1 pin.
GND	10	–	Ground
CC2	11	I/O	Analog input/output that connects to the Type-C receptacle CC2 pin.
OUT	12	O	V_{BUS} power switch output.
Thermal Pad	–	–	Thermal pad on bottom of package.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, voltages are respect to GND (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage, V	IN, EN, CHG, REF, OUT, $\overline{\text{FAULT}}$, CC1, CC2, $\overline{\text{SINK}}$, $\overline{\text{POL}}$	–0.3	6	V
Pin positive source current, I_{SRC}	OUT, REF, CC1, CC2		Internally limited	A
Pin positive sink current, I_{SNK}	OUT (while applying V_{BUS})		2.5	A
	CC1, CC2 (while TPS25820 applying V_{CONN})		1	A
	$\overline{\text{FAULT}}$, $\overline{\text{SINK}}$, $\overline{\text{POL}}$		Internally limited	mA
Operating junction temperature, T_J		–40	180	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (3)	±500	
		IEC61000-4-2 contact discharge, CC1 and CC2 (4)	±8000	
		IEC61000-4-2 air-gap discharge, CC1 and CC2 (4)	±15000	

(1) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by assembly line electrostatic discharges into the device.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(4) Surges per IEC61000-4-2, 1999 applied between CC1/CC2 and output ground of the TPS25820EVM-835.

6.3 Recommended Operating Conditions

Voltages are with respect to GND (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_I	Supply voltage	IN	4.5		5.5	V
V_I	Input voltage	EN, CHG	0		5.5	V
V_{IH}	High-level input voltage	EN, CHG	2			V
V_{IL}	Low-level voltage	EN, CHG			0.8	V
V_{PU}	Pull-up voltage	Used on $\overline{\text{FAULT}}$, $\overline{\text{SINK}}$, $\overline{\text{POL}}$	0		5.5	V
I_{SRC}	Positive source current	OUT			1.5	A
		CC1 or CC2 when supplying V_{CONN}			250	mA
I_{SNK}	Positive sink current (100 ms moving average)	$\overline{\text{SINK}}$, $\overline{\text{POL}}$			5	mA
		$\overline{\text{FAULT}}$			10	
I_{SNK_PULSE}	Positive repetitive pulse sink current	$\overline{\text{FAULT}}$, $\overline{\text{SINK}}$, $\overline{\text{POL}}$			Internally Limited	mA
T_J	Operating junction temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS25820, TPS25821 DSS (WSON) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	57.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

–40°C ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN} ≤ 5.5 V, V_{EN} = V_{CHG} = V_{IN}, R_{REF} = 100 kΩ. Typical values are at 25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated pin (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUT - POWER SWITCH						
$R_{DS(on)}$	On resistance(1)	T_J = 25°C, I_{OUT} = 1.5 A		64	70	mΩ
		–40°C ≤ T_J ≤ 85°C, I_{OUT} = 1.5 A		64	85	
		–40°C ≤ T_J ≤ 125°C, I_{OUT} = 1.5 A		64	98	
I_{REV}	OUT to IN reverse leakage current	V_{OUT} = 5.5 V, 0 ≤ V_{IN} ≤ 5.5 V, V_{EN} = 0 V, –40°C ≤ T_J ≤ 85°C, measure I_{IN}		0	3	µA
OUT - CURRENT LIMIT						
I_{OS}	Short circuit current limit (1)		1.6	1.72	1.84	A
		R_{REF} = 10 Ω			4.0	
OUT - DISCHARGE						
	Discharge resistance	V_{OUT} = 4 V	400	500	600	Ω
	Bleed discharge resistance	V_{OUT} = 4 V, No Sink termination on CC lines, time > $t_{W\_OUT\_DCHG}$	90	150	250	kΩ
V_{TH}	Rising threshold for not discharged				800	mV
REF						
I_{OS}	Short circuit current	R_{REF} = 10 Ω	9.5		17.5	µA
V_O	Output voltage		0.78	0.8	0.82	V
$\overline{FAULT}$						
V_{OL}	Output low voltage	$I_{\overline{FAULT}}$ = 1 mA			250	mV
I_{OFF}	Off-state leakage	$V_{\overline{FAULT}}$ = 5.5 V			1	µA
CC1/CC2 - V_{CONN} POWER SWITCH (TPS25820)						
$R_{DS(on)}$	On resistance	T_J = 25°C, I_{CCx} = 250 mA		480	530	mΩ
		-40°C ≤ T_J ≤ 85°C, I_{CCx} = 250 mA		480	645	
		-40°C ≤ T_J ≤ 125°C, I_{CCx} = 250 mA		480	755	
CC1/CC2 - V_{CONN} POWER SWITCH - CURRENT LIMIT (TPS25820)						
I_{OS}	Short circuit current limit(1)		315	370	425	mA
		R_{REF} = 10 Ω			1000	

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

Electrical Characteristics (continued)

–40°C ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN} ≤ 5.5 V, V_{EN} = V_{CHG} = V_{IN}, R_{REF} = 100 kΩ. Typical values are at 25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated pin (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CC1/CC2 – CONNECT MANAGEMENT						
I_{SRC}	Sourcing current	V_{CHG} = 0 V, 0 V ≤ V_{CCx} ≤ 1.5 V, after V $\overline{SINK}$ = 0 V	73	80	85	µA
		0 V ≤ V_{CCx} ≤ 1.5 V, after V $\overline{SINK}$ = 0 V	168	180	190	
		V_{CHG} = 0 V or V_{IN}, 0 V ≤ V_{CCx} ≤ 1.5 V, before V $\overline{SINK}$ = 0 V	64	80	96	
I_{REV}	Reverse leakage current	CCx is the CC pin under test, CCy is the other CC pin. V_{CCx} = 5.5 V, CCy floating, V_{EN} = 0 V or 0 V ≤ V_{IN} ≤ 5.5 V, –40°C ≤ T_J ≤ 85°C, I_{REV} is current into CCx pin.		0	5	µA
		CCx is the CC pin under test, CCy is the other CC pin. V_{CCx} = 5.5 V, CCy = 0 V, –40°C ≤ T_J ≤ 85°C, I_{REV} is current into CCx pin.		5	10	
CC1/CC2 – CONNECT MANAGEMENT – V_{CONN} DISCHARGE MODE						
	Discharge resistance (TPS25820)	CC pin that was providing V_{CONN} before detach: V_{CCX} = 4 V	400	500	600	Ω
V_{TH}	Falling threshold for discharged (TPS25820)	CC pin that was providing V_{CONN} before detach	570	600	630	mV
	Discharged threshold hysteresis (TPS25820)			100		mV
$\overline{SINK}$, $\overline{POL}$						
V_{OL}	Output low voltage	I_{SNK_PIN} = 1 mA			250	mV
I_{OFF}	Off-state leakage	V_{PIN} = 5.5 V			1	µA
EN, CHG - LOGIC INPUTS						
V_{TH}	Rising threshold voltage for output logic change			1.45	1.8	V
V_{TH}	Falling threshold voltage for output logic change		1.00	1.35		V
	Hysteresis(2)			100		mV
I_{IN}	Input current	V_{PIN} = 0 V or 5.5 V	–0.5		0.5	µA
OVER TEMPERATURE SHUT DOWN						
T_{TH_OTSD2}	Rising threshold temperature for device shutdown		155			°C
	Hysteresis(2)			20		°C
T_{TH_OTSD1}	Rising threshold temperature for OUT/ V_{CONN} switch shutdown in current limit		135			°C
	Hysteresis(2)			20		°C
IN						
V_{TH}	Rising threshold voltage for not UVLO		3.9	4.1	4.3	V
	Hysteresis(2)			100		mV

(2) These parameters are provided for reference only and do not constitute part of TI's published specifications for purposes of TI's product warranty.

Electrical Characteristics (continued)

–40°C ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN} ≤ 5.5 V, V_{EN} = V_{CHG} = V_{IN}, R_{REF} = 100 kΩ. Typical values are at 25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated pin (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Disabled supply current	V_{EN} = 0 V, –40°C ≤ T_J ≤ 85°C			1	µA
	Enabled supply current with CC lines open	–40°C ≤ T_J ≤ 85°C		1	4	
	Enabled supply current with dangling Ra cable attached			150	195	
	Enabled supply current with Sink attached via cable that is electronically marked (includes IN current that provides the CC output current to the sink Rd resistor)	V_{CHG} = 0 V		232	275	
				332	380	
	Enabled supply current with Sink attached via cable that is not electronically marked (includes IN current that provides the CC output current to the sink Rd resistor)	V_{CHG} = 0 V		210	250	
				310	355	

6.6 Switching Characteristics

–40°C ≤ T_J ≤ 125°C, 4.5 V ≤ V_{IN} ≤ 5.5 V, V_{EN} = V_{CHG} = V_{IN}, R_{REF} = 100 kΩ. Typical values are at 25°C. All voltages are with respect to GND. I_{OUT} and I_{OS} defined positive out of the indicated pin (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUT - POWER SWITCH						
t_r	Output voltage rise time	V_{IN} = 5 V, C_L = 1 µF, R_L = 100 Ω (measure between 10% and 90% of final value)	0.5	0.8	1.2	ms
t_f	Output voltage fall time		0.2	0.3	0.4	ms
t_{on}	Output voltage turn-on time	V_{IN} = 5 V, C_L = 1 µF, R_L = 100 Ω	2.1	3.2	4.5	ms
t_{off}	Output voltage turn-off time		0.8	1.3	1.9	ms
$t_{w\_OUT\_DCHG}$	R_{DCHG} application time at OUT turn off	V_{OUT} = 1 V, time I_{SNK_OUT} > 1 mA after Sink termination removed from CC lines	169	262	361	ms
OUT - CURRENT LIMIT						
t_{iOS}	Current limit response time to short circuit	V_{IN} - V_{OUT} = 1 V, R_L = 10 mΩ (see 图 1)		1.5	4	µs
$\overline{FAULT}$						
t_{DEGA}	Asserting deglitch due to overcurrent		5.6	8.2	10.6	ms
t_{DEGA}	Asserting deglitch due to overtemperature in current limit			0		ms
t_{DEGD}	De-asserting deglitch		5.6	8.2	10.6	ms
CC1/CC2 - V_{CONN} POWER SWITCH (TPS25820)						
t_r	Output voltage rise time	V_{IN2} = 5 V, C_L = 1 µF, R_L = 100 Ω	0.13	0.22	0.3	ms
t_f	Output voltage fall time		0.18	0.22	0.26	ms
t_{on}	Output voltage turn-on time	V_{IN2} = 5 V, C_L = 1 µF, R_L = 100 Ω	1.4	2.2	3.2	ms
t_{off}	Output voltage turn-off time		0.25	0.33	0.4	ms
	Minimum VCONN discharge time	TPS25820	42	65	90	ms
CC1/CC2 - V_{CONN} POWER SWITCH - CURRENT LIMIT (TPS25820)						
t_{res}	Current limit response time to short circuit	V_{IN} – V_{CCx} = 1 V, R = 10 mΩ (see 图 1)		1	4	µs
$\overline{SINK}$, $\overline{POL}$						
t_{DEGA}	Asserting deglitch		100	150	200	ms
t_{DEGD}	De-asserting deglitch		7.9	12.5	17.7	ms

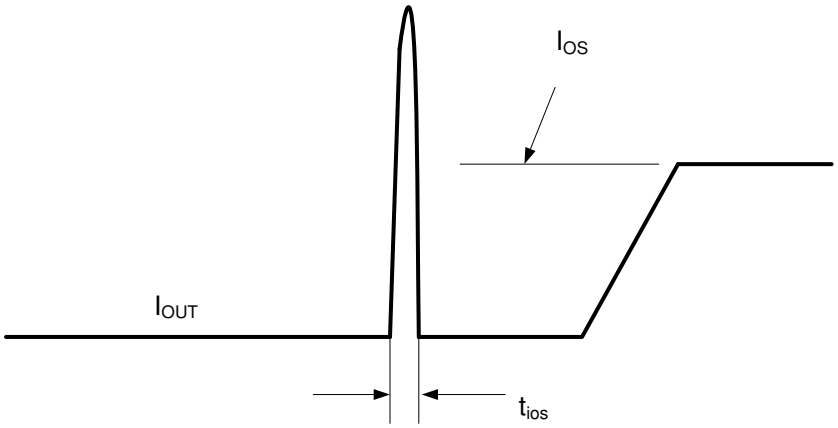


图 1. Output Short Circuit Parameter Diagram

6.7 Typical Characteristics

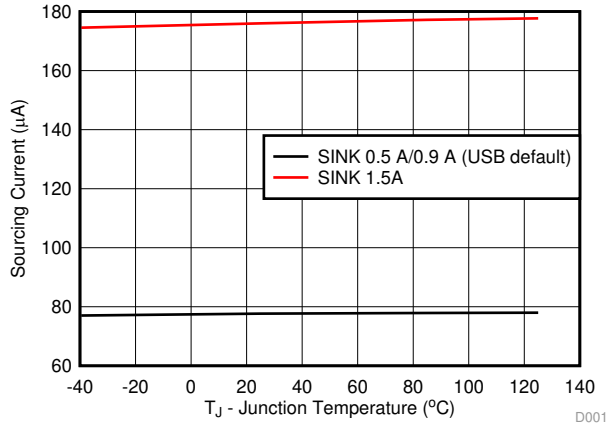


图 2. CC Sourcing Current to SINK vs Temperature

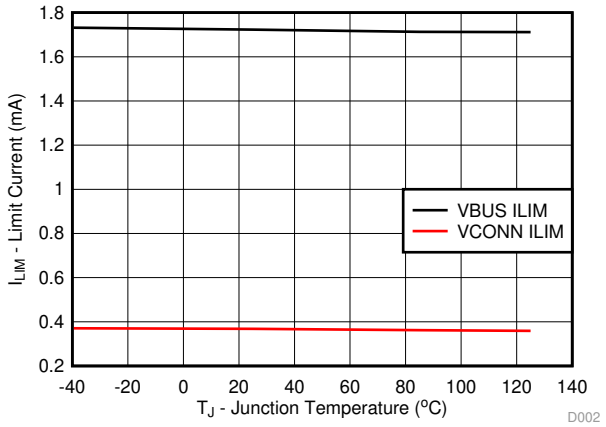
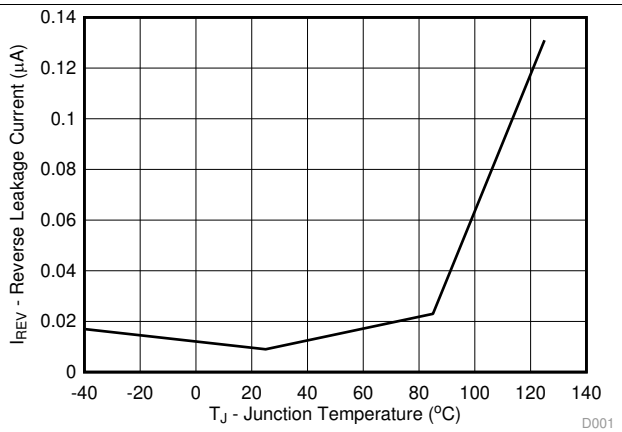


图 3. ILIM for VBUS and VCONN vs Temperature



Device = Disabled; (VOUT-VIN) =6.5V

图 4. OUT Reverse Leakage Current vs Temperature

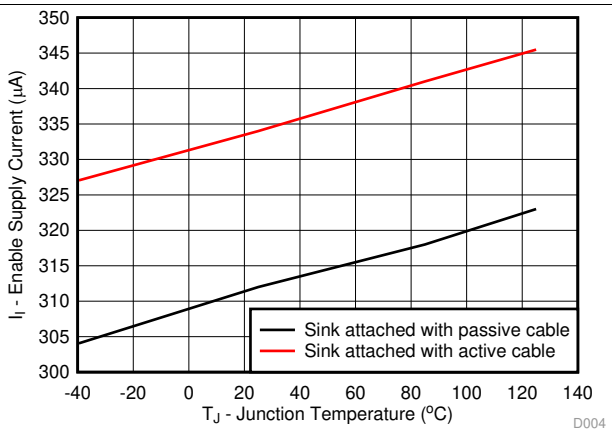


图 5. Supply Current with SINK vs Temperature

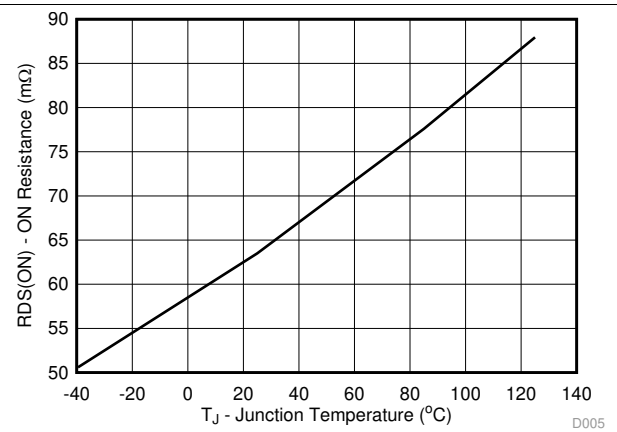


图 6. VBUS Current Limiting Switch On Resistance vs Temperature

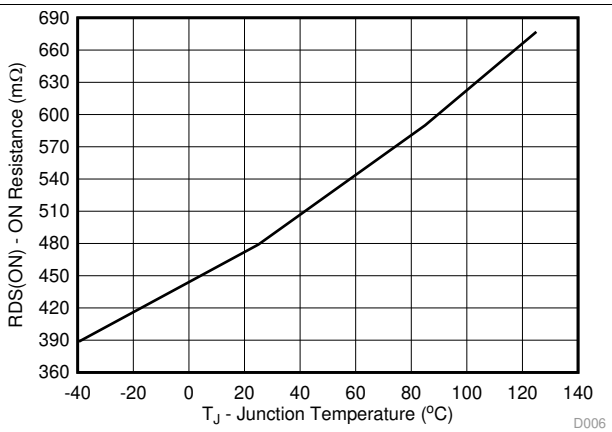


图 7. VCONN Current Limiting Switch On Resistance vs Temperature

7 Detailed Description

7.1 Overview

The TPS25820 and TPS25821 devices are highly integrated USB Type-C source controllers with built-in power switches developed for the USB Type-C connector and cable. The TPS25820 supports VCONN, while the TPS25821 does not. The devices provide all of the functionality needed to support a USB Type-C DFP in a system where USB power delivery (PD) source capabilities (for example, V_{BUS} > 5 V) are not implemented. The devices are designed to be compliant to the USB Type-C specification, release 1.3 which added new requirements to discharge VCONN.

7.1.1 USB Type C Basic

For a detailed description of the Type-C spec refer to the USB-IF website to download the latest released version. Some of the basic concepts of the Type-C spec that pertains to understanding the operation of the TPS25820/21 (a Downward Facing Port, DFP device) are described as follows.

USB Type-C removes the need for different plug and receptacle types for host and device functionality. The Type-C receptacle replaces both Type-A and Type-B receptacles since the Type-C cable is plug-able in either direction between host and device. A host-to-device logical relationship is maintained via the configuration channel (CC). Optionally hosts and devices can be either providers or consumers of power when USB PD communication is used to swap roles.

All USB Type-C ports operate in one of below three data modes:

- Host mode: the port can only be host (also provider of power)
- Device mode: the port can only be device (also consumer of power)
- Dual-Role mode: the port can be either host or device

Port types:

- DFP (Downstream Facing Port): Host, specifically associated with flow of data (Host or Hub) in a USB link
- Source: Port that asserts Rp (pull-up resistor) on CC pin and provides power on VBUS when attached to a Sink (device). At power-up a DFP is a source.
- UFP (Upstream Facing Port): Device, specifically associated with flow of data (device) in a USB link
- Sink: Port that asserts Rd (pull-down) on CC pin and consumes power from VBUS when attached. At power-up a UFP is a sink
- DRP (Dual-Role Port): Host or Device

Valid Source-to-Sink connections:

- 表 1 describes valid Source-to-Sink connections
- Source to Source or Sink to Sink have no function

表 1. Valid Source-to-Sink Connections

POWER ROLES	SOURCE ONLY	SINK ONLY	DUAL ROLE POWER (DRP)
Source Only	Not allowed	Allowed	Allowed
Sink Only	Allowed	Not allowed	Allowed
Dual Role Power (DRP)	Allowed	Allowed	Allowed

7.1.2 Configuration Channel

The function of the configuration channel is to detect connections and configure the interface across the USB Type-C cables and connectors.

Functionally the Configuration Channel (CC) is used to serve the following purposes:

- Detect connect to the USB ports
- Resolve cable orientation and twist connections to establish USB data bus routing
- Establish Source and Sink roles between two connected ports
- Discover and configure power: USB Type-C current modes or USB Power Delivery
- Discovery and configure optional Alternate and Accessory modes

- Enhances flexibility and ease of use

Typical flow of DFP to UFP configuration is shown in 图 8:

图 8. DFP to UFP Connect Flow

7.1.3 Detecting a Connection

Sources and DRPs fulfill the role of detecting a valid connection over USB Type-C. 图 9 shows a Source to Sink connection made with Type-C cable. As shown in 图 9, the detection concept is based on being able to detect terminations in the product which has been attached. A pull-up and pull-down termination model is used. A pull-up termination can be replaced by a current source.

- In the Source-Sink connection the Source monitors both CC pins for a voltage lower than the unterminated voltage.
- A Sink advertises Rd on both its CC pins (CC1 and CC2).
- A powered cable advertises Ra on its V_{CONN} pin.

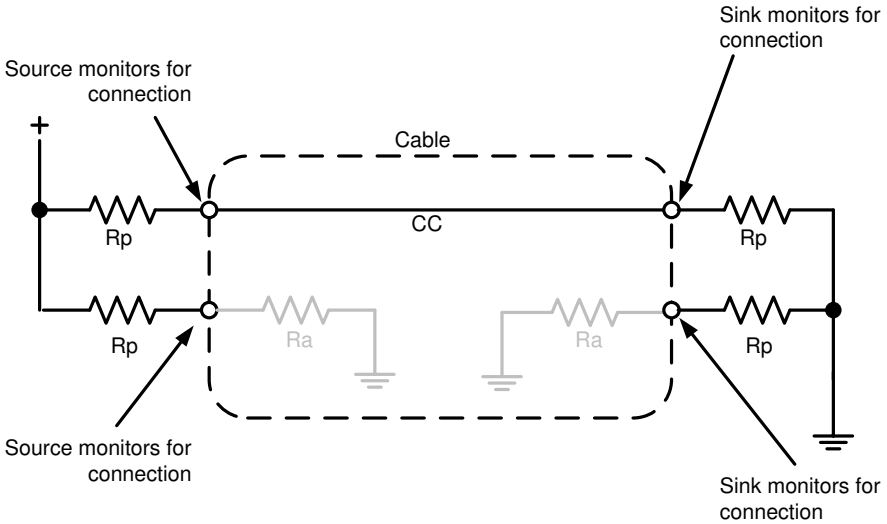


图 9. Source-Sink Connection Mechanism

7.2 Functional Block Diagrams

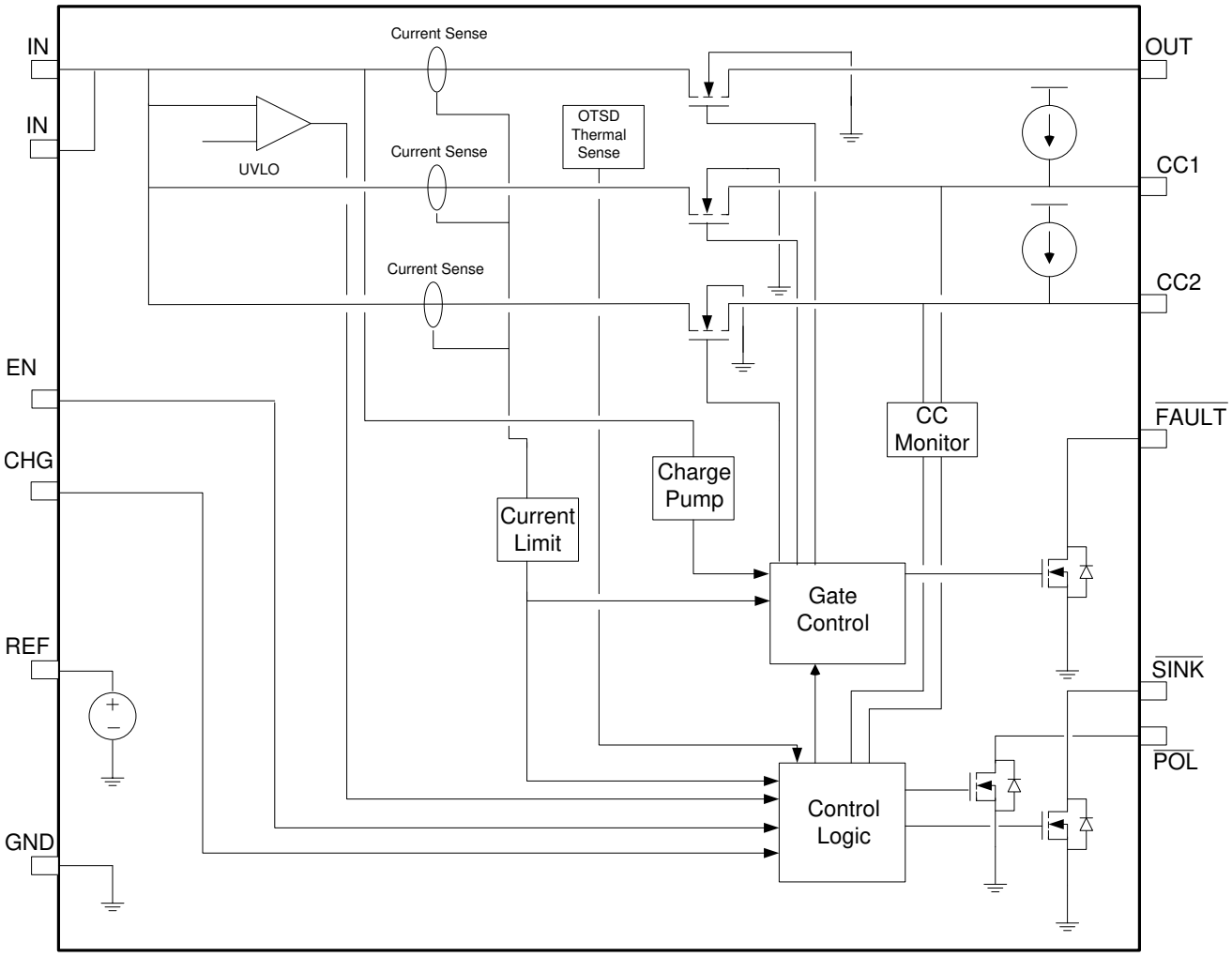


图 10. TPS25820 Functional Block Diagram

Functional Block Diagrams (接下页)

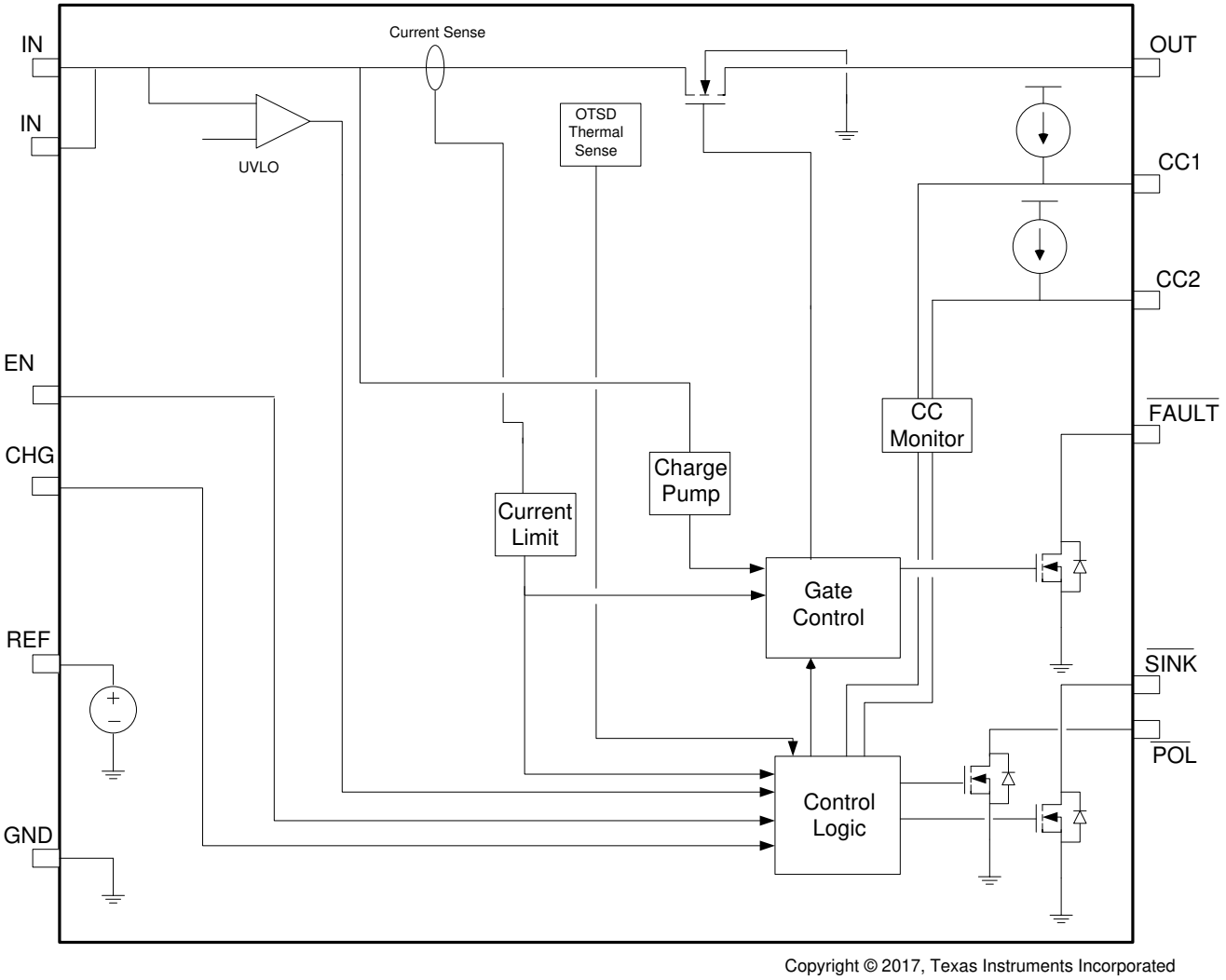


图 11. TPS25821 Functional Block Diagram

7.3 Feature Description

Both the TPS25820 and TPS25821 are source (i.e. DFP) Type-C port controllers with integrated power switches for V_{BUS}. The TPS25820 also has integrated power switches for V_{CONN}. Refer to the functional block diagrams (图 10 and 图 11). The TPS25820/21 devices do not support BC1.2 charging modes, because it does not interact with USB D+ and D– data lines. However supporting DCP mode of BC1.2 can be easily accomplished in data-less ports like wall chargers and CLAs by simply tying a 100-Ω resistor between the D+ and D- pins of the Type-C connector.

The TPS25820 has a built-in V_{CONN} current limiting switch and can be used to implement USB 3.1 DFP, whereas the TPS25821 does not implement a V_{CONN} current limiting switch hence is used in the implementation in USB 2.0 DFP ports or as a USB source only port. Other than the V_{CONN} current limiting switch there are no other functional differences between the TPS25820 and TPS25821.

7.3.1 Configuration Channel Pins CC1 and CC2

The TPS25820/21 devices have two pins, CC1 and CC2 that serve to detect an attachment to the port and resolve cable orientation. These pins are also used to establish the current broadcast to a valid sink and configure V_{CONN} (TPS25820 only).

Feature Description (接下页)

表 2 lists the TPS25820/21 response to various attachments to its port.

表 2. Response to Attachments

TPS25820/21 TYPE-C PORT	CC1	CC2	TPS25820/21 RESPONSE(1)			
			OUT	V_{CONN}(2) On CC1 or CC2	$\overline{POL}$	$\overline{SINK}$
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z
Sink Connected	Rd	OPEN	IN	NO	Hi-Z	LOW
Sink Connected	OPEN	Rd	IN	NO	LOW	LOW
Powered Cable/No Sink Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z
Powered Cable/No Sink Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z
Powered Cable/Sink Connected	Rd	Ra	IN	CC2	Hi-Z	LOW
Powered Cable/Sink Connected	Ra	Rd	IN	CC1	LOW	LOW
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z

(1) $\overline{POL}$ and $\overline{SINK}$ are open drain outputs; pull high with 100 kΩ to IN when used. Tie to GND or leave open when not used.
(2) TPS25820 Only

7.3.2 Current Capability Advertisement and VBUS Overload Protection

The TPS25820/21 supports two Type-C current advertisements as defined by the USB Type-C standard. Current broadcast to a connected Sink is controlled by the CHG pin. For each broadcast level the device protects itself from a Sink that draws current in excess of the port's USB Type-C Current advertisement by setting the current limit as shown in 表 3.

表 3. USB Type-C Current Advertisement

CHG	CC CAPABILITY BROADCAST	CURRENT LIMIT
0	STD (500 mA for USB 2.0 port)	1.67 A
0	STD (900 mA for USB 3.1 port)	1.67 A
1	1.5 A	1.67 A

Under overload conditions, the internal current-limit regulator limits the output current on the OUT pin as shown in the Electrical Characteristics table. When an overload condition is present, the device maintains a constant output current, with the output voltage determined by (I_{OS} x R_{LOAD}). Two possible overload conditions can occur. The first overload condition occurs when either: 1) input voltage is first applied, enable is true, and a short circuit is present (load which draws I_{OUT} > I_{OS}), or 2) input voltage is present and the TPS25820/21 is enabled into a short circuit. The output voltage is held near zero potential with respect to ground and the TPS25820/21 ramps the output current to I_{OS}.

In either case the TPS25820/21 will limit the load current to I_{OS} until the overload condition is removed or the device begins to thermal cycle. This is demonstrated in 图 16 where the device was enabled into a short, and subsequently cycles current off and on as the thermal protection engages.

7.3.3 FAULT Response

The $\overline{FAULT}$ pin is an open drain output that asserts (active low) after a deglitch time (t_{DEGA}) when device OUT current exceeds its programmed value and/or overtemperature threshold is crossed. The $\overline{FAULT}$ signal remains asserted until the fault condition is removed for t_{DEGD}. The TPS25820/21 are designed to eliminate false overcurrent fault reporting by using an internal deglitch circuit.

Connect $\overline{FAULT}$ with a 100-kΩ pull-up resistor to IN. $\overline{FAULT}$ can be left open or tied to GND when not used.

7.3.4 Thermal Shutdown

The device has two internal overtemperature shutdown thresholds, T_{TH_OTSD1} and T_{TH_OTSD2}, to protect the internal FET from damage and overall safety of the system. When the device temperature exceeds T_{TH_OTSD1}, any switch in current limit (OUT switch or VCONN switch) is disabled. The device does auto-retry recovery by re-enabling the switch when die temperature decreases by 20°C. When T_{TH_OTSD2} is exceeded all open drain outputs are left open and the device is disabled such that minimum power/heat is dissipated. The device does auto-retry recovery by attempting to power-up when die temperature decreases by 20°C.

7.3.5 REF

A 100-kΩ resistor is connected from this pin to GND. This pin sets the reference current required to bias the internal circuitry of the device. The overload current limit tolerance and CC currents depend upon the accuracy of this resistor. A ±0.5% low temp CO resistor, or better, yields the best current limit accuracy and overall device performance. If the CC capability broadcast will only be set to STD (CHG pulled low) then up to a ±10% resistor may be used as long as the additional error in the current limit is acceptable.

7.3.6 Plug Polarity Detection

Reversible Type-C plug orientation is reported by the $\overline{\text{POL}}$ pin when a Sink is connected, however when no Sink is attached, $\overline{\text{POL}}$ remains de-asserted irrespective of cable plug orientation. 表 2 describes the $\overline{\text{POL}}$ state based on which device CC pin detects V_{Rd} from an attached Sink pull-down. In a typical USB 3.x DFP port, this pin controls a superspeed data MUX for proper data connectivity irrespective of plug orientation. See 图 20.

7.3.7 Sink Attachment Indicator

The attachment of a Type-C sink is reported by $\overline{\text{SINK}}$. See 表 2.

7.3.8 Device Enable Control

The logic enable pin controls the power switch and device supply current. The supply current is reduced to less than 1 μA when a logic low is present on EN. The EN pin provides a convenient way to turn on or turn off the device while it is powered. When this pin is pulled high, the device is turned on or enabled. When the device is disabled (EN pulled low), the internal FETs tied to IN are disconnected, all open drain outputs are left open (Hi-Z), and the CC1/CC2 monitor block is turned off. The EN pin should not be left floating.

7.3.9 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage droop during turn on.

7.4 Device Functional Modes

The TPS25820/21 is a Type-C controller with integrated power switch that supports all Type-C functions in a downstream facing port (DFP). It is also used to manage current advertisement and protection to a connected sink and active cable. The device starts its operation by monitoring the IN bus. When IN exceeds the undervoltage lockout threshold, the device samples the EN pin. A high level on this pin enables the device and normal operation begins. Having successfully completed its start-up sequence, the device now actively monitors its CC1 and CC2 pins for attachment to a sink. When a sink is detected on either the CC1 or CC2 pin the internal MOSFET starts to turn-on after the required de-bounce time is met. The internal MOSFET starts conducting and allows current to flow from IN to OUT. For the TPS25820 if Ra is detected on the other CC pin (not connected to sink), VCONN is applied to allow current to flow from IN to the CC pin connected to Ra. For a complete listing of various device operational modes refer to 表 2.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS25820/21 are Type-C source controllers. The TPS25820 supports all Type-C DFP required functions to support a USB 3.x port and the TPS25821 supports all required functions for a USB 2.0 DFP. The TPS25820/21 only applies power to V_{BUS} when it detects a sink is attached and removes power when it detects the sink is detached. The device exposes its identity via its CC pin advertising its current capability based on the CHG pin setting. The TPS25820/21 also limits its advertised current internally and provides robust protection against faults on the system V_{BUS} power rail.

After a connection is established by the TPS25820/21, the TPS25820/21 device is capable of providing V_{CONN} to power circuits in the cable plug on the CC pin that is not connected to the CC wire in the cable. V_{CONN} is internally current limited. The TPS25820/21 do not support Type-C optional accessory modes (Ra/Ra and Rd/Rd in 表 2).

The following design procedure can be used to implement a full featured Type-C source.

8.2 Typical Applications

8.2.1 Type-C Source Port Implementation without BC 1.2 Support

图 12 shows a minimal Type-C source implementation capable of supporting 5-V and 1.5-A charging.

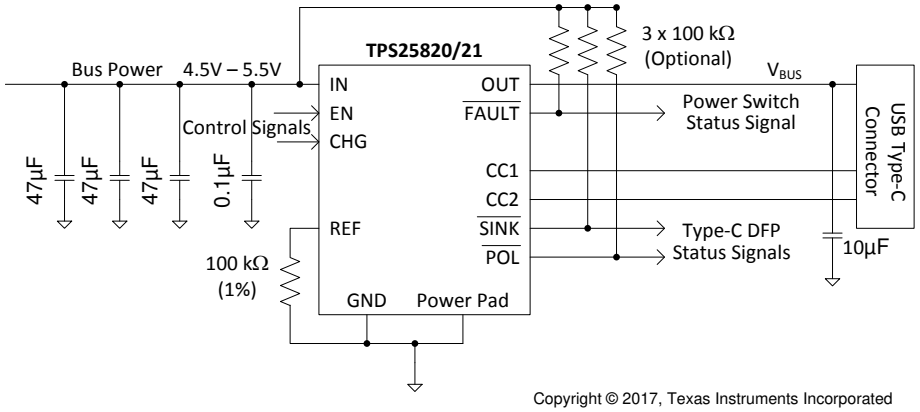


图 12. Type-C Source Port Implementation without BC 1.2 Support

8.2.1.1 Design Requirements

8.2.1.1.1 Input and Output Capacitance Considerations

Input and output capacitance improves the performance of the device. The actual capacitance should be optimized for the particular application. For all applications, a 0.1-µF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling.

All protection circuits, including those of the TPS25820/21 device, have the potential for input voltage overshoots and output voltage undershoots. Input voltage overshoots can be caused by either of two effects. The first cause is an abrupt application of input voltage in conjunction with input power-bus inductance and input capacitance when the IN pin is high-impedance (before OUT turn-on, i.e. not connected to a Type-C sink device). Theoretically, the peak voltage is 2 times the applied voltage. The second cause is due to the abrupt reduction of

Typical Applications (接下页)

output short-circuit current when the device turns off and energy stored in the input inductance drives the input voltage high. Input voltage droops may also occur with large load steps and as the output is shorted. Applications with large input inductance (for instance, connecting the evaluation board to the bench power supply through long cables) may require large input capacitance to prevent the voltage overshoot from exceeding the absolute maximum voltage of the device.

The fast current-limit speed of the TPS25820/21 device to hard output short circuits isolates the input bus from faults. However, ceramic input capacitance in the range of 1 μF to 22 μF adjacent to the input aids in both response time and limiting the transient seen on the input power bus. Output voltage undershoot is caused by the inductance of the output power bus just after a short has occurred and the device has abruptly reduced the OUT current. Energy stored in the inductance drives the OUT voltage down, and potentially negative, as it discharges. An application with large output inductance (such as from a cable) benefits from the use of a high-value output capacitor to control voltage undershoot.

Since the source is considered cold socketed when not attached to a sink, the output capacitance should be placed at the IN pin rather than the OUT pin, which has been commonly used in USB Type-A ports. A 120-μF capacitance is recommended in this situation. It is also recommended to a ceramic capacitor less than 10 μF on the OUT pin for better voltage bypass and compliance to Type-C spec.

8.2.1.1.2 System Level ESD Protection

System-level ESD (per EN61000-4-2) may occur as the result of a cable being plugged in, or a user touching the USB receptacle or cable plug exposed pins. The recommended capacitor on the OUT pin helps reduce the severity of ESD hit on the VBUS path thereby protecting the OUT pin of device. The device has ESD protection built into the CC1 and CC2 pins so that no external protection is necessary as long as proper trace layout guidelines are practiced. Refer to the Layout Guidelines section for external component placement and routing recommendations.

8.2.1.2 Detailed Design Procedure

Design considerations are listed below:

- Place at least 120 μF of bypass capacitance close to the IN pins versus OUT as Type C is a cold socket connector.
- A <10-μF bypass capacitor is recommended placed near Type-C receptacle V_{BUS} pin to handle load transients.
- Depending on the max current level advertisement supported by the Type-C port in the system, set CHG levels accordingly.
- EN and CHG pins can be tied directly to GND or IN without a pull-up resistor.
  - CHG can also be dynamically controlled by a μC to change the current advertisement level to the sink.
- When an open drain output of the TPS25820 is not used, it can be left as NC or tied to GND or when used, pulled up to IN supply via a 100-kΩ resistor.
- Connect a 0.5% 100-kΩ resistor between the REF and GND pins placing it close to the device pin and isolated from switching noise on the board.

Typical Applications (接下页)

8.2.1.3 Application Curves

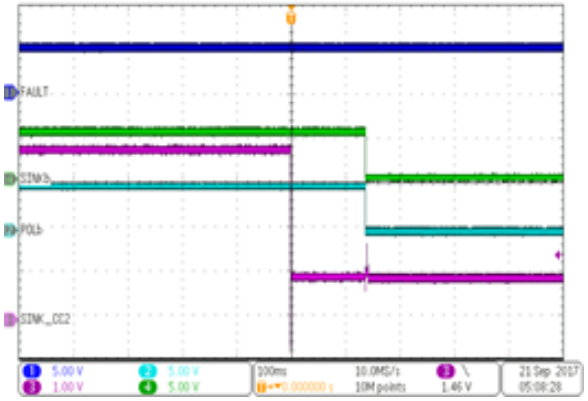


图 13. Sink Attach Event

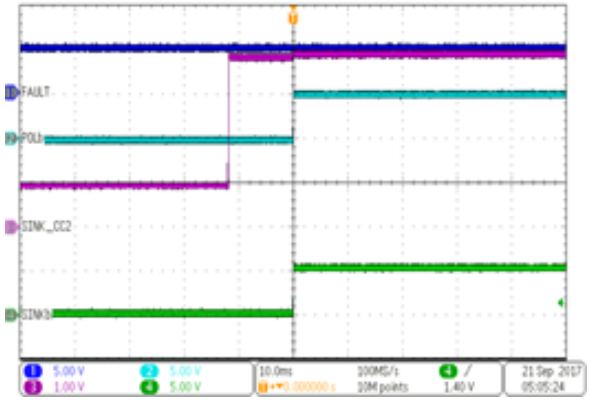
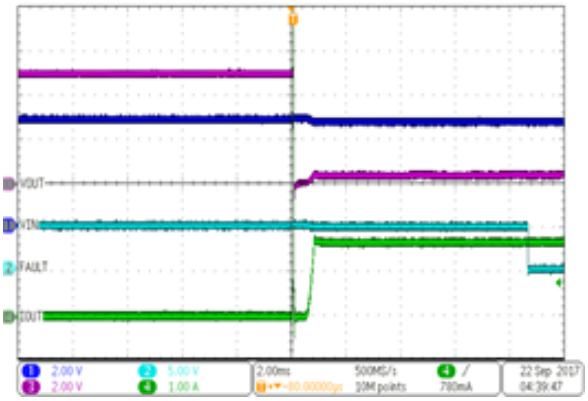


图 14. Sink Detach Event



C_{OUT} = 6.8 µF, Short Output, IN=EN=5V, CC1=Rd, CC2 open

图 15. Out Short Event

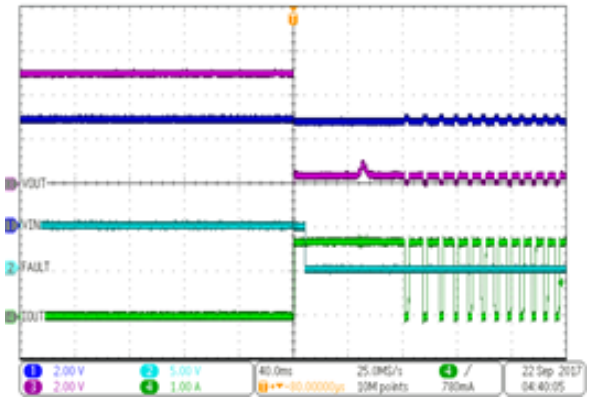


图 16. Extended Period OUT Short Event

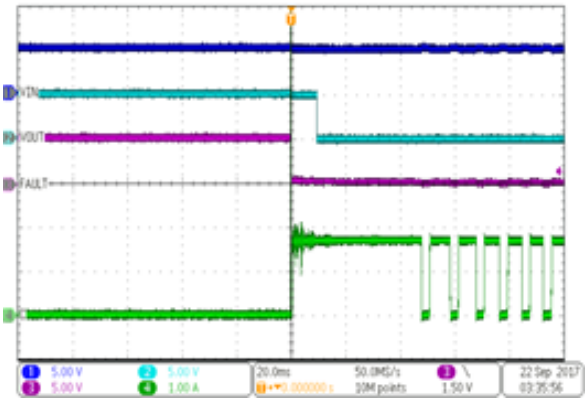
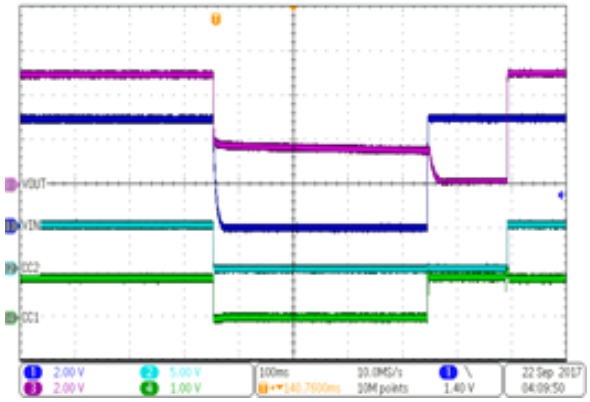


图 17. Screw Driver Short on VBUS



V_{IN}: 5V ≥ 0V - 5V;1V/ms,365 ms wait,CC1 = Rd,CC2 = open

图 18. Brownout Test

Typical Applications (接下页)

8.2.2 Type -C Source Port Implementation with BC 1.2 (DCP Mode) Support

BC1.2 charging is not supported in the TPS25820/21, however adding BC1.2 DCP (Dedicated Charging Port) support with the TPS25820/21 can be done by having the D+ and D- shorted together with a maximum impedance of 200 Ω between them and left floating with respect to ground. This is shown in 图 19. However with DCP implementation the port will not support any data transfer, but is capable of advertising charge currents up to 1.5 A to a legacy device that is connected using a Type-C to Type-A or Micro-B cable. This type of port allows for wall chargers and car chargers with high-charge capability without the need for enumeration. 图 19 shows a Type-C source implementation capable of supporting 5-V and 1.5-A charging in a Type-C port that is also able to support charging of legacy devices when used with a Type-C - μB cable assembly.

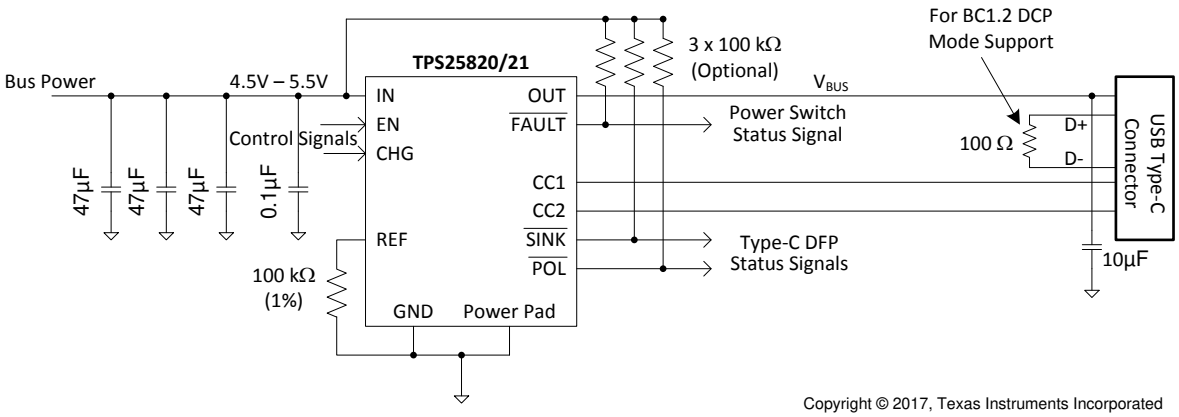


图 19. Type-C Source Port Implementation with BC 1.2 (DCP Mode) Support

8.2.2.1 Design Requirements

Refer to *Design Requirements* for the Design Requirements.

8.2.2.2 Detailed Design Procedure

Refer to *Detailed Design Procedure* for the Detailed Design Procedure.

8.2.2.3 Application Curves

Refer to *Application Curves* for the Application Curves.

8.2.3 Implementing a USB 3.1 Type-C Charging Port with the TPS25820

图 20 shows a conceptual implementation of USB 3.1 capable Type-C DFP, used in notebook, desktop, LCD monitor or dock application where both USB data and charging is supported. USB 2.0 data lines are connected directly to Type-C receptacle while USB 3.1 data is connected through a USB 3.1 MUX. The TPS25820 controls the USB 3.1 MUX via its $\overline{\text{POL}}$ pin. In this implementation if the USB host/hub is capable of supporting BC1.2 charging then it is possible to support both BC1.2 and Type-C charging from the same Type-C port.

Typical Applications (接下页)

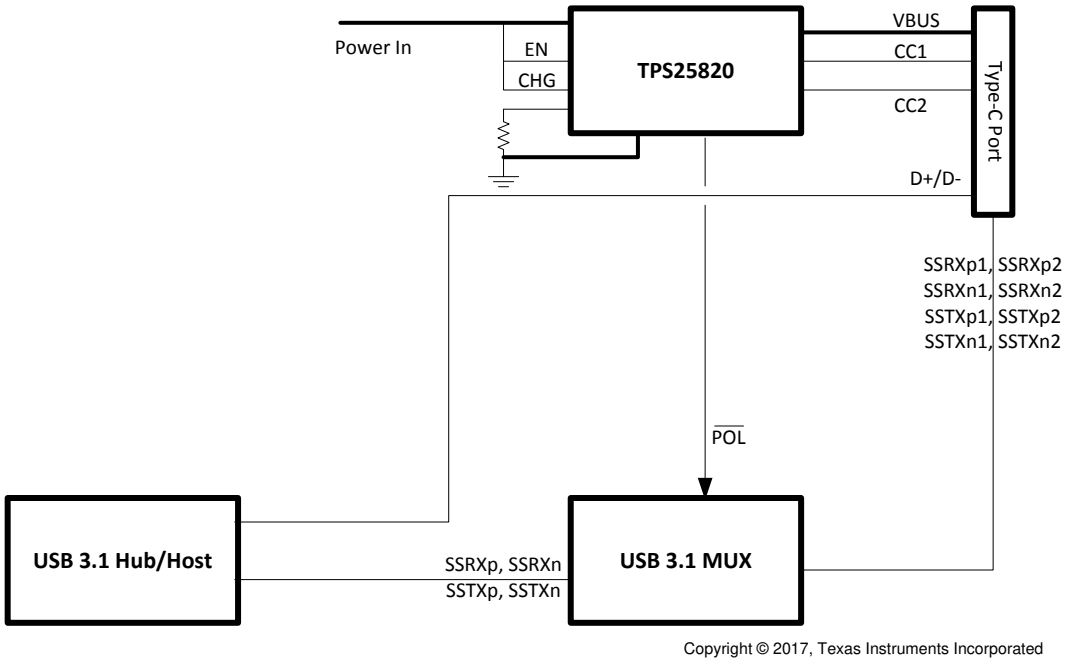


图 20. USB 3.1 Type-C Charging Port

8.2.3.1 Design Requirements

Refer to *Design Requirements* for the Design Requirements.

8.2.3.2 Detailed Design Procedure

Refer to *Detailed Design Procedure* for the Detailed Design Procedure.

8.2.3.3 Application Curves

Refer to *Application Curves* for the Application Curves.

8.2.4 Implementing TPS25821 in USB Car Chargers

Given its small footprint, highly integrated design and ultralow standby current, the TPS25821 is ideal for use in cigarette lighter adapter (CLA) USB car chargers capable of supporting Type-C 1.5-A and BC1.2 DCP charging from same Type-C port. This makes it suitable for fast charging phones with either µB or Type-C connector. 图 21 shows such an implementation for a two port CLA design. The LMS3635 was chosen for its wide VIN and high efficiency to allow for the compact design needed in a CLA body.

Typical Applications (接下页)

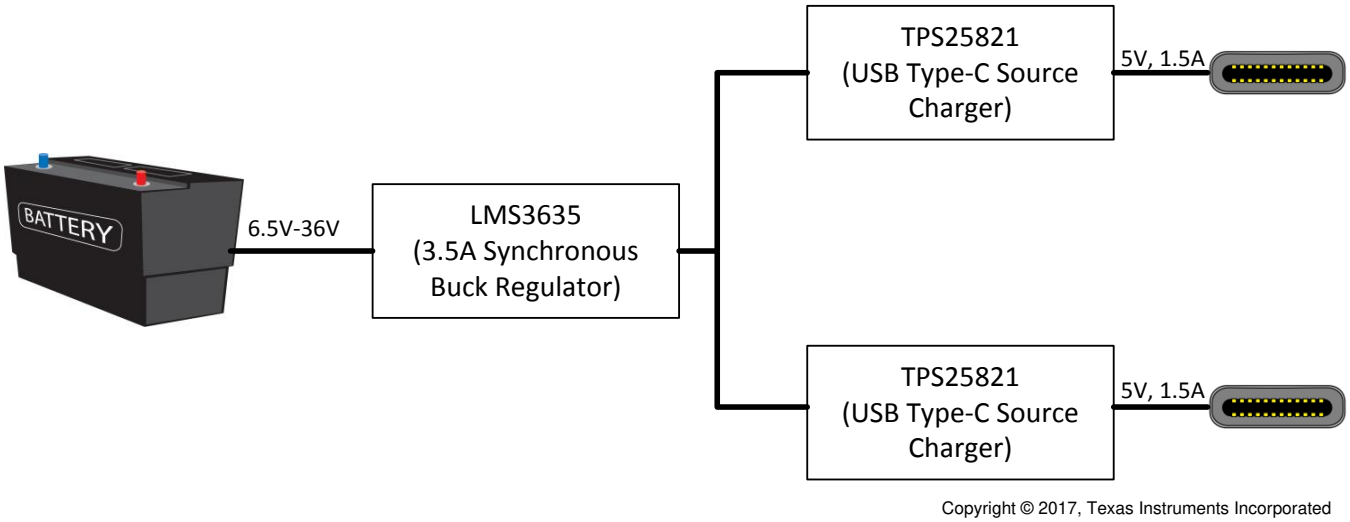


图 21. USB Car Charger

8.2.4.1 Design Requirements

Refer to *Design Requirements* for the Design Requirements.

8.2.4.2 Detailed Design Procedure

Refer to *Detailed Design Procedure* for the Detailed Design Procedure.

8.2.4.3 Application Curves

Refer to *Application Curves* for the Application Curves.

9 Power Supply Recommendations

The device has one power supply input, IN, which is the chip supply. It is connected to the OUT pin via a power integrated MOSFET and in the case of the TPS25820 it also is MUXed either to CC1 or CC2 pin in the Type-C receptacle depending on cable plug polarity.

USB Specification Revision 2.0 and 3.1 requires VBUS voltage at the connector be between 4.75 V to 5.5 V. Depending on layout and routing from supply to the connector, the voltage droop on VBUS has to be tightly controlled especially when providing 1.5 A. Locate the input supply close to the device. For all applications, a ceramic bypass capacitor between OUT and GND less than 10 μF is recommended and should be placed as close to the Type-C connector and device as possible for local noise decoupling. The power supply should be rated higher than the current limit set to avoid voltage droops during overcurrent and short-circuit conditions. Also see *Input and Output Capacitance Considerations* on chip by-passing considerations.

10 Layout

10.1 Layout Guidelines

Layout best practices as it applies to the TPS25820/21 are listed below.

- For all applications a ceramic capacitor less than 10 µF is recommended near the Type-C receptacle and another 120-µF ceramic capacitor placed close to the IN pin.
  - The optimum placement of the 120-µF capacitor is closest to the IN and GND pins of the device.
  - Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN pin, and the GND pin of the IC. See 图 22 for a PCB layout example.
- High current carrying power path connections to the device should be as short as possible and should be sized to carry at least twice the full-load current.
  - Have the input and output traces as short as possible. The most common cause of voltage drop failure in USB power delivery is the resistance associated with the VBUS trace. Trace length, maximum current being supplied for normal operation, and total resistance associated with the VBUS trace must be taken into account while budgeting for voltage drop.
  - For example, a power carrying trace that supplies 1.5 A, at a distance of 20 inches, 0.100-in. wide, with 2-oz. copper on the outer layer will have a total resistance of approximately 0.046 Ω and voltage drop of 0.07 V. The same trace at 0.050-in.-wide will have a total resistance of approximately 0.09 Ω and voltage drop of 0.14 V.
  - Make power traces as wide as possible.
- The resistor attached to the REF pin of the device has several requirements:
  - It is recommended to use a 0.5% 100-kΩ resistor.
  - It should be connected to pins REF and GND.
  - The trace routing between the REF and GND pins of the device should be as short as possible to reduce parasitic effects on the current limit and current advertisement accuracy. These traces should not have any coupling to switching signals on the board.
- Locate all TPS25820/21 pull-up resistors for open-drain outputs close to their connection pin. Pull-up resistors should be 100 kΩ.
  - When a particular open drain output is not used/needed in the system leave the associated pin open or tied to GND.
- Keep the CC lines close to the same length.
- Thermal Considerations:
  - When properly mounted, the thermal pad package provides significantly greater cooling ability than an ordinary package. To operate at rated power, the thermal pad must be soldered to the board GND plane directly under the device. The thermal pad is at GND potential and can be connected using multiple vias to inner layer GND. Other planes, such as the bottom side of the circuit board can be used to increase heat sinking in higher current applications. Refer to Technical Briefs: *PowerPad™ Thermally Enhanced Package* (TI literature Number SLMA002) and *PowerPAD™ Made Easy* (TI Literature Number SLMA004) or more information on using this thermal pad package.
  - The thermal via land pattern specific to the TPS25820/21 can be downloaded from the device web page at www.ti.com.
  - Obtaining acceptable performance with alternate layout schemes is possible; however the layout example in the following section has been shown to produce good results and is intended as a guideline.

10.2 Layout Example

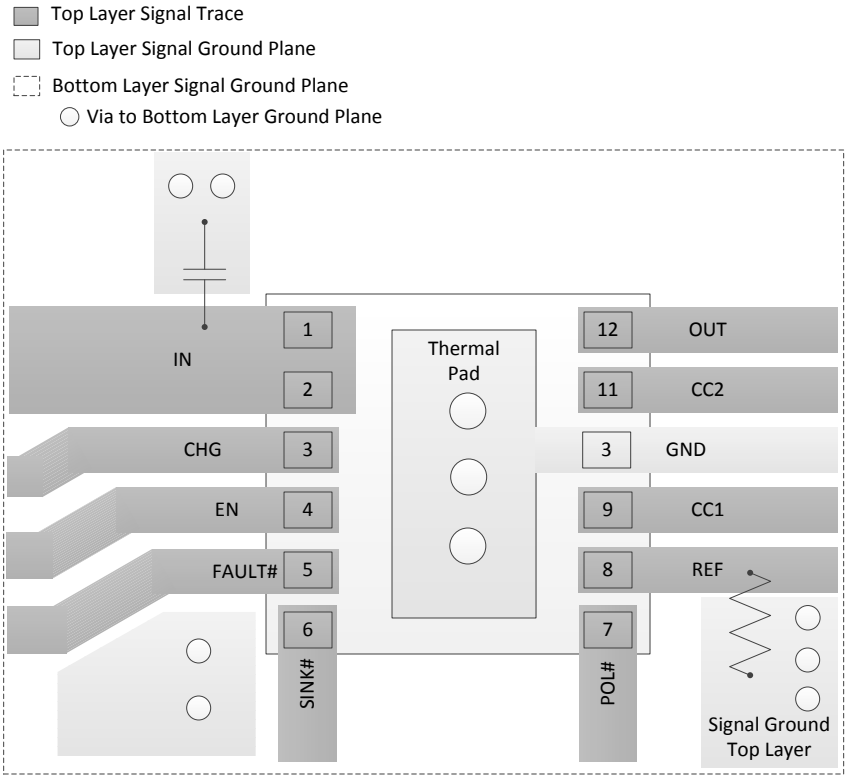


图 22. Layout Example

11 器件和文档支持

11.1 器件支持

11.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

- 《*PowerPad™ 耐热增强型封装*》（TI 文献编号：SLMA002）
- 《*PowerPAD™ 速成*》（TI 文献编号：SLMA004）
- 《*TPS25810EVM-745 用户指南*》（文献编号：SLVUA0）
- 《*TPS25810 高压 DFP 保护*》（文献编号：SLVA751）

11.3 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **4.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
TPS25820	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS25821	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.4 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.5 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 商标

E2E is a trademark of Texas Instruments.

11.7 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS25820DSSR	ACTIVE	WSON	DSS	12	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25820	Samples
TPS25820DSST	ACTIVE	WSON	DSS	12	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25820	Samples
TPS25821DSSR	ACTIVE	WSON	DSS	12	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25821	Samples
TPS25821DSST	ACTIVE	WSON	DSS	12	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25821	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

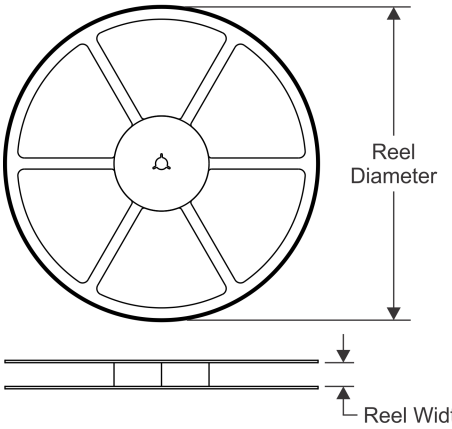
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

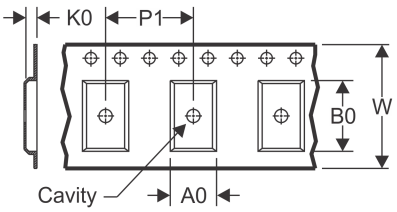
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

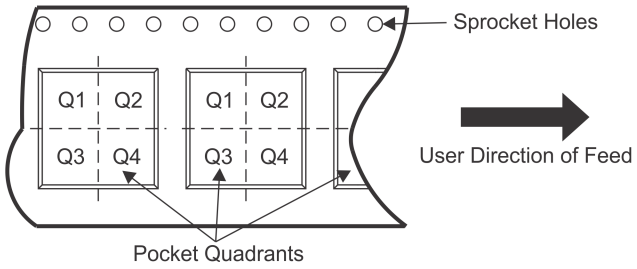


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

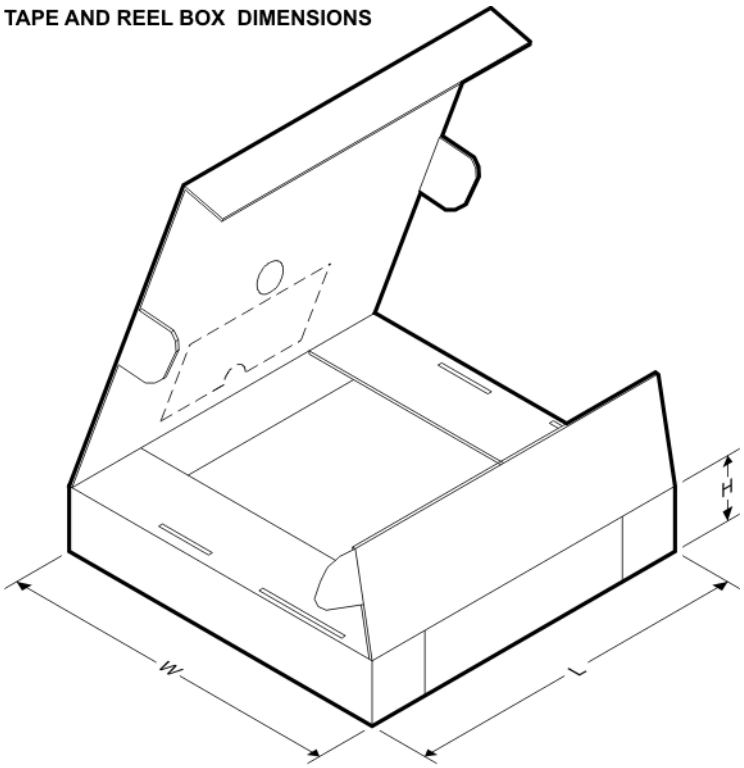
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25820DSSR	WSON	DSS	12	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS25820DSST	WSON	DSS	12	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS25821DSSR	WSON	DSS	12	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS25821DSST	WSON	DSS	12	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



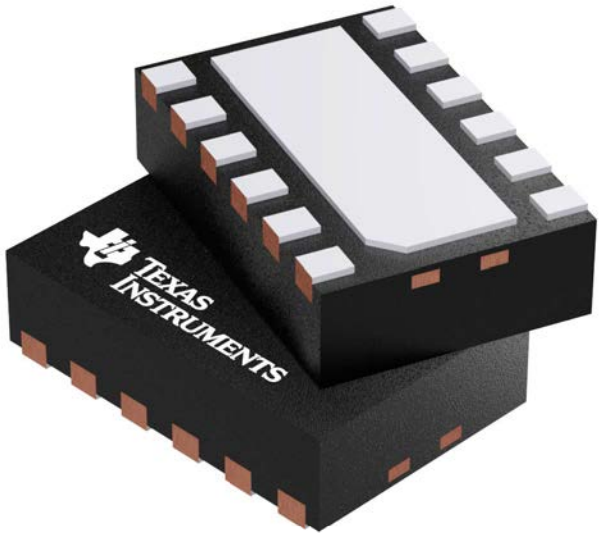
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25820DSSR	WSON	DSS	12	3000	210.0	185.0	35.0
TPS25820DSST	WSON	DSS	12	250	210.0	185.0	35.0
TPS25821DSSR	WSON	DSS	12	3000	210.0	185.0	35.0
TPS25821DSST	WSON	DSS	12	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DSS 12 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



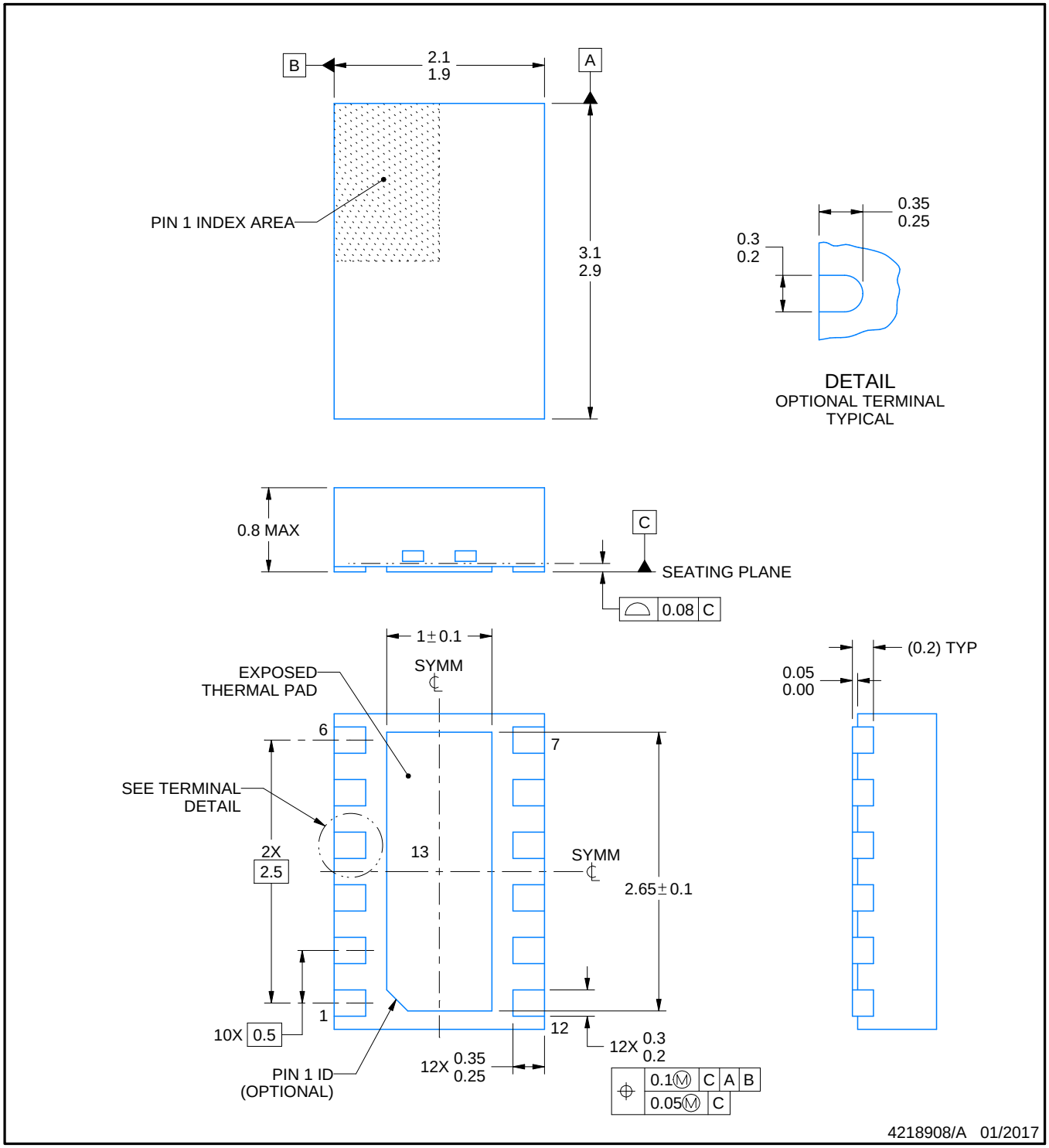
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DSS0012B

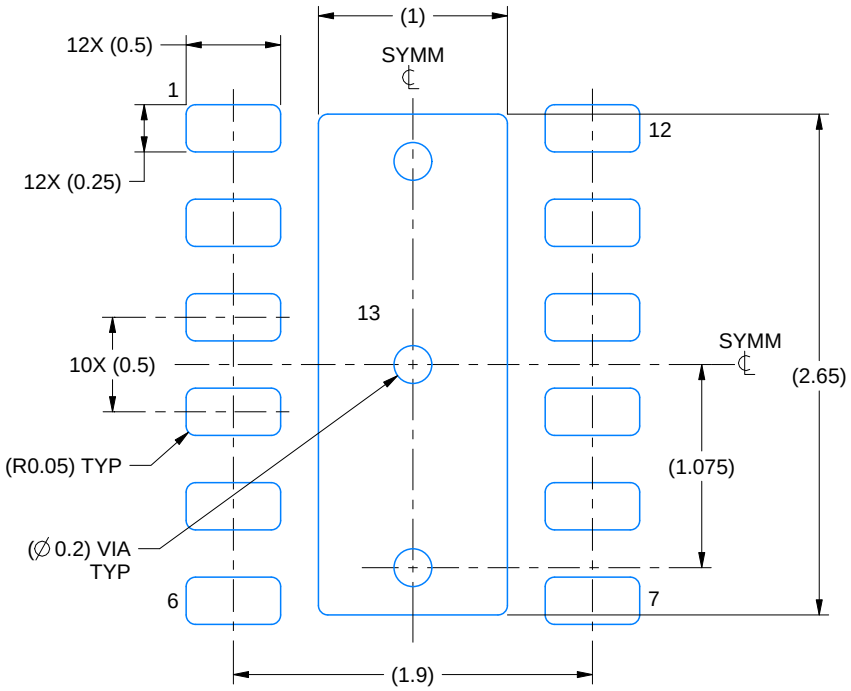
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

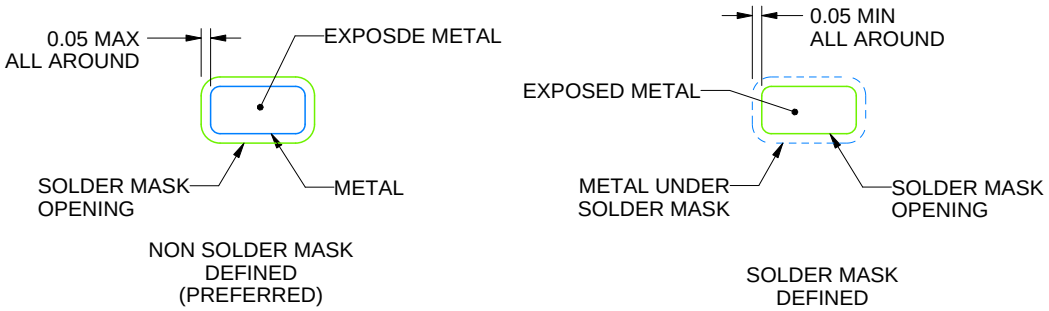


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS

4218908/A 01/2017

NOTES: (continued)

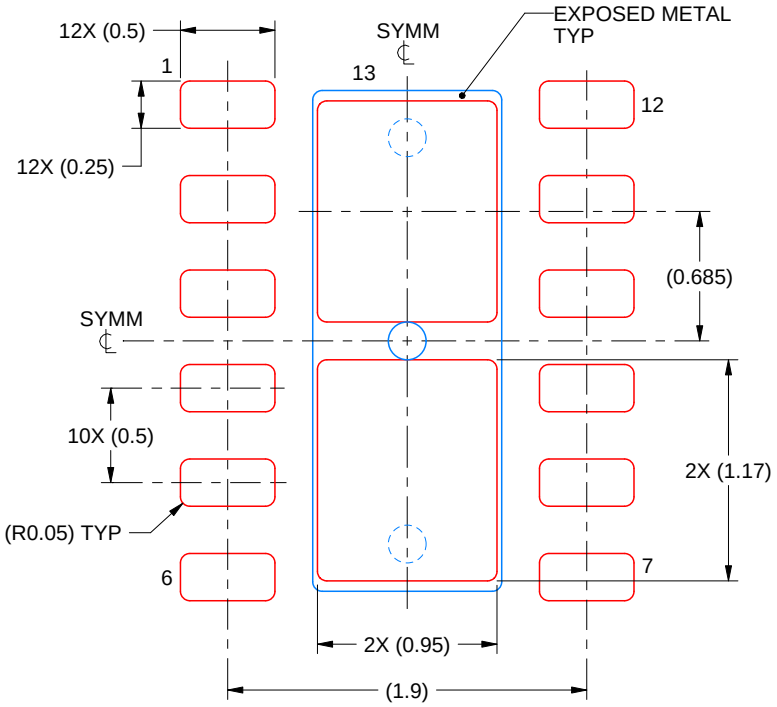
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSS0012B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 13:
83% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218908/A 01/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (https:www.ti.com.cn/zh-cn/legal/termsofsale.html) 或 ti.com.cn 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122