TEXAS INSTRUMENTS

AMC1311

ZHCSH46C – DECEMBER 2017 – REVISED JUNE 2022

AMC1311x 高阻抗 2V 输入增强型隔离放大器

1 特性

- 针对隔离式电压测量优化了 2V 高阻抗输入电压范围
- 固定增益：1
- 低直流误差：
  - AMC1311：
    - 失调电压误差：±9.9mV（最大值）
    - 温漂±20μV/°C（典型值）
    - 增益误差：±1%（最大值）
    - 增益漂移：±30ppm/°C（典型值）
  - AMC1311B：
    - 失调电压误差：±1.5mV（最大值）
    - 温漂±10μV/°C（最大值）
    - 增益误差：±0.2%（最大值）
    - 增益漂移：±40ppm/°C（最大值）
  - 非线性度：0.04%（最大值）
- 高侧 3.3V 工作电压 (AMC1311B)
- 高 CMTI：100kV/μs（最小值）(AMC1311B)
- 高侧电源缺失指示
- 安全相关认证：
  - 符合 DIN EN IEC 60747-17 (VDE 0884-17) 标准的 7000V$_{PK}$ 增强型隔离
  - 符合 UL1577 标准且长达 1 分钟的 5000V$_{RMS}$ 隔离
  - 针对更大工业温度范围进行了全面优化：–40°C 至 +125°C

2 应用

- 可用于以下应用的隔离式电压感应：
  - 电机驱动器
  - 变频器
  - 不间断电源
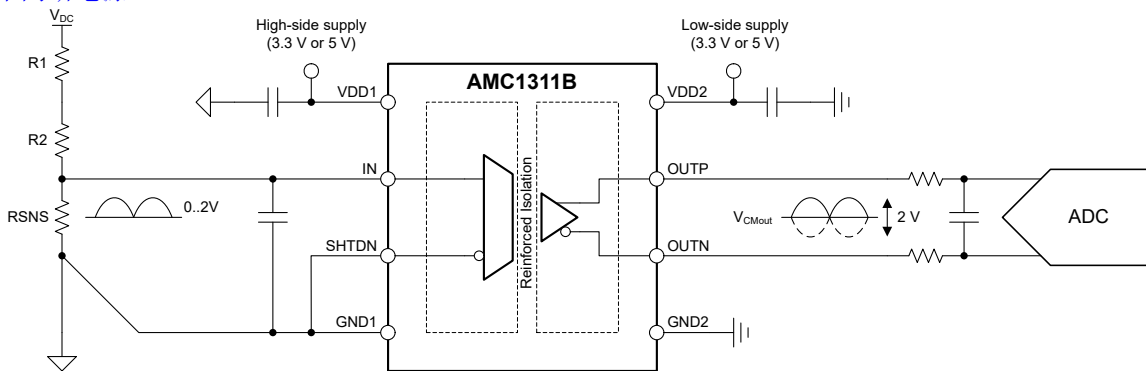
3 说明

AMC1311 是一款隔离式精密放大器，此放大器的输出与输入电路由抗电磁干扰性能极强的电容隔离层隔开。该隔离栅经认证可提供高达 5kV$_{RMS}$ 的增强型电隔离，符合 DIN EN IEC 60747-17 (VDE 0884-17) 和 UL1577 标准，并且可支持高达 1500V$_{RMS}$ 的工作电压。

该隔离层可将系统中以不同共模电压电平运行的各器件隔开，防止高电压冲击导致低压侧器件电气损坏或对操作员造成伤害。

AMC1311 的高阻抗输入针对与高阻抗电阻分压器或任何其他高阻抗电压信号源的连接进行了优化。出色的直流精度和低温漂支持在闭环系统中进行精确的隔离式电压检测和控制。集成的高侧电源电压缺失检测功能可简化系统级设计和诊断。

AMC1311 提供两种性能级别选项：AMC1311B 的额定工业工作温度范围为 –55°C 至 +125°C，AMC1311 为 –40°C 至 +125°C。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
AMC1311	SOIC (8)	5.85mm × 7.50mm
AMC1311B		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化版原理图

English Data Sheet: SBAS786

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (June 2018) to Revision B (May 2020)   **Page**

Product Folder Links: *AMC1311*

5 Device Comparison Table

PARAMETER		AMC1311B	AMC1311
High-side supply voltage, VDD1		3.0 V to 5.5 V	4.5 V to 5.5 V
Specified ambient temperature, T_A		– 55°C to +125°C	– 40°C to +125°C
Input offset voltage, V_{OS}	4.5 V $\leqslant$ VDD1 $\leqslant$ 5.5 V	±1.5 mV	±9.9 mV
	3.0 V $\leqslant$ VDD1 $\leqslant$ 5.5 V	±2.5 mV	Not applicable
Input offset drift, TCV_{OS}		±3 µV/°C (typ), ±10 µV/°C (max)	±20 µV/°C (typ)
Gain error, E_G		±0.2%	±1%
Gain error drift, TCE_G		±5 ppm/°C (typ), ±40 ppm/°C (max)	±30 ppm/°C (typ)
Common-mode transient immunity, CMTI		100 kV/µs (min)	15 kV/µs (min)

6 Pin Configuration and Functions
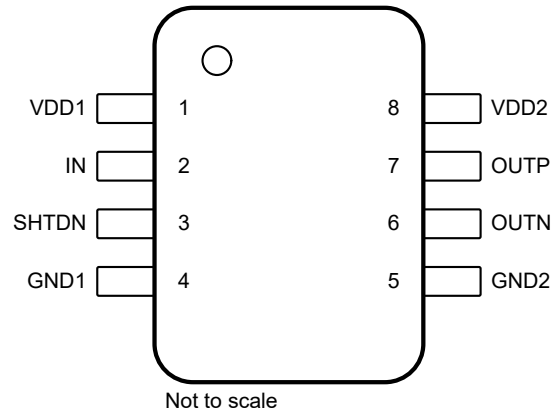
图 6-1. DWV Package, 8-Pin SOIC (Top View)

Not to scale

表 6-1. Pin Functions

| PIN | | TYPE | DESCRIPTION |
NO.	NAME		
1	VDD1	High-side power	High-side power supply[1]
2	IN	Analog input	Analog input
3	SHTDN	Digital input	Shutdown input, active high, with internal pullup resistor (typical value: 100 kΩ)
4	GND1	High-side ground	High-side analog ground
5	GND2	Low-side ground	Low-side analog ground
6	OUTN	Analog output	Inverting analog output
7	OUTP	Analog output	Noninverting analog output
8	VDD2	Low-side power	Low-side power supply[1]

(1)   See the *Power Supply Recommendations* section for power-supply decoupling recommendations.

7 Specifications

7.1 Absolute Maximum Ratings

see[1]

		MIN	MAX	UNIT
Power-supply voltage	High-side VDD1 to GND1	− 0.3	6.5	V
	Low-side VDD2 to GND2	− 0.3	6.5	
Input voltage	IN	GND1 − 6	VDD1 + 0.5	V
	SHTDN	GND1 − 0.5	VDD1 + 0.5	
Output voltage	OUTP, OUTN	GND2 − 0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply pins	− 10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	− 65	150	

(1)   Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±1000	

(1)   JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2)   JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	High-side power supply	VDD1 to GND1, AMC1311	4.5	5	5.5	V
		VDD1 to GND1, AMC1311B	3	5	5.5	
	Low-side power supply	VDD2 to GND2	3	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Input voltage before clipping output	IN to GND1		2.516		V
V_{FSR}	Specified linear full-scale voltage	IN to GND1	− 0.1		2	V
ANALOG OUTPUT						
C_{LOAD}	Capacitive load	On OUTP or OUTN to GND2			500	pF
		OUTP to OUTN			250	
R_{LOAD}	Resistive load	On OUTP or OUTN to GND2		10	1	kΩ
DIGITAL INPUT						
	Input voltage	SHTDN to GND1	0		VDD1	V
TEMPERATURE RANGE						
T_A	Specified ambient temperature	AMC1311	− 40		125	°C
		AMC1311B	− 55		125	

Product Folder Links: *AMC1311*

7.4 Thermal Information

THERMAL METRIC[1]		DWV (SOIC)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	39.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	VDD1 = VDD2 = 5.5 V	98	mW
		VDD1 = VDD2 = 3.6V, AMC1311B only	56	
P_{D1}	Maximum power dissipation (high-side)	VDD1 = 5.5 V	53	mW
		VDD1 = 3.6 V, AMC1311B only	30	
P_{D2}	Maximum power dissipation (low-side)	VDD2 = 5.5 V	45	mW
		VDD2 = 3.6 V, AMC1311B only	26	

7.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance[1]	Shortest pin-to-pin distance through air	⩾ 8.5	mm
CPG	External creepage[1]	Shortest pin-to-pin distance across the package surface	⩾ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	⩾ 0.021	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	⩾ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ⩽ 600 V_{RMS}	I-IV	
		Rated mains voltage ⩽ 1000 V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	2120	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	1500	V_{RMS}
		At DC voltage	2120	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test)	7000	V_{PK}
		$V_{TEST} = 1.2 × V_{IOTM}$, t = 1 s (100% production test)	8400	
V_{IMP}	Maximum impulse voltage[3]	Tested in air, 1.2/50-µs waveform per IEC 62368-1	9800	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[4]	Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	12800	V_{PK}
q_{pd}	Apparent charge[5]	Method a, after input/output safety test subgroups 2 and 3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s	⩽ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10 s	⩽ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1 s	⩽ 5	
C_{IO}	Barrier capacitance, input to output[6]	V_{IO} = 0.5 V_{PP} at 1 MHz	~1.5	pF
R_{IO}	Insulation resistance, input to output[6]	V_{IO} = 500 V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V at 100°C ⩽ T_A ⩽ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 5000 V_{RMS}, t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO} = 6000 V_{RMS}, t = 1 s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.

(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

(3) Testing is carried out in air to determine the surge immunity of the package.

(4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.

(5) Apparent charge is electrical discharge caused by a partial discharge (pd).

(6) All pins on each side of the barrier are tied together, creating a two-pin device.

Product Folder Links: *AMC1311*

7.7 Safety-Related Certifications

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9	Recognized under 1577 component recognition
Reinforced insulation	Single protection
Certificate number: 40040142	File number: E181974

7.8 Safety Limiting Values

Safety limiting[1] intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 84.6°C/W, VDDx = 5.5 V, T_J = 150°C, T_A = 25°C			268	mA
		$R_{\theta JA}$ = 84.6°C/W, VDDx = 3.6 V, T_J = 150°C, T_A = 25°C, AMC1311B only			410	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 84.6°C/W, T_J = 150°C, T_A = 25°C			1477	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.

$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum supply voltage for high-side and low-side.

Product Folder Links: *AMC1311*

7.9 Electrical Characteristics

minimum and maximum specifications of the AMC1311 apply from T_A = – 40°C to +125°C, VDD1 = 4.5 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, V_{IN} = – 0.1 V to 2 V, and SHTDN = GND1 = 0 V; minimum and maximum specifications of the AMC1311B apply from T_A = – 55°C to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, V_{IN} = – 0.1 V to 2 V, and SHTDN = GND1 = 0 V (unless otherwise noted); typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
V_{OS}	Input offset voltage[1] [2]	T_A = 25°C, 4.5 V ⩽ VDD1 ⩽ 5.5 V, AMC1311	– 9.9	±0.4	9.9	mV
		T_A = 25°C, AMC1311B[3]	– 1.5	±0.4	1.5	
TCV_{OS}	Input offset thermal drift[1] [2] [5]	AMC1311		±20		µV/°C
		AMC1311B	– 10	±3	10	
R_{IN}	Input resistance	T_A = 25°C		1		GΩ
I_{IB}	Input bias current	IN = GND1, T_A = 25°C	– 15	3.5	15	nA
C_{IN}	Input capacitance	f_{IN} = 275 kHz		7		pF
ANALOG OUTPUT						
	Nominal gain			1		V/V
E_G	Gain error[1]	T_A = 25°C, AMC1311	– 1%	0.4%	1%	
		T_A = 25°C, AMC1311B	– 0.2%	±0.05%	0.2%	
TCE_G	Gain error drift[1] [6]	AMC1311		±30		ppm/°C
		AMC1311B	– 40	±5	40	
	Nonlineartity[1]		– 0.04%	±0.01%	0.04%	
THD	Total harmonic distortion[4]	V_{IN} = 2 V_{PP}, V_{IN} > 0 V, f_{IN} = 10 kHz, BW = 10 kHz		– 87		dB
SNR	Signal-to-noise ratio	V_{IN} = 2 V_{PP}, f_{IN} = 1 kHz, BW = 10 kHz	79	82.6		dB
		V_{IN} = 2 V_{PP}, f_{IN} = 10 kHz, BW = 100 kHz		70.9		
	Output noise	V_{IN} = GND1, BW = 100 kHz		220		µVrms
PSRR	Power-supply rejection ratio[2]	vs VDD1, at DC		– 80		dB
		vs VDD2, at DC		– 85		
		vs VDD1, 10 kHz / 100-mV ripple		– 65		
		vs VDD2, 10 kHz / 100-mV ripple		– 70		
V_{CMout}	Output common-mode voltage		1.39	1.44	1.49	V
$V_{CLIPout}$	Clipping differential output voltage	V_{OUT} = (V_{OUTP} – V_{OUTN}); V_{IN} > $V_{Clipping}$		2.49		V
$V_{FAILSAFE}$	Failsafe differential output voltage	SHTDN = high, or VDD1 undervoltage, or VDD1 missing		– 2.6	– 2.5	V
BW	Output bandwidth	AMC1311	100	220		kHz
		AMC1311B	220	275		
R_{OUT}	Output resistance	On OUTP or OUTN		<0.2		Ω
	Output short-circuit current	On OUTP or OUTN, sourcing or sinking, IN = GND1, outputs shorted to either GND or VDD2		14		mA
CMTI	Common-mode transient immunity	AMC1311	15	30		kV/µs
		AMC1311B	100	150		

Product Folder Links: *AMC1311*

7.9 Electrical Characteristics (continued)

minimum and maximum specifications of the AMC1311 apply from T_A = ‑40°C to +125°C, VDD1 = 4.5 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, V_{IN} = ‑0.1 V to 2 V, and SHTDN = GND1 = 0 V; minimum and maximum specifications of the AMC1311B apply from T_A = ‑55°C to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, V_{IN} = ‑0.1 V to 2 V, and SHTDN = GND1 = 0 V (unless otherwise noted); typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT						
I_{IN}	Input current	SHTDN pin, GND1 ⩽ SHTDN ⩽ VDD1	‑70		1	µA
C_{IN}	Input capacitance	SHTDN pin		5		pF
V_{IH}	High-level input voltage		0.7 × VDD1			V
V_{IL}	Low-level input voltage				0.3 × VDD1	V
POWER SUPPLY						
$VDD1_{UV}$	VDD1 undervoltage detection threshold	VDD1 rising	2.5	2.7	2.9	V
		VDD1 falling	2.4	2.6	2.8	
$VDD2_{UV}$	VDD2 undervoltage detection threshold	VDD2 rising	2.2	2.45	2.65	V
		VDD2 falling	1.85	2.0	2.2	
I_{DD1}	High-side supply current	3.0 V < VDD1 < 3.6 V, SHTDN = low, AMC1311B only		6.0	8.4	mA
		4.5 V < VDD1 < 5.5 V, SHTDN = low		7.1	9.7	
		SHTDN = VDD1		1.3		µA
I_{DD2}	Low-side supply current	3.0 V < VDD2 < 3.6 V		5.3	7.2	mA
		4.5 V < VDD2 < 5.5 V		5.9	8.1	

(1) The typical value includes one standard deviation (*sigma*) at nominal operating conditions.
(2) This parameter is input referred.
(3) The typical value is at VDD1 = 3.3 V.
(4) THD is the ratio of the rms sum of the amplitudes of first five higher harmonics to the amplitude of the fundamental.
(5) Offset error temperature drift is calculated using the box method, as described by the following equation:
TCV_{OS} = (Value$_{MAX}$ - Value$_{MIN}$) / TempRange
(6) Gain error temperature drift is calculated using the box method, as described by the following equation:
TCE_G (ppm) = (Value$_{MAX}$ - Value$_{MIN}$) / (Value$_{(T=25°C)}$ x TempRange) x 10^6

7.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time			1.3		µs
t_f	Output signal fall time			1.3		µs
	IN to OUTx signal delay (50% – 10%)	Unfiltered output, AMC1311		1.5	2.5	µs
		Unfiltered output, AMC1311B		1.0	1.5	
	IN to OUTx signal delay (50% – 50%)	Unfiltered output, AMC1311		2.1	3.1	µs
		Unfiltered output, AMC1311B		1.6	2.1	
	IN to OUTx signal delay (50% – 90%)	Unfiltered output, AMC1311		3.0	4.0	µs
		Unfiltered output, AMC1311B		2.5	3.0	
t_{AS}	Analog settling time	VDD1 step to 3.0 V with VDD2 $\geqslant$ 3.0 V, to V_{OUTP}, V_{OUTN} valid, 0.1% settling		50	100	µs
t_{EN}	Device enable time	SHTDN high to low		50	100	µs
t_{SHTDN}	Device shutdown time	SHTDN low to high		3	10	µs

7.11 Timing Diagram
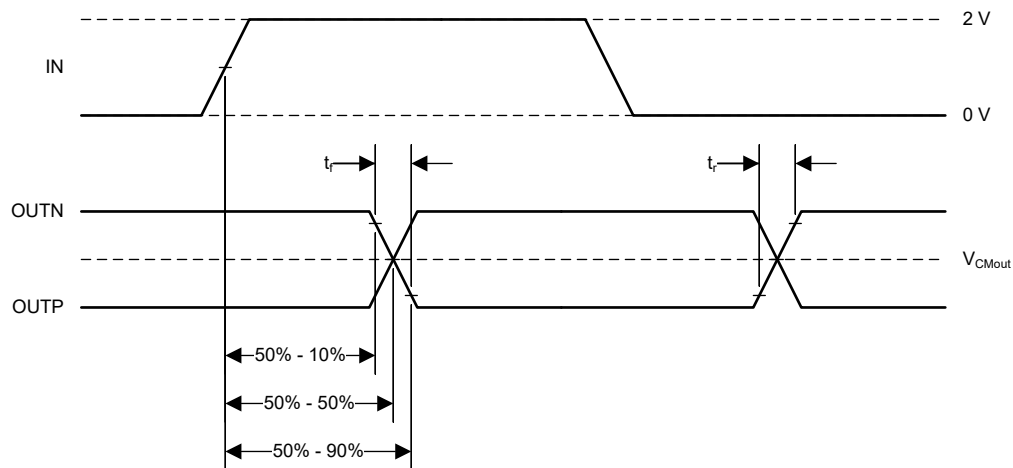
图 **7-1. Rise, Fall, and Delay Time Definition**

Product Folder Links: *AMC1311*

7.12 Insulation Characteristics Curves
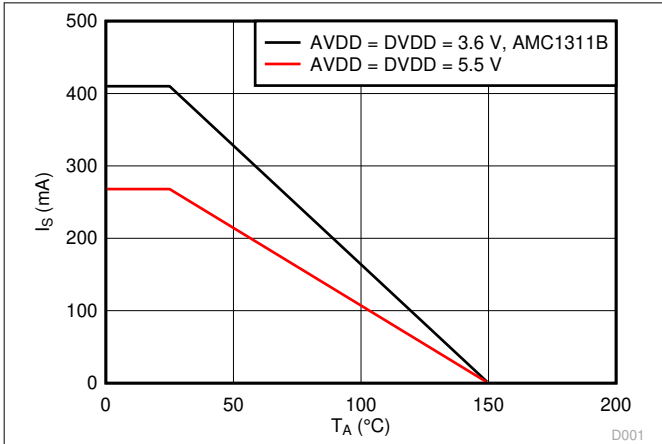
图 **7-2. Thermal Derating Curve for Safety-Limiting Current per VDE**
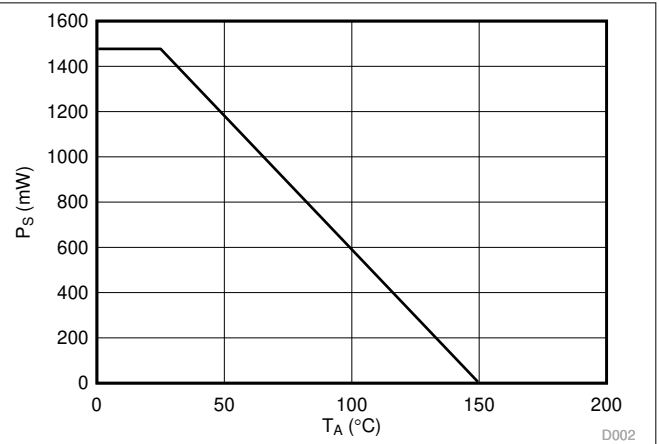
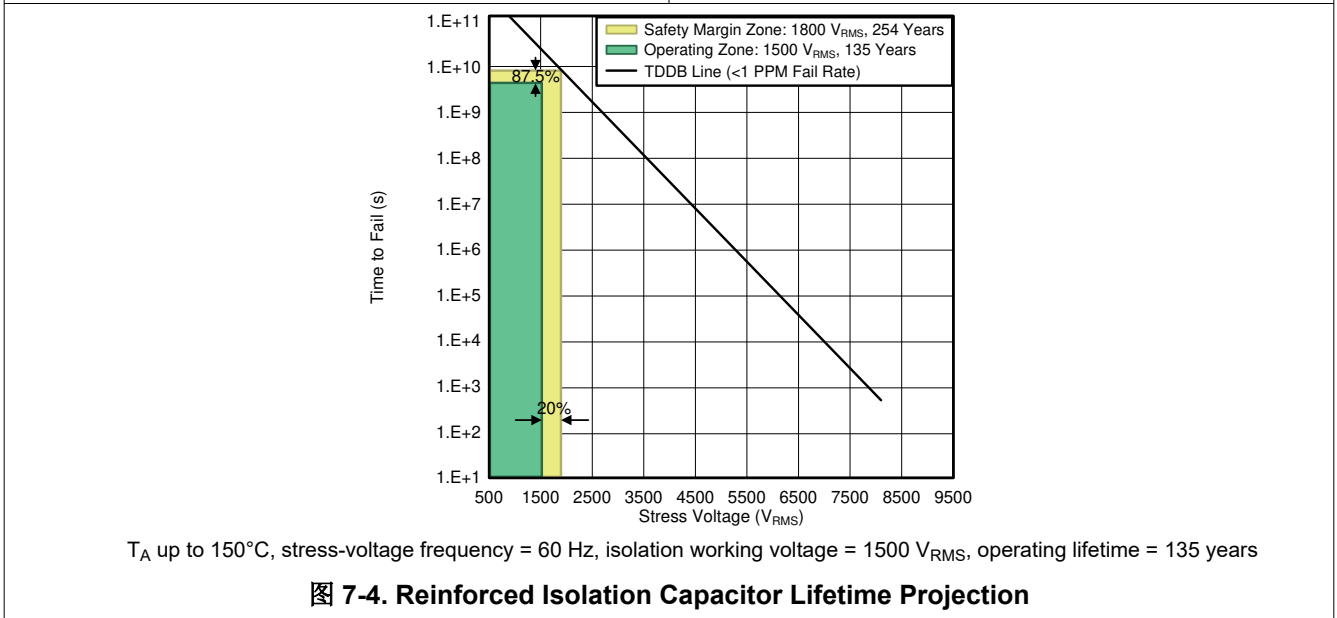图 **7-3. Thermal Derating Curve for Safety-Limiting Power per VDE**

T_A up to 150°C, stress-voltage frequency = 60 Hz, isolation working voltage = 1500 V_{RMS}, operating lifetime = 135 years

图 **7-4. Reinforced Isolation Capacitor Lifetime Projection**

Product Folder Links: *AMC1311*

7.13 Typical Characteristics

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V, f_{IN} = 10 kHz, and BW = 100 kHz (unless otherwise noted)

3.0 V ≤ VDD1 < 4.5 V for the AMC1311B only
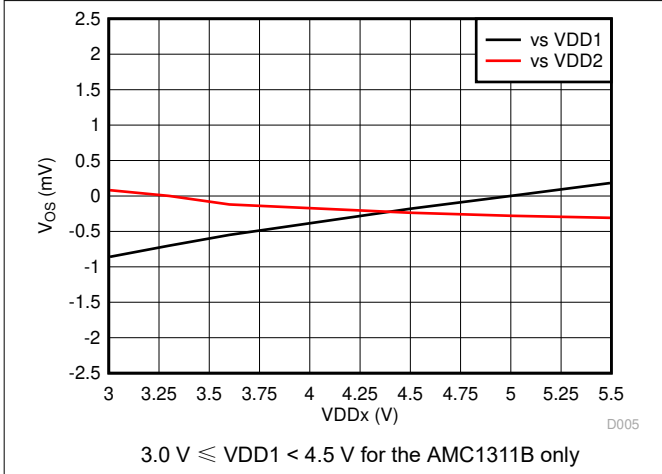
图 7-5. Input Offset Voltage vs Supply Voltage

AMC1311
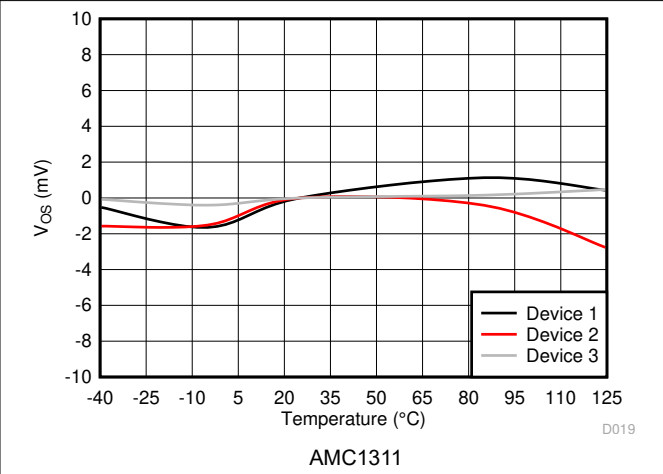
图 7-6. Input Offset Voltage vs Temperature

VDD1 = 5 V, AMC1311B
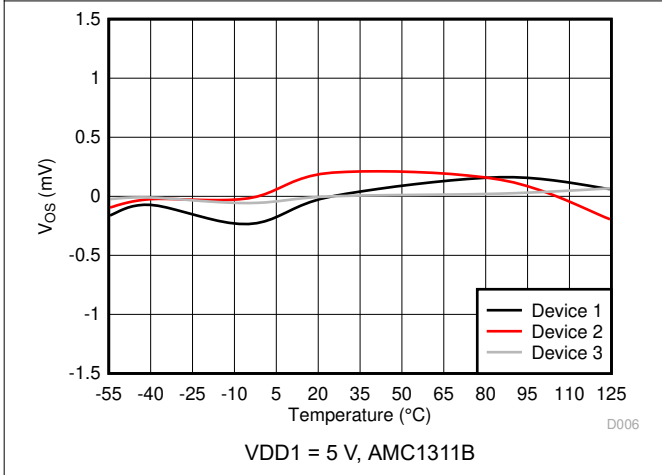
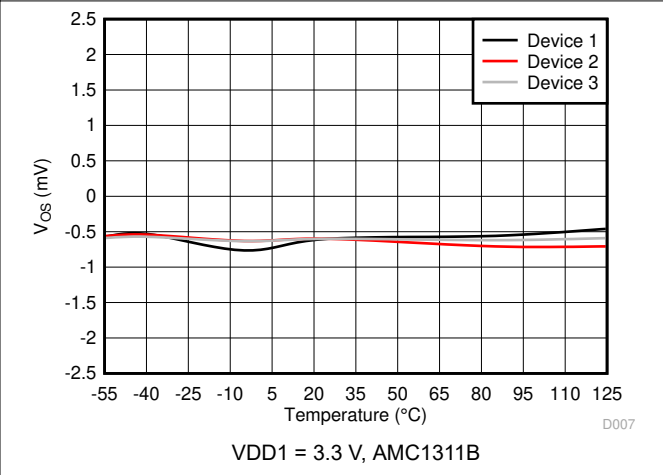**图 7-7. Input Offset Voltage vs Temperature**

VDD1 = 3.3 V, AMC1311B

图 7-8. Input Offset Voltage vs Temperature
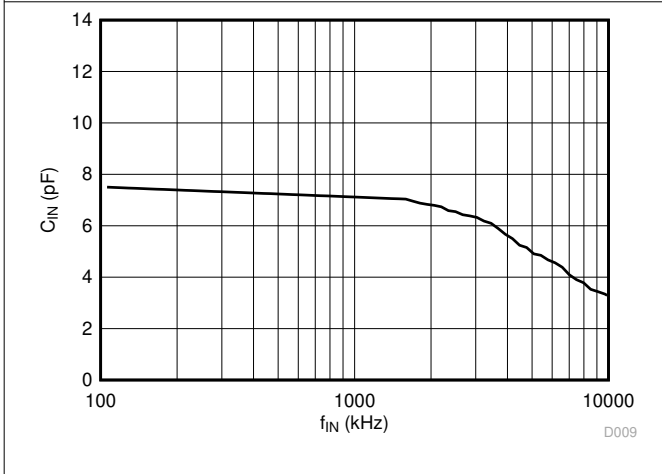
图 7-9. Input Capacitance vs Input Signal Frequency

3.0 V ≤ VDD1 < 4.5 V for the AMC1311B only
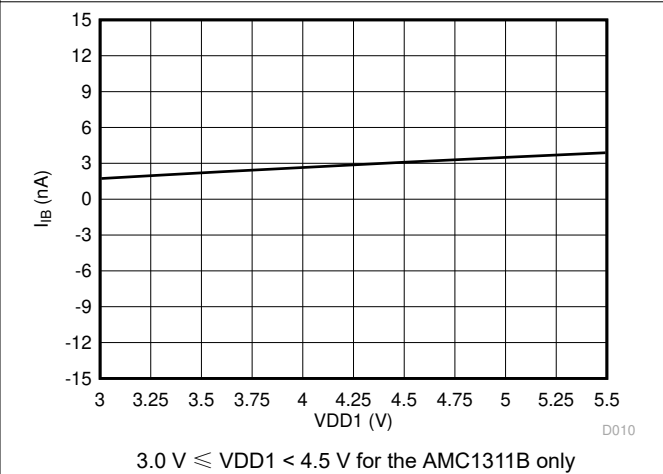
图 7-10. Input Bias Current vs High-Side Supply Voltage
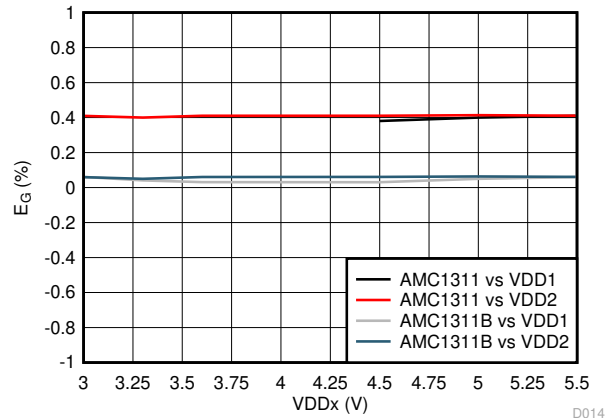
Product Folder Links: *AMC1311*

7.13 Typical Characteristics (continued)

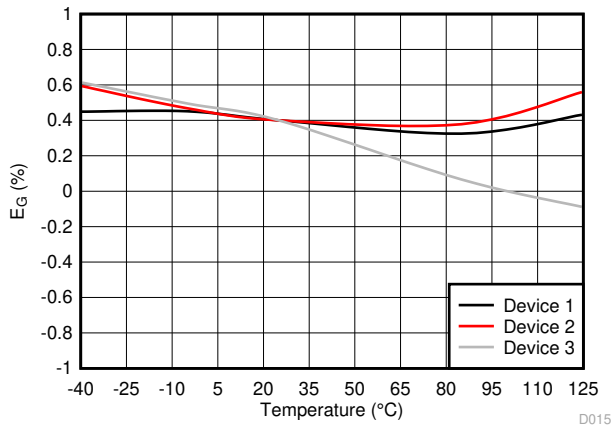at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V, f_{IN} = 10 kHz, and BW = 100 kHz (unless otherwise noted)

−55°C ⩽ T_A < −40°C for the AMC1311B only

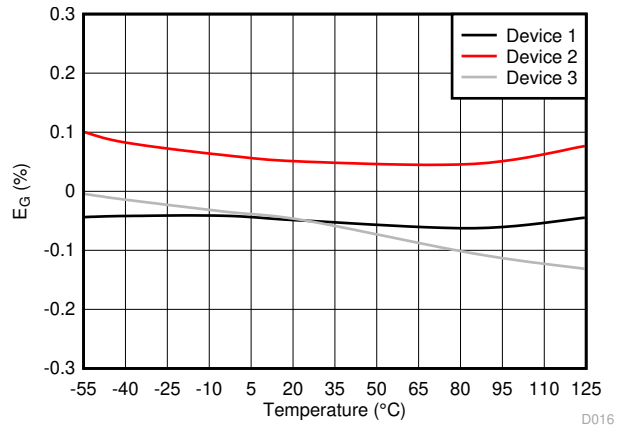**图 7-11. Input Bias Current vs Temperature**

3.0 V ⩽ VDD1 < 4.5 V for the AMC1311B only

图 7-12. Gain Error vs Supply Voltage

AMC1311

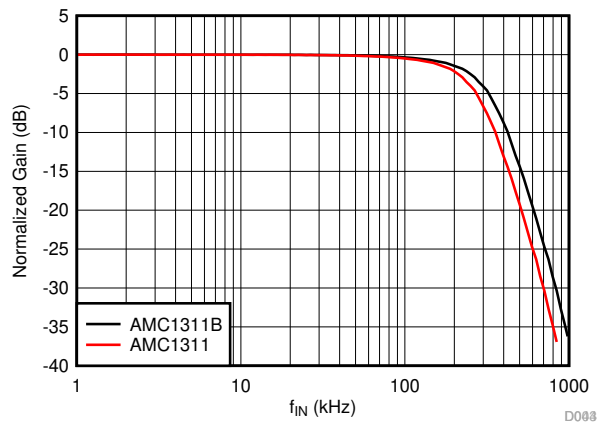**图 7-13. Gain Error vs Temperature**

AMC1311B

图 7-14. Gain Error vs Temperature
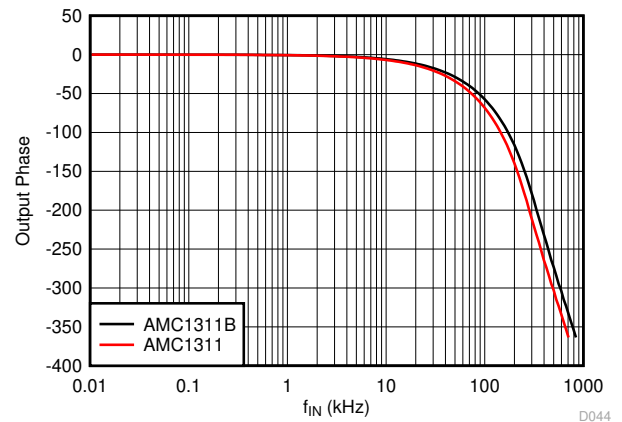
图 7-15. Normalized Gain vs Input Frequency

图 7-16. Output Phase vs Input Frequency

Product Folder Links: *AMC1311*

7.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V, f_{IN} = 10 kHz, and BW = 100 kHz (unless otherwise noted)
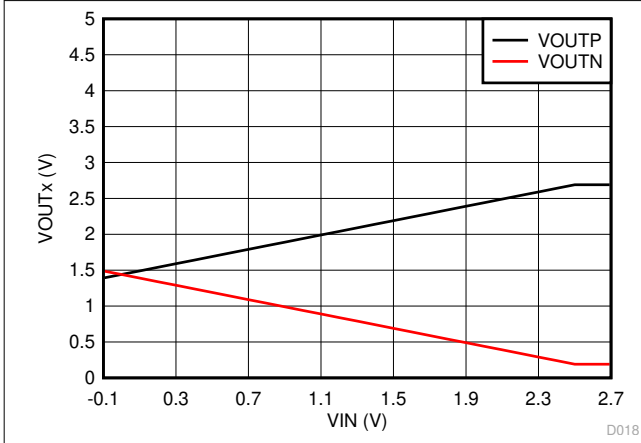
图 **7-17. Output Voltage vs Input Voltage**
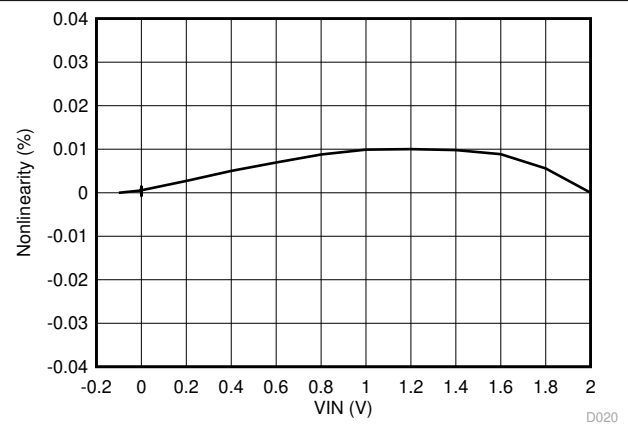
图 **7-18. Nonlinearity vs Input Voltage**

3.0 V ⩽ VDD1 < 4.5 V for the AMC1311B only

图 **7-19. Nonlinearity vs Supply Voltage**
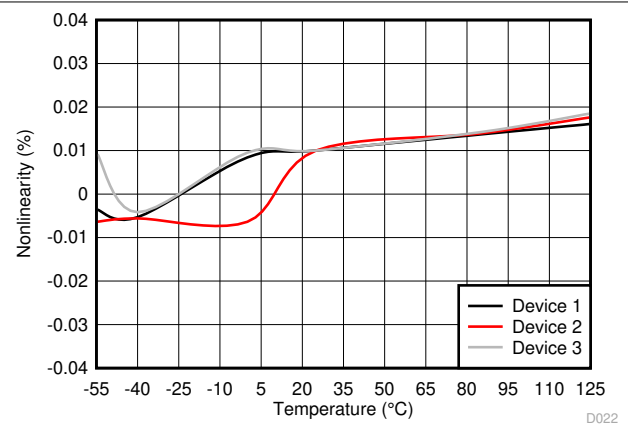
– 55°C ⩽ T_A < – 40°C for the AMC1311B only

图 **7-20. Nonlinearity vs Temperature**
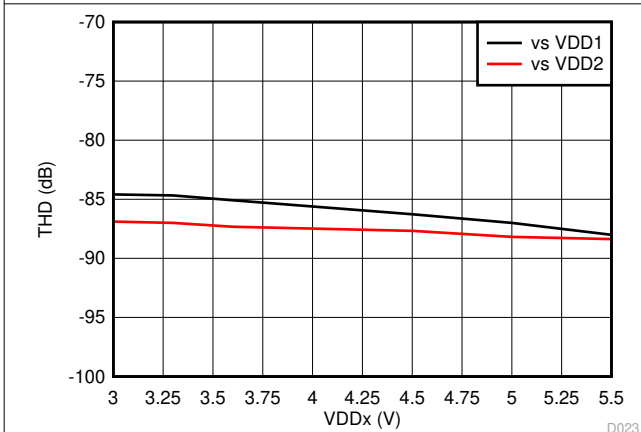
3.0 V ⩽ VDD1 < 4.5 V for the AMC1311B only

图 **7-21. Total Harmonic Distortion vs Supply Voltage**
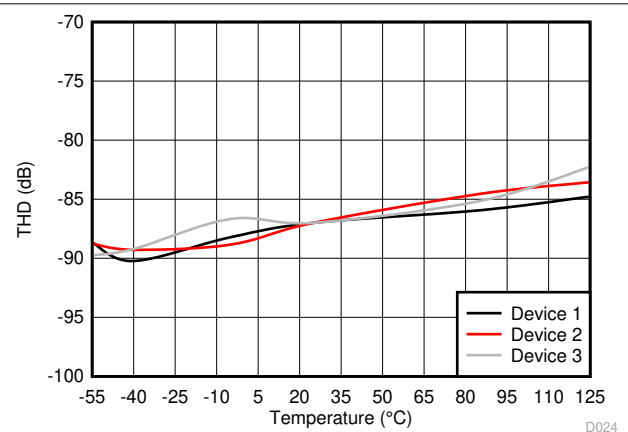
– 55°C ⩽ T_A < – 40°C for the AMC1311B only

图 **7-22. Total Harmonic Distortion vs Temperature**

Product Folder Links: *AMC1311*

7.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V, f_{IN} = 10 kHz, and BW = 100 kHz (unless otherwise noted)

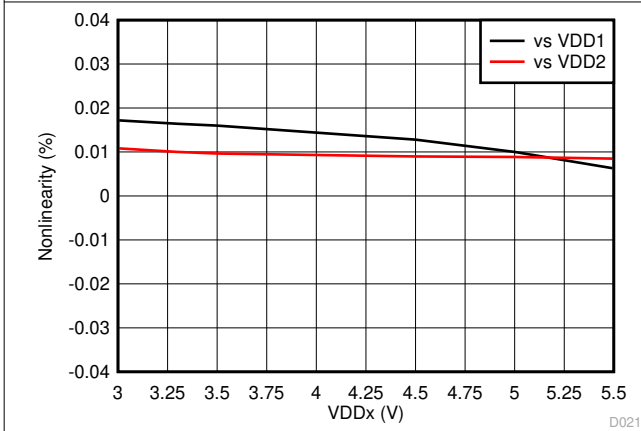图 7-23. Input-Referred Noise Density vs Frequency
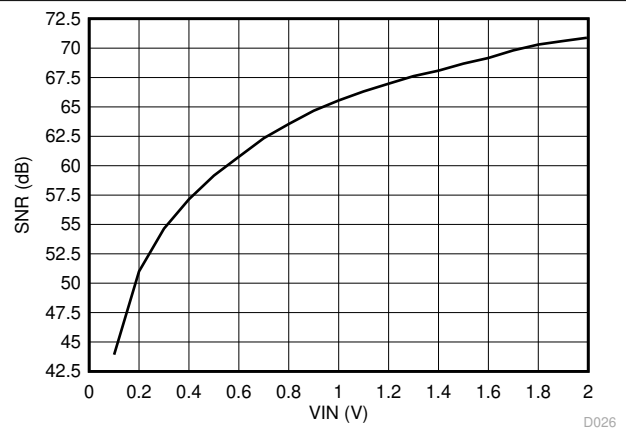
图 7-24. Signal-to-Noise Ratio vs Input Voltage
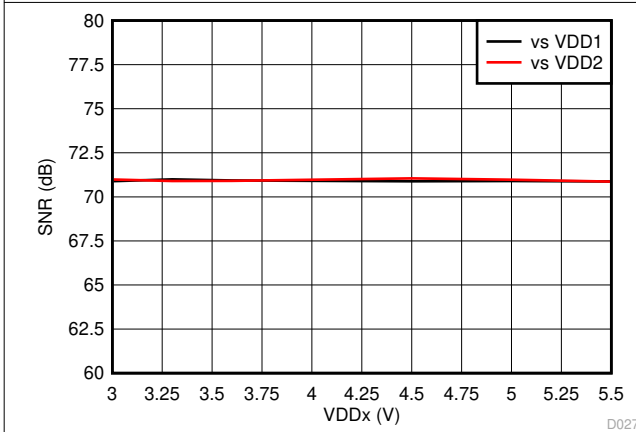
3.0 V ≤ VDD1 < 4.5 V for the AMC1311B only

图 7-25. Signal-to-Noise Ratio vs Supply Voltage
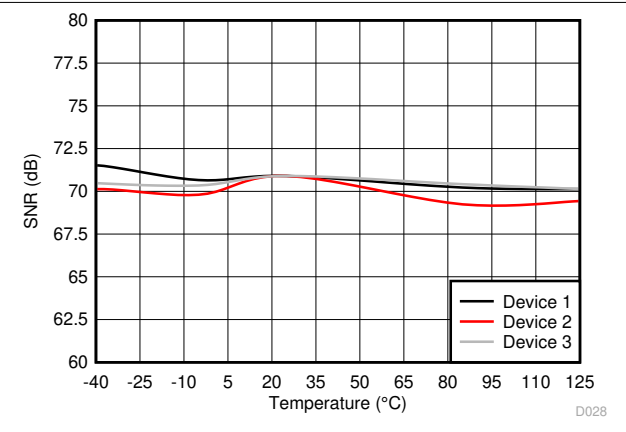
–55°C ≤ T_A < –40°C for the AMC1311B only

图 7-26. Signal-to-Noise Ratio vs Temperature
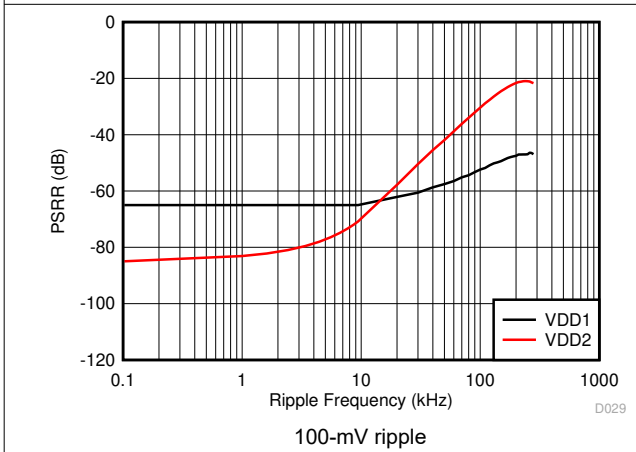
100-mV ripple

图 7-27. Power-Supply Rejection Ratio vs Ripple Frequency
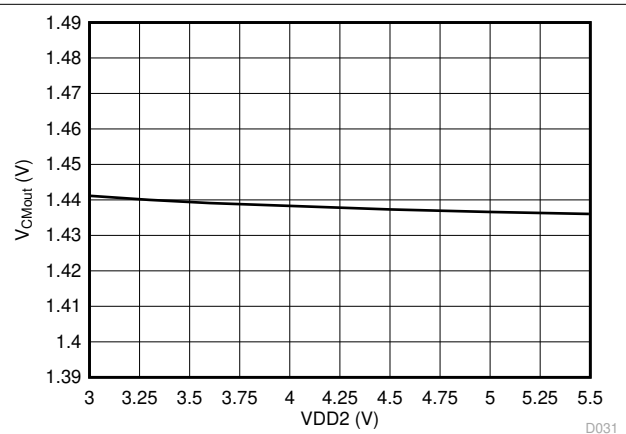
图 7-28. Output Common-Mode Voltage vs Low-Side Supply Voltage

7.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V, f_{IN} = 10 kHz, and BW = 100 kHz (unless otherwise noted)
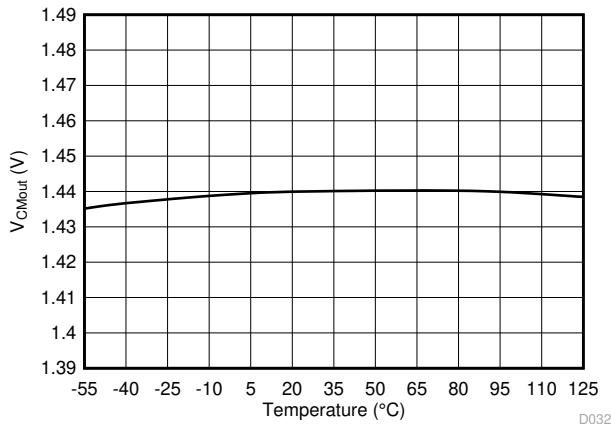
−55°C ≤ T_A < −40°C for the AMC1311B only

图 7-29. Output Common-Mode Voltage vs Temperature
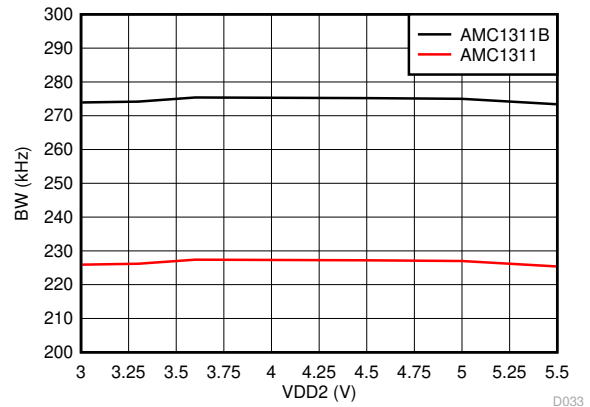
图 7-30. Output Bandwidth vs Low-Side Supply Voltage
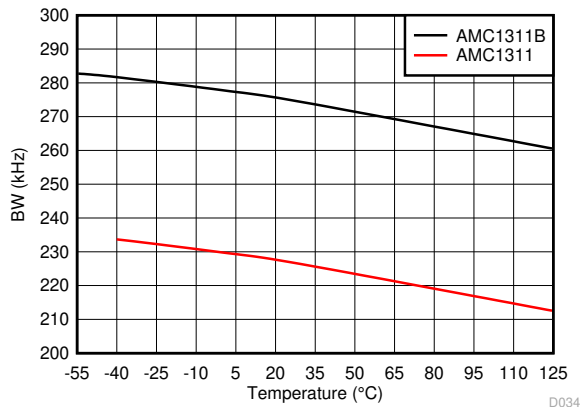
图 7-31. Output Bandwidth vs Temperature
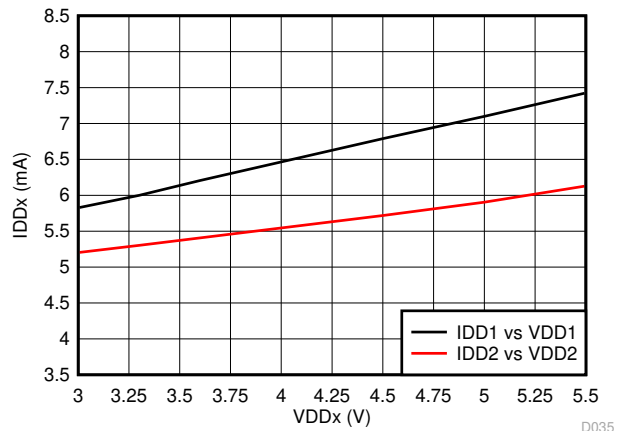
3.0 V ≤ VDD1 < 4.5 V for the AMC1311B only

图 7-32. Supply Current vs Supply Voltage
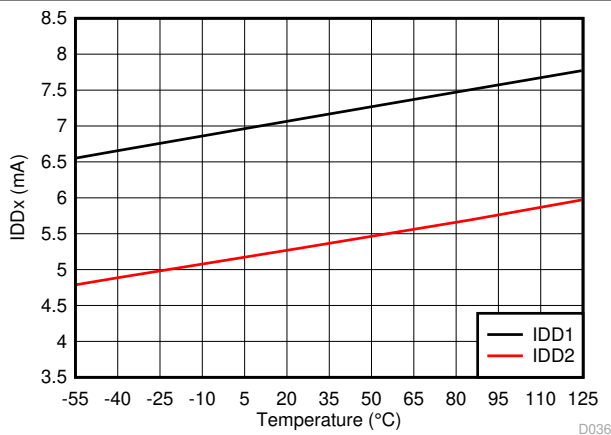
−55°C ≤ T_A < −40°C for the AMC1311B only

图 7-33. Supply Current vs Temperature
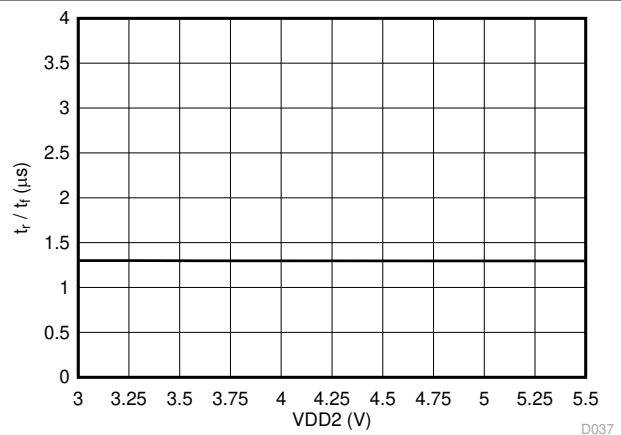
图 7-34. Output Rise and Fall Time vs Low-Side Supply Voltage

Product Folder Links: *AMC1311*

7.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V, f_{IN} = 10 kHz, and BW = 100 kHz (unless otherwise noted)

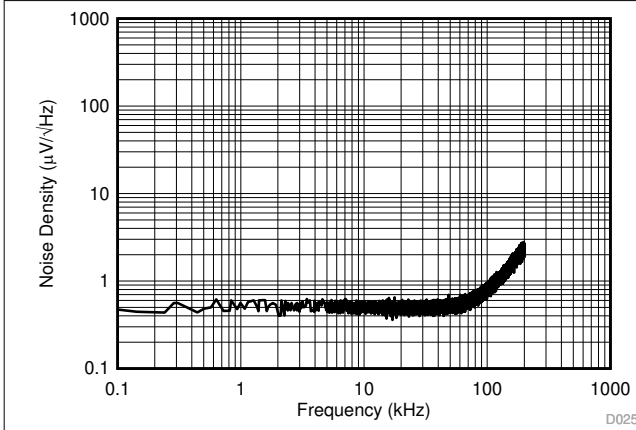−55°C ≤ T_A < −40°C for the AMC1311B only

图 7-35. Output Rise and Fall Time vs Temperature

AMC1311
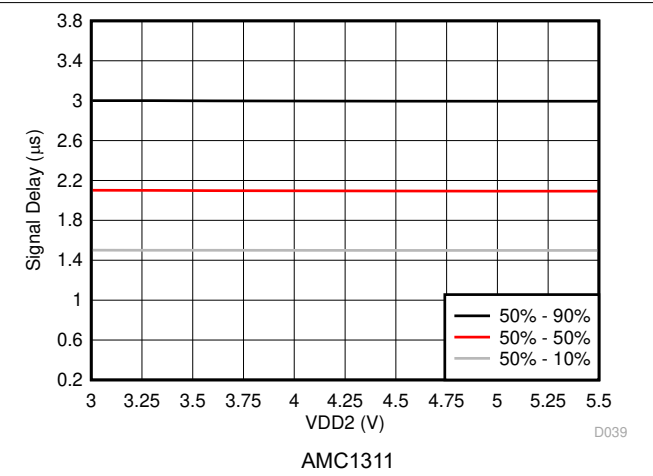
图 7-36. IN to OUTP, OUTN Signal Delay vs Low-Side Supply Voltage
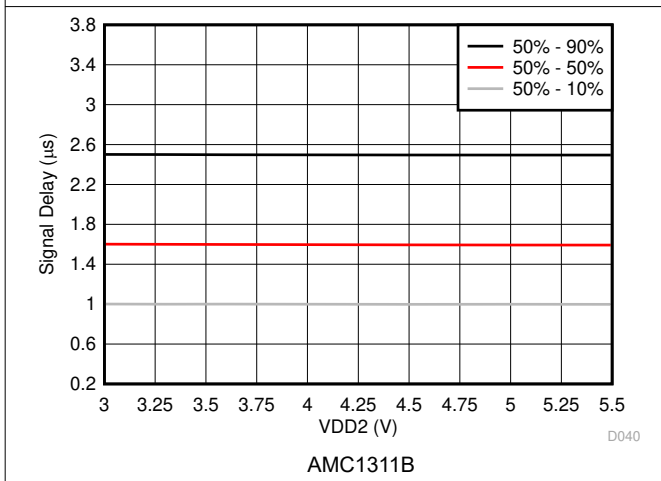
AMC1311B

图 7-37. IN to OUTP, OUTN Signal Delay vs Low-Side Supply Voltage
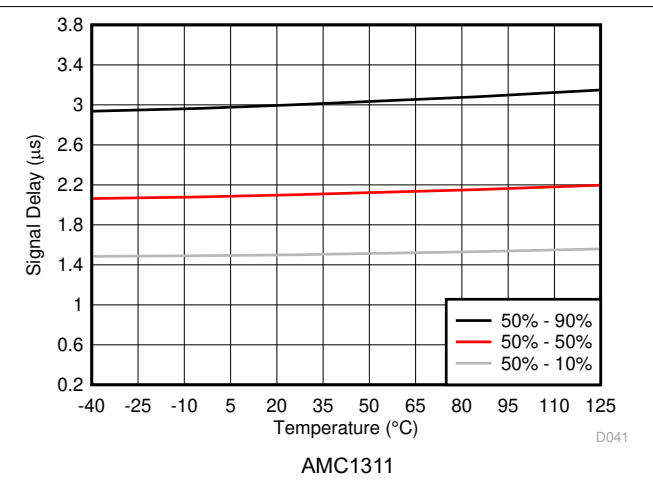
AMC1311

图 7-38. IN to OUTP, OUTN Signal Delay vs Temperature

AMC1311B

图 7-39. IN to OUTP, OUTN Signal Delay vs Temperature

Product Folder Links: *AMC1311*
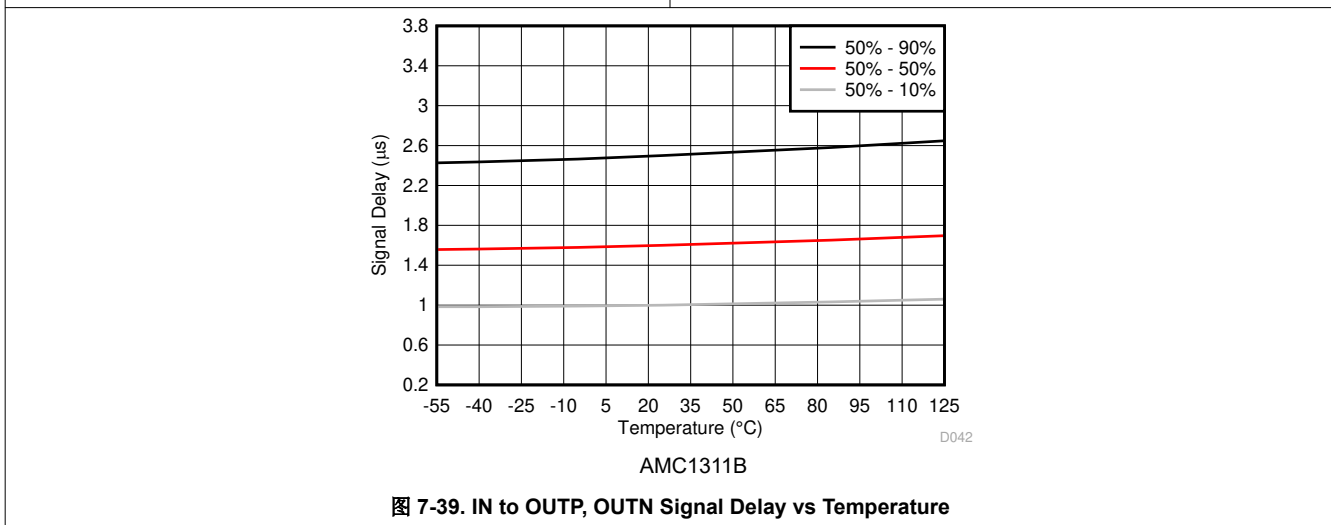
8 Detailed Description

8.1 Overview

The AMC1311 is a precision, single-ended input, isolated amplifier with a high input impedance and wide input voltage range. The input stage of the device drives a second-order, delta-sigma ($\Delta\Sigma$) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier and separates the high-side from the low-side. On the low-side, the received bitstream is processed by a fourth-order analog filter that outputs a differential signal at the OUTP and OUTN pins proportional to the input signal.

The SiO_2-based, capacitive isolation barrier supports a high level of magnetic field immunity, as described in the *ISO72x Digital Isolator Magnetic-Field Immunity* application report. The digital modulation used in the AMC1311 to transmit data across the isolation barrier, and the isolation barrier characteristics itself, result in high reliability and high common-mode transient immunity.

8.2 Functional Block Diagram
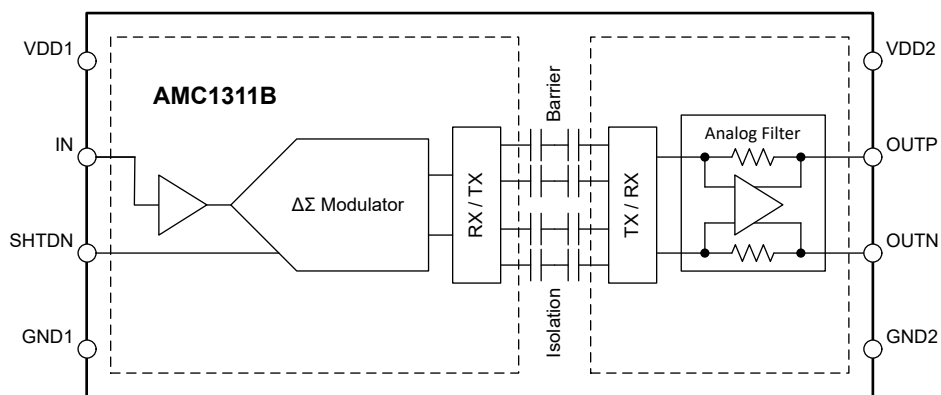
8.3 Feature Description

8.3.1 Analog Input

The single-ended, high-impedance input stage of the AMC1311 feeds a second-order, switched-capacitor, feed-forward $\Delta\Sigma$ modulator. The modulator converts the analog signal into a bitstream that is transferred across the isolation barrier, as described in the *Isolation Channel Signal Transmission* section.

There are two restrictions on the analog input signal IN. First, if the input voltage V_{IN} exceeds the range specified in the *Absolute Maximum Ratings* table, the input current must be limited to the absolute maximum value because the electrostatic discharge (ESD) protection turns on. Secondly, the linearity and parametric performance of the device is ensured only when the analog input voltage remains within the linear full-scale range (V_{FSR}) as specified in the *Recommended Operating Conditions* table.

Product Folder Links: *AMC1311*

8.3.2 Isolation Channel Signal Transmission

The AMC1311 uses an on-off keying (OOK) modulation scheme, as shown in 图 8-1, to transmit the modulator output bitstream across the SiO$_2$-based isolation barrier. The transmit driver (TX) shown in the *Functional Block Diagram* transmits an internally-generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC1311 is 480 MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the input to the fourth-order analog filter. The AMC1311 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and lowest level of radiated emissions caused by the high-frequency carrier and RX/TX buffer switching.

Internal Clock

Modulator Bitstream on High-side

Signal Across Isolation Barrier

Recovered Sigal on Low-side
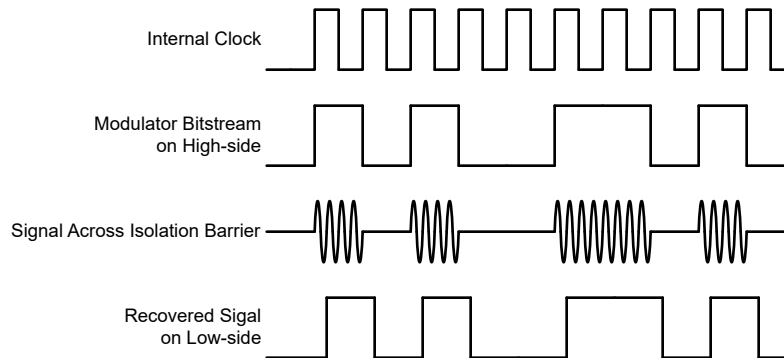
图 8-1. OOK-Based Modulation Scheme

Product Folder Links: *AMC1311*

8.3.3 Analog Output

The AMC1311 provides a differential analog output on the OUTP and OUTN pins. For input voltages of V_{IN} in the range from – 0.1 V to +2 V, the device provides a linear response with a nominal gain of 1. For example, for an input voltage of 2 V, the differential output voltage (V_{OUTP} – V_{OUTN}) is 2 V. At zero input (IN shorted to GND1), both pins output the same common-mode output voltage V_{CMout}, as specified in the *Electrical Characteristics* table. For input voltages greater than 2 V but less than approximately 2.5 V, the differential output voltage continues to increase but with reduced linearity performance. The outputs saturate at a differential output voltage of $V_{CLIPout}$, as shown in 图 8-2, if the input voltage exceeds the $V_{Clipping}$ value.
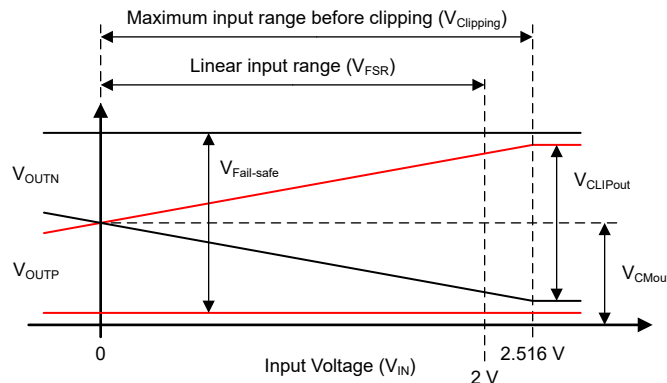
图 **8-2. Output Behavior of the AMC1311**

The AMC1311 output offers a fail-safe feature that simplifies diagnostics on a system level. 图 8-2 shows the fail-safe mode, in which the AMC1311 outputs a negative differential output voltage that does not occur under normal operating conditions. The fail-safe output is active in three cases:

- When the high-side supply VDD1 of the AMC1311 device is missing
- When the high-side supply VDD1 falls below the undervoltage threshold $VDD1_{UV}$
- When the SHTDN pin is pulled high

Use the maximum $V_{Fail-safe}$ voltage specified in the *Electrical Characteristics* table as a reference value for fail-safe detection on a system level.

8.4 Device Functional Modes

The AMC1311 is operational when the power supplies VDD1 and VDD2 are applied, as specified in the *Recommended Operating Conditions* table.

9 Application and Implementation

9.1 Application Information

The high input impedance, low input bias current, low AC and DC errors, and low temperature drift make the AMC1311 a high-performance solution for industrial applications where voltage sensing in the presence of high common-mode voltage levels is required.

9.2 Typical Application

图 9-1 shows the AMC1311 in a typical application. The DC bus voltage is divided down to an approximate 2-V level across the bottom resistor (RSNS) of a high-impedance resistive divider that is sensed by the AMC1311. The AMC1311 digitizes the analog input signal on the high-side, transfers the data across the isolation barrier to the low-side, reconstructs the analog signal, and presents this signal as a differential voltage signal on the output pins.

The high-impedance input and the high common-mode transient immunity (CMTI) of the AMC1311 ensure reliable and accurate operation even in high-noise environments.
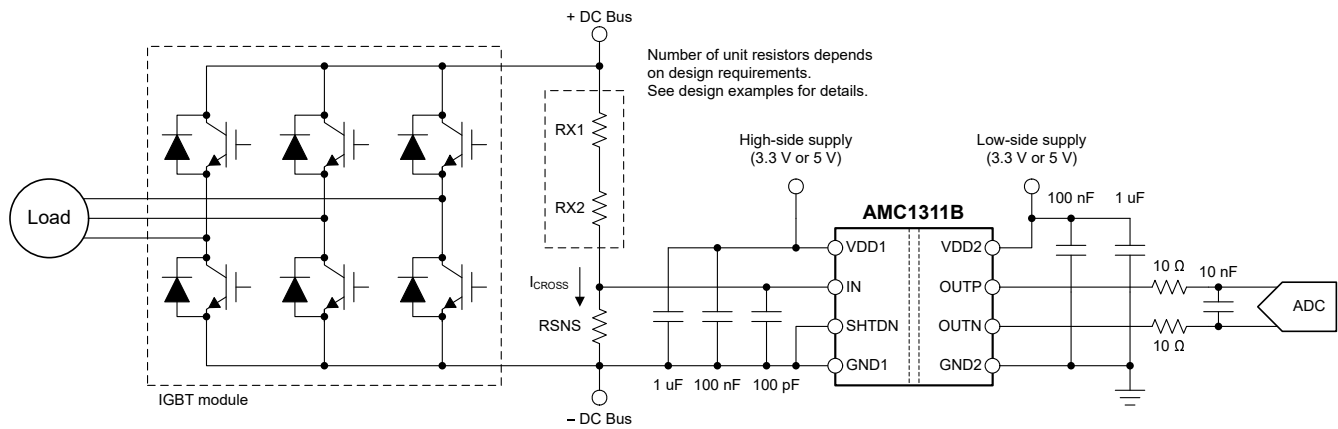
图 9-1. **Using the AMC1311 for DC Link Voltage Sensing in Frequency Inverters**

9.2.1 Design Requirements

表 9-1 lists the parameters for this typical application.

表 9-1. Design Requirements

PARAMETER	VALUE
System input voltage	Single phase, 230 V, 50 Hz
Maximum DC link voltage	400 V
High-side supply voltage	3.3 V or 5 V
Low-side supply voltage	3.3 V or 5 V
Maximum resistor operating voltage	75 V
Voltage drop across the sense resistor (RSNS) for a linear response	2 V (maximum)
Current through the resistive divider, I_{CROSS}	100 µA (maximum)

9.2.2 Detailed Design Procedure

The 100-µA, cross-current requirement at the maximum DC link voltage (400 V) determines that the total impedance of the resistive divider is 4 MΩ. The impedance of the resistive divider is dominated by the top portion (shown exemplary as RX1 and RX2 in 图 9-1) and the voltage drop across RSNS can be neglected for a moment. The maximum allowed voltage drop per unit resistor is specified as 75 V; therefore, the minimum number of unit resistors in the top portion of the resistive divider is 400 V / 75 V = 6. The calculated unit value is 4 MΩ / 6 = 666 kΩ and the next closest value from the E96 series is 665 kΩ.

RSNS is sized such that the voltage drop across the resistor at the maximum DC link voltage (400 V) equals the linear full-scale range input voltage (V_{FSR}) of the AMC1311, which is 2 V. This voltage is calculated as RSNS = V_{FSR} / ($V_{DC\text{-}link, max}$ − V_{FSR}) × R_{TOP}, where R_{TOP} is the total value of the top resistor string (6 × 665 kΩ = 3990 kΩ). RSNS is calculated as 20.05 kΩ and matches a value from the E96 series.

表 9-2. Resistor Value Example

PARAMETER	VALUE
Unit resistor R_X	665 kΩ
Number of unit resistors	6
Sense resistor RSNS	20.05 kΩ
Resulting current through resistive divider I_{CROSS}	99.7 µA
Resulting voltage drop across sense resistor	2.000 V
Power dissipated in unit resistor RX	6.6 mW
Total power dissipated in resistive divider	39.9 mW

Product Folder Links: *AMC1311*

9.2.2.1 Input Filter Design

Placing an RC filter in front of the isolated amplifier improves signal-to-noise performance of the signal path. In practice, however, the impedance of the resistor divider is high and only a small-value filter capacitor can be used to not limit the signal bandwidth to an unacceptable low value. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (20 MHz) of the internal $\Delta\Sigma$ modulator
- The input bias current does not generate significant voltage drop across the DC impedance of the input filter

Most voltage-sensing applications use high-impedance resistor dividers in front of the isolated amplifier to scale down the input voltage. In this case, a single capacitor (as shown in 图 9-2) is sufficient to filter the input signal.
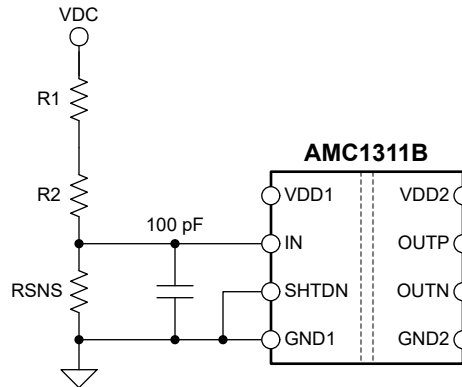
图 9-2. Input Filter

9.2.2.2 Differential to Single-Ended Output Conversion

图 9-3 shows an example of a TLV900x-based signal conversion and filter circuit for systems using single-ended input ADCs to convert the analog output voltage into digital. With R1 = R2 = R3 = R4, the output voltage equals $(V_{OUTP} - V_{OUTN}) + V_{REF}$. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system and use NP0-type capacitors for best performance. For most applications, R1 = R2 = R3 = R4 = 3.3 kΩ and C1 = C2 = 330 pF yields good performance.
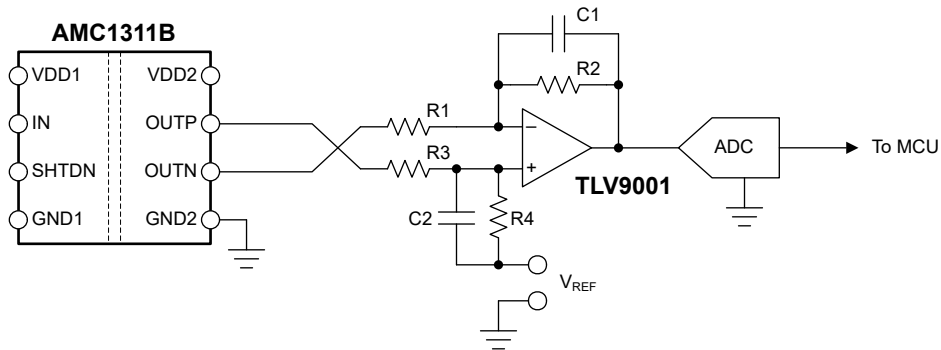
图 9-3. Connecting the AMC1311 Output to a Single-Ended Input ADC

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, see the *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* and *18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guides, available for download at www.ti.com.

9.2.3 Application Curve

One important aspect of system design is the effective detection of an overvoltage condition to protect switching devices and passive components from damage. To power off the system quickly in the event of an overvoltage condition, a low delay caused by the isolated amplifier is required. 图 9-4 shows the typical full-scale step response of the AMC1311.
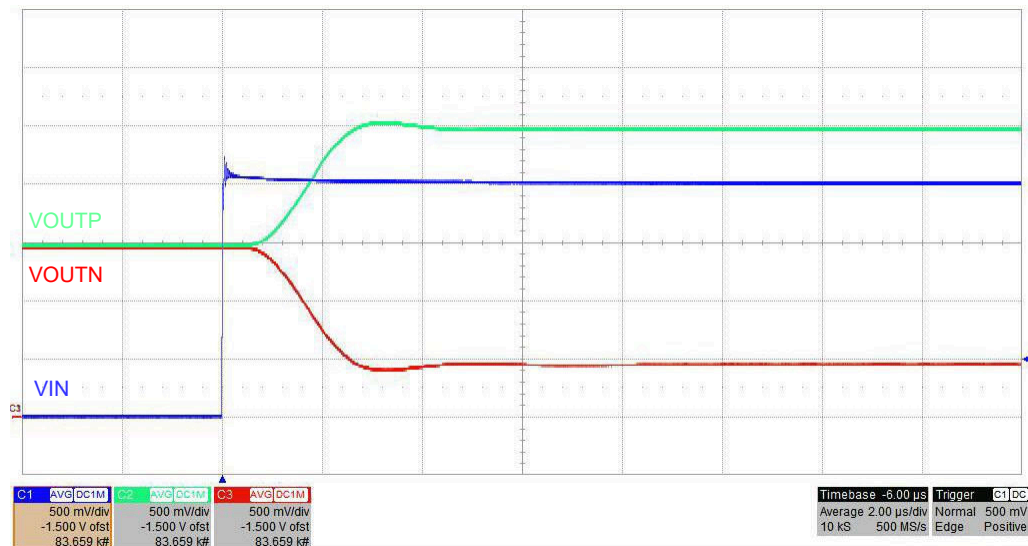
图 **9-4. Step Response of the AMC1311**

9.3 What To Do and What Not To Do

Do not leave the analog input (IN pin) of the AMC1311 unconnected (floating) when the device is powered up on the high-side. If the device input is left floating, the bias current may generate a negative input voltage that exceeds the specified input voltage range, causing the output of the device to be invalid.

Do not connect protection diodes to the input (IN pin) of the AMC1311. Diode leakage current can introduce significant measurement error especially at high temperatures. The input pin is protected against high voltages by its ESD protection circuit and the high impedance of the external restive divider.

10 Power Supply Recommendations

In a typical application, the high-side (VDD1) of the AMC1311 is powered from an already existing, high-side, ground-referenced, 3.3-V or 5-V power supply in the system. Alternatively, the high-side supply can be generated from the low-side supply (VDD2) by an isolated DC/DC converter. A low-cost solution is based on the push-pull driver SN6501 and a transformer that supports the desired isolation voltage ratings.

The AMC1311 does not require any specific power-up sequencing. The high-side power supply (VDD1) is decoupled with a low-ESR, 100-nF capacitor (C1) parallel to a low-ESR, 1-μF capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR, 100-nF capacitor (C3) parallel to a low-ESR, 1-μF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible. 图 10-1 shows the proper decoupling layout for the AMC1311.
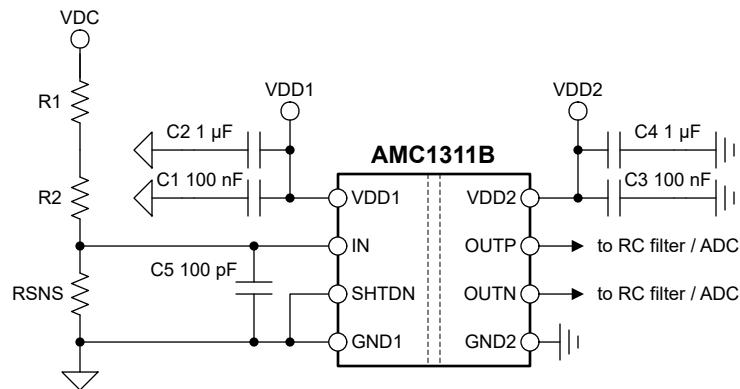
图 10-1. Decoupling of the AMC1311

Capacitors must provide adequate effective capacitance under the applicable DC bias conditions they experience in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of their nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

Product Folder Links: AMC1311

11 Layout

11.1 Layout Guidelines

图 11-1 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC1311 supply pins) and placement of the other components required by the device. For best performance, place the sense resistor close to the device input pin (IN).

11.2 Layout Example
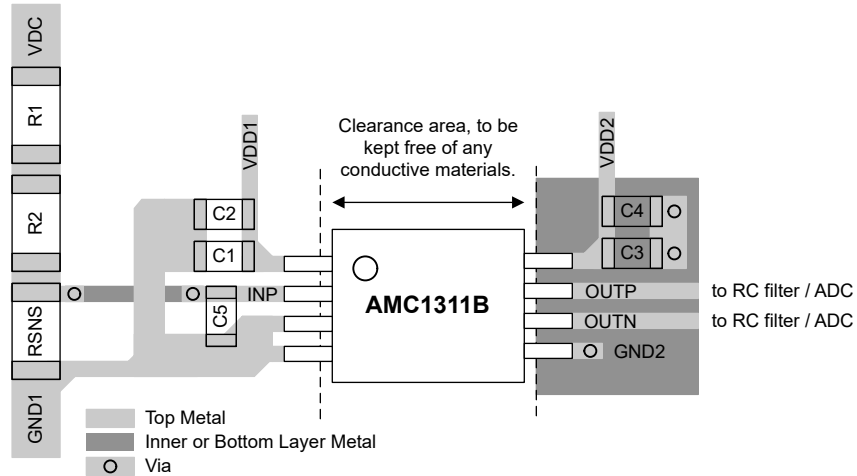
图 **11-1. Recommended Layout of the AMC1311**

Product Folder Links: *AMC1311*

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Isolation Glossary* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application report
- Texas Instruments, *TLV900x Low-Power, RRIO, 1-MHz Operational Amplifier for Cost-Sensitive Systems* data sheet
- Texas Instruments, *SN6501 Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *AMC1311EVM Users Guide*
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* reference guide
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guide
- Texas Instruments, *Isolated Amplifier Voltage Sensing Excel Calculator* design tool

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者"按原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

TI 术语表 　　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC1311BDWV	ACTIVE	SOIC	DWV	8	64	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	1311B	Samples
AMC1311BDWVR	ACTIVE	SOIC	DWV	8	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	1311B	Samples
AMC1311DWV	ACTIVE	SOIC	DWV	8	64	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	1311	Samples
AMC1311DWVR	ACTIVE	SOIC	DWV	8	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	1311	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

| Q1 | Q2 |
| Q3 | Q4 |

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1311BDWVR	SOIC	DWV	8	1000	330.0	16.4	12.15	6.2	3.05	16.0	16.0	Q1
AMC1311DWVR	SOIC	DWV	8	1000	330.0	16.4	12.15	6.2	3.05	16.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1311BDWVR	SOIC	DWV	8	1000	356.0	356.0	35.0
AMC1311DWVR	SOIC	DWV	8	1000	356.0	356.0	35.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width
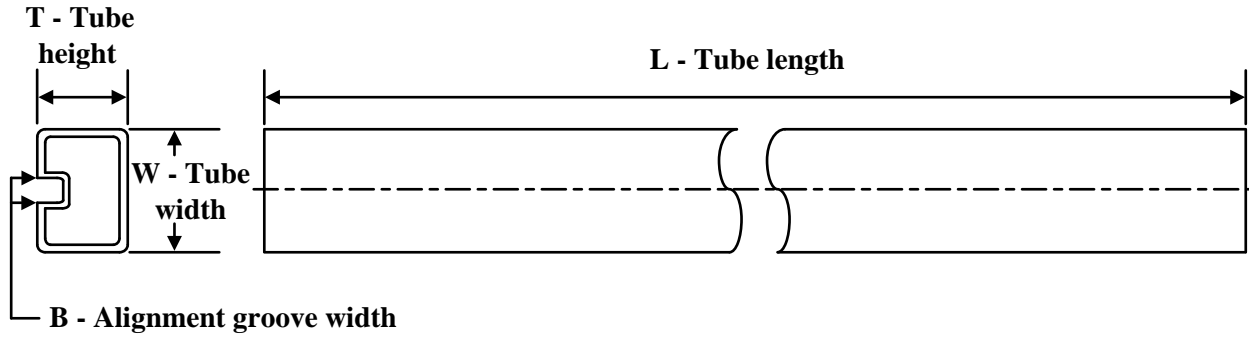
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
AMC1311BDWV	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1311DWV	DWV	SOIC	8	64	505.46	13.94	4826	6.6

DWV0008A

SOIC

SEATING PLANE

C

0.1 C

PIN 1 ID
AREA

11.5 ± 0.25
TYP

6X 1.27

1

8

5.95
5.75
NOTE 3

2X
3.81

4

5

A

7.6
7.4
NOTE 4

B

8X 0.51
0.31

⊕ 0.25 Ⓜ C AⓈ BⓈ

2.8 MAX

SEE DETAIL A

0.33 TYP
0.13

0.25
GAGE PLANE
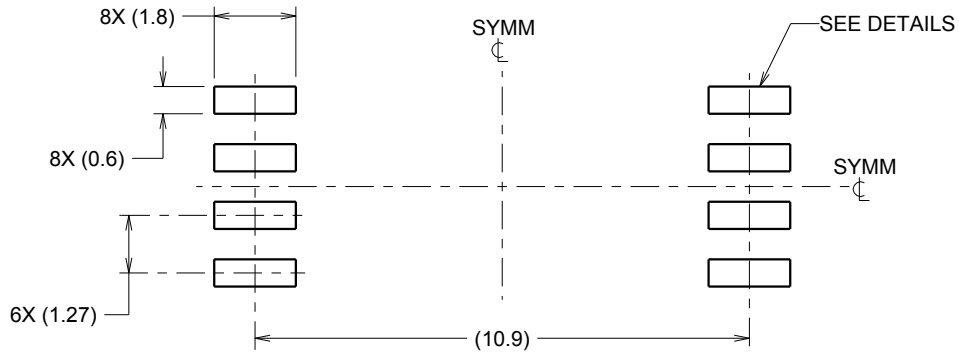
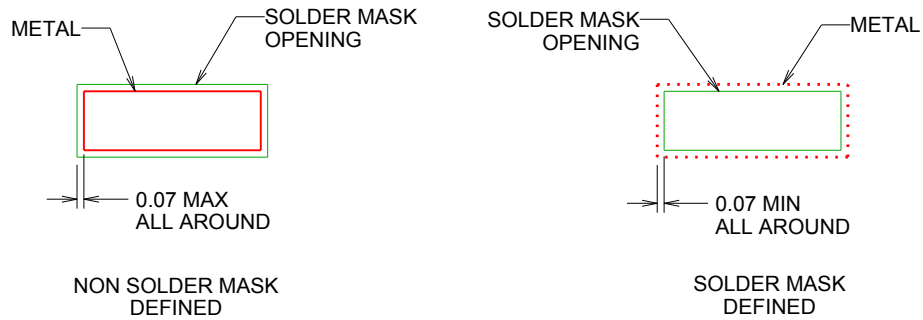(2.286)

0°-8°

0.46
0.36

1.0
0.5

(2)

DETAIL A
TYPICAL

4218796/A   09/2013

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

TEXAS
INSTRUMENTS
www.ti.com

DWV0008A

8X (1.8)

SYMM

SEE DETAILS

8X (0.6)

SYMM

6X (1.27)

(10.9)

LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X

METAL

SOLDER MASK
OPENING

SOLDER MASK
OPENING

METAL

0.07 MAX
ALL AROUND

0.07 MIN
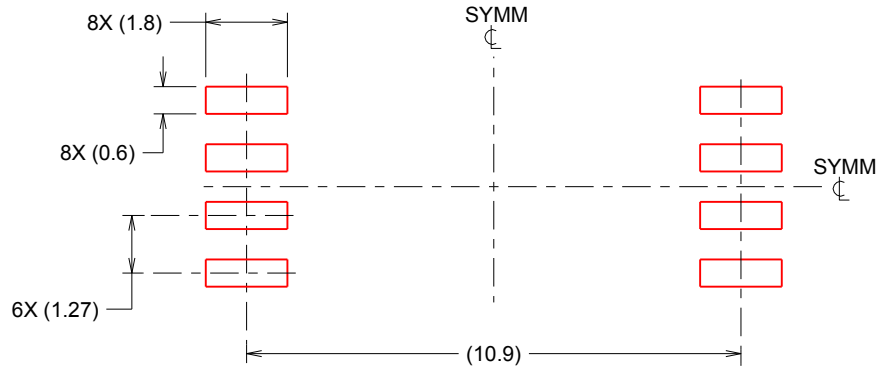ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218796/A   09/2013

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DWV0008A

SOIC - 2.8 mm max height

SOIC

8X (1.8)

SYMM

8X (0.6)

SYMM

6X (1.27)

(10.9)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A   09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.