CC1352R SimpleLink™ 高性能多频带无线 MCU

1 特性

- 微控制器
  - 功能强大的 48MHz Arm® Cortex®-M4F 处理器
  - EEMBC CoreMark® 评分：148
  - 352KB 系统内可编程闪存
  - 256KB ROM，用于协议和库函数
  - 8KB 缓存 SRAM（也可作为通用 RAM 提供）
  - 80KB 超低泄漏 SRAM。SRAM 通过奇偶校验得到保护，从而确保高度可靠运行。
  - 2 引脚 cJTAG 和 JTAG 调试
  - 支持无线 (OTA) 升级
- 具有 4KB SRAM 的超低功耗传感器控制器
  - 采样、存储和处理传感器数据
  - 独立于系统 CPU 运行
  - 快速唤醒进入低功耗运行
- TI-RTOS、驱动程序、引导加载程序、低功耗 *Bluetooth*® 5.2 控制器和 IEEE 802.15.4 MAC 嵌入在 ROM 中，优化了应用尺寸
- 符合 RoHS 标准的封装
  - 7mm × 7mm RGZ VQFN48（28 个 GPIO）
- 外设
  - 数字外设可连接至任何 GPIO
  - 4 个 32 位或 8 个 16 位通用计时器
  - 12 位 ADC、200ksps、8 通道
  - 2 个具有内部基准 DAC 的比较器（1 个连续时间比较器、1 个超低功耗比较器）
  - 可编程电流源
  - 2 个异步收发器 (UART)
  - 2 个同步串行接口 (SSI)（SPI、MICROWIRE 和 TI）
  - I^2C 和 I^2S
  - 实时时钟 (RTC)
  - AES 128 位和 256 位加密加速计
  - ECC 和 RSA 公钥硬件加速器
  - SHA2 加速器（包括至 SHA-512 的全套装）
  - 真随机数发生器 (TRNG)
  - 电容式检测，最多 8 通道
  - 集成温度和电池监控器
- 外部系统
  - 片上降压直流/直流转换器
  - TCXO 支持
- 低功耗
  - 宽电源电压范围：1.8V 至 3.8V
  - 有源模式 RX：5.8mA（3.6V，868MHz）、6.9mA（3.0V，2.4GHz）
  - 有源模式 TX (0dBm)：8.0mA（3.6V，868MHz）、7.1mA（3.0V，2.4GHz）
  - 有源模式 TX (+14dBm)：24.9mA (868MHz)
  - 有源模式 MCU 48MHz (CoreMark)：2.9 mA (60 µA/MHz)
  - 传感器控制器（低功耗模式、2MHz、运行无限环路）：30.1 µA
  - 传感器控制器，有源模式，24MHz，运行无限循环：808 µA
  - 待机：0.85 µA（RTC 运行，80KB RAM 和 CPU 保持）
  - 关断电流：150nA（发生外部事件时唤醒）
- 无线电部分
  - 多频带 Sub-1GHz 和 2.4GHz 射频收发器，兼容低功耗蓝牙 5.2 与早期 LE 规范以及 IEEE 802.15.4 PHY 和 MAC
  - 3 线、2 线、1 线 PTA 共存机制
  - 出色的接收器灵敏度：SimpleLink 远距离模式下为 -121dBm 50kbps 时为 -110dBm，蓝牙 125kbps 时（LE 编码 PHY）为 -105dBm
  - 高达 +14dBm (Sub-1GHz) 和 +5dBm (2.4GHz) 的输出功率，具有温度补偿
  - 适用于符合各项全球射频规范的系统
    - ETSI EN 300 220 接收器类别 1.5 和 2、 EN 300 328、 EN 303 131、EN 303 204（欧洲）
    - EN 300 440 类别 2
    - FCC CFR47 第 15 部分
    - ARIB STD-T108 和 STD-T66
  - 支持广泛的标准
- 无线协议
  - Thread、Zigbee®、低功耗 *Bluetooth*® 5.2、IEEE 802.15.4g、支持 IPv6 的智能对象 (6LoWPAN)、MIOTY®、无线 M-Bus、Wi-SUN®、KNX RF、Amazon Sidewalk、专有系统、SimpleLink™ TI 15.4-Stack（Sub-1GHz），以及动态多协议管理器 (DMM) 驱动程序。
- 开发*工具和软件*
  - CC1352R LaunchPad™ 开发套件
  - SimpleLink™ CC13x2 和 CC26x2 软件开发套件 (SDK)
  - 用于简单无线电配置的 SmartRF™ Studio

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。
English Data Sheet: SWRS196

– 用于构建低功耗检测应用的 Sensor Controller Studio

2 应用

- 169、433、470 至 510、868、902 至 928 和 2400 至 2480MHz ISM 和 SRD 系统，[1] 接收带宽低至 4kHz
- 楼宇自动化
  – 楼宇安防系统 – 运动检测器、电子智能锁、门窗传感器、车库门系统、网关
  – HVAC – 恒温器、无线环境传感器、HVAC 系统控制器、网关
  – 防火安全系统 – 烟雾和热量探测器、火警控制面板 (FACP)
  – 视频监控 – IP 网络摄像头
  – 升降机和自动扶梯 – 升降机和自动扶梯的电梯主控板
- 电网基础设施
  – 智能仪表 – 水表、燃气表、电表和热量分配表
  – 电网通信 – 无线通信 – 远距离传感器应用
  – 其他替代能源 – 能量收集
- 工业运输 – 资产跟踪
- 工厂自动化和控制
- 医疗
- 电子销售终端 (EPOS) – 电子货架标签 (ESL)
- 通信设备
  – 有线网络 – 无线 LAN 或 Wi-Fi 接入点、边缘路由器
- 个人电子产品
  – 便携式电子产品 – 射频智能遥控器
  – 家庭影院和娱乐 – 智能扬声器、智能显示器、机顶盒
  – 联网外设 – 消费类无线模块、指点设备、键盘
  – 游戏 – 电子玩具和机器人玩具
  – 可穿戴设备（非医用）– 智能追踪器、智能服装

3 说明

SimpleLink™ CC1352R 器件是一款多协议、多频带 Sub-1GHz 和 2.4GHz 无线微控制器 (MCU)，支持 Thread、Zigbee®、低功耗 *Bluetooth®* 5.2、IEEE 802.15.4g、支持 IPv6 的智能对象 (6LoWPAN)、MIOTY®、Wi-SUN®、专有系统（包括 Sub-1GHz 和 2.4GHz 的 TI 15.4-Stack）和通过动态多协议管理器 (DMM) 驱动程序实现的并发多协议。该器件经过优化，可用于楼宇安防系统、HVAC、智能仪表、医疗、有线网络、便携式电子产品、家庭影院和娱乐以及联网外设市场中的低功耗无线通信和高级检测。该器件的突出特性包括：

- 多频带器件，通过 DMM 驱动程序支持面向 Sub-1GHz 和 2.4GHz 的并发多协议。
- SimpleLink™ CC13x2 和 CC26x2 软件开发套件 (SDK) 提供丰富灵活的协议栈支持。
- 对于 Sub-1GHz，最大发送功耗为 +14dBm（电流消耗为 24.9mA）；对于 2.4GHz，最大发送功耗为 +5dBm（电流消耗为 9.6mA）。
- 具有 0.85μA 的低待机电流（完全 RAM 保持），从而延长无线应用的电池寿命。
- 支持工业温度，在 85°C 下最低待机电流为 5μA。
- 通过具有快速唤醒功能的可编程、自主式超低功耗传感器控制器 CPU 实现高级检测。例如，传感器控制器能够在 1μA 系统电流下进行 1Hz ADC 采样。
- 低 SER（软错误率）FIT（时基故障），可延长运行寿命，不会对工业市场造成干扰，SRAM 奇偶校验功能始终开启，可防止潜在辐射事件导致的损坏。
- 软件控制的专用无线电控制器 (Arm® Cortex®-M0) 提供灵活的低功耗射频收发器功能，支持多个物理层和射频标准。
- 出色的无线电敏感度 (-121dBm) 和稳健性（选择性与阻断）性能，适用于 SimpleLink™ 远距离模式。

CC1352R 器件是 SimpleLink™ MCU 平台的一部分，该平台包括 Wi-Fi®、低功耗*蓝牙*、Thread、Zigbee、Sub-1GHz MCU 和主机 MCU，它们共用一个通用、易于使用的开发环境，其中包含单核软件开发套件 (SDK) 和丰富的工具集。借助一次性集成的 SimpleLink™ 平台，可以将产品组合中的任何器件组合添加至您的设计中，从而在设计要求变更时实现 100% 的代码重用。如需更多信息，请访问 SimpleLink™ MCU 平台。

器件信息

器件型号[(1)]	封装	封装尺寸（标称值）
CC1352R1F3RGZ	VQFN (48)	7.00mm × 7.00mm

(1) 如需所有可用器件的最新器件、封装和订购信息，请参阅节 12 中的“封装选项附录”或访问 TI 网站。

[1] 请参阅*射频内核*，了解有关支持的协议标准、调制格式和数据速率的其他详细信息。

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4 Functional Block Diagram

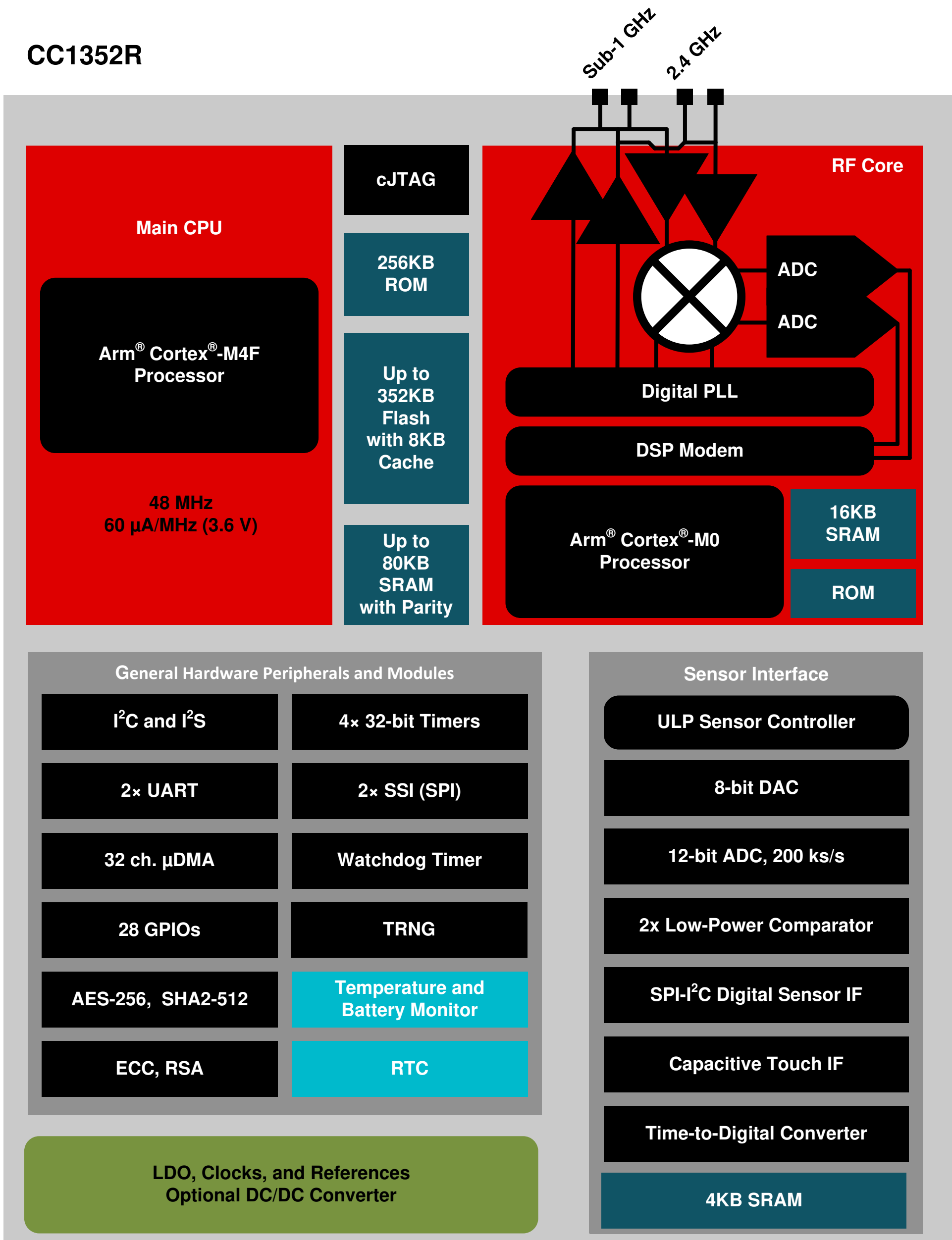

图 4-1. CC1352R Block Diagram

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5 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from November 19, 2020 to February 12, 2021 (from Revision H (November 2020) to Revision I (February 2021)) **Page**

- 通篇更新为蓝牙 5.2..1
- 向节 1，*特性* 的“无线电部分”列表中添加了 3 线、2 线和 1 线 PTA 共存机制.............. 1
- Added PTA description in 节 9.3, *Radio (RF Core)* 71

6 Device Comparison

表 6-1. Device Family Overview

DEVICE	RADIO SUPPORT	FLASH (KB)	RAM (KB)	GPIO	PACKAGE SIZE
CC1312R	Sub-1 GHz	352	80	30	RGZ (7-mm × 7-mm VQFN48)
CC1352P	Multiprotocol Sub-1 GHz Bluetooth 5.2 Low Energy Zigbee Thread 2.4 GHz proprietary FSK-based formats +20-dBm high-power amplifier	352	80	26	RGZ (7-mm × 7-mm VQFN48)
CC1352R	Multiprotocol Sub-1 GHz Bluetooth 5.2 Low Energy Zigbee Thread 2.4 GHz proprietary FSK-based formats	352	80	28	RGZ (7-mm × 7-mm VQFN48)
CC2642R	Bluetooth 5.2 Low Energy 2.4 GHz proprietary FSK-based formats	352	80	31	RGZ (7-mm × 7-mm VQFN48)
CC2642R-Q1	Bluetooth 5.2 Low Energy	352	80	31	RTC (7-mm × 7-mm VQFN48)
CC2652R	Multiprotocol Bluetooth 5.2 Low Energy Zigbee Thread 2.4 GHz proprietary FSK-based formats	352	80	31	RGZ (7-mm × 7-mm VQFN48)
CC2652RB	Multiprotocol Bluetooth 5.2 Low Energy Zigbee Thread 2.4 GHz proprietary FSK-based formats	352	80	31	RGZ (7-mm × 7-mm VQFN48)
CC2652P	Multiprotocol Bluetooth 5.2 Low Energy Zigbee Thread 2.4 GHz proprietary FSK-based formats +19.5-dBm high-power amplifier	352	80	26	RGZ (7-mm × 7-mm VQFN48)
CC1310	Sub-1 GHz	32 – 128	16 – 20	10 – 31	RGZ (7-mm × 7-mm VQFN48) RHB (5-mm × 5-mm VQFN32) RSM (4-mm × 4-mm VQFN32)
CC1350	Sub-1 GHz Bluetooth 4.2 Low Energy	128	20	10 – 31	RGZ (7-mm × 7-mm VQFN48) RHB (5-mm × 5-mm VQFN32) RSM (4-mm × 4-mm VQFN32)
CC2640R2F	Bluetooth 5.1 Low Energy 2.4 GHz proprietary FSK-based formats	128	20	10 – 31	RGZ (7-mm × 7-mm VQFN48) RHB (5-mm × 5-mm VQFN32) RSM (4-mm × 4-mm VQFN32) YFV (2.7-mm × 2.7-mm DSBGA34)
CC2640R2F-Q1	Bluetooth 5.1 Low Energy 2.4 GHz proprietary FSK-based formats	128	20	31	RGZ (7-mm × 7-mm VQFN48)

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7 Terminal Configuration and Functions

7.1 Pin Diagram – RGZ Package (Top View)

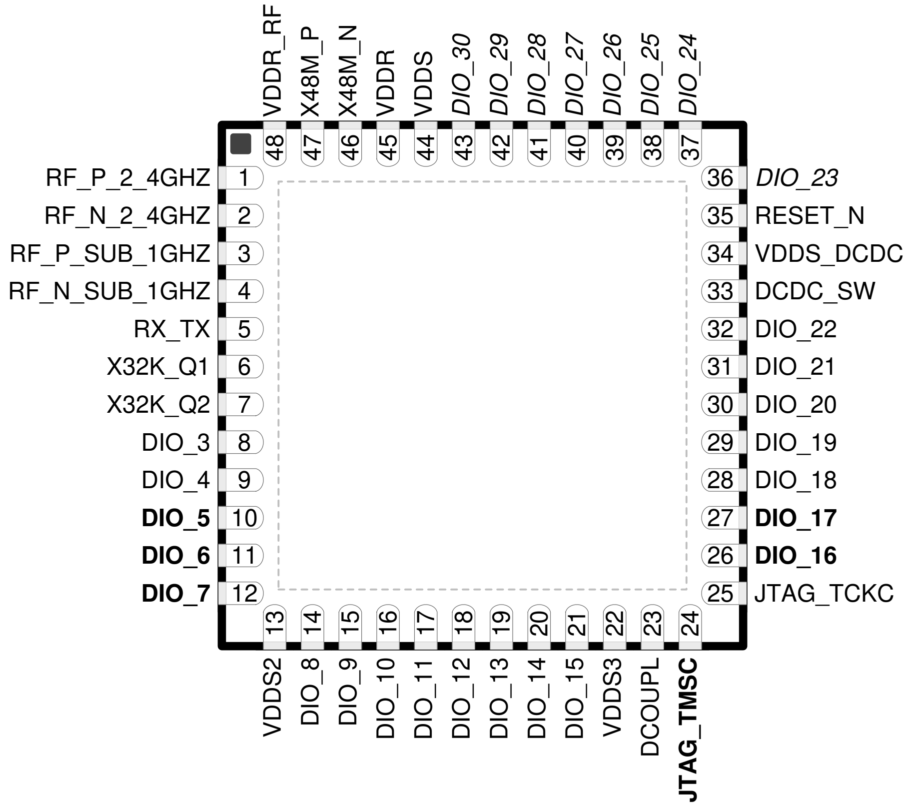

图 7-1. RGZ (7-mm × 7-mm) Pinout, 0.5-mm Pitch (Top View)

The following I/O pins marked in 图 7-1 in **bold** have high-drive capabilities:

- Pin 10, DIO_5
- Pin 11, DIO_6
- Pin 12, DIO_7
- Pin 24, JTAG_TMSC
- Pin 26, DIO_16
- Pin 27, DIO_17

The following I/O pins marked in 图 7-1 in *italics* have analog capabilities:

- Pin 36, DIO_23
- Pin 37, DIO_24
- Pin 38, DIO_25
- Pin 39, DIO_26
- Pin 40, DIO_27
- Pin 41, DIO_28
- Pin 42, DIO_29
- Pin 43, DIO_30

7.2 Signal Descriptions – RGZ Package

表 7-1. Signal Descriptions – RGZ Package

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
DCDC_SW	33	—	Power	Output from internal DC/DC converter(1)
DCOUPL	23	—	Power	For decoupling of internal 1.27 V regulated digital-supply (2)
DIO_3	8	I/O	Digital	GPIO
DIO_4	9	I/O	Digital	GPIO
DIO_5	10	I/O	Digital	GPIO, high-drive capability
DIO_6	11	I/O	Digital	GPIO, high-drive capability
DIO_7	12	I/O	Digital	GPIO, high-drive capability
DIO_8	14	I/O	Digital	GPIO
DIO_9	15	I/O	Digital	GPIO
DIO_10	16	I/O	Digital	GPIO
DIO_11	17	I/O	Digital	GPIO
DIO_12	18	I/O	Digital	GPIO
DIO_13	19	I/O	Digital	GPIO
DIO_14	20	I/O	Digital	GPIO
DIO_15	21	I/O	Digital	GPIO
DIO_16	26	I/O	Digital	GPIO, JTAG_TDO, high-drive capability
DIO_17	27	I/O	Digital	GPIO, JTAG_TDI, high-drive capability
DIO_18	28	I/O	Digital	GPIO
DIO_19	29	I/O	Digital	GPIO
DIO_20	30	I/O	Digital	GPIO
DIO_21	31	I/O	Digital	GPIO
DIO_22	32	I/O	Digital	GPIO
DIO_23	36	I/O	Digital or Analog	GPIO, analog capability
DIO_24	37	I/O	Digital or Analog	GPIO, analog capability
DIO_25	38	I/O	Digital or Analog	GPIO, analog capability
DIO_26	39	I/O	Digital or Analog	GPIO, analog capability
DIO_27	40	I/O	Digital or Analog	GPIO, analog capability
DIO_28	41	I/O	Digital or Analog	GPIO, analog capability
DIO_29	42	I/O	Digital or Analog	GPIO, analog capability
DIO_30	43	I/O	Digital or Analog	GPIO, analog capability
EGP	—	—	GND	Ground – exposed ground pad(3)
JTAG_TMSC	24	I/O	Digital	JTAG TMSC, high-drive capability
JTAG_TCKC	25	I	Digital	JTAG TCKC
RESET_N	35	I	Digital	Reset, active low. No internal pullup resistor
RF_P_2_4GHZ	1	—	RF	Positive 2.4-GHz RF input signal to LNA during RX Positive 2.4-GHz RF output signal from PA during TX
RF_N_2_4GHZ	2	—	RF	Negative 2.4-GHz RF input signal to LNA during RX Negative 2.4-GHz RF output signal from PA during TX
RF_P_SUB_1GHZ	3	—	RF	Positive Sub-1 GHz RF input signal to LNA during RX Positive Sub-1 GHz RF output signal from PA during TX
RF_N_SUB_1GHZ	4	—	RF	Negative Sub-1 GHz RF input signal to LNA during RX Negative Sub-1 GHz RF output signal from PA during TX
RX_TX	5	—	RF	Optional bias pin for the RF LNA

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表 7-1. Signal Descriptions – RGZ Package (continued)

PIN NAME	PIN NO.	I/O	TYPE	DESCRIPTION
VDDR	45	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO[2] [4] [6]
VDDR_RF	48	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO[2] [5] [6]
VDDS	44	—	Power	1.8-V to 3.8-V main chip supply[1]
VDDS2	13	—	Power	1.8-V to 3.8-V DIO supply[1]
VDDS3	22	—	Power	1.8-V to 3.8-V DIO supply[1]
VDDS_DCDC	34	—	Power	1.8-V to 3.8-V DC/DC converter supply
X48M_N	46	—	Analog	48-MHz crystal oscillator pin 1
X48M_P	47	—	Analog	48-MHz crystal oscillator pin 2
X32K_Q1	6	—	Analog	32-kHz crystal oscillator pin 1
X32K_Q2	7	—	Analog	32-kHz crystal oscillator pin 2

(1) For more details, see technical reference manual listed in 节 11.2.
(2) Do not supply external circuitry from this pin.
(3) EGP is the only ground connection for the device. Good electrical connection to device ground on printed circuit board (PCB) is imperative for proper device operation.
(4) If internal DC/DC converter is not used, this pin is supplied internally from the main LDO.
(5) If internal DC/DC converter is not used, this pin must be connected to VDDR for supply from the main LDO.
(6) Output from internal DC/DC and LDO is trimmed to 1.68 V.

7.3 Connections for Unused Pins and Modules

表 7-2. Connections for Unused Pins

FUNCTION	SIGNAL NAME	PIN NUMBER	ACCEPTABLE PRACTICE[1]	PREFERRED PRACTICE[1]
GPIO	DIO_n	8 – 12 14 – 21 26 – 32 36 – 43	NC or GND	NC
32.768-kHz crystal	X32K_Q1	6	NC or GND	NC
	X32K_Q2	7		
DC/DC converter[2]	DCDC_SW	33	NC	NC
	VDDS_DCDC	34	VDDS	VDDS

(1) NC = No connect
(2) When the DC/DC converter is not used, the inductor between DCDC_SW and VDDR can be removed. VDDR and VDDR_RF must still be connected and the 22 uF DCDC capacitor must be kept on the VDDR net.

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1] [2]

			MIN	MAX	UNIT
VDDS[3]	Supply voltage		–0.3	4.1	V
	Voltage on any digital pin[4]		–0.3	VDDS + 0.3, max 4.1	V
	Voltage on crystal oscillator pins, X32K_Q1, X32K_Q2, X48M_N and X48M_P		–0.3	VDDR + 0.3, max 2.25	V
V_{in}	Voltage on ADC input	Voltage scaling enabled	–0.3	VDDS	V
		Voltage scaling disabled, internal reference	–0.3	1.49	
		Voltage scaling disabled, VDDS as reference	–0.3	VDDS / 2.9	
	Input level, Sub-1 GHz RF pins			10	dBm
	Input level, 2.4 GHz RF pins			5	dBm
T_{stg}	Storage temperature		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ground, unless otherwise noted.
(3) VDDS_DCDC, VDDS2 and VDDS3 must be at the same potential as VDDS.
(4) Including analog capable DIOs.

8.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	All pins	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	All pins	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Operating junction temperature[2]		–40	105	°C
Operating supply voltage (VDDS)		1.8	3.8	V
Operating supply voltage (VDDS), boost mode	VDDR = 1.95 V +14 dBm RF output power	2.1	3.8	V
Rising supply voltage slew rate		0	100	mV/µs
Falling supply voltage slew rate[1]		0	20	mV/µs

(1) For small coin-cell batteries, with high worst-case end-of-life equivalent source resistance, a 22-µF VDDS input capacitor must be used to ensure compliance with this slew rate.
(2) For thermal resistance characteristics refer to Thermal Resistance Characteristics. For application considerations, refer to Junction Temperature.

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8.4 Power Supply and Modules

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
VDDS Power-on-Reset (POR) threshold			1.1 - 1.55		V
VDDS Brown-out Detector (BOD) (1)	Rising threshold		1.77		V
VDDS Brown-out Detector (BOD), before initial boot (2)	Rising threshold		1.70		V
VDDS Brown-out Detector (BOD) (1)	Falling threshold		1.75		V

(1) For boost mode (VDDR =1.95 V), TI drivers software initialization will trim VDDS BOD limits to maximum (approximately 2.0 V)
(2) Brown-out Detector is trimmed at initial boot, value is kept until device is reset by a POR reset or the RESET_N pin

8.5 Power Consumption - Power Modes

When measured on the CC1352REM-XD7793-XD24 reference design with T_c = 25 °C, V_{DDS} = 3.6 V with DC/DC enabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	TYP	UNIT
Core Current Consumption				
I_{core}	Reset and Shutdown	Reset. RESET_N pin asserted or VDDS below power-on-reset threshold	150	nA
		Shutdown. No clocks running, no retention	150	
	Standby without cache retention	RTC running, CPU, 80KB RAM and (partial) register retention. RCOSC_LF	0.85	µA
		RTC running, CPU, 80KB RAM and (partial) register retention XOSC_LF	0.99	µA
	Standby with cache retention	RTC running, CPU, 80KB RAM and (partial) register retention. RCOSC_LF	2.78	µA
		RTC running, CPU, 80KB RAM and (partial) register retention. XOSC_LF	2.92	µA
	Idle	Supply Systems and RAM powered RCOSC_HF	590	µA
	Active	MCU running CoreMark at 48 MHz RCOSC_HF	2.89	mA
Peripheral Current Consumption (1), (2)				
I_{peri}	Peripheral power domain	Delta current with domain enabled	82.3	µA
	Serial power domain	Delta current with domain enabled	5.5	
	RF Core	Delta current with power domain enabled, clock enabled, RF core idle	178.9	
	µDMA	Delta current with clock enabled, module is idle	53.6	
	Timers	Delta current with clock enabled, module is idle(5)	67.8	
	I2C	Delta current with clock enabled, module is idle	8.2	
	I2S	Delta current with clock enabled, module is idle	21.7	
	SSI	Delta current with clock enabled, module is idle(4)	69.4	
	UART	Delta current with clock enabled, module is idle(3)	140.8	
	CRYPTO (AES)	Delta current with clock enabled, module is idle	21.1	
	PKA	Delta current with clock enabled, module is idle	71.1	
	TRNG	Delta current with clock enabled, module is idle	29.7	
Sensor Controller Engine Consumption				
I_{SCE}	Active mode	24 MHz, infinite loop, V_{DDS} = 3.0 V	808.5	µA
	Low-power mode	2 MHz, infinite loop, V_{DDS} = 3.0 V	30.1	

(1) Adds to core current I_{core} for each peripheral unit activated.
(2) I_{peri} is not supported in Standby or Shutdown modes.
(3) Only one UART running
(4) Only one SSI running
(5) Only one GPTimer running

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8.6 Power Consumption - Radio Modes

When measured on the CC1352REM-XD7793-XD24 reference design with T_c = 25 °C, V_{DDS} = 3.6 V with DC/DC enabled unless otherwise noted.
Using boost mode (increasing VDDR up to 1.95 V), will increase system current by 15% (does not apply to TX +14 dBm setting where this current is already included).
Relevant I_{core} and I_{peri} currents are included in below numbers.

PARAMETER		TEST CONDITIONS	TYP	UNIT
	Radio receive current, 868 MHz		5.8	mA
	Radio receive current, 2.44 GHz (BLE)	V_{DDS} = 3.0 V	6.9	mA
	Radio transmit current Sub-1 GHz PA	0 dBm output power setting 868 MHz	8.0	mA
		+10 dBm output power setting 868 MHz	14.3	mA
	Radio transmit current Boost mode, Sub-1 GHz PA	+14 dBm output power setting 868 MHz	24.9	mA
	Radio transmit current 2.4 GHz PA (BLE)	0 dBm output power setting, V_{DDS} = 3.0 V	7.1	mA
	Radio transmit current 2.4 GHz PA (BLE)	+5 dBm output power setting 2440 MHz, V_{DDS} = 3.0 V	9.6	mA

8.7 Nonvolatile (Flash) Memory Characteristics

Over operating free-air temperature range and V_{DDS} = 3.0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Flash sector size			8		KB
Supported flash erase cycles before failure, full bank[1] [5]		30			k Cycles
Supported flash erase cycles before failure, single sector[2]		60			k Cycles
Maximum number of write operations per row before sector erase[3]				83	Write Operations
Flash retention	105 °C	11.4			Years at 105 °C
Flash sector erase current	Average delta current		10.7		mA
Flash sector erase time[4]	Zero cycles		10		ms
Flash write current	Average delta current, 4 bytes at a time		6.2		mA
Flash write time[4]	4 bytes at a time		21.6		µs

(1) A full bank erase is counted as a single erase cycle on each sector
(2) Up to 4 customer-designated sectors can be individually erased an additional 30k times beyond the baseline bank limitation of 30k cycles
(3) Each wordline is 2048 bits (or 256 bytes) wide. This limitation corresponds to sequential memory writes of 4 (3.1) bytes minimum per write over a whole wordline. If additional writes to the same wordline are required, a sector erase is required once the maximum number of write operations per row is reached.
(4) This number is dependent on Flash aging and increases over time and erase cycles
(5) Aborting flash during erase or program modes is not a safe operation.

8.8 Thermal Resistance Characteristics

THERMAL METRIC[1]		PACKAGE RGZ (VQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	23.4	°C/W[2]
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.3	°C/W[2]

8.8 Thermal Resistance Characteristics (continued)

THERMAL METRIC[(1)]		PACKAGE RGZ (VQFN) 48 PINS	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance	8.0	°C/W[(2)]
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W[(2)]
ψ_{JB}	Junction-to-board characterization parameter	7.9	°C/W[(2)]
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	°C/W[(2)]

(1) For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics.
(2) °C/W = degrees Celsius per watt.

8.9 RF Frequency Bands

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	MIN	TYP	MAX	UNIT
Frequency bands	2360		2500	MHz
	1076		1315	
	861		1054	
	431		527	
	359		439	
	287		351	
	143		176	

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8.10 861 MHz to 1054 MHz - Receive (RX)

When measured on the CC1352REM-XD7793-XD24 reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters					
Digital channel filter programmable receive bandwidth		4		4000	kHz
Data rate step size			1.5		bps
Spurious emissions 25 MHz to 1 GHz	868 MHz Conducted emissions measured according to ETSI EN 300 220		< -57		dBm
Spurious emissions 1 GHz to 13 GHz			< -47		dBm
IEEE 802.15.4, 50 kbps, ±25 kHz Deviation, 2-GFSK, 100 kHz RX Bandwidth					
Sensitivity	BER = 10^{-2}, 868 MHz		–110		dBm
Saturation limit	BER = 10^{-2}, 868 MHz		10		dBm
Selectivity, ±200 kHz	BER = 10^{-2}, 868 MHz(1)		44		dB
Selectivity, ±400 kHz	BER = 10^{-2}, 868 MHz(1)		48		dB
Blocking, ±1 MHz	BER = 10^{-2}, 868 MHz(1)		57		dB
Blocking, ±2 MHz	BER = 10^{-2}, 868 MHz(1)		61		dB
Blocking, ±5 MHz	BER = 10^{-2}, 868 MHz(1)		67		dB
Blocking, ±10 MHz	BER = 10^{-2}, 868 MHz(1)		76		dB
Image rejection (image compensation enabled)	BER = 10^{-2}, 868 MHz(1)		39		dB
RSSI dynamic range	Starting from the sensitivity limit		95		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		±3		dB
100 kbps, ±25 kHz Deviation, 2-GFSK, 137 kHz RX Bandwidth					
Sensitivity 100 kbps	1% PER, 127 byte payload, 868 MHz		-104		dBm
Selectivity, ±200 kHz	1% PER, 127 byte payload, 868 MHz. Wanted signal at -96 dBm		31		dB
Selectivity, ±400 kHz	1% PER, 127 byte payload, 868 MHz. Wanted signal at -96 dBm		37		dB
Co-channel rejection	1% PER, 127 byte payload, 868 MHz. Wanted signal at -79 dBm		-9		dB
200 kbps, ±50 kHz Deviation, 2-GFSK, 311 kHz RX Bandwidth					
Sensitivity	BER = 10^{-2}, 868 MHz		–103		dBm
Sensitivity	BER = 10^{-2}, 915 MHz		–103		dBm
Selectivity, ±400 kHz	BER = 10^{-2}, 915 MHz. Wanted signal 3 dB above sensitivity limit.		41		dB
Selectivity, ±800 kHz	BER = 10^{-2}, 915 MHz. Wanted signal 3 dB above sensitivity limit.		47		dB
Blocking, ±2 MHz	BER = 10^{-2}, 915 MHz. Wanted signal 3 dB above sensitivity limit.		55		dB
Blocking, ±10 MHz	BER = 10^{-2}, 915 MHz. Wanted signal 3 dB above sensitivity limit.		67		dB
500 kbps, ±190 kHz Deviation, 2-GFSK, 1150 kHz RX Bandwidth					
Sensitivity 500 kbps	1% PER, 127 byte payload, 915 MHz		-94		dBm
Selectivity, ±1 MHz	1% PER, 127 byte payload, 915 MHz. Wanted signal at -88 dBm		14		dB
Selectivity, ±2 MHz	1% PER, 127 byte payload, 915 MHz. Wanted signal at -88 dBm		42		dB

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8.10 861 MHz to 1054 MHz - Receive (RX) (continued)

When measured on the CC1352REM-XD7793-XD24 reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Co-channel rejection	1% PER, 127 byte payload, 915 MHz. Wanted signal at -71 dBm		-9		dB
1 Mbps, ±350 kHz Deviation, 2-GFSK, 2.2 MHz RX Bandwidth					
Sensitivity	BER = 10^{-2}, 868 MHz		-97		dBm
Sensitivity	BER = 10^{-2}, 915 MHz		-96		dBm
Blocking, +2 MHz	BER = 10^{-2}, 915 MHz. Wanted signal 3 dB above sensitivity limit.		43		dB
Blocking, -2 MHz	BER = 10^{-2}, 915 MHz. Wanted signal 3 dB above sensitivity limit.		26		dB
Blocking, +10 MHz	BER = 10^{-2}, 915 MHz. Wanted signal 3 dB above sensitivity limit.		54		dB
Blocking, -10 MHz	BER = 10^{-2}, 915 MHz. Wanted signal 3 dB above sensitivity limit.		48		dB
SimpleLink™ Long Range, 2.5/5 kbps (20 ksps), ±5 kHz Deviation, 2-GFSK, 34 kHz RX Bandwidth, FEC = 1:2, DSSS = 1:4/1:2					
Sensitivity	2.5 kbps, BER = 10^{-2} , 868 MHz		-121		dBm
Sensitivity	5 kbps, BER = 10^{-2} , 868 MHz		-120		dBm
Saturation limit	2.5 kbps, BER = 10^{-2} , 868 MHz		10		dBm
Selectivity, ±100 kHz	2.5 kbps, BER = 10^{-2}, 868 MHz[(1)]		49		dB
Selectivity, ±200 kHz	2.5 kbps, BER = 10^{-2}, 868 MHz[(1)]		50		dB
Selectivity, ±300 kHz	2.5 kbps, BER = 10^{-2}, 868 MHz[(1)]		51		dB
Blocking, ±1 MHz	2.5 kbps, BER = 10^{-2}, 868 MHz[(1)]		63		dB
Blocking, ±2 MHz	2.5 kbps, BER = 10^{-2}, 868 MHz[(1)]		68		dB
Blocking, ±5 MHz	2.5 kbps, BER = 10^{-2}, 868 MHz[(1)]		78		dB
Blocking, ±10 MHz	2.5 kbps, BER = 10^{-2}, 868 MHz[(1)]		88		dB
Image rejection (image compensation enabled)	2.5 kbps, BER = 10^{-2}, 868 MHz[(1)]		45		dB
RSSI dynamic range	Starting from the sensitivity limit		97		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		±3		dB
4.8 kbps, OOK, 39 kHz RX Bandwidth					
Sensitivity	BER = 10^{-2}, 868 MHz, 38.9 kHz RX bandwidth		-115		dBm
Sensitivity	BER = 10^{-2}, 915 MHz, 41.0 kHz RX bandwidth		-115		dBm
Narrowband, 9.6 kbps, ±2.4 kHz Deviation, 2-GFSK, 17.1 kHz RX Bandwidth					
Sensitivity	BER = 10^{-2}, 868 MHz		-118		dBm
Adjacent Channel Rejection	BER = 10^{-2}, 868 MHz. Wanted signal 3 dB above the ETSI reference sensitivity limit (-104.6 dBm). Interferer ±20 kHz		39		dB
Alternate Channel Rejection	BER = 10^{-2}, 868 MHz. Wanted signal 3 dB above the ETSI reference sensitivity limit (-104.6 dBm). Interferer ±40 kHz		40		dB
Blocking, ±1 MHz	BER = 10^{-2}, 868 MHz. Wanted signal 3 dB above the ETSI reference sensitivity limit (-104.6 dBm).		65		dB
Blocking, ±2 MHz	BER = 10^{-2}, 868 MHz. Wanted signal 3 dB above the ETSI reference sensitivity limit (-104.6 dBm).		69		dB
Blocking, ±10 MHz	BER = 10^{-2}, 868 MHz. Wanted signal 3 dB above the ETSI reference sensitivity limit (-104.6 dBm).		85		dB
Wi-SUN					

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8.10 861 MHz to 1054 MHz - Receive (RX) (continued)

When measured on the CC1352REM-XD7793-XD24 reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Sensitivity	50 kbps, ±12.5 kHz deviation, 2-GFSK, 868 MHz, 68 kHz RX BW, 10% PER, 250 byte payload		-107		dBm
Sensitivity	100 kbps, ±25 kHz deviation, 2-GFSK, 868 MHz, 135 kHz RX BW, 10% PER, 250 byte payload		-104		dBm
Sensitivity	100 kbps, ±50 kHz deviation, 2-GFSK, 920.9 MHz, 196 kHz RX BW, 10% PER, 250 byte payload		-102		dBm
Sensitivity	200 kbps, ±100 kHz deviation, 2-GFSK, 920.8 MHz, 273 kHz RX BW, 10% PER, 250 byte payload		-99		dBm
WB-DSSS, 30/60/120/240 kbps (480 ksps), ±195 kHz Deviation, 2-GFSK, 622 RX Bandwidth, FEC = 1:2, DSSS = 1:8/1:4/1:2/1:1					
Sensitivity	30 kbps, BER = 10^{-2}, 915 MHz		-109		dBm
Sensitivity	60 kbps, BER = 10^{-2}, 915 MHz		-108		dBm
Sensitivity	120 kbps, BER = 10^{-2}, 915 MHz		-106		dBm
Sensitivity	240 kbps, BER = 10^{-2}, 915 MHz		-105		dBm
Blocking ±1 MHz	240 kbps, BER = 10^{-2}, 915 MHz		49		dB
Blocking ±2 MHz	240 kbps, BER = 10^{-2}, 915 MHz		53		dB
Blocking ±5 MHz	240 kbps, BER = 10^{-2}, 915 MHz		54		dB
Blocking ±10 MHz	240 kbps, BER = 10^{-2}, 915 MHz		65		dB

(1) Wanted signal 3 dB above the reference sensitivity limit according to ETSI EN 300 220 v. 3.1.1

8.11 861 MHz to 1054 MHz - Transmit (TX)

When measured on the CC1352REM-XD7793-XD24 reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted. [1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
General parameters						
Max output power, boost mode Sub-1 GHz PA[2]		VDDR = 1.95 V Minimum supply voltage (VDDS) for boost mode is 2.1 V 868 MHz and 915 MHz		14		dBm
Max output power, Sub-1 GHz PA[2]		868 MHz and 915 MHz		12		dBm
Output power programmable range Sub-1 GHz PA		868 MHz and 915 MHz		24		dB
Output power variation over temperature Sub-1 GHz PA		+10 dBm setting Over recommended temperature operating range		±2		dB
Output power variation over temperature Boost mode, Sub-1 GHz PA		+14 dBm setting Over recommended temperature operating range		±1.5		dB
Spurious emissions and harmonics						
Spurious emissions (excluding harmonics) Sub-1 GHz PA, 868 MHz [3]	30 MHz to 1 GHz	+14 dBm setting ETSI restricted bands		< -54		dBm
		+14 dBm setting ETSI outside restricted bands		< -36		dBm
	1 GHz to 12.75 GHz (outside ETSI restricted bands)	+14 dBm setting measured in 1 MHz bandwidth (ETSI)		< -30		dBm
Adjacent Channel Power	9.6 kbps, ±2.4 kHz deviation, 2-GFSK, 20 kHz channel spacing. Narrowband mode.	Adjacent channel (ETSI EN 300 220 requirement). TxPower = 12.5 dBm. 868 MHz		-24		dBm
Alternate Channel Power	9.6 kbps, ±2.4 kHz deviation, 2-GFSK, 20 kHz channel spacing. Narrowband mode.	Alternate channel (ETSI EN 300 220 requirement). TxPower = 12.5 dBm. 868 MHz		-31		dBm
Spurious emissions out-of-band Sub-1 GHz PA, 915 MHz [3]	30 MHz to 88 MHz (within FCC restricted bands)	+14 dBm setting		< -56		dBm
	88 MHz to 216 MHz (within FCC restricted bands)	+14 dBm setting		< -52		dBm
	216 MHz to 960 MHz (within FCC restricted bands)	+14 dBm setting		< -50		dBm
	960 MHz to 2390 MHz and above 2483.5 MHz (within FCC restricted band)	+14 dBm setting		<-42		dBm
	1 GHz to 12.75 GHz (outside FCC restricted bands)	+14 dBm setting		< -40		dBm

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8.11 861 MHz to 1054 MHz - Transmit (TX) (continued)

When measured on the CC1352REM-XD7793-XD24 reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted. [(1)]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Spurious emissions out-of-band Sub-1 GHz PA, 920.6/928 MHz [(3)]	Below 710 MHz (ARIB T-108)	+14 dBm setting		< -36		dBm
	710 MHz to 900 MHz (ARIB T-108)	+14 dBm setting		< -55		dBm
	900 MHz to 915 MHz (ARIB T-108)	+14 dBm setting		< -55		dBm
	930 MHz to 1000 MHz (ARIB T-108)	+14 dBm setting		< -55		dBm
	1000 MHz to 1215 MHz (ARIB T-108)	+14 dBm setting		< -45		dBm
	Above 1215 MHz (ARIB T-108)	+14 dBm setting		< -30		dBm
Harmonics Sub-1 GHz PA	Second harmonic	+14 dBm setting, 868 MHz		< -30		dBm
		+14 dBm setting, 915 MHz		< -30		
	Third harmonic	+14 dBm setting, 868 MHz		< -30		dBm
		+14 dBm setting, 915 MHz		< -42		
	Fourth harmonic	+14 dBm setting, 868 MHz		< -30		dBm
		+14 dBm setting, 915 MHz		< -30		
	Fifth harmonic	+14 dBm setting, 868 MHz		< -30		dBm
		+14 dBm setting, 915 MHz		< -42		

(1) Some combinations of frequency, data rate and modulation format requires use of external crystal load capacitors for regulatory compliance. More details can be found in the device errata.
(2) Output power is dependent on RF match. For dual-band devices in the CC13x2 platform, output power might be slightly reduced depending on RF layout trade-offs.
(3) Suitable for systems targeting compliance with EN 300 220, EN 303 131, EN 303 204, FCC CFR47 Part 15, ARIB STD-T108.

8.12 861 MHz to 1054 MHz - PLL Phase Noise Wideband Mode

When measured on the CC1352REM-XD7793-XD24 reference design with T_c = 25 °C, V_{DDS} = 3.0 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise in the 868- and 915-MHz bands 20 kHz PLL loop bandwidth	±10 kHz offset		–74		dBc/Hz
	±100 kHz offset		–97		dBc/Hz
	±200 kHz offset		–107		dBc/Hz
	±400 kHz offset		–113		dBc/Hz
	±1000 kHz offset		–120		dBc/Hz
	±2000 kHz offset		–127		dBc/Hz
	±10000 kHz offset		–141		dBc/Hz

8.13 861 MHz to 1054 MHz - PLL Phase Noise Narrowband Mode

When measured on the CC1352REM-XD7793-XD24 reference design with T_c = 25 °C, V_{DDS} = 3.0 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise in the 868- and 915-MHz bands 150 kHz PLL loop bandwith	±10 kHz offset		–93		dBc/Hz
	±100 kHz offset		–93		dBc/Hz
	±200 kHz offset		–94		dBc/Hz
	±400 kHz offset		–104		dBc/Hz
	±1000 kHz offset		–121		dBc/Hz
	±2000 kHz offset		–130		dBc/Hz
	±10000 kHz offset		–140		dBc/Hz

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8.14 359 MHz to 527 MHz - Receive (RX)

When measured on the LAUNCHXL-CC1352P-4 reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters					
Spurious emissions 25 MHz to 1 GHz	433.92 MHz Conducted emissions measured according to ETSI EN 300 220		< -57		dBm
Spurious emissions 1 GHz to 13 GHz			< -47		dBm
IEEE 802.15.4, 50 kbps, ±25 kHz Deviation, 2-GFSK, 78 kHz RX Bandwidth					
Sensitivity	BER = 10^{-2}, 433.92 MHz		–110		dBm
Saturation limit	BER = 10^{-2}, 433.92 MHz		10		dBm
Selectivity, +200 kHz	BER = 10^{-2}, 433.92 MHz[(1)]		48		dB
Selectivity, -200 kHz	BER = 10^{-2}, 433.92 MHz[(1)]		43		dB
Selectivity, +400 kHz	BER = 10^{-2}, 433.92 MHz[(1)]		53		dB
Selectivity, -400 kHz	BER = 10^{-2}, 433.92 MHz[(1)]		44		dB
Blocking, +1 MHz	BER = 10^{-2}, 433.92 MHz[(1)]		60		dB
Blocking, -1 MHz	BER = 10^{-2}, 433.92 MHz[(1)]		54		dB
Blocking, +2 MHz	BER = 10^{-2}, 433.92 MHz[(1)]		62		dB
Blocking, -2 MHz	BER = 10^{-2}, 433.92 MHz[(1)]		61		dB
Blocking, +10 MHz	BER = 10^{-2}, 433.92 MHz[(1)]		75		dB
Blocking, -10 MHz	BER = 10^{-2}, 433.92 MHz[(1)]		75		dB
Image rejection (image compensation enabled)	BER = 10^{-2}, 433.92 MHz[(1)]		44		dB
RSSI dynamic range	Starting from the sensitivity limit		95		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		±3		dB
200 kbps, ±50 kHz Deviation, 2-GFSK, 273 kHz RX Bandwidth					
Sensitivity	BER = 10^{-2}, 433.92 MHz		–104		dBm
Saturation limit	BER = 10^{-2}, 433.92 MHz		10		dBm
Selectivity, ±400 kHz	BER = 10^{-2}, 433.92 MHz[(1)]		48		dB
Blocking, ±1 MHz	BER = 10^{-2}, 433.92 MHz[(1)]		51		dB
Blocking, ±2 MHz	BER = 10^{-2}, 433.92 MHz[(1)]		53		dB
Blocking, ±10 MHz	BER = 10^{-2}, 433.92 MHz[(1)]		68		dB
Image rejection (image compensation enabled)	BER = 10^{-2}, 433.92 MHz[(1)]		45		dB
RSSI dynamic range	Starting from the sensitivity limit		89		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		±3		dB
Narrowband, 4.8 kbps, ±2 kHz Deviation, 2-GFSK, 10.1 kHz RX Bandwidth					
Sensitivity	BER = 10^{-2}, 426.1 MHz		–120		dBm
Saturation limit	BER = 10^{-2}, 426.1 MHz		10		dBm
Selectivity, +12.5 kHz	BER = 10^{-2}, 426.1 MHz[(1)]		53		dB
Selectivity, -12.5 kHz	BER = 10^{-2}, 426.1 MHz[(1)]		52		dB
Selectivity, +25 kHz	BER = 10^{-2}, 426.1 MHz[(1)]		53		dB
Selectivity, -25 kHz	BER = 10^{-2}, 426.1 MHz[(1)]		52		dB
Blocking, +1 MHz	BER = 10^{-2}, 426.1 MHz[(1)]		70		dB
Blocking, -1 MHz	BER = 10^{-2}, 426.1 MHz[(1)]		66		dB
Blocking, +2 MHz	BER = 10^{-2}, 426.1 MHz[(1)]		72		dB

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8.14 359 MHz to 527 MHz - Receive (RX) (continued)

When measured on the LAUNCHXL-CC1352P-4 reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Blocking, -2 MHz	BER = 10^{-2}, 426.1 MHz(1)		70		dB
Blocking, +10 MHz	BER = 10^{-2}, 426.1 MHz(1)		84		dB
Blocking, -10 MHz	BER = 10^{-2}, 426.1 MHz(1)		84		dB
Image rejection (image compensation enabled)	BER = 10^{-2}, 426.1 MHz(1)		44		dB
RSSI dynamic range	Starting from the sensitivity limit		102		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		±3		dB
4.8 kbps, OOK, 34.1 kHz RX Bandwidth					
Sensitivity	BER = 10^{-2}, 433.92 MHz		-116		dBm
SimpleLink™ Long Range, 2.5/5 kbps (20 ksps), ±5 kHz Deviation, 2-GFSK, 34 kHz RX Bandwidth, FEC = 1:2, DSSS = 1:4/1:2					
Sensitivity	2.5 kbps, BER = 10^{-2}, 433.92 MHz		-121		dBm
Sensitivity	5 kbps, BER = 10^{-2}, 433.92 MHz		-119		dBm
Saturation limit	5 kbps, BER = 10^{-2}, 433.92 MHz		10		dBm
Selectivity, +100 kHz	5 kbps, BER = 10^{-2}, 433.92 MHz(1)		55		dB
Selectivity, -100 kHz	5 kbps, BER = 10^{-2}, 433.92 MHz(1)		53		dB
Blocking, +1 MHz	5 kbps, BER = 10^{-2}, 433.92 MHz(1)		69		dB
Blocking, -1 MHz	5 kbps, BER = 10^{-2}, 433.92 MHz(1)		65		dB
Blocking, +2 MHz	5 kbps, BER = 10^{-2}, 433.92 MHz(1)		71		dB
Blocking, -2 MHz	5 kbps, BER = 10^{-2}, 433.92 MHz(1)		70		dB
Blocking, +10 MHz	5 kbps, BER = 10^{-2}, 433.92 MHz(1)		84		dB
Blocking, -10 MHz	5 kbps, BER = 10^{-2}, 433.92 MHz(1)		84		dB
Image rejection (image compensation enabled)	5 kbps, BER = 10^{-2}, 433.92 MHz		49		dB
RSSI dynamic range	Starting from the sensitivity limit		101		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		±3		dB

(1) Wanted signal 3 dB above sensitivity limit

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8.15 359 MHz to 527 MHz - Transmit (TX)

When measured on the LAUNCHXL-CC1352P-4 reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted. (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
General parameters						
Max output power, Sub-1 GHz PA(2)		433.92 MHz, without BOOST (VDDR = 1.7 V)		13		dBm
Output power programmable range Sub-1 GHz PA		433.92 MHz, without BOOST (VDDR = 1.7 V)		24		dB
Output power variation over temperature, Sub-1 GHz PA		+13 dBm setting. 433.92 MHz Over recommended temperature operating range		±1.5		dB
Spurious emissions and harmonics						
Spurious emissions (excluding harmonics) Sub-1 GHz PA, 433.92 MHz (3)	30 MHz to 1 GHz	+10 dBm setting ETSI restricted bands		< -54		dBm
		+10 dBm setting ETSI outside restricted bands		< -36		dBm
	1 GHz to 12.75 GHz (outside ETSI restricted bands)	+10 dBm setting measured in 1 MHz bandwidth (ETSI)		< -30		dBm
Spurious emissions out-of-band Sub-1 GHz PA, 429 MHz (3)	Outside the necessary requency band (ARIB T-67)	+10 dBm setting		< -26		dBm
	710 MHz to 900 MHz (ARIB T-67)	+10 dBm setting		< -55		dBm
	900 MHz to 915 MHz (ARIB T-67)	+10 dBm setting		< -55		dBm
	930 MHz to 1000 MHz (ARIB T-67)	+10 dBm setting		< -55		dBm
	1000 MHz to 1215 MHz (ARIB T-67)	+10 dBm setting		< -45		dBm
	Above 1215 MHz (ARIB T-67)	+10 dBm setting		< -30		dBm
Harmonics Sub-1 GHz PA	Second harmonic	+13 dBm setting, 433 MHz		< -36		dBm
Harmonics Sub-1 GHz PA	Third harmonic	+13 dBm setting, 433 MHz		< -30		dBm
Harmonics Sub-1 GHz PA	Fourth harmonic	+13 dBm setting, 433 MHz		< -30		dBm
Harmonics Sub-1 GHz PA	Fifth harmonic	+13 dBm setting, 433 MHz		< -30		dBm

(1) Some combinations of frequency, data rate and modulation format requires use of external crystal load capacitors for regulatory compliance. More details can be found in the device errata.
(2) Output power is dependent on RF match. For dual-band devices in the CC13x2 platform, output power might be slightly reduced depending on RF layout trade-offs.
(3) Suitable for systems targeting compliance with EN 300 220, EN 303 131, EN 303 204, FCC CFR47 Part 15, ARIB STD-T108.

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8.16 359 MHz to 527 MHz - PLL Phase Noise

When measured on the LAUNCHXL-CC1352P-4 reference design with T_c = 25 °C, V_{DDS} = 3.0 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise in the 429 MHz band 200 kHz PLL loop bandwidth	±10 kHz offset		-103		dBc/Hz
	±100 kHz offset		-101		dBc/Hz
	±200 kHz offset		-101		dBc/Hz
	±400 kHz offset		-106		dBc/Hz
	±1000 kHz offset		-122		dBc/Hz
	±2000 kHz offset		-133		dBc/Hz
	±10000 kHz offset		-143		dBc/Hz
Phase noise in the 433 MHz band 20 kHz PLL loop bandwidth	±10 kHz offset		-86		dBc/Hz
	±100 kHz offset		-108		dBc/Hz
	±200 kHz offset		-115		dBc/Hz
	±400 kHz offset		-122		dBc/Hz
	±1000 kHz offset		-130		dBc/Hz
	±2000 kHz offset		-137		dBc/Hz
	±10000 kHz offset		-145		dBc/Hz

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8.17 143 MHz to 176 MHz - Receive (RX)

When measured on the CC1352EM-XS169-XS24 reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters					
Spurious emissions 25 MHz to 1 GHz	169.44375 MHz Conducted emissions measured according to ETSI EN 300 220		< -57		dBm
Spurious emissions 1 GHz to 13 GHz			< -47		dBm
WMBUS N-MODE, 4.8 kbps, ±2.4 kHz Deviation, 2-GFSK, 10 kHz RX Bandwidth					
Sensitivity 4.8 kbps ± 2.4 kHz	BER = 10^{-2}, 169.40625 MHz		–119		dBm
Saturation limit	BER = 10^{-2}, 169.40625 MHz		10		dBm
Selectivity, +12.5 kHz (1)	BER = 10^{-2}, 169.40625 MHz		51		dB
Selectivity, -12.5 kHz (1)	BER = 10^{-2}, 169.40625 MHz		51		dB
Selectivity, +25 kHz (1)	BER = 10^{-2}, 169.40625 MHz		52		dB
Selectivity, -25 kHz (1)	BER = 10^{-2}, 169.40625 MHz		52		dB
Blocking, +1 MHz (1)	BER = 10^{-2}, 169.40625 MHz		73		dB
Blocking, -1 MHz (1)	BER = 10^{-2}, 169.40625 MHz		72		dB
Blocking, +2 MHz (1)	BER = 10^{-2}, 169.40625 MHz		77		dB
Blocking, -2 MHz (1)	BER = 10^{-2}, 169.40625 MHz		75		dB
Blocking, +10 MHz (1)	BER = 10^{-2}, 169.40625 MHz		86		dB
Blocking, -10 MHz (1)	BER = 10^{-2}, 169.40625 MHz		86		dB
Image rejection (image compensation enabled) (1)	BER = 10^{-2}, 169.40625 MHz		46		dB
RSSI dynamic range	Starting from the sensitivity limit		91		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		±3		dB
WMBUS N-MODE, 2.4 kbps, ±2.4 kHz Deviation, 2-GFSK, 10 kHz RX Bandwidth					
Sensitivity	BER = 10^{-2}, 169.43125 MHz		–121		dBm
Saturation limit	BER = 10^{-2}, 169.43125 MHz		10		dBm
Selectivity, +12.5 kHz (1)	BER = 10^{-2}, 169.43125 MHz		51		dB
Selectivity, -12.5 kHz (1)	BER = 10^{-2}, 169.43125 MHz		51		dB
Selectivity, +25 kHz (1)	BER = 10^{-2}, 169.43125 MHz		52		dB
Selectivity, -25 kHz (1)	BER = 10^{-2}, 169.43125 MHz		52		dB
Blocking, +1 MHz (1)	BER = 10^{-2}, 169.43125 MHz		74		dB
Blocking, -1 MHz (1)	BER = 10^{-2}, 169.43125 MHz		73		dB
Blocking, +2 MHz (1)	BER = 10^{-2}, 169.43125 MHz		78		dB
Blocking, -2 MHz (1)	BER = 10^{-2}, 169.43125 MHz		77		dB
Blocking, +10 MHz (1)	BER = 10^{-2}, 169.43125 MHz		88		dB
Blocking, -10 MHz (1)	BER = 10^{-2}, 169.43125 MHz		87		dB
Image rejection (image compensation enabled) (1)	BER = 10^{-2}, 169.43125 MHz		50		dB
RSSI dynamic range	Starting from the sensitivity limit		92		dB
RSSI accuracy	Starting from the sensitivity limit across the given dynamic range		±3		dB

(1) Wanted signal 3 dB above sensitivity limit

8.18 143 MHz to 176 MHz - Transmit (TX)

When measured on the CC1352EM-XS169-XS24 reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
General parameters						
Min output power, Sub-1 GHz PA(1)	Min output power, Sub-1 GHz PA(1)	169.44375 MHz, without BOOST (VDDR = 1.7 V), single ended configuration.		-10		dBm
Max output power, Sub-1 GHz PA(1)		169.44375 MHz, without BOOST (VDDR = 1.7 V), single ended configuration.		9		dBm
Adjacent channel power Sub-1 GHz PA		0 dBm setting, 4.8 kbit/s, 169.44375 MHz, without BOOST (VDDR = 1.7 V), single ended configuration.		-47		dBc
Spurious emissions and harmonics						
Spurious emissions (excluding harmonics) Sub-1 GHz PA, 433.92 MHz (2)	30 MHz to 1 GHz	0 dBm setting, ETSI restricted bands. Measured in 100 kHz bandwidth		< -54		dBm
		0 dBm setting, ETSI outside restricted bands		< -36		dBm
	1 GHz to 12.75 GHz (outside ETSI restricted bands)	0 dBm setting, measured in 1 MHz bandwidth (ETSI)		< -30		dBm
Harmonics Sub-1 GHz PA	Second harmonic	0 dBm setting, 169.44375 MHz		< -36		dBm
Harmonics Sub-1 GHz PA	Third harmonic	0 dBm setting, 169.44375 MHz		< -54		dBm
Harmonics Sub-1 GHz PA	Fourth harmonic	0 dBm setting, 169.44375 MHz		< -54		dBm
Harmonics Sub-1 GHz PA	Fifth harmonic	0 dBm setting, 169.44375 MHz		< -36		dBm

(1) Output power is dependent on RF match. For dual-band devices in the CC13x2 platform, output power might be slightly reduced depending on RF layout trade-offs.
(2) Suitable for systems targeting compliance with EN 300 220.

8.19 143 MHz to 176 MHz - PLL Phase Noise

When measured on the CC1352REM-XD7793-XD24 reference design with T_c = 25 °C, V_{DDS} = 3.0 V. PLL settings for narrowband operation is used.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise in the 169 MHz band, 150 kHz PLL loop bandwidth	±10 kHz offset		– 108		dBc/Hz
	±100 kHz offset		– 108		dBc/Hz
	±200 kHz offset		– 110		dBc/Hz
	±400 kHz offset		-114		dBc/Hz
	±1000 kHz offset		-131		dBc/Hz
	±2000 kHz offset		– 141		dBc/Hz
	±10000 kHz offset		-150		dBc/Hz

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8.20 Bluetooth Low Energy - Receive (RX)

When measured on the CC1352REM-XD7793-XD24 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF}= 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
125 kbps (LE Coded)					
Receiver sensitivity	Differential mode. BER = 10^{-3}		–105		dBm
Receiver saturation	Differential mode. BER = 10^{-3}		>5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–300 / 300)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–320 / 240)		ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (255-byte packets)		> (–125 / 125)		ppm
Co-channel rejection(1)	Wanted signal at –79 dBm, modulated interferer in channel, BER = 10^{-3}		–1.5		dB
Selectivity, ±1 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		8 / 4.5(2)		dB
Selectivity, ±2 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ±2 MHz, BER = 10^{-3}		44 / 39 (2)		dB
Selectivity, ±3 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}		46 / 44(2)		dB
Selectivity, ±4 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		44 / 46(2)		dB
Selectivity, ±6 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ⩾ ±6 MHz, BER = 10^{-3}		48 / 44(2)		dB
Selectivity, ±7 MHz	Wanted signal at –79 dBm, modulated interferer at ⩾ ±7 MHz, BER = 10^{-3}		51 / 45(2)		dB
Selectivity, Image frequency(1)	Wanted signal at –79 dBm, modulated interferer at image frequency, BER = 10^{-3}		39		dB
Selectivity, Image frequency ±1 MHz(1)	Note that Image frequency + 1 MHz is the Co-channel –1 MHz. Wanted signal at –79 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}		4.5 / 44 (2)		dB
500 kbps (LE Coded)					
Receiver sensitivity	Differential mode. BER = 10^{-3}		–100		dBm
Receiver saturation	Differential mode. BER = 10^{-3}		> 5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–300 / 300)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–450 / 450)		ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (255-byte packets)		> (–175 / 175)		ppm
Co-channel rejection(1)	Wanted signal at –72 dBm, modulated interferer in channel, BER = 10^{-3}		–3.5		dB
Selectivity, ±1 MHz(1)	Wanted signal at –72 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		8 / 4(2)		dB
Selectivity, ±2 MHz(1)	Wanted signal at –72 dBm, modulated interferer at ±2 MHz, BER = 10^{-3}		44 / 37 (2)		dB
Selectivity, ±3 MHz(1)	Wanted signal at –72 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}		46 / 46(2)		dB

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8.20 Bluetooth Low Energy - Receive (RX) (continued)

When measured on the CC1352REM-XD7793-XD24 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF}= 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Selectivity, ±4 MHz(1)	Wanted signal at –72 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		45 / 47(2)		dB
Selectivity, ±6 MHz(1)	Wanted signal at –72 dBm, modulated interferer at ⩾ ±6 MHz, BER = 10^{-3}		46 / 45(2)		dB
Selectivity, ±7 MHz	Wanted signal at –72 dBm, modulated interferer at ⩾ ±7 MHz, BER = 10^{-3}		49 / 45(2)		dB
Selectivity, Image frequency(1)	Wanted signal at –72 dBm, modulated interferer at image frequency, BER = 10^{-3}		37		dB
Selectivity, Image frequency ±1 MHz(1)	Note that Image frequency + 1 MHz is the Co-channel –1 MHz. Wanted signal at –72 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}		4 / 46(2)		dB
1 Mbps (LE 1M)					
Receiver sensitivity	Differential mode. BER = 10^{-3}		–97		dBm
Receiver saturation	Differential mode. BER = 10^{-3}		> 5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–350 / 350)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–750 / 750)		ppm
Co-channel rejection(1)	Wanted signal at –67 dBm, modulated interferer in channel, BER = 10^{-3}		–6		dB
Selectivity, ±1 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		7 / 4(2)		dB
Selectivity, ±2 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±2 MHz,BER = 10^{-3}		40 / 33(2)		dB
Selectivity, ±3 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}		36 / 41 (2)		dB
Selectivity, ±4 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		36 / 45(2)		dB
Selectivity, ±5 MHz or more(1)	Wanted signal at –67 dBm, modulated interferer at ⩾ ±5 MHz, BER = 10^{-3}		40		dB
Selectivity, image frequency(1)	Wanted signal at –67 dBm, modulated interferer at image frequency, BER = 10^{-3}		33		dB
Selectivity, image frequency ±1 MHz(1)	Note that Image frequency + 1 MHz is the Co-channel –1 MHz. Wanted signal at –67 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}		4 / 41(2)		dB
Out-of-band blocking(3)	30 MHz to 2000 MHz		–10		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		–18		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		–12		dBm
Out-of-band blocking	3000 MHz to 12.75 GHz		–2		dBm
Intermodulation	Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level		–42		dBm
Spurious emissions, 30 to 1000 MHz(4)	Measurement in a 50-Ω single-ended load.		< –59		dBm

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8.20 Bluetooth Low Energy - Receive (RX) (continued)

When measured on the CC1352REM-XD7793-XD24 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF}= 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Spurious emissions, 1 to 12.75 GHz[(4)]	Measurement in a 50-Ω single-ended load.		< –47		dBm
RSSI dynamic range			70		dB
RSSI accuracy			±4		dB
2 Mbps (LE 2M)					
Receiver sensitivity	Differential mode. Measured at SMA connector, BER = 10^{-3}		–92		dBm
Receiver saturation	Differential mode. Measured at SMA connector, BER = 10^{-3}		> 5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–500 / 500)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–700 / 750)		ppm
Co-channel rejection[(1)]	Wanted signal at –67 dBm, modulated interferer in channel,BER = 10^{-3}		–7		dB
Selectivity, ±2 MHz[(1)]	Wanted signal at –67 dBm, modulated interferer at ±2 MHz, Image frequency is at –2 MHz, BER = 10^{-3}		8 / 4[(2)]		dB
Selectivity, ±4 MHz[(1)]	Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		36 / 36 [(2)]		dB
Selectivity, ±6 MHz[(1)]	Wanted signal at –67 dBm, modulated interferer at ±6 MHz, BER = 10^{-3}		37 / 36[(2)]		dB
Selectivity, image frequency[(1)]	Wanted signal at –67 dBm, modulated interferer at image frequency, BER = 10^{-3}		4		dB
Selectivity, image frequency ±2 MHz[(1)]	Note that Image frequency + 2 MHz is the Co-channel. Wanted signal at –67 dBm, modulated interferer at ±2 MHz from image frequency, BER = 10^{-3}		–7 / 36[(2)]		dB
Out-of-band blocking[(3)]	30 MHz to 2000 MHz		–16		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		–21		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		–15		dBm
Out-of-band blocking	3000 MHz to 12.75 GHz		–12		dBm
Intermodulation	Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2408 and 2414 MHz respectively, at the given power level		–38		dBm

(1) Numbers given as I/C dB
(2) X / Y, where X is +N MHz and Y is –N MHz
(3) Excluding one exception at F_{wanted} / 2, per Bluetooth Specification
(4) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)

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8.21 Bluetooth Low Energy - Transmit (TX)

When measured on the CC1352REM-XD7793-XD24 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF}= 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
General Parameters						
Max output power, 2.4 GHz PA	Differential mode, delivered to a single-ended 50 Ω load through a balun			5		dBm
Output power programmable range, 2.4 GHz PA	Differential mode, delivered to a single-ended 50 Ω load through a balun			26		dB
Spurious emissions and harmonics						
Spurious emissions, 2.4 GHz PA (1)	f < 1 GHz, outside restricted bands	+5 dBm setting		< –36		dBm
	f < 1 GHz, restricted bands ETSI			< –54		dBm
	f < 1 GHz, restricted bands FCC			< –55		dBm
	f > 1 GHz, including harmonics			< –42		dBm
Harmonics, 2.4 GHz PA (1)	Second harmonic			< –42		dBm
	Third harmonic			< –42		dBm

(1) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

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8.22 Zigbee and Thread - IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) - RX

When measured on the CC1352REM-XD7793-XD24 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF}= 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters					
Receiver sensitivity	PER = 1%		–100		dBm
Receiver saturation	PER = 1%		> 5		dBm
Adjacent channel rejection	Wanted signal at –82 dBm, modulated interferer at ±5 MHz, PER = 1%		36		dB
Alternate channel rejection	Wanted signal at –82 dBm, modulated interferer at ±10 MHz, PER = 1%		57		dB
Channel rejection, ±15 MHz or more	Wanted signal at –82 dBm, undesired signal is IEEE 802.15.4 modulated channel, stepped through all channels 2405 to 2480 MHz, PER = 1%		59		dB
Blocking and desensitization, 5 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		57		dB
Blocking and desensitization, 10 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		63		dB
Blocking and desensitization, 20 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		63		dB
Blocking and desensitization, 50 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		66		dB
Blocking and desensitization, –5 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		60		dB
Blocking and desensitization, –10 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		60		dB
Blocking and desensitization, –20 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		63		dB
Blocking and desensitization, –50 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		65		dB
Spurious emissions, 30 MHz to 1000 MHz(1)	Measurement in a 50-Ω single-ended load		–66		dBm
Spurious emissions, 1 GHz to 12.75 GHz(1)	Measurement in a 50-Ω single-ended load		–53		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> 350		ppm
Symbol rate error tolerance	Difference between incoming symbol rate and the internally generated symbol rate		> 1000		ppm
RSSI dynamic range			95		dB
RSSI accuracy			±4		dB

(1) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)

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8.23 Zigbee and Thread - IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) - TX

When measured on the CC1352REM-XD7793-XD24 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF}= 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
General Parameters						
Max output power, 2.4 GHz PA	Differential mode, delivered to a single-ended 50-Ω load through a balun			5		dBm
Output power programmable range, 2.4 GHz PA	Differential mode, delivered to a single-ended 50-Ω load through a balun			26		dB
Spurious emissions and harmonics						
Spurious emissions, 2.4 GHz PA (1) (2)	f < 1 GHz, outside restricted bands	+5 dBm setting		< -36		dBm
	f < 1 GHz, restricted bands ETSI			< -47		dBm
	f < 1 GHz, restricted bands FCC			< -55		dBm
	f > 1 GHz, including harmonics			< –42		dBm
Harmonics, 2.4 GHz PA (1)	Second harmonic			< -42		dBm
	Third harmonic			< -42		dBm
IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps)						
Error vector magnitude, 2.4-GHz PA	+5 dBm setting			2		%

(1) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).
(2) To ensure margins for passing FCC band edge requirements at 2483.5 MHz, a lower than maximum output-power setting or less than 100% duty cycle may be used when operating at 2480 MHz.

8.24 Timing and Switching Characteristics

8.24.1 Reset Timing

PARAMETER	MIN	TYP	MAX	UNIT
RESET_N low duration	1			µs

8.24.2 Wakeup Timing

Measured over operating free-air temperature with V_{DDS} = 3.0 V (unless otherwise noted). The times listed here do not include software overhead.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MCU, Reset to Active(1)			850 - 3000		µs
MCU, Shutdown to Active(1)			850 - 3000		µs
MCU, Standby to Active			160		µs
MCU, Active to Standby			36		µs
MCU, Idle to Active			14		µs

(1) The wakeup time is dependent on remaining charge on VDDR capacitor when starting the device, and thus how long the device has been in Reset or Shutdown before starting up again. The wake up time increases with a higher capacitor value.

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8.24.3 Clock Specifications

8.24.3.1 48 MHz Clock Input (TCXO)

Measured on a Texas Instruments reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.(1) (2)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Clock frequency			48		MHz
	TCXO clipped sine output, peak-to-peak	TCXO clipped sine output connected to pin X48M_P through series capacitor	0.8		1.7	V
	TCXO with CMOS output, High input voltage	TCXO with CMOS output directly coupled to pin X48M_P	1.3		VDDR	V
	TCXO with CMOS output, Low input voltage		0		0.3	V

(1) Probing or otherwise stopping the TCXO while the DC/DC converter is enabled may cause permanent damage to the device.
(2) See CC13xx/CC26xx Hardware Configuration and PCB Design Considerations on how to add TCXO support

8.24.3.2 48 MHz Crystal Oscillator (XOSC_HF)

Measured on a Texas Instruments reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.(1)

	PARAMETER	MIN	TYP	MAX	UNIT
	Crystal frequency		48		MHz
ESR	Equivalent series resistance 6 pF < C_L ⩽ 9 pF		20	60	Ω
ESR	Equivalent series resistance 5 pF < C_L ⩽ 6 pF			80	Ω
L_M	Motional inductance, relates to the load capacitance that is used for the crystal (C_L in Farads)(5)		$< 3 \times 10^{-25} / C_L^2$		H
C_L	Crystal load capacitance(4)	5	7(3)	9	pF
	Start-up time(2)		200		µs

(1) Probing or otherwise stopping the crystal while the DC/DC converter is enabled may cause permanent damage to the device.
(2) Start-up time using the TI-provided power driver. Start-up time may increase if driver is not used.
(3) On-chip default connected capacitance including reference design parasitic capacitance. Connected internal capacitance is changed through software in the Customer Configuration section (CCFG).
(4) Adjustable load capacitance is integrated into the device. External load capacitors are required for systems targeting compliance with certain regulations. See the device errata for further details.
(5) The crystal manufacturer's specification must satisfy this requirement for proper operation.

8.24.3.3 48 MHz RC Oscillator (RCOSC_HF)

Measured on a Texas Instruments reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Frequency		48		MHz
Uncalibrated frequency accuracy		±1		%
Calibrated frequency accuracy(1)		±0.25		%
Start-up time		5		µs

(1) Accuracy relative to the calibration source (XOSC_HF)

8.24.3.4 2 MHz RC Oscillator (RCOSC_MF)

Measured on a Texas Instruments reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Calibrated frequency		2		MHz
Start-up time		5		µs

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8.24.3.5 32.768 kHz Crystal Oscillator (XOSC_LF)

Measured on a Texas Instruments reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

		MIN	TYP	MAX	UNIT
	Crystal frequency		32.768		kHz
ESR	Equivalent series resistance		30	100	kΩ
C_L	Crystal load capacitance	6	7(1)	12	pF

(1) Default load capacitance using TI reference designs including parasitic capacitance. Crystals with different load capacitance may be used.

8.24.3.6 32 kHz RC Oscillator (RCOSC_LF)

Measured on a Texas Instruments reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Calibrated frequency		32.8 (1)		kHz
Temperature coefficient.		50		ppm/°C

(1) When using RCOSC_LF as source for the low frequency system clock (SCLK_LF), the accuracy of the SCLK_LF-derived Real Time Clock (RTC) can be improved by measuring RCOSC_LF relative to XOSC_HF and compensating for the RTC tick speed. This functionality is available through the TI-provided Power driver.

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8.24.4 Synchronous Serial Interface (SSI) Characteristics

8.24.4.1 Synchronous Serial Interface (SSI) Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER NO.	PARAMETER		MIN	TYP	MAX	UNIT
S1	t_{clk_per}	SSIClk cycle time	12		65024	System Clocks [(2)]
S2[(1)]	t_{clk_high}	SSIClk high time		0.5		t_{clk_per}
S3[(1)]	t_{clk_low}	SSIClk low time		0.5		t_{clk_per}

(1) Refer to SSI timing diagrams 图 8-1, 图 8-2, and 图 8-3
(2) When using the TI-provided Power driver, the SSI system clock is always 48 MHz.

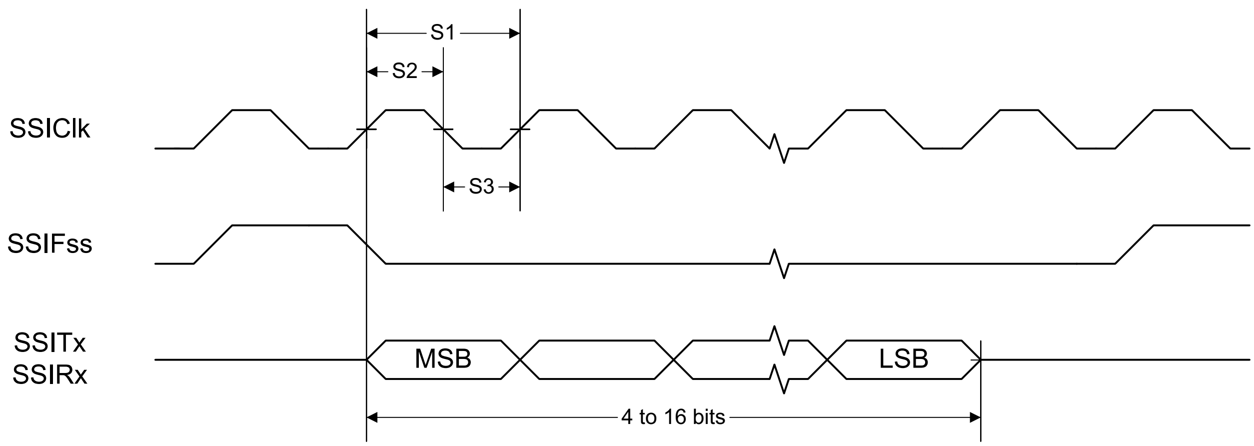

图 8-1. SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement

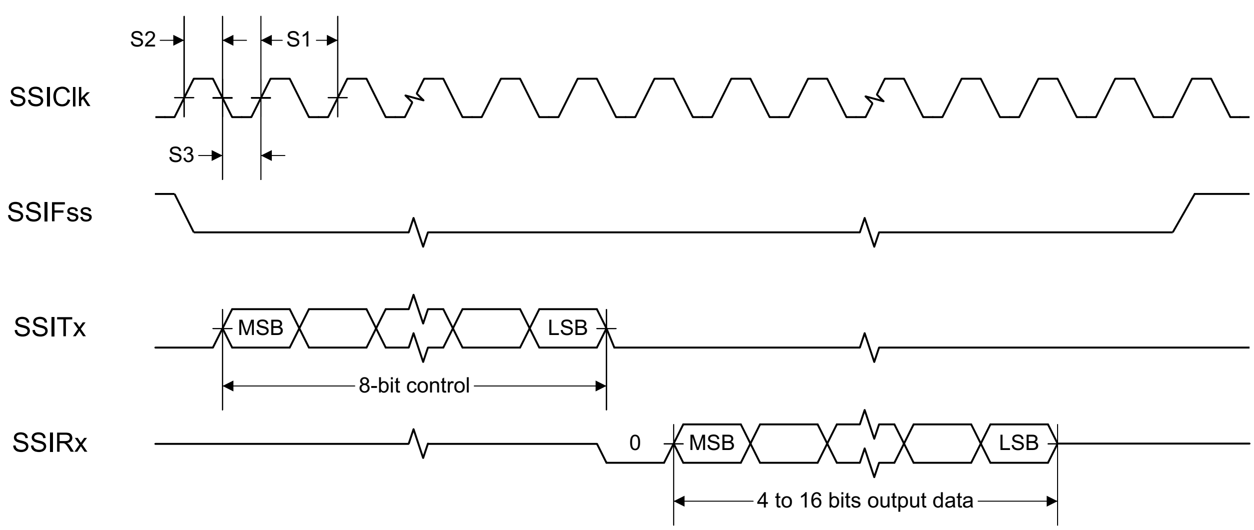

图 8-2. SSI Timing for MICROWIRE Frame Format (FRF = 10), Single Transfer

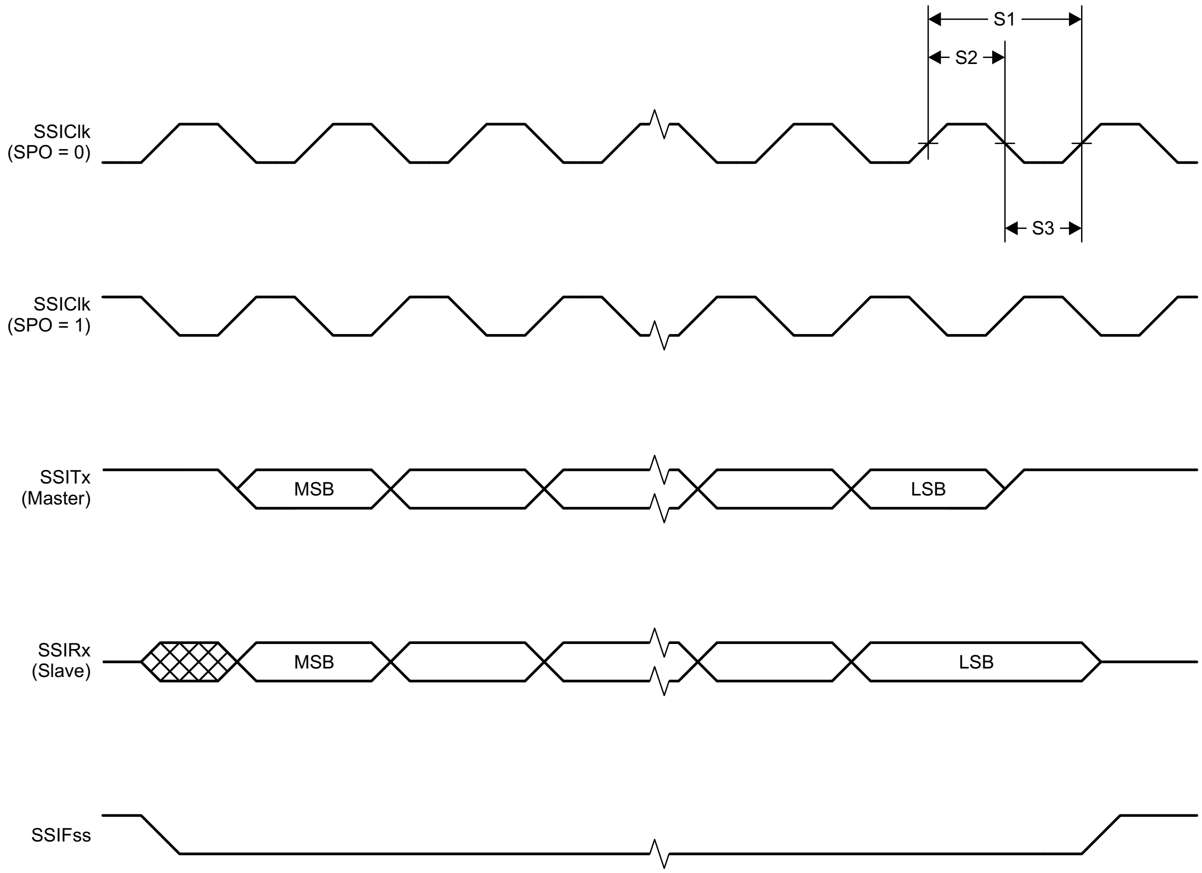

图 8-3. SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1

8.24.5 UART

8.24.5.1 UART Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
UART rate			3	MBaud

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8.25 Peripheral Characteristics

8.25.1 ADC

8.25.1.1 Analog-to-Digital Converter (ADC) Characteristics

T_c = 25 °C, V_{DDS} = 3.0 V and voltage scaling enabled, unless otherwise noted.(1)
Performance numbers require use of offset and gain adjustements in software by TI-provided ADC drivers.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input voltage range		0		VDDS	V
	Resolution			12		Bits
	Sample Rate				200	ksps
	Offset	Internal 4.3 V equivalent reference(2)		–0.24		LSB
	Gain error	Internal 4.3 V equivalent reference(2)		7.14		LSB
DNL(4)	Differential nonlinearity			>–1		LSB
INL	Integral nonlinearity			±4		LSB
ENOB	Effective number of bits	Internal 4.3 V equivalent reference(2), 200 kSamples/s, 9.6 kHz input tone		9.8		Bits
		Internal 4.3 V equivalent reference(2), 200 kSamples/s, 9.6 kHz input tone, DC/DC enabled		9.8		
		VDDS as reference, 200 kSamples/s, 9.6 kHz input tone		10.1		
		Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone		11.1		
		Internal reference, voltage scaling disabled, 14-bit mode, 200 kSamples/s, 600 Hz input tone (5)		11.3		
		Internal reference, voltage scaling disabled, 15-bit mode, 200 kSamples/s, 150 Hz input tone (5)		11.6		
THD	Total harmonic distortion	Internal 4.3 V equivalent reference(2), 200 kSamples/s, 9.6 kHz input tone		–65		dB
		VDDS as reference, 200 kSamples/s, 9.6 kHz input tone		–70		
		Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone		–72		
SINAD, SNDR	Signal-to-noise and distortion ratio	Internal 4.3 V equivalent reference(2), 200 kSamples/s, 9.6 kHz input tone		60		dB
		VDDS as reference, 200 kSamples/s, 9.6 kHz input tone		63		
		Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone		68		
SFDR	Spurious-free dynamic range	Internal 4.3 V equivalent reference(2), 200 kSamples/s, 9.6 kHz input tone		70		dB
		VDDS as reference, 200 kSamples/s, 9.6 kHz input tone		73		
		Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone		75		
	Conversion time	Serial conversion, time-to-output, 24 MHz clock		50		Clock Cycles
	Current consumption	Internal 4.3 V equivalent reference(2)		0.42		mA
	Current consumption	VDDS as reference		0.6		mA

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8.25.1.1 Analog-to-Digital Converter (ADC) Characteristics (continued)

T_c = 25 °C, V_{DDS} = 3.0 V and voltage scaling enabled, unless otherwise noted.(1)
Performance numbers require use of offset and gain adjustements in software by TI-provided ADC drivers.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Reference voltage	Equivalent fixed internal reference (input voltage scaling enabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1		4.3(2) (3)		V
	Reference voltage	Fixed internal reference (input voltage scaling disabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1. This value is derived from the scaled value (4.3 V) as follows: V_{ref} = 4.3 V × 1408 / 4095		1.48		V
	Reference voltage	VDDS as reference, input voltage scaling enabled		VDDS		V
	Reference voltage	VDDS as reference, input voltage scaling disabled		VDDS / 2.82(3)		V
	Input impedance	200 kSamples/s, voltage scaling enabled. Capacitive input, Input impedance depends on sampling frequency and sampling time		>1		MΩ

(1) Using IEEE Std 1241-2010 for terminology and test methods
(2) Input signal scaled down internally before conversion, as if voltage range was 0 to 4.3 V
(3) Applied voltage must be within Absolute Maximum Ratings (see 节 8.1) at all times
(4) No missing codes
(5) ADC_output = $\Sigma(4^n$ samples $) >> n$, n = desired extra bits

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8.25.2 DAC

8.25.2.1 Digital-to-Analog Converter (DAC) Characteristics

T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters						
	Resolution			8		Bits
V_{DDS}	Supply voltage	Any load, any V_{REF}, pre-charge OFF, DAC charge-pump ON	1.8		3.8	V
		External Load[4], any V_{REF}, pre-charge OFF, DAC charge-pump OFF	2.0		3.8	
		Any load, V_{REF} = DCOUPL, pre-charge ON	2.6		3.8	
F_{DAC}	Clock frequency	Buffer ON (recommended for external load)	16		250	kHz
		Buffer OFF (internal load)	16		1000	
	Voltage output settling time	V_{REF} = VDDS, buffer OFF, internal load		13		1 / F_{DAC}
		V_{REF} = VDDS, buffer ON, external capacitive load = 20 pF[3]		13.8		
	External capacitive load			20	200	pF
	External resistive load		10			MΩ
	Short circuit current				400	µA
Z_{MAX}	Max output impedance Vref = VDDS, buffer ON, CLK 250 kHz	VDDS = 3.8 V, DAC charge-pump OFF		50.8		kΩ
		VDDS = 3.0 V, DAC charge-pump ON		51.7		
		VDDS = 3.0 V, DAC charge-pump OFF		53.2		
		VDDS = 2.0 V, DAC charge-pump ON		48.7		
		VDDS = 2.0 V, DAC charge-pump OFF		70.2		
		VDDS = 1.8 V, DAC charge-pump ON		46.3		
		VDDS = 1.8 V, DAC charge-pump OFF		88.9		
Internal Load - Continuous Time Comparator / Low Power Clocked Comparator						
DNL	Differential nonlinearity	V_{REF} = VDDS, load = Continuous Time Comparator or Low Power Clocked Comparator F_{DAC} = 250 kHz		±1		LSB[1]
	Differential nonlinearity	V_{REF} = VDDS, load = Continuous Time Comparator or Low Power Clocked Comparator F_{DAC} = 16 kHz		±1.2		
	Offset error[2] Load = Continuous Time Comparator	V_{REF} = VDDS = 3.8 V		±0.64		LSB[1]
		V_{REF} = VDDS= 3.0 V		±0.81		
		V_{REF} = VDDS = 1.8 V		±1.27		
		V_{REF} = DCOUPL, pre-charge ON		±3.43		
		V_{REF} = DCOUPL, pre-charge OFF		±2.88		
		V_{REF} = ADCREF		±2.37		
	Offset error[2] Load = Low Power Clocked Comparator	V_{REF} = VDDS= 3.8 V		±0.78		LSB[1]
		V_{REF} = VDDS = 3.0 V		±0.77		
		V_{REF} = VDDS= 1.8 V		±3.46		
		V_{REF} = DCOUPL, pre-charge ON		±3.44		
		V_{REF} = DCOUPL, pre-charge OFF		±4.70		
		V_{REF} = ADCREF		±4.11		

8.25.2.1 Digital-to-Analog Converter (DAC) Characteristics (continued)

T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Max code output voltage variation[2] Load = Continuous Time Comparator	V_{REF} = VDDS = 3.8 V		±1.53		LSB[1]
		V_{REF} = VDDS = 3.0 V		±1.71		
		V_{REF} = VDDS= 1.8 V		±2.10		
		V_{REF} = DCOUPL, pre-charge ON		±6.00		
		V_{REF} = DCOUPL, pre-charge OFF		±3.85		
		V_{REF} = ADCREF		±5.84		
	Max code output voltage variation[2] Load = Low Power Clocked Comparator	V_{REF} = VDDS= 3.8 V		±2.92		LSB[1]
		V_{REF} =VDDS= 3.0 V		±3.06		
		V_{REF} = VDDS= 1.8 V		±3.91		
		V_{REF} = DCOUPL, pre-charge ON		±7.84		
		V_{REF} = DCOUPL, pre-charge OFF		±4.06		
		V_{REF} = ADCREF		±6.94		
	Output voltage range[2] Load = Continuous Time Comparator	V_{REF} = VDDS = 3.8 V, code 1		0.03		V
		V_{REF} = VDDS = 3.8 V, code 255		3.62		
		V_{REF} = VDDS= 3.0 V, code 1		0.02		
		V_{REF} = VDDS= 3.0 V, code 255		2.86		
		V_{REF} = VDDS= 1.8 V, code 1		0.01		
		V_{REF} = VDDS = 1.8 V, code 255		1.71		
		V_{REF} = DCOUPL, pre-charge OFF, code 1		0.01		
		V_{REF} = DCOUPL, pre-charge OFF, code 255		1.21		
		V_{REF} = DCOUPL, pre-charge ON, code 1		1.27		
		V_{REF} = DCOUPL, pre-charge ON, code 255		2.46		
		V_{REF} = ADCREF, code 1		0.01		
		V_{REF} = ADCREF, code 255		1.41		
	Output voltage range[2] Load = Low Power Clocked Comparator	V_{REF} = VDDS = 3.8 V, code 1		0.03		V
		V_{REF} = VDDS= 3.8 V, code 255		3.61		
		V_{REF} = VDDS= 3.0 V, code 1		0.02		
		V_{REF} = VDDS= 3.0 V, code 255		2.85		
		V_{REF} = VDDS = 1.8 V, code 1		0.01		
		V_{REF} = VDDS = 1.8 V, code 255		1.71		
		V_{REF} = DCOUPL, pre-charge OFF, code 1		0.01		
		V_{REF} = DCOUPL, pre-charge OFF, code 255		1.21		
		V_{REF} = DCOUPL, pre-charge ON, code 1		1.27		
		V_{REF} = DCOUPL, pre-charge ON, code 255		2.46		
		V_{REF} = ADCREF, code 1		0.01		
		V_{REF} = ADCREF, code 255		1.41		
External Load (Keysight 34401A Multimeter)						
INL	Integral nonlinearity	V_{REF} = VDDS, F_{DAC} = 250 kHz		±1		LSB[1]
		V_{REF} = DCOUPL, F_{DAC} = 250 kHz		±1		
		V_{REF} = ADCREF, F_{DAC} = 250 kHz		±1		
DNL	Differential nonlinearity	V_{REF} = VDDS, F_{DAC} = 250 kHz		±1		LSB[1]

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8.25.2.1 Digital-to-Analog Converter (DAC) Characteristics (continued)

T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Offset error	V_{REF} = VDDS= 3.8 V		±0.20		LSB(1)
		V_{REF} = VDDS= 3.0 V		±0.25		
		V_{REF} = VDDS = 1.8 V		±0.45		
		V_{REF} = DCOUPL, pre-charge ON		±1.55		
		V_{REF} = DCOUPL, pre-charge OFF		±1.30		
		V_{REF} = ADCREF		±1.10		
	Max code output voltage variation	V_{REF} = VDDS= 3.8 V		±0.60		LSB(1)
		V_{REF} = VDDS= 3.0 V		±0.55		
		V_{REF} = VDDS= 1.8 V		±0.60		
		V_{REF} = DCOUPL, pre-charge ON		±3.45		
		V_{REF} = DCOUPL, pre-charge OFF		±2.10		
		V_{REF} = ADCREF		±1.90		
	Output voltage range Load = Low Power Clocked Comparator	V_{REF} = VDDS = 3.8 V, code 1		0.03		V
		V_{REF} = VDDS = 3.8 V, code 255		3.61		
		V_{REF} = VDDS = 3.0 V, code 1		0.02		
		V_{REF} = VDDS= 3.0 V, code 255		2.85		
		V_{REF} = VDDS= 1.8 V, code 1		0.02		
		V_{REF} = VDDS = 1.8 V, code 255		1.71		
		V_{REF} = DCOUPL, pre-charge OFF, code 1		0.02		
		V_{REF} = DCOUPL, pre-charge OFF, code 255		1.20		
		V_{REF} = DCOUPL, pre-charge ON, code 1		1.27		
		V_{REF} = DCOUPL, pre-charge ON, code 255		2.46		
		V_{REF} = ADCREF, code 1		0.02		
		V_{REF} = ADCREF, code 255		1.42		

(1) 1 LSB (V_{REF} 3.8 V/3.0 V/1.8 V/DCOUPL/ADCREF) = 14.10 mV/11.13 mV/6.68 mV/4.67 mV/5.48 mV
(2) Includes comparator offset
(3) A load > 20 pF will increases the settling time
(4) Keysight 34401A Multimeter

8.25.3 Temperature and Battery Monitor

8.25.3.1 Temperature Sensor

Measured on a Texas Instruments reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			2		°C
Accuracy	-40 °C to 0 °C		±4.0		°C
Accuracy	0 °C to 105 °C		±2.5		°C
Supply voltage coefficient[(1)]			3.6		°C/V

(1) The temperature sensor is automatically compensated for VDDS variation when using the TI-provided driver.

8.25.3.2 Battery Monitor

Measured on a Texas Instruments reference design with T_c = 25 °C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			25		mV
Range		1.8		3.8	V
Integral nonlinearity (max)			23		mV
Accuracy	VDDS = 3.0 V		22.5		mV
Offset error			-32		mV
Gain error			-1		%

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8.25.4 Comparators

8.25.4.1 Low-Power Clocked Comparator

T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		V_{DDS}	V
Clock frequency			SCLK_LF		
Internal reference voltage(1)	Using internal DAC with VDDS as reference voltage, DAC code = 0 - 255		0.024 - 2.865		V
Offset	Measured at V_{DDS} / 2, includes error from internal DAC		±5		mV
Decision time	Step from – 50 mV to 50 mV		1		Clock Cycle

(1) The comparator can use an internal 8 bits DAC as its reference. The DAC output voltage range depends on the reference voltage selected. See 节 8.25.2.1

8.25.4.2 Continuous Time Comparator

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range(1)		0		V_{DDS}	V
Offset	Measured at V_{DDS} / 2		±5		mV
Decision time	Step from – 10 mV to 10 mV		0.78		µs
Current consumption	Internal reference		8.6		µA

(1) The input voltages can be generated externally and connected throughout I/Os or an internal reference voltage can be generated using the DAC

8.25.5 Current Source

8.25.5.1 Programmable Current Source

T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current source programmable output range (logarithmic range)			0.25 - 20		µA
Resolution			0.25		µA

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8.25.6 GPIO

8.25.6.1 GPIO DC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A = 25 °C, V_{DDS} = 1.8 V					
GPIO VOH at 8 mA load	IOCURR = 2, high-drive GPIOs only		1.56		V
GPIO VOL at 8 mA load	IOCURR = 2, high-drive GPIOs only		0.24		V
GPIO VOH at 4 mA load	IOCURR = 1		1.59		V
GPIO VOL at 4 mA load	IOCURR = 1		0.21		V
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		73		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS		19		µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.08		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		0.73		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.35		V
T_A = 25 °C, V_{DDS} = 3.0 V					
GPIO VOH at 8 mA load	IOCURR = 2, high-drive GPIOs only		2.59		V
GPIO VOL at 8 mA load	IOCURR = 2, high-drive GPIOs only		0.42		V
GPIO VOH at 4 mA load	IOCURR = 1		2.63		V
GPIO VOL at 4 mA load	IOCURR = 1		0.40		V
T_A = 25 °C, V_{DDS} = 3.8 V					
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		282		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS		110		µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.97		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		1.55		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.42		V
T_A = 25 °C					
VIH	Lowest GPIO input voltage reliably interpreted as a *High*	$0.8 \cdot V_{DDS}$			V
VIL	Highest GPIO input voltage reliably interpreted as a *Low*			$0.2 \cdot V_{DDS}$	V

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8.26 Typical Characteristics

All measurements in this section are done with T_c = 25 °C and V_{DDS} = 3.0 V, unless otherwise noted. See *Recommended Operating Conditions* for device limits. Values exceeding these limits are for reference only.

8.26.1 MCU Current

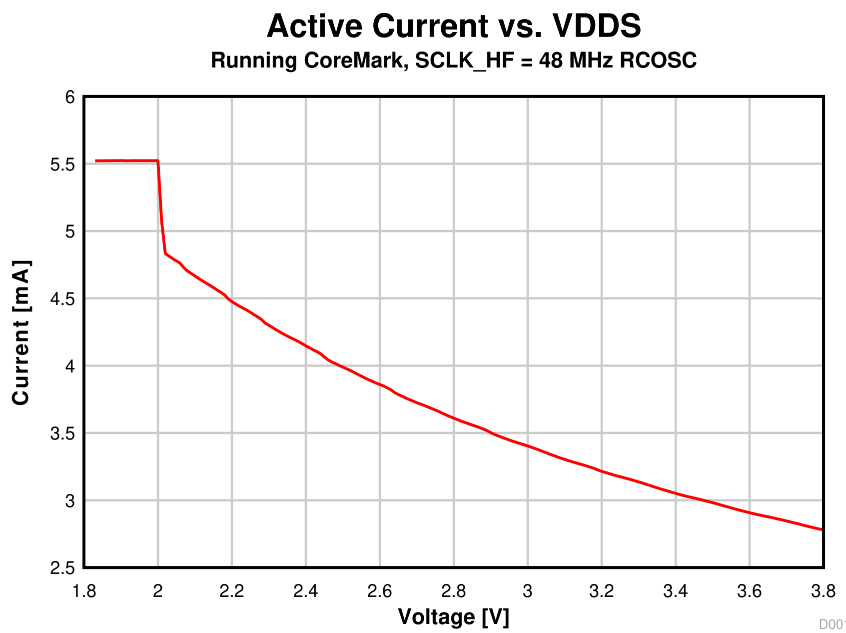

图 8-4. Active Mode (MCU) Current vs. Supply Voltage (VDDS)

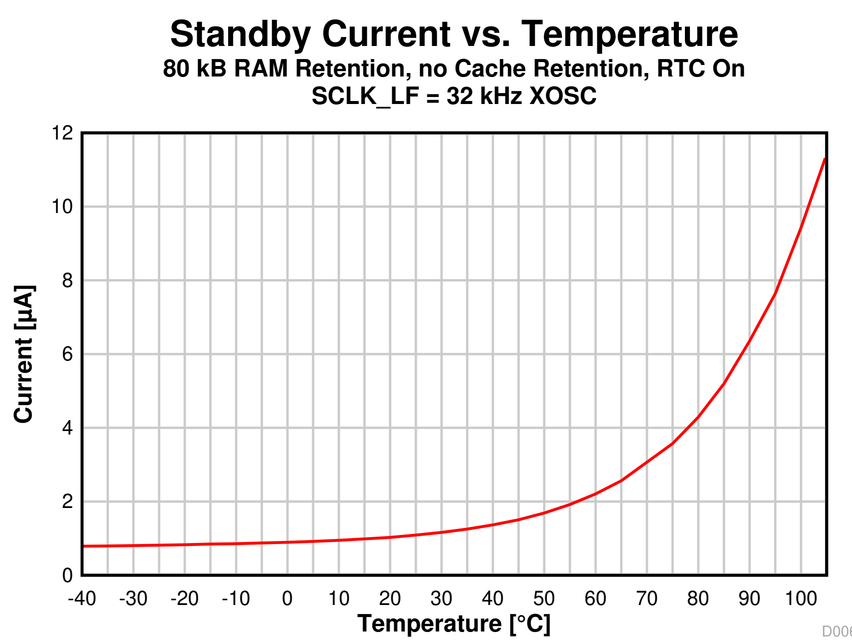

图 8-5. Standby Mode (MCU) Current vs. Temperature

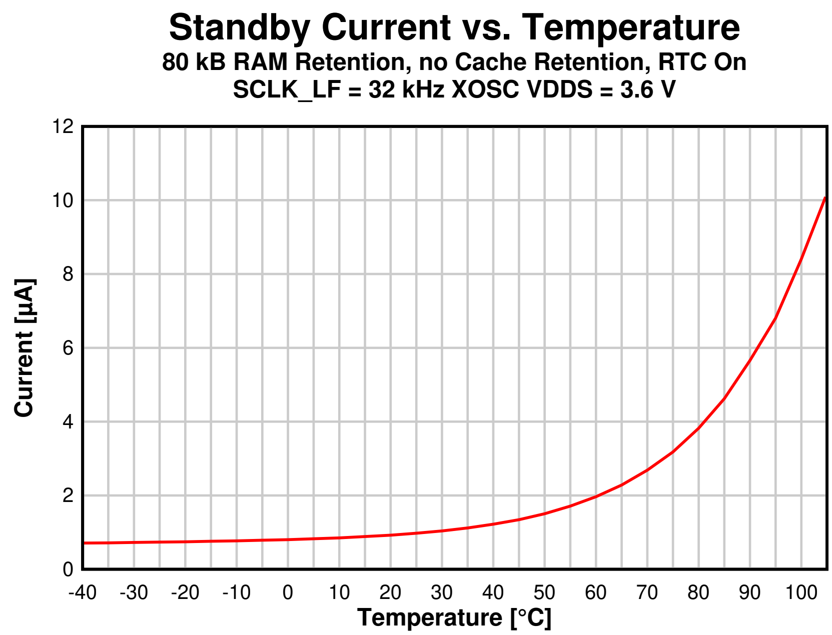

图 8-6. Standby Mode (MCU) Current vs. Temperature (VDDS = 3.6 V)

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8.26.2 RX Current

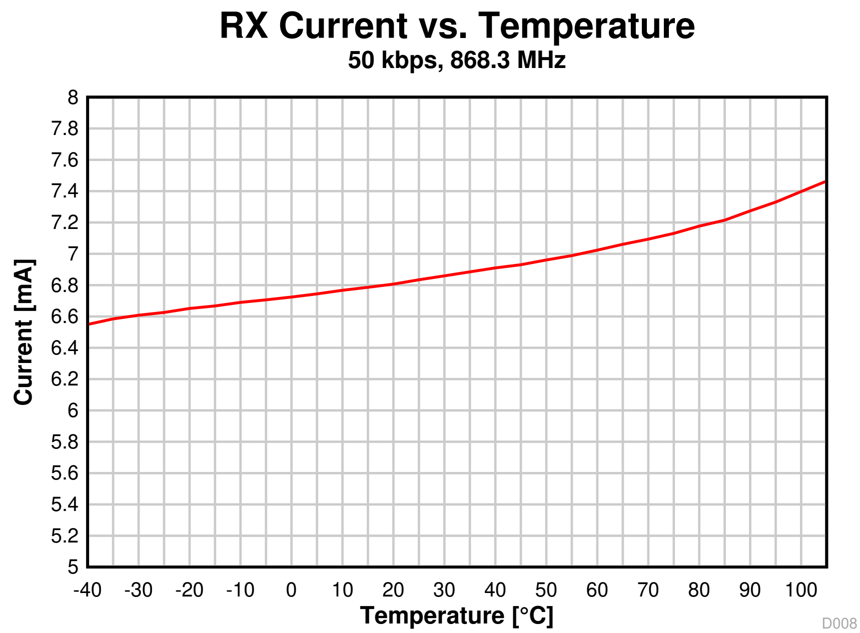

图 8-7. RX Current vs. Temperature (50 kbps, 868.3 MHz)

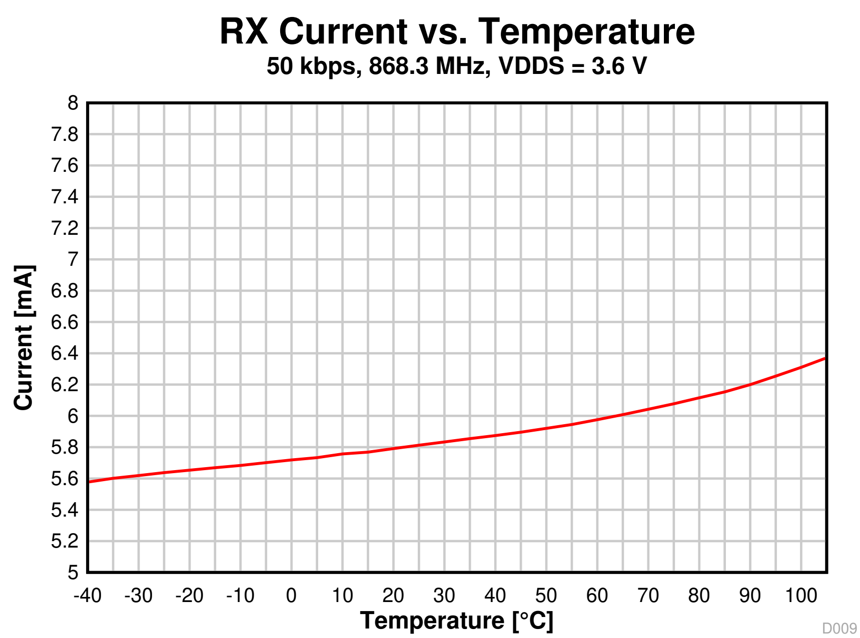

图 8-8. RX Current vs. Temperature (50 kbps, 868.3 MHz, VDDS = 3.6 V)

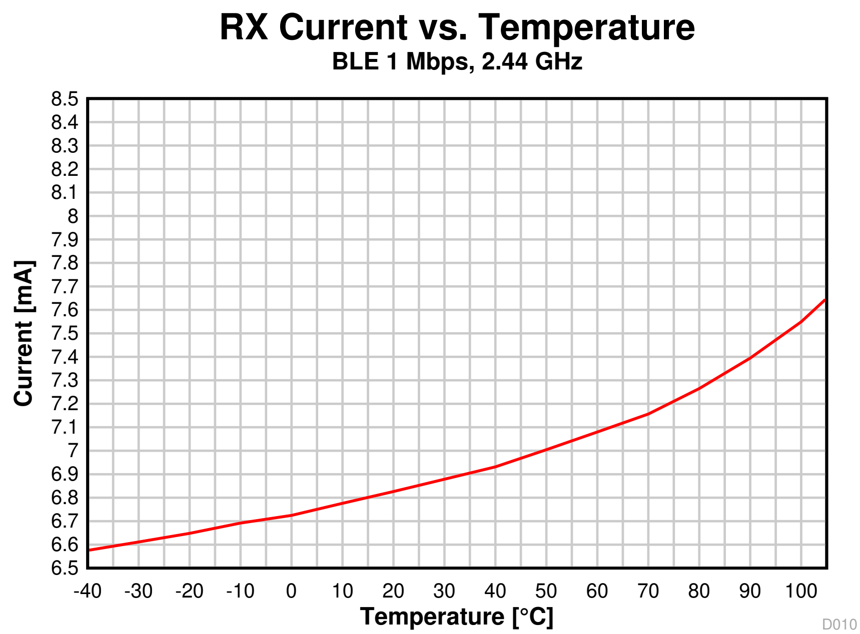

图 8-9. RX Current vs. Temperature (BLE 1 Mbps, 2.44 GHz)

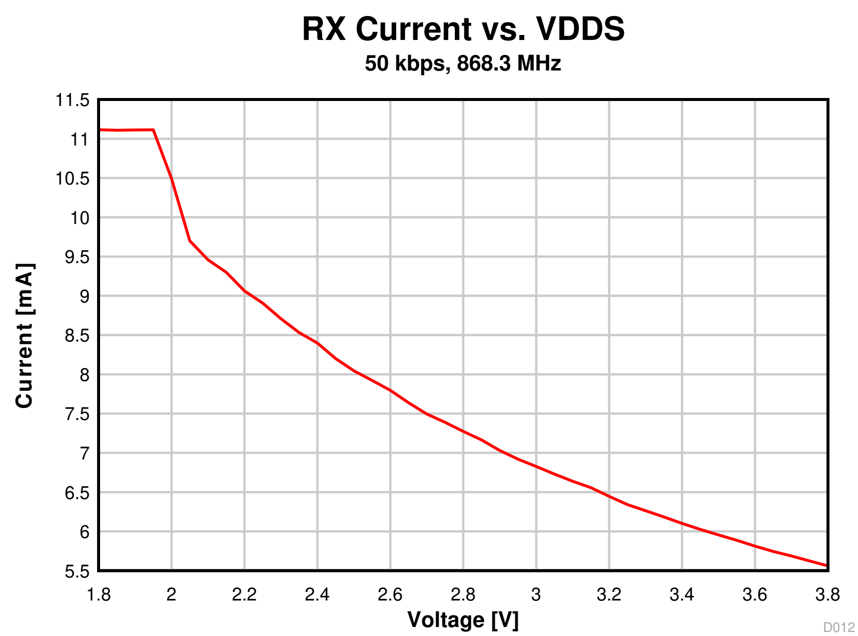

图 8-10. RX Current vs. Supply Voltage (VDDS) (50 kbps, 868.3 MHz)

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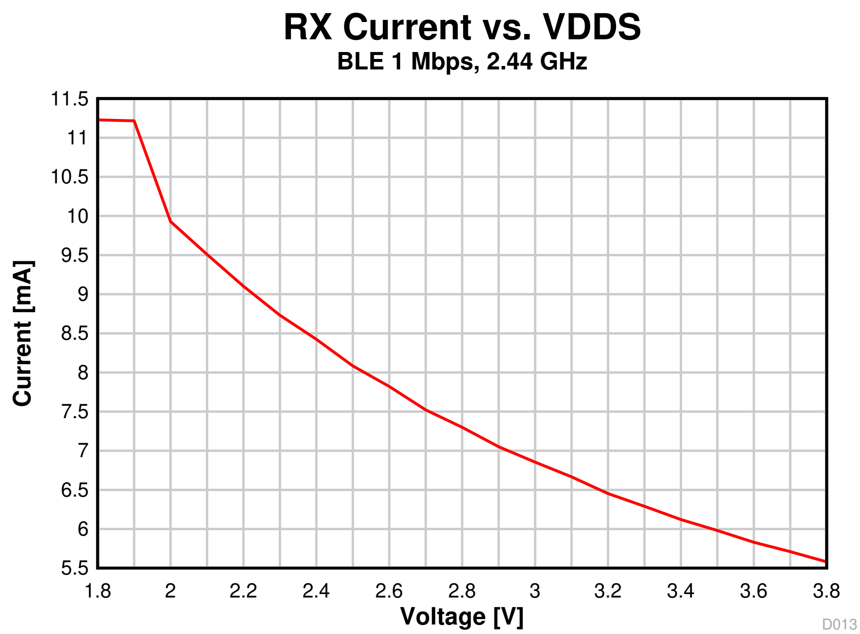

图 8-11. RX Current vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz)

8.26.3 TX Current

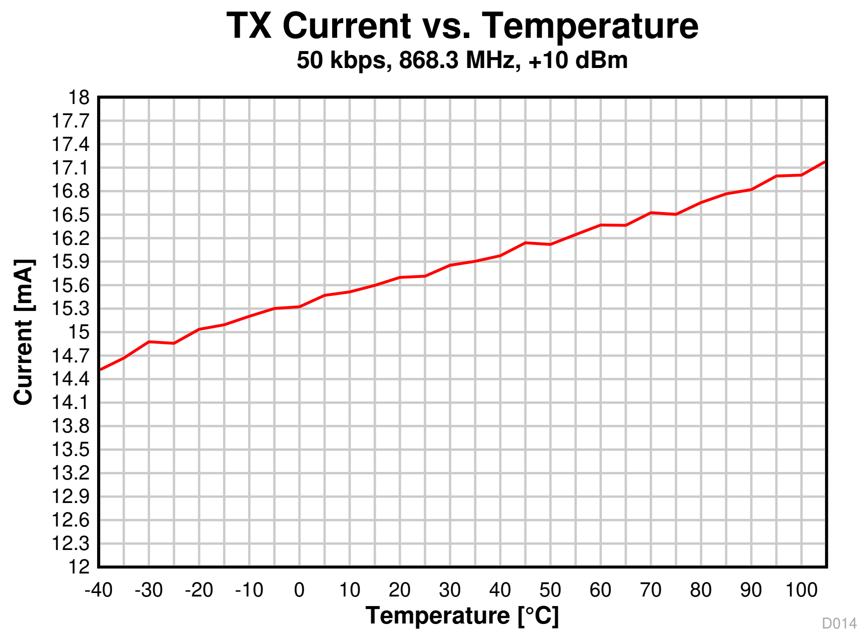

图 8-12. TX Current vs. Temperature (50 kbps, 868.3 MHz)

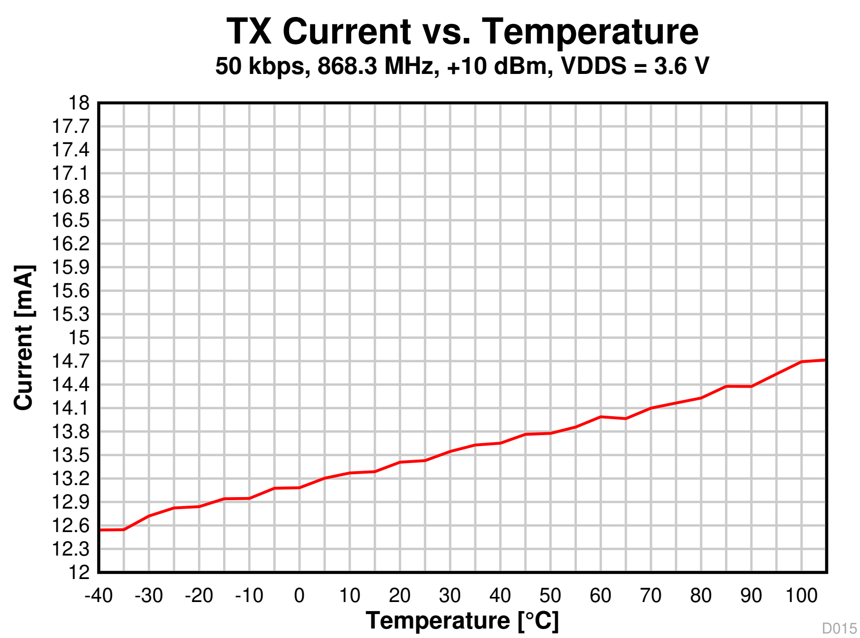

图 8-13. TX Current vs. Temperature (50 kbps, 868.3 MHz, VDDS = 3.6 V)

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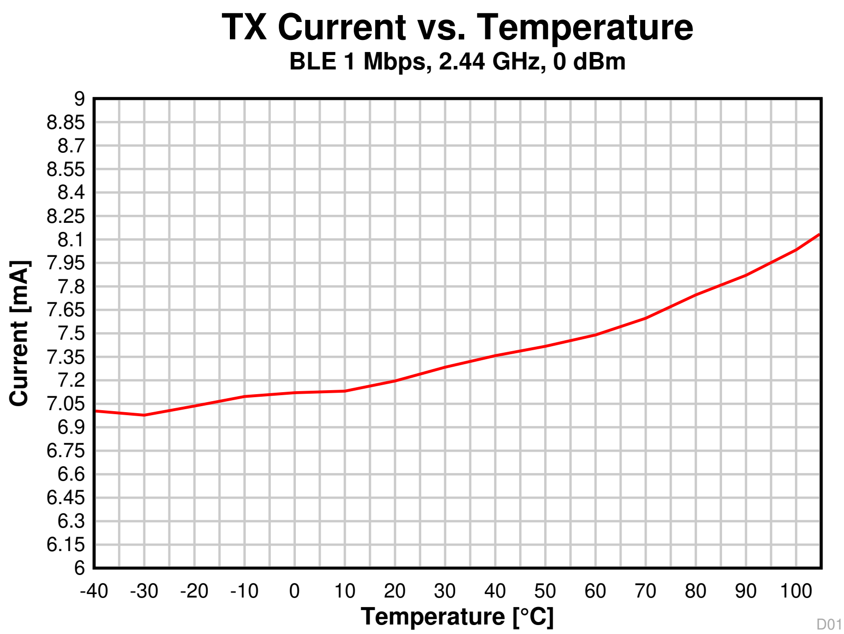

图 8-14. TX Current vs. Temperature (BLE 1 Mbps, 2.44 GHz)

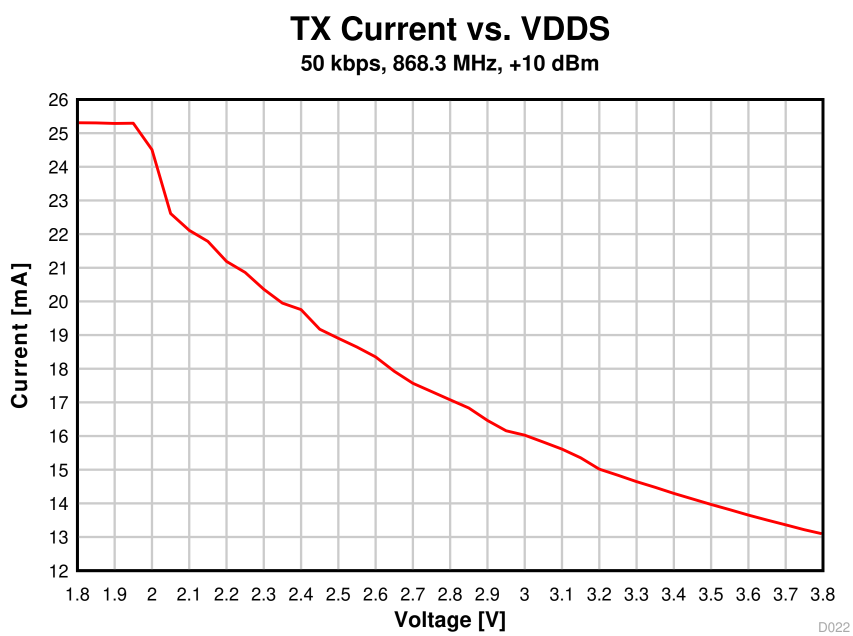

图 8-15. TX Current vs. Supply Voltage (VDDS) (50 kbps, 868.3 MHz)

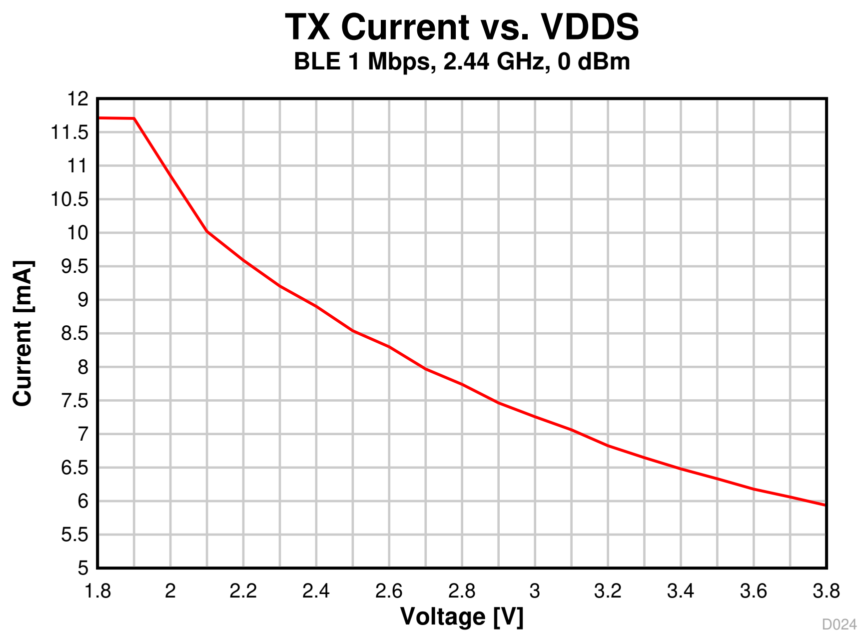

图 8-16. TX Current vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz)

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表 8-1 and 表 8-2 show typical TX current and output power for different output power settings.

表 8-1. Typical TX Current and Output Power (915 MHz, VDDS = 3.6 V)

CC1352R at 915 MHz, VDDS = 3.6 V (Measured on CC1352REM-XD7793-XD24)			
txPower	**TX Power Setting (SmartRF Studio)**	**Typical Output Power [dBm]**	**Typical Current Consumption [mA]**
0x013F	14	13.6	24.2
0xB224	12.5	12	17.6
0xA410	12	11.5	16.5
0x669A	11	10.5	14.9
0x3E92	10	9.4	13.5
0x3EDC	9	8.5	12.7
0x2CD8	8	7.7	11.9
0x26D4	7	6.5	11
0x20D1	6	5.4	10.2
0x1CCE	5	3.8	9.3
0x16CD	4	3.2	9
0x14CB	3	1.7	8.3
0x12CA	2	0.8	8
0x12C9	1	-0.3	7.6
0x10C8	0	-1.4	7.3
0x0AC4	-5	-8.6	5.8
0x0AC2	-10	-15.9	5.1
0x06C1	-15	-22.3	4.8
0x04C0	-20	-24.4	4.6

表 8-2. Typical TX Current and Output Power (2.4 GHz, VDDS = 3.0 V)

CC1352R at 2.4 GHz, VDDS = 3.0 V (Measured on CC1352REM-XD7793-XD24)			
txPower	**TX Power Setting (SmartRF Studio)**	**Typical Output Power [dBm]**	**Typical Current Consumption [mA]**
0x7217	5	4.4	9.6
0x4E63	4	3.0	8.9
0x385D	3	1.8	8.3
0x3259	2	0.7	7.9
0x2856	1	-0.3	7.5
0x2853	0	-1.5	7.1
0x12D6	-5	-6.7	6.1
0x0ACF	-10	-11.5	5.5
0x06CA	-15	-16.7	5.1
0x04C6	-20	-22.7	4.8

8.26.4 RX Performance

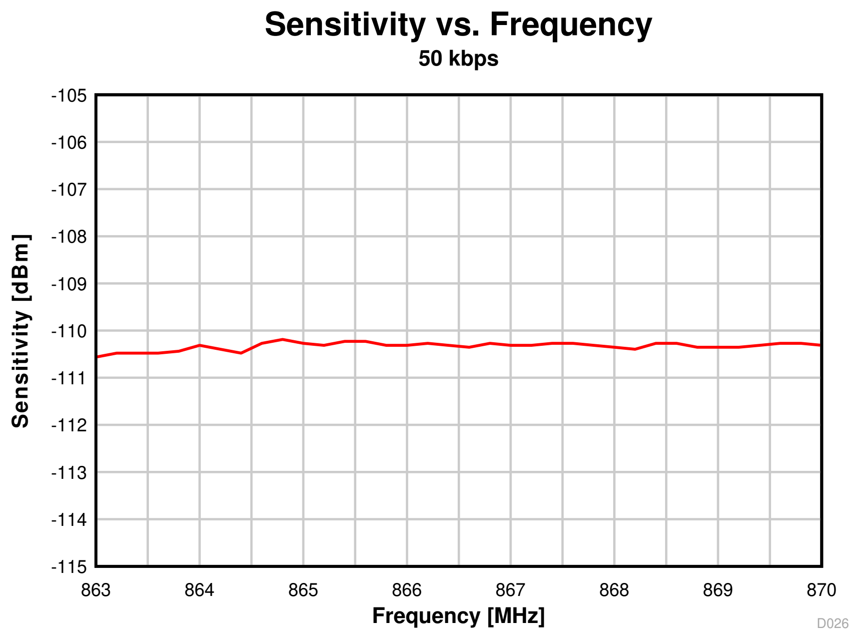

图 8-17. Sensitivity vs. Frequency (50 kbps, 868 MHz)

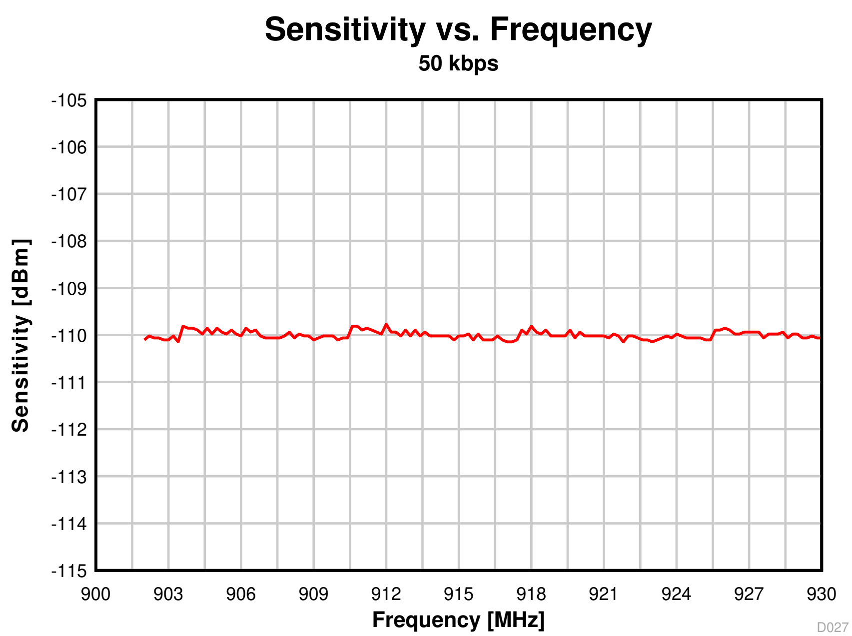

图 8-18. Sensitivity vs. Frequency (50 kbps, 915 MHz)

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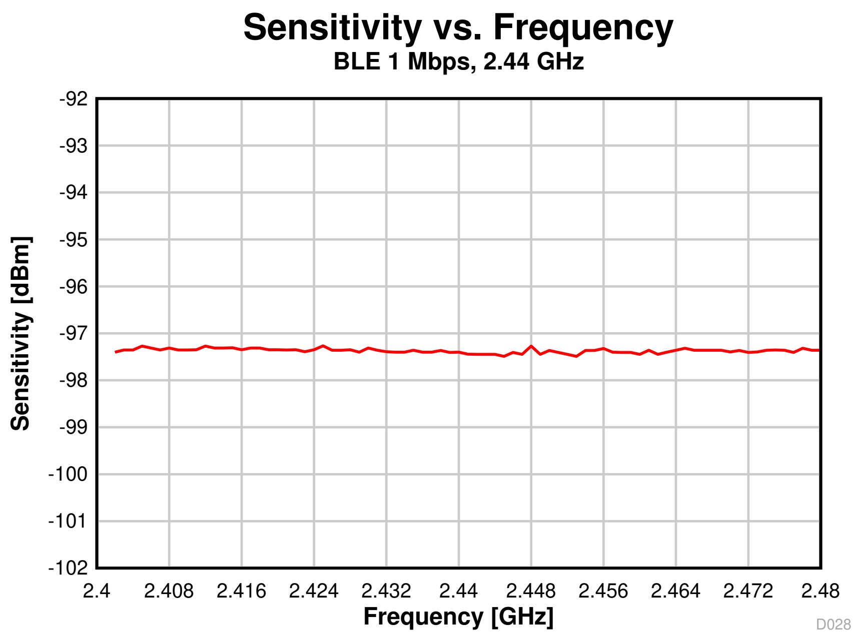

图 8-19. Sensitivity vs. Frequency (BLE 1 Mbps, 2.44 GHz)

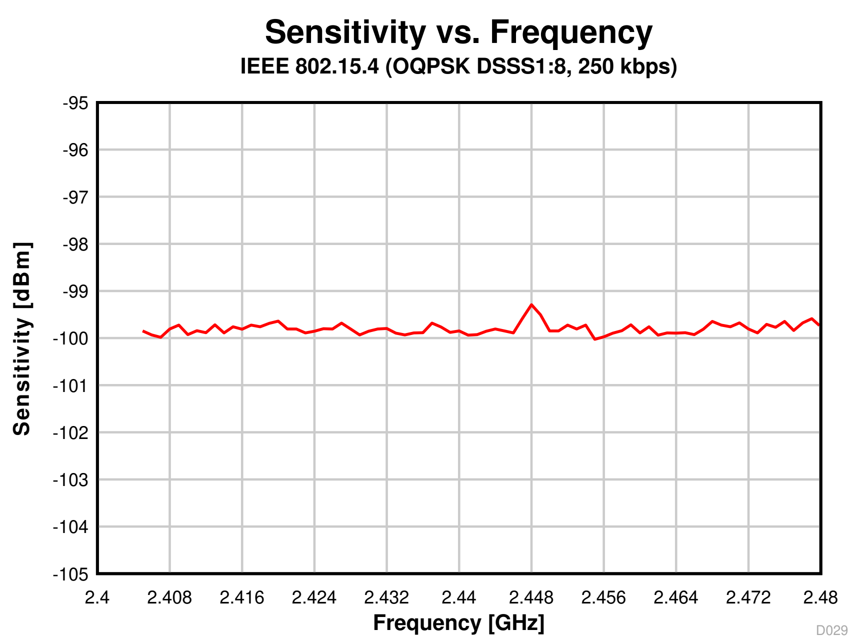

图 8-20. Sensitivity vs. Frequency (250 kbps, 2.44 GHz)

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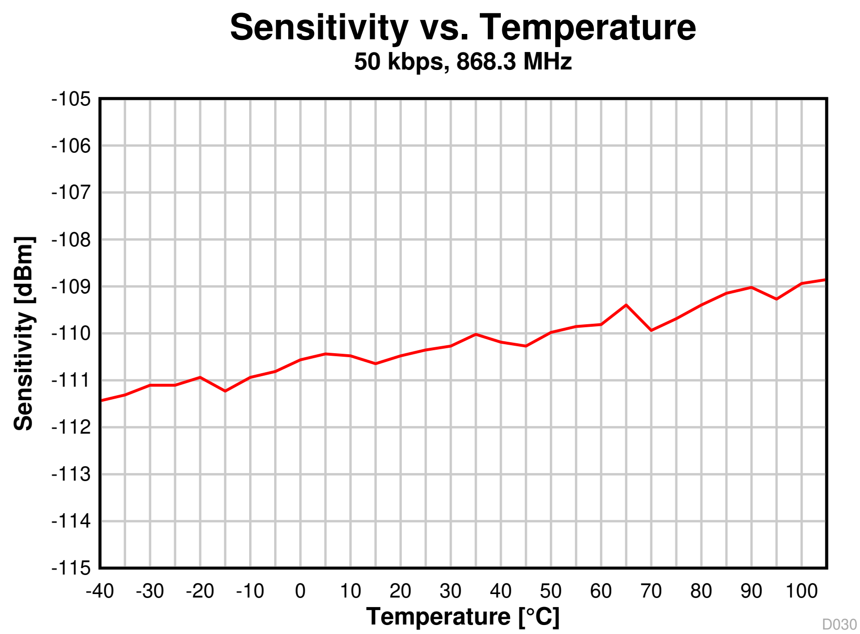

图 8-21. Sensitivity vs. Temperature (50 kbps, 868.3 MHz)

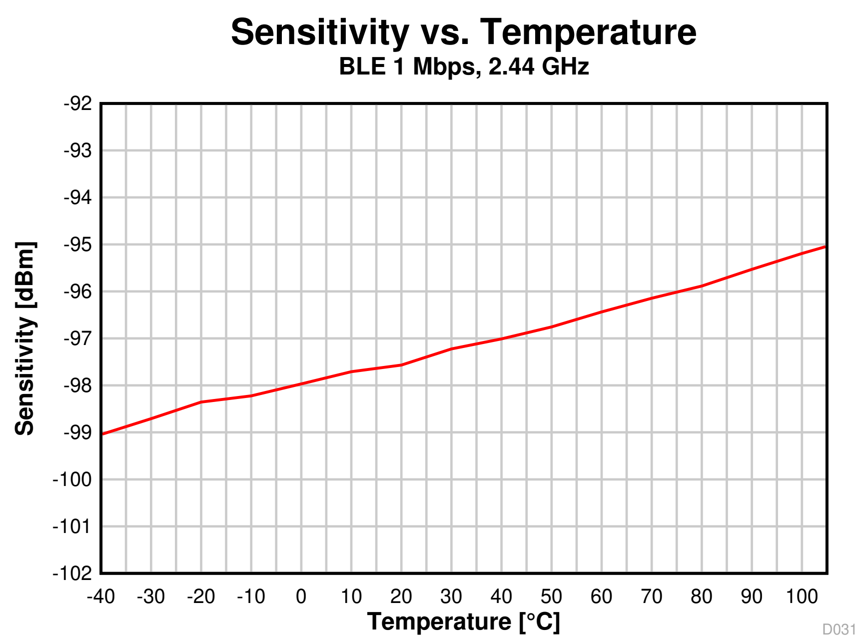

图 8-22. Sensitivity vs. Temperature (BLE 1 Mbps, 2.44 GHz)

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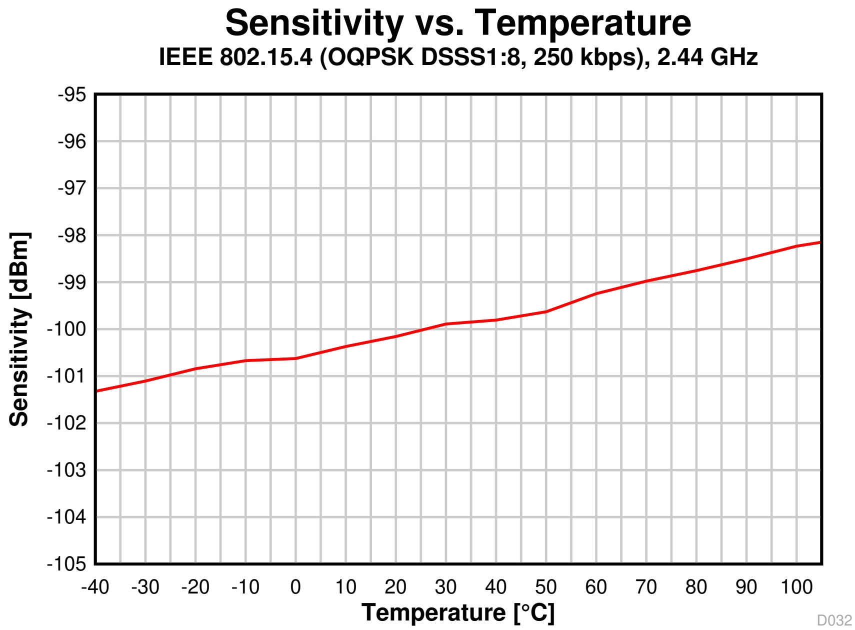

图 8-23. Sensitivity vs. Temperature (250 kbps, 2.44 GHz)

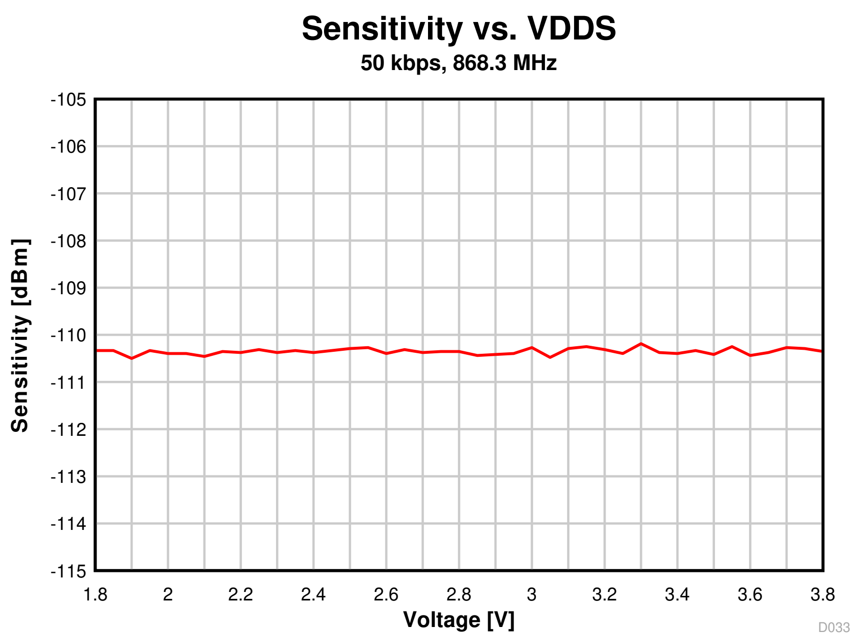

图 8-24. Sensitivity vs. Supply Voltage (VDDS) (50 kbps, 868.3 MHz)

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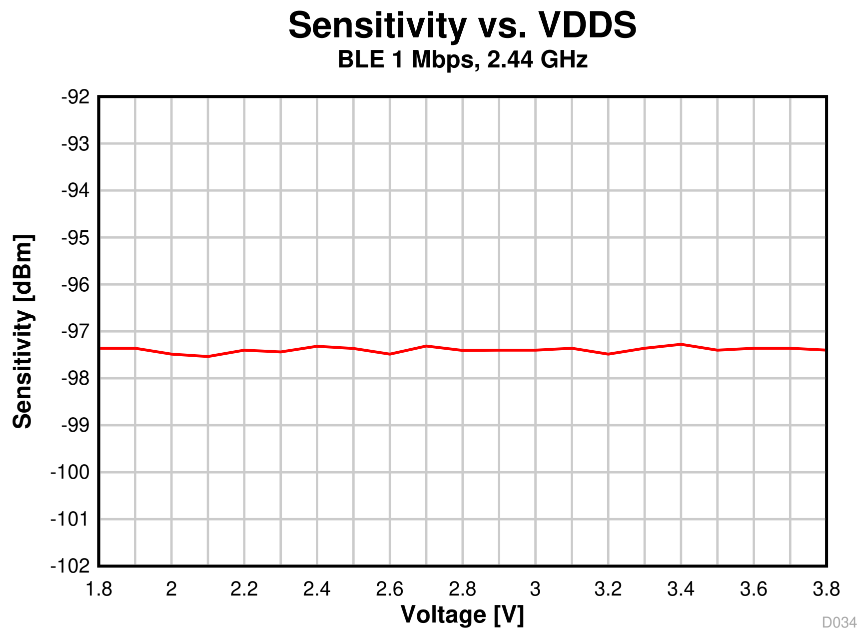

图 8-25. Sensitivity vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz)

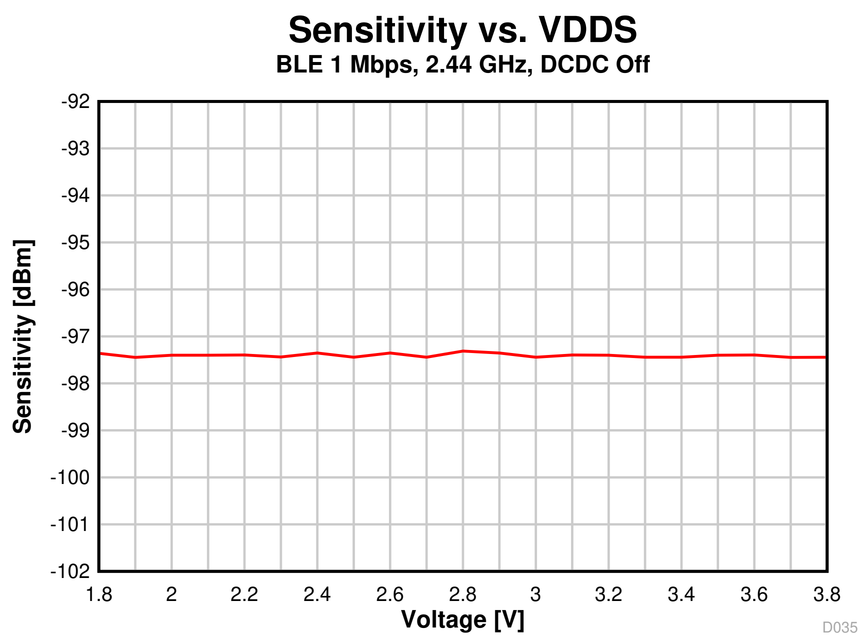

图 8-26. Sensitivity vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, DCDC Off)

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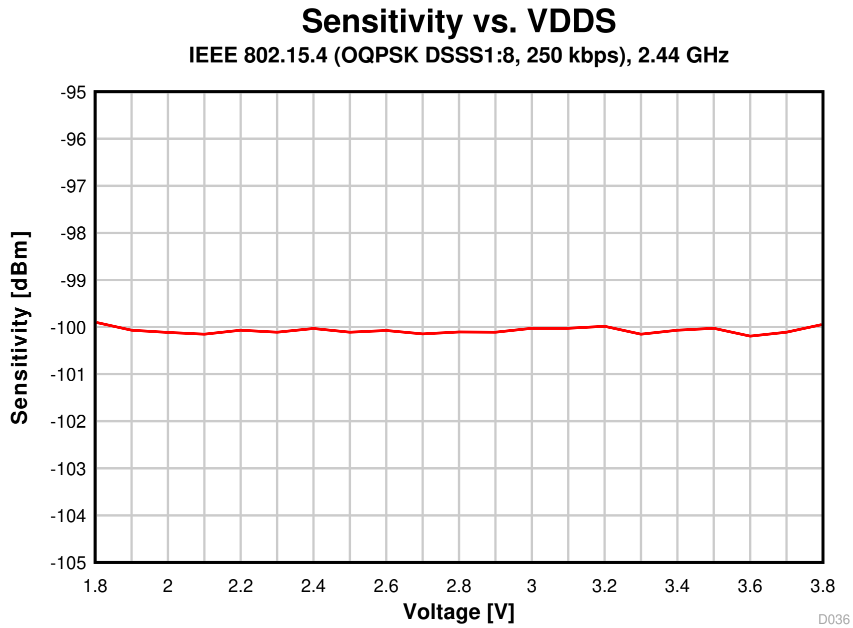

图 8-27. Sensitivity vs. Supply Voltage (VDDS) (250 kbps, 2.44 GHz)

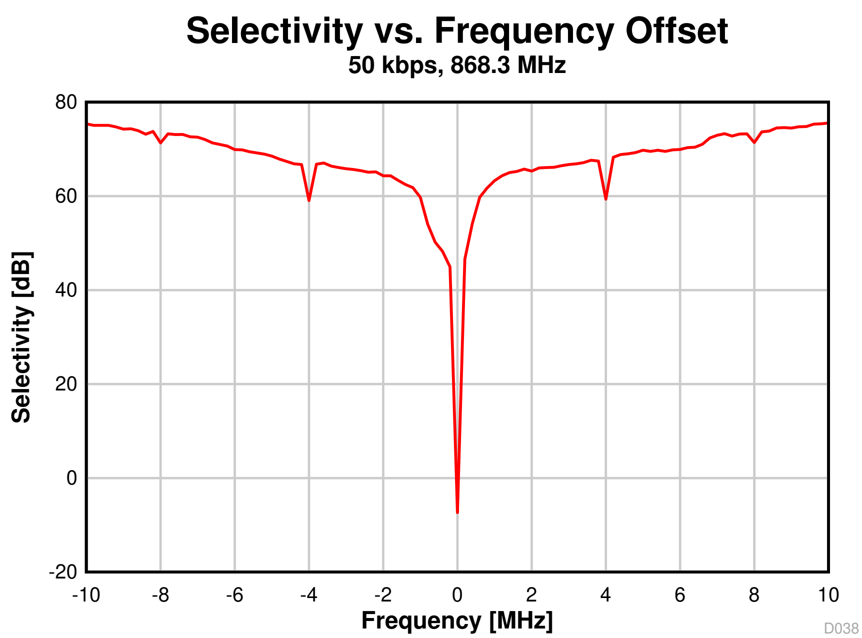

图 8-28. Selectivity vs. Frequency Offset (50 kbps, 868.3 MHz)

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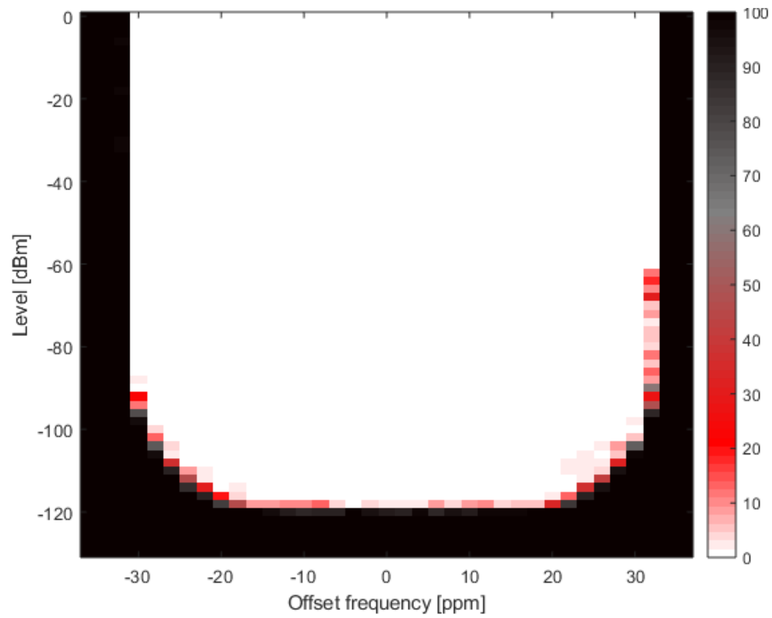

图 8-29. PER vs. Level vs. Frequency (SimpleLink™ Long Range 5 kbps, 868 MHz)

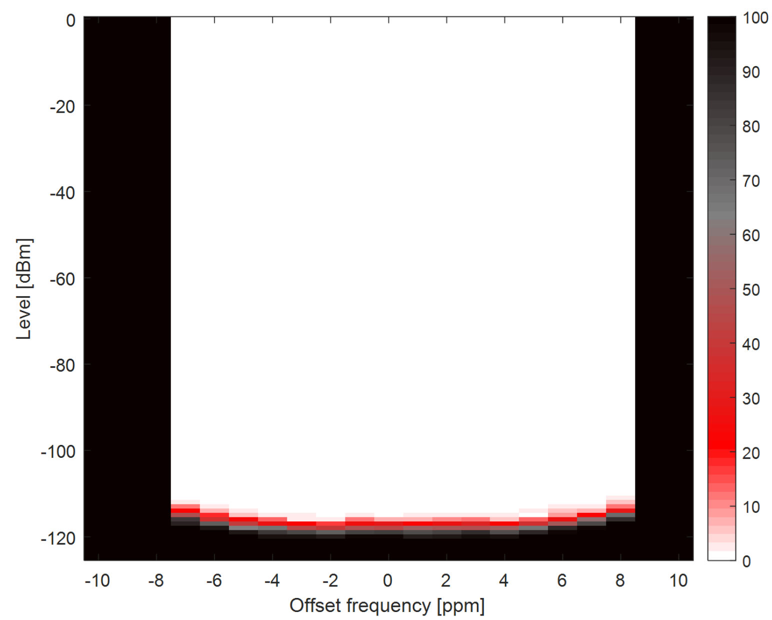

图 8-30. Narrowband, 9.6 kbps ±2.4 kHz deviation, 2-GFSK, 868 MHz, 17.1 kHz RX Bandwidth

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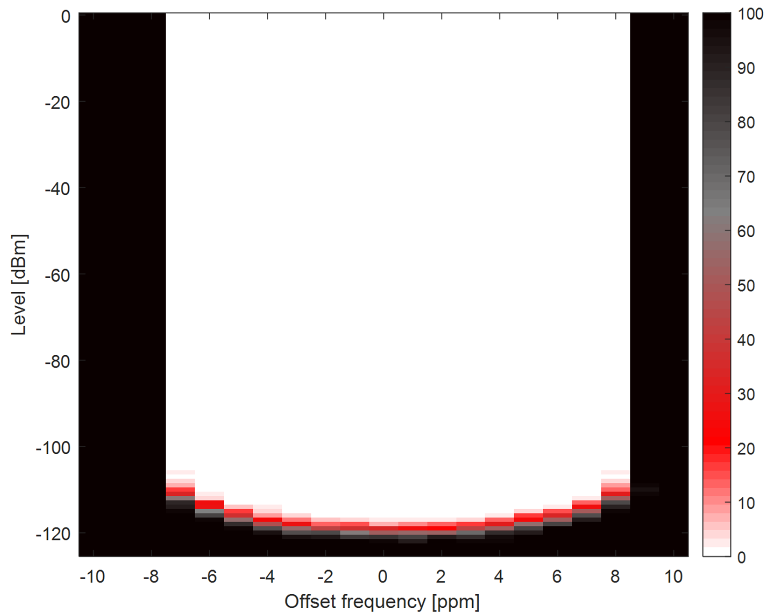

图 8-31. Narrowband, 4.8 kbps ±2 kHz deviation, 2-GFSK, 426.1 MHz, 10.1 kHz RX Bandwidth

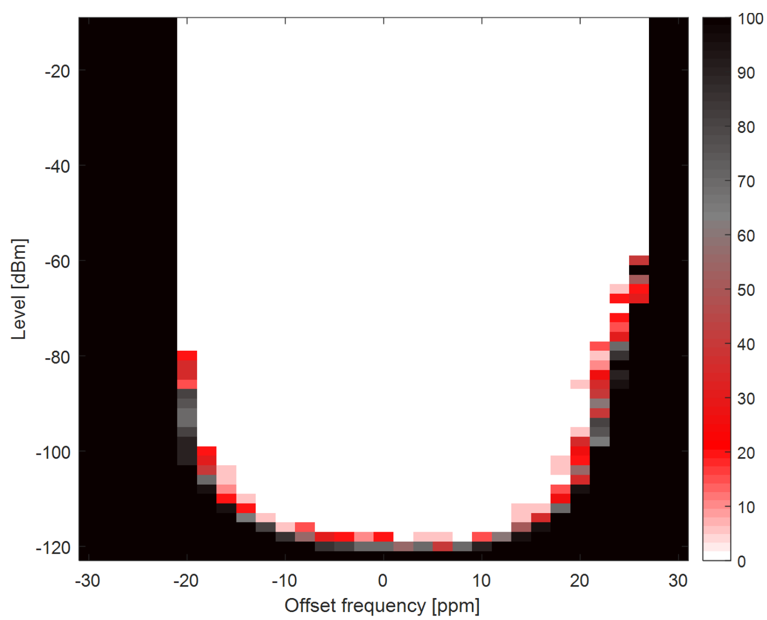

图 8-32. Narrowband, WMBUS N-MODE, 2.4 kbps, 169 MHz

8.26.5 TX Performance

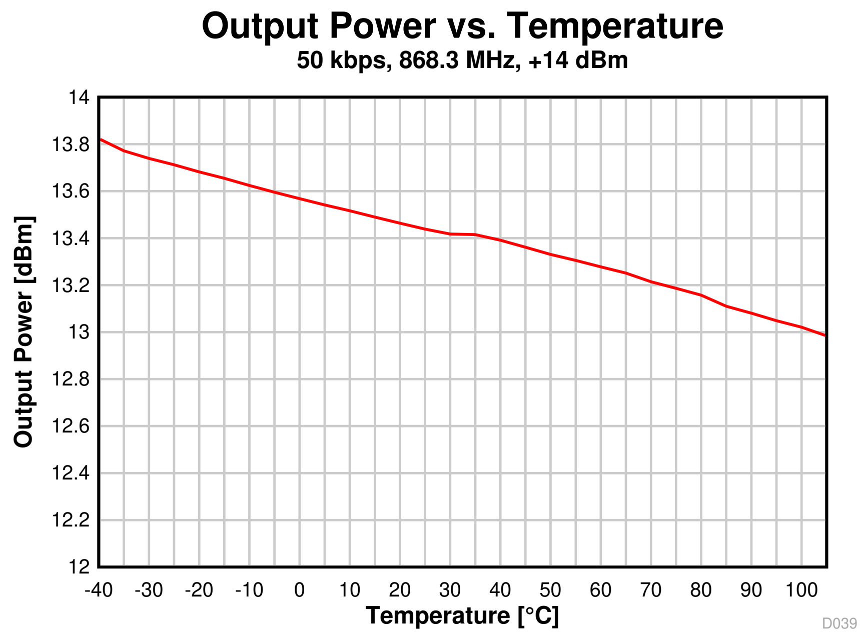

图 8-33. Output Power vs. Temperature (50 kbps, 868.3 MHz)

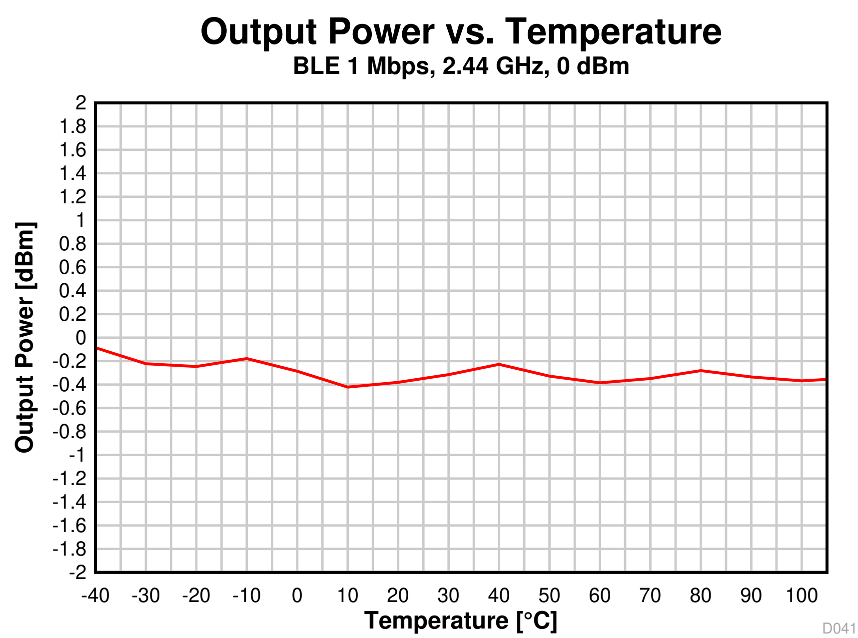

图 8-34. Output Power vs. Temperature (BLE 1 Mbps, 2.44 GHz)

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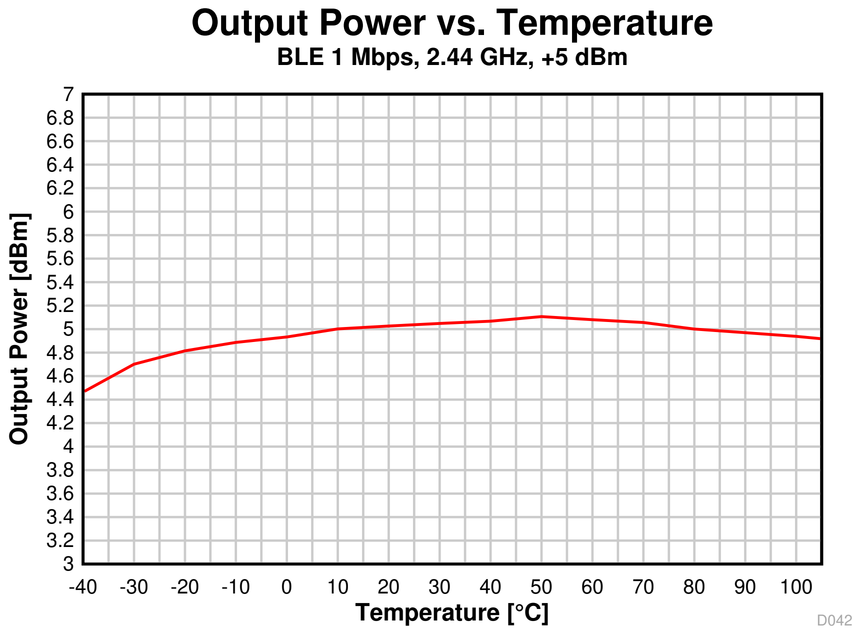

图 8-35. Output Power vs. Temperature (BLE 1 Mbps, 2.44 GHz, +5 dBm)

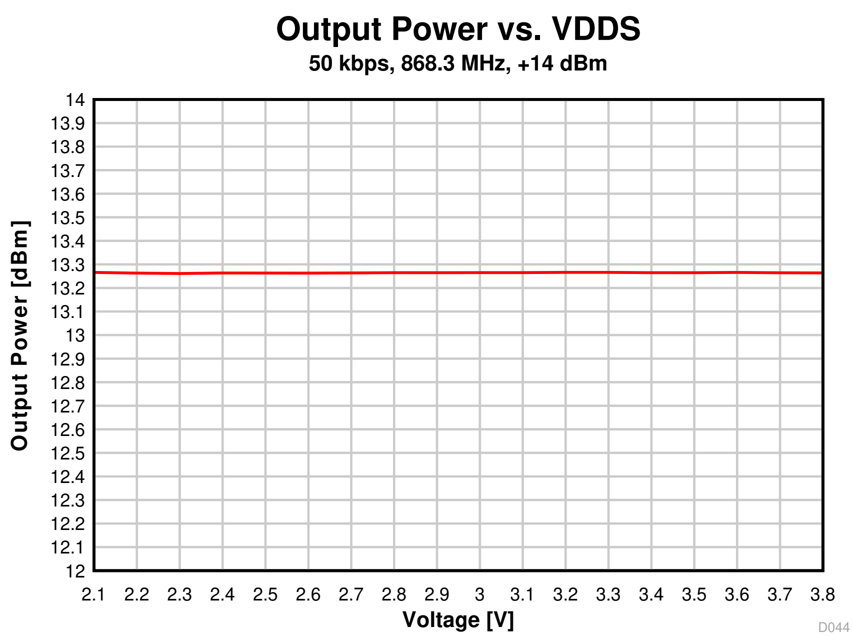

图 8-36. Output Power vs. Supply Voltage (VDDS) (50 kbps, 868.3 MHz)

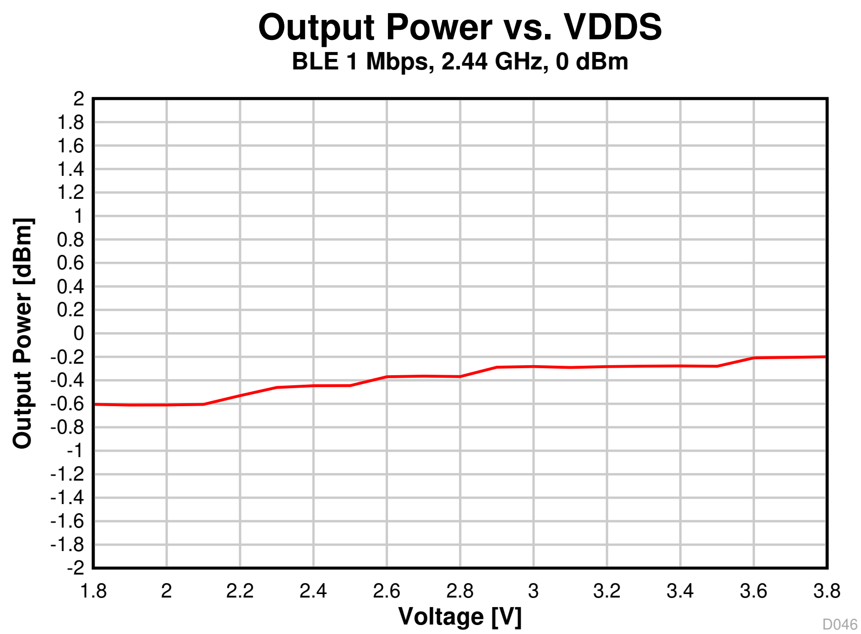

图 8-37. Output Power vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz)

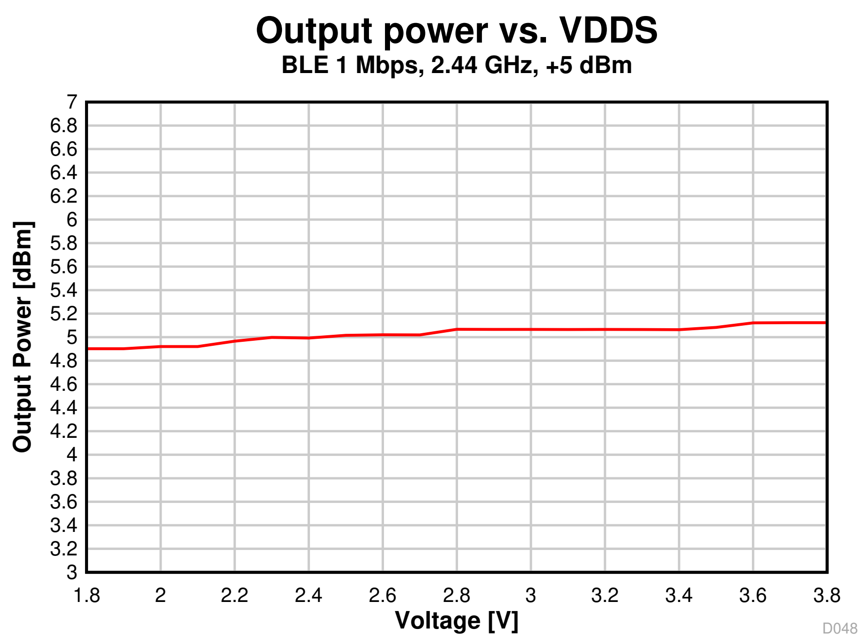

图 8-38. Output Power vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, +5 dBm)

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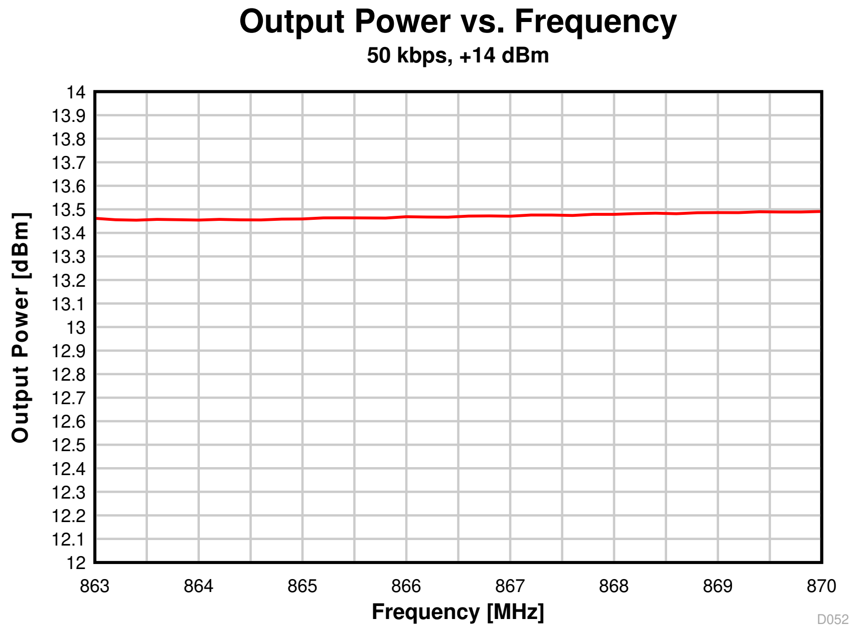

图 8-39. Output Power vs. Frequency (50 kbps, 868 MHz)

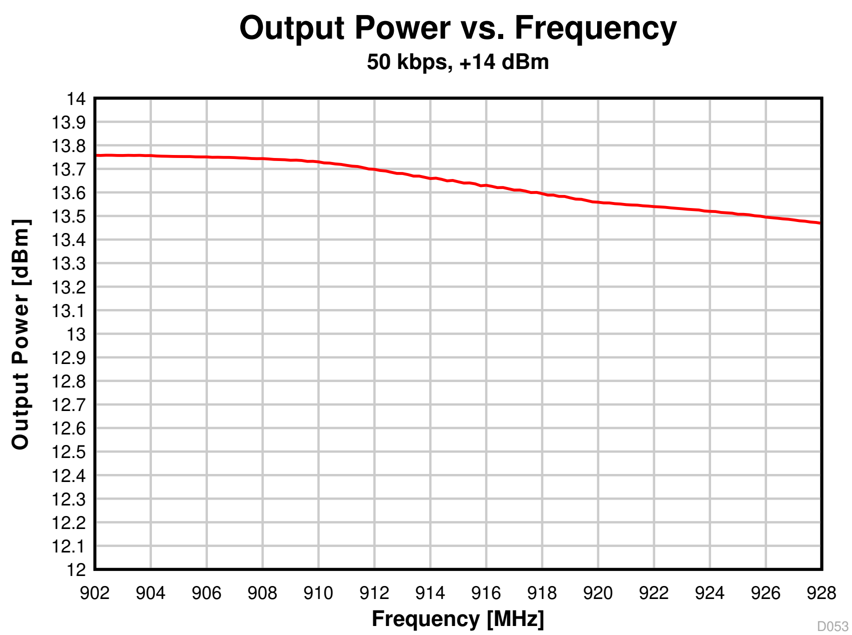

图 8-40. Output Power vs. Frequency (50 kbps, 915 MHz)

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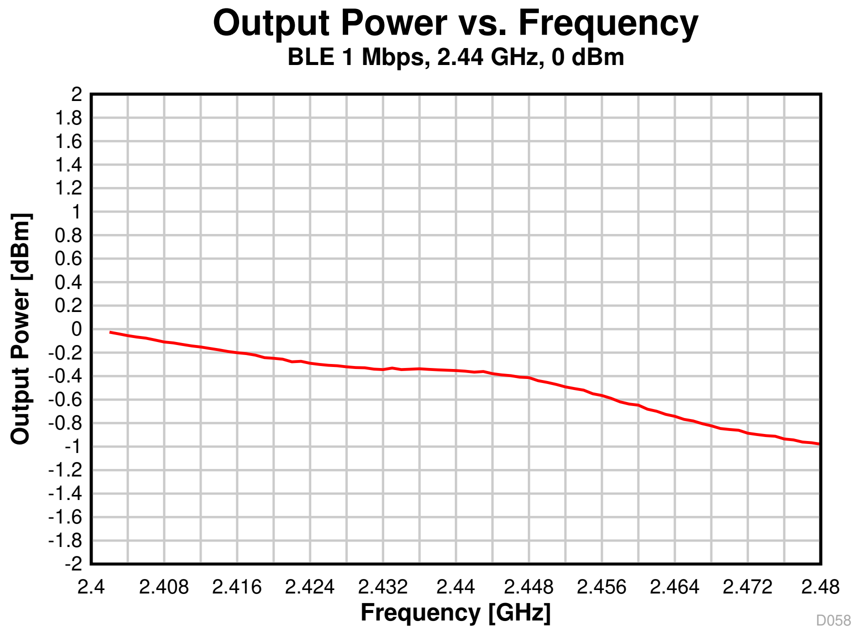

图 8-41. Output Power vs. Frequency (BLE 1 Mbps, 2.44 GHz)

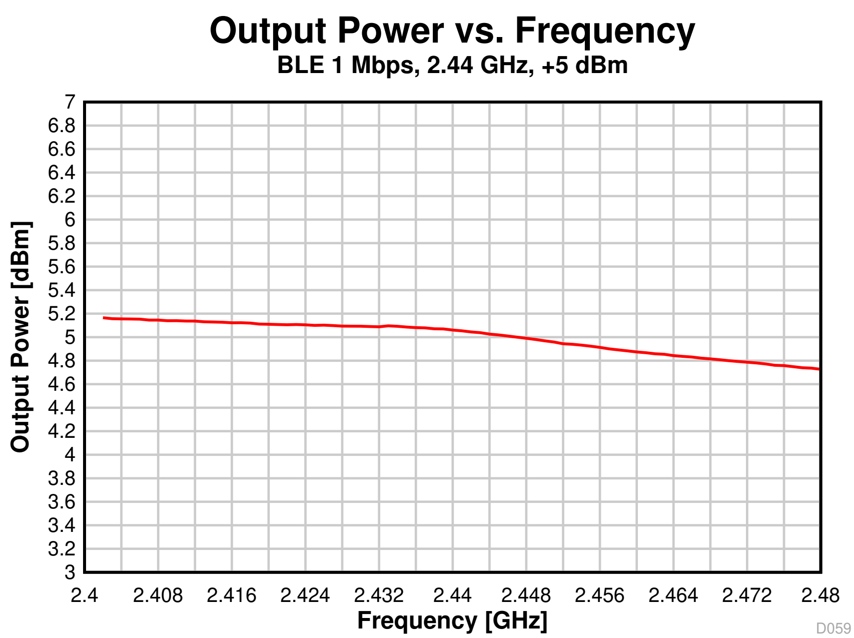

图 8-42. Output Power vs. Frequency (BLE 1 Mbps, 2.44 GHz, +5 dBm)

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8.26.6 ADC Performance

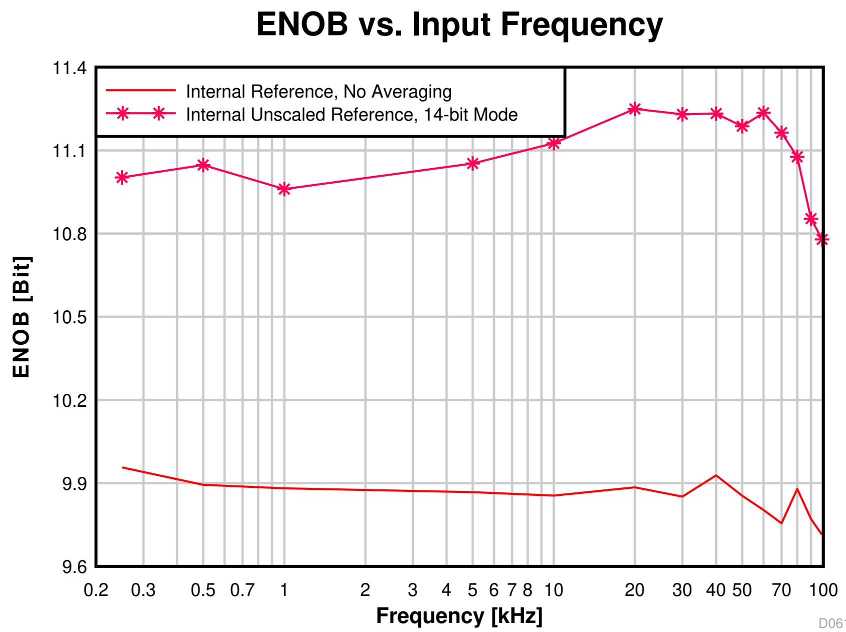

图 8-43. ENOB vs. Input Frequency

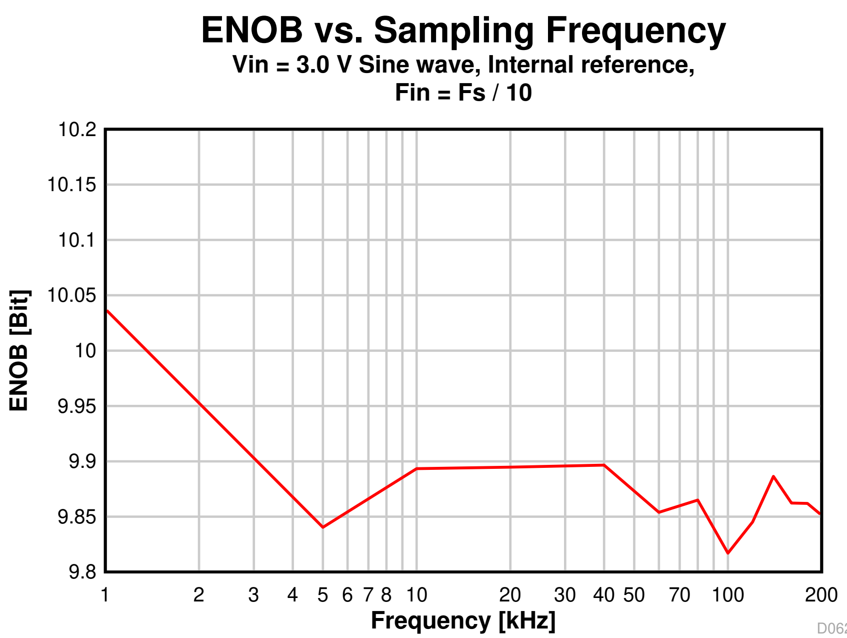

图 8-44. ENOB vs. Sampling Frequency

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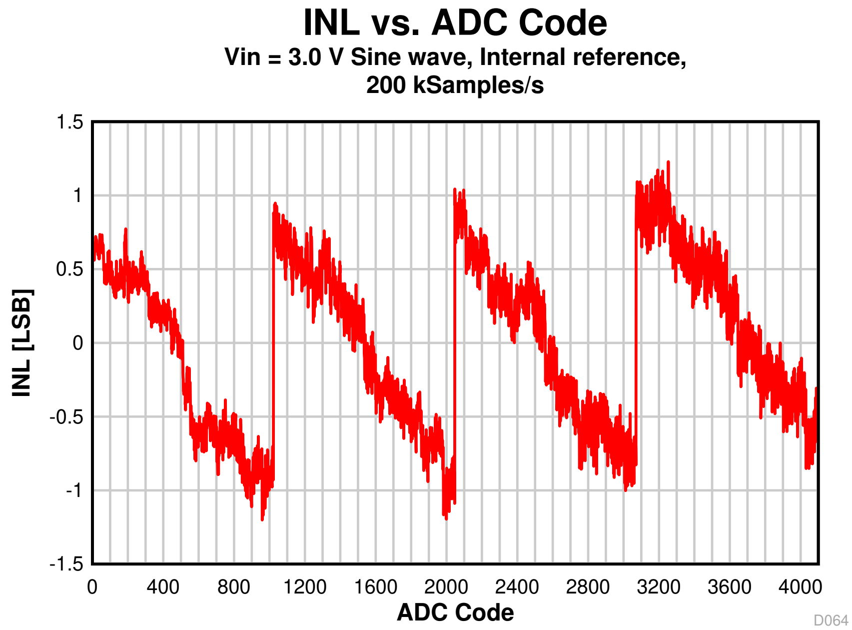

图 8-45. INL vs. ADC Code

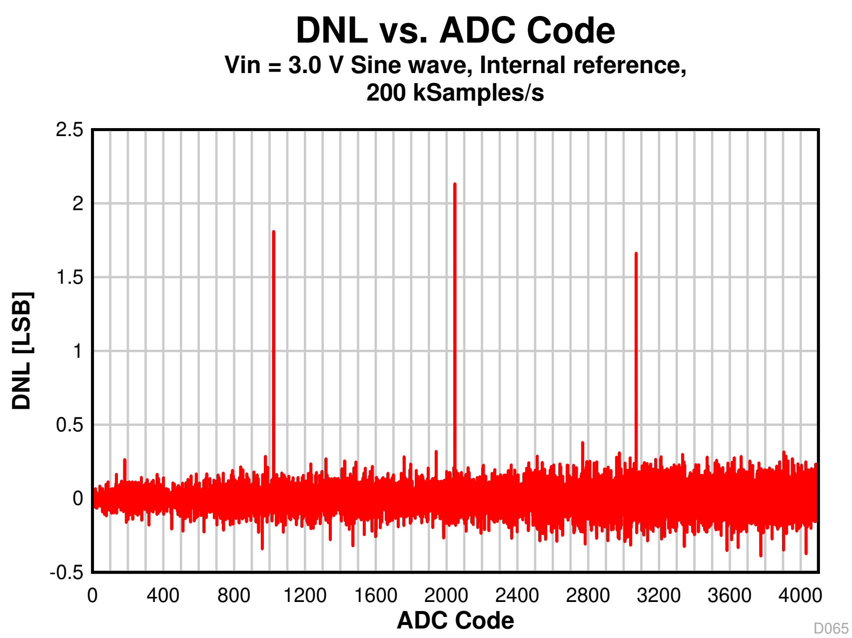

图 8-46. DNL vs. ADC Code

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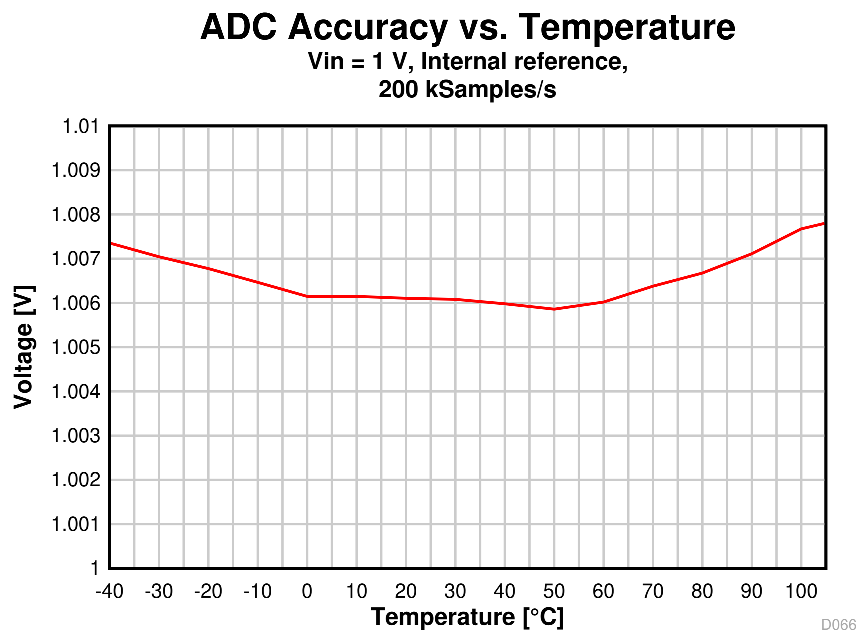

图 8-47. ADC Accuracy vs. Temperature

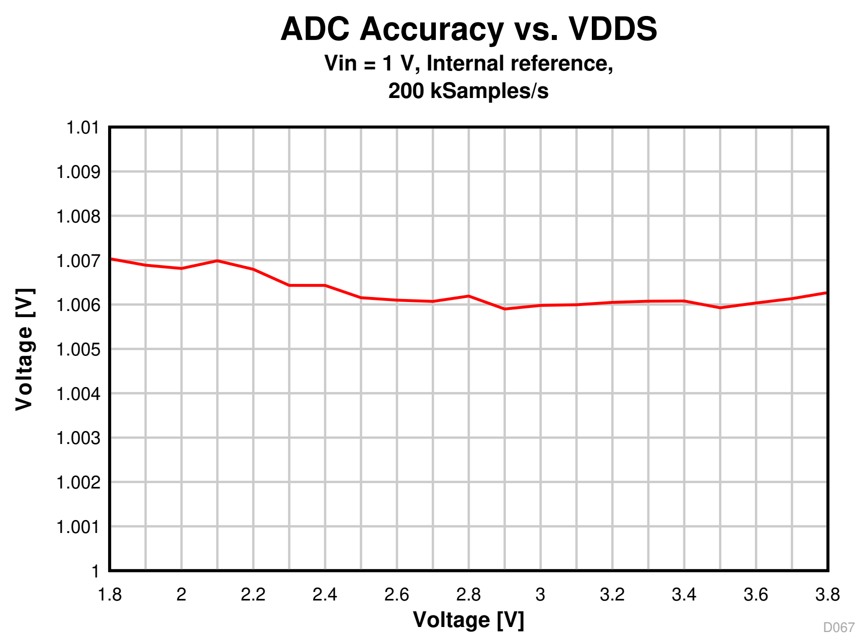

图 8-48. ADC Accuracy vs. Supply Voltage (VDDS)

9 Detailed Description

9.1 Overview

节 4 shows the core modules of the CC1352R device.

9.2 System CPU

The CC1352R SimpleLink™ Wireless MCU contains an Arm® Cortex®-M4F system CPU, which runs the application and the higher layers of radio protocol stacks.

The system CPU is the foundation of a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

Its features include the following:

- ARMv7-M architecture optimized for small-footprint embedded applications
- Arm Thumb®-2 mixed 16- and 32-bit instruction set delivers the high performance expected of a 32-bit Arm core in a compact memory size
- Fast code execution permits increased sleep mode time
- Deterministic, high-performance interrupt handling for time-critical applications
- Single-cycle multiply instruction and hardware divide
- Hardware division and fast digital-signal-processing oriented multiply accumulate
- Saturating arithmetic for signal processing
- IEEE 754-compliant single-precision Floating Point Unit (FPU)
- Memory Protection Unit (MPU) for safety-critical applications
- Full debug with data matching for watchpoint generation
  - Data Watchpoint and Trace Unit (DWT)
  - JTAG Debug Access Port (DAP)
  - Flash Patch and Breakpoint Unit (FPB)
- Trace support reduces the number of pins required for debugging and tracing
  - Instrumentation Trace Macrocell Unit (ITM)
  - Trace Port Interface Unit (TPIU) with asynchronous serial wire output (SWO)
- Optimized for single-cycle flash memory access
- Tightly connected to 8-KB 4-way random replacement cache for minimal active power consumption and wait states
- Ultra-low-power consumption with integrated sleep modes
- 48 MHz operation
- 1.25 DMIPS per MHz

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9.3 Radio (RF Core)

The RF Core is a highly flexible and future proof radio module which contains an Arm Cortex-M0 processor that interfaces the analog RF and base-band circuitry, handles data to and from the system CPU side, and assembles the information bits in a given packet structure. The RF core offers a high level, command-based API to the main CPU that configurations and data are passed through. The Arm Cortex-M0 processor is not programmable by customers and is interfaced through the TI-provided RF driver that is included with the SimpleLink Software Development Kit (SDK).

The RF core can autonomously handle the time-critical aspects of the radio protocols, thus offloading the main CPU, which reduces power and leaves more resources for the user application. Several signals are also available to control external circuitry such as RF switches or range extenders autonomously.

Dual-band and multiprotocol solutions are enabled through time-sliced access of the radio, handled transparently for the application through the TI-provided RF driver and dual-mode manager.

A Packet Traffic Arbitrator (PTA) scheme is available for the managed coexistence of BLE and a co-located 2.4-GHz radio. This is based on 802.15.2 recommendations and common industry standards. The 3-wire coexistence interface has multiple modes of operation, encompassing different use cases and number of lines used for signaling. The radio acting as a slave is able to request access to the 2.4-GHz ISM band, and the master to grant it. Information about the request priority and TX or RX operation can also be conveyed.

The various physical layer radio formats are partly built as a software defined radio where the radio behavior is either defined by radio ROM contents or by non-ROM radio formats delivered in form of firmware patches with the SimpleLink SDKs. This allows the radio platform to be updated for support of future versions of standards even with over-the-air (OTA) updates while still using the same silicon.

备注

Not all combinations of features, frequencies, data rates, and modulation formats described in this chapter are supported. Over time, TI can enable new physical radio formats (PHYs) for the device and provides performance numbers for selected PHYs in the data sheet. Supported radio formats for a specific device, including optimized settings to use with the TI RF driver, are included in the SmartRF Studio tool with performance numbers of selected formats found in the *Specifications* section.

9.3.1 Proprietary Radio Formats

The CC1352R radio can support a wide range of physical radio formats through a set of hardware peripherals combined with firmware available in the device ROM, covering various customer needs for optimizing towards parameters such as speed or sensitivity. This allows great flexibility in tuning the radio both to work with legacy protocols as well as customizing the behavior for specific application needs.

表 9-1 gives a simplified overview of features of the various radio formats available in ROM. Other radio formats may be available in the form of radio firmware patches or programs through the Software Development Kit (SDK) and may combine features in a different manner, as well as add other features.

表 9-1. Feature Support

Feature	Main 2-(G)FSK Mode	High Data Rates	Low Data Rates	SimpleLink™ Long Range
Programmable preamble, sync word, and CRC	Yes	Yes	Yes	No
Programmable receive bandwidth	Yes	Yes	Yes (down to 4 kHz)	Yes
Data / Symbol rate(3)	20 to 1000 kbps	⩽ 2 Msps	⩽ 100 ksps	⩽ 20 ksps
Modulation format	2-(G)FSK	2-(G)FSK 4-(G)FSK	2-(G)FSK 4-(G)FSK	2-(G)FSK
Dual Sync Word	Yes	Yes	No	No
Carrier Sense (1) (2)	Yes	No	No	No
Preamble Detection(2)	Yes	Yes	Yes	No
Data Whitening	Yes	Yes	Yes	Yes
Digital RSSI	Yes	Yes	Yes	Yes
CRC filtering	Yes	Yes	Yes	Yes
Direct-sequence spread spectrum (DSSS)	No	No	No	1:2 1:4 1:8
Forward error correction (FEC)	No	No	No	Yes
Link Quality Indicator (LQI)	Yes	Yes	Yes	Yes

(1) Carrier Sense can be used to implement HW-controlled listen-before-talk (LBT) and Clear Channel Assessment (CCA) for compliance with such requirements in regulatory standards. This is available through the CMD_PROP_CS radio API.
(2) Carrier Sense and Preamble Detection can be used to implement sniff modes where the radio is duty cycled to save power.
(3) Data rates are only indicative. Data rates outside this range may also be supported. For some specific combinations of settings, a smaller range might be supported.

9.3.2 Bluetooth 5.2 Low Energy

The RF Core offers full support for Bluetooth 5.2 Low Energy, including the high-sped 2-Mbps physical layer and the 500-kbps and 125-kbps long range PHYs (Coded PHY) through the TI provided Bluetooth 5.2 stack or through a high-level Bluetooth API. The Bluetooth 5.2 PHY and part of the controller are in radio and system ROM, providing significant savings in memory usage and more space available for applications.

The new high-speed mode allows data transfers up to 2 Mbps, twice the speed of Bluetooth 4.2 and five times the speed of Bluetooth 4.0, without increasing power consumption. In addition to faster speeds, this mode offers significant improvements for energy efficiency and wireless coexistence with reduced radio communication time.

Bluetooth 5.2 also enables unparalleled flexibility for adjustment of speed and range based on application needs, which capitalizes on the high-speed or long-range modes respectively. Data transfers are now possible at 2 Mbps, enabling development of applications using voice, audio, imaging, and data logging that were not previously an option using Bluetooth low energy. With high-speed mode, existing applications deliver faster responses, richer engagement, and longer battery life. Bluetooth 5.2 enables fast, reliable firmware updates.

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9.3.3 802.15.4 (Thread, Zigbee, 6LoWPAN)

Through a dedicated IEEE radio API, the RF Core supports the 2.4-GHz IEEE 802.15.4-2011 physical layer (2 Mchips per second Offset-QPSK with DSSS 1:8), used in Thread, Zigbee, and 6LoWPAN protocols. The 802.15.4 PHY and MAC are in radio and system ROM. TI also provides royalty-free protocol stacks for Thread and Zigbee as part of the SimpleLink SDK, enabling a robust end-to-end solution.

9.4 Memory

The up to 352-KB nonvolatile (Flash) memory provides storage for code and data. The flash memory is in-system programmable and erasable. The last flash memory sector must contain a Customer Configuration section (CCFG) that is used by boot ROM and TI provided drivers to configure the device. This configuration is done through the ccfg.c source file that is included in all TI provided examples.

The ultra-low leakage system static RAM (SRAM) is split into up to five 16-KB blocks and can be used for both storage of data and execution of code. Retention of SRAM contents in Standby power mode is enabled by default and included in Standby mode power consumption numbers. Parity checking for detection of bit errors in memory is built-in, which reduces chip-level soft errors and thereby increases reliability. System SRAM is always initialized to zeroes upon code execution from boot.

To improve code execution speed and lower power when executing code from nonvolatile memory, a 4-way nonassociative 8-KB cache is enabled by default to cache and prefetch instructions read by the system CPU. The cache can be used as a general-purpose RAM by enabling this feature in the Customer Configuration Area (CCFG).

There is a 4-KB ultra-low leakage SRAM available for use with the Sensor Controller Engine which is typically used for storing Sensor Controller programs, data and configuration parameters. This RAM is also accessible by the system CPU. The Sensor Controller RAM is not cleared to zeroes between system resets.

The ROM includes a TI-RTOS kernel and low-level drivers, as well as significant parts of selected radio stacks, which frees up flash memory for the application. The ROM also contains a serial (SPI and UART) bootloader that can be used for initial programming of the device.

9.5 Sensor Controller

The Sensor Controller contains circuitry that can be selectively enabled in both Standby and Active power modes. The peripherals in this domain can be controlled by the Sensor Controller Engine, which is a proprietary power-optimized CPU. This CPU can read and monitor sensors or perform other tasks autonomously; thereby significantly reducing power consumption and offloading the system CPU.

The Sensor Controller Engine is user programmable with a simple programming language that has syntax similar to C. This programmability allows for sensor polling and other tasks to be specified as sequential algorithms rather than static configuration of complex peripheral modules, timers, DMA, register programmable state machines, or event routing.

The main advantages are:

- Flexibility - data can be read and processed in unlimited manners while still ensuring ultra-low power
- 2 MHz low-power mode enables lowest possible handling of digital sensors
- Dynamic reuse of hardware resources
- 40-bit accumulator supporting multiplication, addition and shift
- Observability and debugging options

Sensor Controller Studio is used to write, test, and debug code for the Sensor Controller. The tool produces C driver source code, which the System CPU application uses to control and exchange data with the Sensor Controller. Typical use cases may be (but are not limited to) the following:

- Read analog sensors using integrated ADC or comparators
- Interface digital sensors using GPIOs, SPI, UART, or I^2C (UART and I^2C are bit-banged)
- Capacitive sensing
- Waveform generation

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- Very low-power pulse counting (flow metering)
- Key scan

The peripherals in the Sensor Controller include the following:

- The low-power clocked comparator can be used to wake the system CPU from any state in which the comparator is active. A configurable internal reference DAC can be used in conjunction with the comparator. The output of the comparator can also be used to trigger an interrupt or the ADC.
- Capacitive sensing functionality is implemented through the use of a constant current source, a time-to-digital converter, and a comparator. The continuous time comparator in this block can also be used as a higher-accuracy alternative to the low-power clocked comparator. The Sensor Controller takes care of baseline tracking, hysteresis, filtering, and other related functions when these modules are used for capacitive sensing.
- The ADC is a 12-bit, 200-ksamples/s ADC with eight inputs and a built-in voltage reference. The ADC can be triggered by many different sources including timers, I/O pins, software, and comparators.
- The analog modules can connect to up to eight different GPIOs
- Dedicated SPI master with up to 6 MHz clock speed

The peripherals in the Sensor Controller can also be controlled from the main application processor.

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9.6 Cryptography

The CC1352R device comes with a wide set of modern cryptography-related hardware accelerators, drastically reducing code footprint and execution time for cryptographic operations. It also has the benefit of being lower power and improves availability and responsiveness of the system because the cryptography operations runs in a background hardware thread.
Together with a large selection of open-source cryptography libraries provided with the Software Development Kit (SDK), this allows for secure and future proof IoT applications to be easily built on top of the platform. The hardware accelerator modules are:

- **True Random Number Generator (TRNG)** module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear-combinatorial circuit.
- **Secure Hash Algorithm 2 (SHA-2)** with support for SHA224, SHA256, SHA384, and SHA512
- **Advanced Encryption Standard (AES)** with 128 and 256 bit key lengths
- **Public Key Accelerator** - Hardware accelerator supporting mathematical operations needed for elliptic curves up to 512 bits and RSA key pair generation up to 1024 bits.

Through use of these modules and the TI provided cryptography drivers, the following capabilities are available for an application or stack:

- **Key Agreement Schemes**
  - Elliptic curve Diffie–Hellman with static or ephemeral keys (ECDH and ECDHE)
  - Elliptic curve Password Authenticated Key Exchange by Juggling (ECJ-PAKE)
- **Signature Generation**
  - Elliptic curve Diffie-Hellman Digital Signature Algorithm (ECDSA)
- **Curve Support**
  - Short Weierstrass form (full hardware support), such as:
    - NIST-P224, NIST-P256, NIST-P384, NIST-P521
    - Brainpool-256R1, Brainpool-384R1, Brainpool-512R1
    - secp256r1
  - Montgomery form (hardware support for multiplication), such as:
    - Curve25519
- **SHA2 based MACs**
  - HMAC with SHA224, SHA256, SHA384, or SHA512
- Block cipher mode of operation
  - AESCCM
  - AESGCM
  - AESECB
  - AESCBC
  - AESCBC-MAC
- **True random number generation**

Other capabilities, such as RSA encryption and signatures as well as Edwards type of elliptic curves such as Curve1174 or Ed25519, can also be implemented using the provided hardware accelerators but are not part of the TI SimpleLink SDK for the CC1352R device.

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9.7 Timers

A large selection of timers are available as part of the CC1352R device. These timers are:

- **Real-Time Clock (RTC)**

  A 70-bit 3-channel timer running on the 32 kHz low frequency system clock (SCLK_LF)
  This timer is available in all power modes except Shutdown. The timer can be calibrated to compensate for frequency drift when using the LF RCOSC as the low frequency system clock. If an external LF clock with frequency different from 32.768 kHz is used, the RTC tick speed can be adjusted to compensate for this. When using TI-RTOS, the RTC is used as the base timer in the operating system and should thus only be accessed through the kernel APIs such as the Clock module. The real time clock can also be read by the Sensor Controller Engine to timestamp sensor data and also has dedicated capture channels. By default, the RTC halts when a debugger halts the device.
- **General Purpose Timers (GPTIMER)**

  The four flexible GPTIMERs can be used as either 4× 32 bit timers or 8× 16 bit timers, all running on up to 48 MHz. Each of the 16- or 32-bit timers support a wide range of features such as one-shot or periodic counting, pulse width modulation (PWM), time counting between edges and edge counting. The inputs and outputs of the timer are connected to the device event fabric, which allows the timers to interact with signals such as GPIO inputs, other timers, DMA and ADC. The GPTIMERs are available in Active and Idle power modes.
- **Sensor Controller Timers**

  The Sensor Controller contains 3 timers:

  AUX Timer 0 and 1 are 16-bit timers with a 2^N prescaler. Timers can either increment on a clock or on each edge of a selected tick source. Both one-shot and periodical timer modes are available.

  AUX Timer 2 is a 16-bit timer that can operate at 24 MHz, 2 MHz or 32 kHz independent of the Sensor Controller functionality. There are 4 capture or compare channels, which can be operated in one-shot or periodical modes. The timer can be used to generate events for the Sensor Controller Engine or the ADC, as well as for PWM output or waveform generation.
- **Radio Timer**

  A multichannel 32-bit timer running at 4 MHz is available as part of the device radio. The radio timer is typically used as the timing base in wireless network communication using the 32-bit timing word as the network time. The radio timer is synchronized with the RTC by using a dedicated radio API when the device radio is turned on or off. This ensures that for a network stack, the radio timer seems to always be running when the radio is enabled. The radio timer is in most cases used indirectly through the trigger time fields in the radio APIs and should only be used when running the accurate 48 MHz high frequency crystal is the source of SCLK_HF.
- **Watchdog timer**

  The watchdog timer is used to regain control if the system operates incorrectly due to software errors. It is typically used to generate an interrupt to and reset of the device for the case where periodic monitoring of the system components and tasks fails to verify proper functionality. The watchdog timer runs on a 1.5 MHz clock rate and cannot be stopped once enabled. The watchdog timer pauses to run in Standby power mode and when a debugger halts the device.

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9.8 Serial Peripherals and I/O

The SSIs are synchronous serial interfaces that are compatible with SPI, MICROWIRE, and TI's synchronous serial interfaces. The SSIs support both SPI master and slave up to 4 MHz. The SSI modules support configurable phase and polarity.

The UARTs implement universal asynchronous receiver and transmitter functions. They support flexible baud-rate generation up to a maximum of 3 Mbps.

The I^2S interface is used to handle digital audio and can also be used to interface pulse-density modulation microphones (PDM).

The I^2C interface is also used to communicate with devices compatible with the I^2C standard. The I^2C interface can handle 100 kHz and 400 kHz operation, and can serve as both master and slave.

The I/O controller (IOC) controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high-drive capabilities, which are marked in **bold** in 节 7. All digital peripherals can be connected to any digital pin on the device.

For more information, see the CC13x2, CC26x2 SimpleLink™ Wireless MCU Technical Reference Manual.

9.9 Battery and Temperature Monitor

A combined temperature and battery voltage monitor is available in the CC1352R device. The battery and temperature monitor allows an application to continuously monitor on-chip temperature and supply voltage and respond to changes in environmental conditions as needed. The module contains window comparators to interrupt the system CPU when temperature or supply voltage go outside defined windows. These events can also be used to wake up the device from Standby mode through the Always-On (AON) event fabric.

9.10 µDMA

The device includes a direct memory access (µDMA) controller. The µDMA controller provides a way to offload data-transfer tasks from the system CPU, thus allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform a transfer between memory and peripherals. The µDMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

Some features of the µDMA controller include the following (this is not an exhaustive list):

- Highly flexible and configurable channel operation of up to 32 channels
- Transfer modes: memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits
- Ping-pong mode for continuous streaming of data

9.11 Debug

The on-chip debug support is done through a dedicated cJTAG (IEEE 1149.7) or JTAG (IEEE 1149.1) interface. The device boots by default into cJTAG mode and must be reconfigured to use 4-pin JTAG.

9.12 Power Management

To minimize power consumption, the CC1352R supports a number of power modes and power management features (see 表 9-2).

表 9-2. Power Modes

MODE	SOFTWARE CONFIGURABLE POWER MODES				RESET PIN HELD
	ACTIVE	IDLE	STANDBY	SHUTDOWN	
CPU	Active	Off	Off	Off	Off
Flash	On	Available	Off	Off	Off
SRAM	On	On	Retention	Off	Off
Supply System	On	On	Duty Cycled	Off	Off
Register and CPU retention	Full	Full	Partial	No	No
SRAM retention	Full	Full	Full	No	No
48 MHz high-speed clock (SCLK_HF)	XOSC_HF or RCOSC_HF	XOSC_HF or RCOSC_HF	Off	Off	Off
2 MHz medium-speed clock (SCLK_MF)	RCOSC_MF	RCOSC_MF	Available	Off	Off
32 kHz low-speed clock (SCLK_LF)	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	Off	Off
Peripherals	Available	Available	Off	Off	Off
Sensor Controller	Available	Available	Available	Off	Off
Wake-up on RTC	Available	Available	Available	Off	Off
Wake-up on pin edge	Available	Available	Available	Available	Off
Wake-up on reset pin	On	On	On	On	On
Brownout detector (BOD)	On	On	Duty Cycled	Off	Off
Power-on reset (POR)	On	On	On	Off	Off
Watchdog timer (WDT)	Available	Available	Paused	Off	Off

In **Active** mode, the application system CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see 表 9-2).

In **Idle** mode, all active peripherals can be clocked, but the Application CPU core and memory are not clocked and no code is executed. Any interrupt event brings the processor back into active mode.

In **Standby** mode, only the always-on (AON) domain is active. An external wake-up event, RTC event, or Sensor Controller event is required to bring the device back to active mode. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In **Shutdown** mode, the device is entirely turned off (including the AON domain and Sensor Controller), and the I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a *wake from shutdown pin* wakes up the device and functions as a reset trigger. The CPU can differentiate between reset in this way and reset-by-reset pin or power-on reset by reading the reset status register. The only state retained in this mode is the latched I/O state and the flash memory contents.

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The Sensor Controller is an autonomous processor that can control the peripherals in the Sensor Controller independently of the system CPU. This means that the system CPU does not have to wake up, for example to perform an ADC sampling or poll a digital sensor over SPI, thus saving both current and wake-up time that would otherwise be wasted. The Sensor Controller Studio tool enables the user to program the Sensor Controller, control its peripherals, and wake up the system CPU as needed. All Sensor Controller peripherals can also be controlled by the system CPU.

备注

The power, RF and clock management for the CC1352R device require specific configuration and handling by software for optimized performance. This configuration and handling is implemented in the TI-provided drivers that are part of the CC1352R software development kit (SDK). Therefore, TI highly recommends using this software framework for all application development on the device. The complete SDK with TI-RTOS (optional), device drivers, and examples are offered free of charge in source code.

9.13 Clock Systems

The CC1352R device has several internal system clocks.

The 48 MHz SCLK_HF is used as the main system (MCU and peripherals) clock. This can be driven by the internal 48 MHz RC Oscillator (RCOSC_HF) or an external 48 MHz crystal (XOSC_HF). Radio operation requires an external 48 MHz crystal or TCXO.

SCLK_MF is an internal 2 MHz clock that is used by the Sensor Controller in low-power mode and also for internal power management circuitry. The SCLK_MF clock is always driven by the internal 2 MHz RC Oscillator (RCOSC_MF).

SCLK_LF is the 32.768 kHz internal low-frequency system clock. It can be used by the Sensor Controller for ultra-low-power operation and is also used for the RTC and to synchronize the radio timer before or after Standby power mode. SCLK_LF can be driven by the internal 32.8 kHz RC Oscillator (RCOSC_LF), a 32.768 kHz watch-type crystal, or a clock input on any digital IO.

When using a crystal or the internal RC oscillator, the device can output the 32 kHz SCLK_LF signal to other devices, thereby reducing the overall system cost.

9.14 Network Processor

Depending on the product configuration, the CC1352R device can function as a wireless network processor (WNP - a device running the wireless protocol stack with the application running on a separate host MCU), or as a system-on-chip (SoC) with the application and protocol stack running on the system CPU inside the device.

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

10 Application, Implementation, and Layout

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

For general design guidelines and hardware configuration guidelines, refer to the *CC13xx/CC26xx Hardware Configuration and PCB Design Considerations Application Report*.

10.1 Reference Designs

The following reference designs should be followed closely when implementing designs using the CC1352R device.

Special attention must be paid to RF component placement, decoupling capacitors and DCDC regulator components, as well as ground connections for all of these.

Integrated matched filter-balun devices can be used both at sub-1 GHz frequencies and at 2.4 GHz for the low-power RF outputs. Refer to the "Integrated Passive Component" section in CC13xx/CC26xx Hardware Configuration and PCB Design Considerations for further information.

CC1352REM-XD7793-XD24 Design Files — The CC1352REM-XD7793-XD24 reference design provides schematic, layout and production files for the characterization board used for deriving the performance number found in this document.

LAUNCHXL-CC1352R1 Design Files — The CC1352R LaunchPad Design Files contain detailed schematics and layouts to build application specific boards using the CC1352R device.

LAUNCHXL-CC1352P-4 Design Files — Detailed schematics and layouts for the multi-band CC1352P LaunchPad evaluation board featuring 2.4 GHz RF matching optimized for 10 dBm operation on the 20 dBm PA output and up to 13 dBm TX power at 433 MHz.

Sub-1 GHz and 2.4 GHz Antenna Kit for LaunchPad ™ Development Kit and SensorTag — The antenna kit allows real-life testing to identify the optimal antenna for your application. The antenna kit includes 16 antennas for frequencies from 169 MHz to 2.4 GHz, including:

- PCB antennas
- Helical antennas
- Chip antennas
- Dual-band antennas for 868 MHz and 915 MHz combined with 2.4 GHz

The antenna kit includes a JSC cable to connect to the Wireless MCU LaunchPad development kits and SensorTags.

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10.2 Junction Temperature Calculation

This section shows the different techniques for calculating the junction temperature under various operating conditions. For more details, see Semiconductor and IC Package Thermal Metrics.

There are three recommended ways to derive the junction temperature from other measured temperatures:

1. From package temperature:

$$T_J = \psi_{\mathrm{JT}} \times P + T_{\mathrm{case}} \quad (1)$$

2. From board temperature:

$$T_J = \psi_{\mathrm{JB}} \times P + T_{\mathrm{board}} \quad (2)$$

3. From ambient temperature:

$$T_J = R_{\theta\mathrm{JA}} \times P + T_A \quad (3)$$

P is the power dissipated from the device and can be calculated by multiplying current consumption with supply voltage. Thermal resistance coefficients are found in *Thermal Resistance Characteristics*.

Example:

Using 方程式 3, the temperature difference between ambient temperature and junction temperature is calculated. In this example, we assume a simple use case where the radio is transmitting continuously at 10 dBm output power. Let us assume the ambient temperature is 85 °C and the supply voltage is 3.6 V. To calculate P, we need to look up the current consumption for Tx at 85 °C in 节 8.26. From the plot, we see that the current consumption is 14.4 mA. This means that P is 14.4 mA × 3.6 V = 51.8 mW.

The junction temperature is then calculated as:

$$T_J = 23.4 {}^{\circ C}\!/_{W} \times 51.8mW + T_A = 1.2°C + T_A \quad (4)$$

As can be seen from the example, the junction temperature is 1.2 °C higher than the ambient temperature when running continuous Tx at 85 °C and, thus, well within the recommended operating conditions.

For various application use cases current consumption for other modules may have to be added to calculate the appropriate power dissipation. For example, the MCU may be running simultaneously as the radio, peripheral modules may be enabled, etc. Typically, the easiest way to find the peak current consumption, and thus the peak power dissipation in the device, is to measure as described in Measuring CC13xx and CC26xx current consumption.

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed as follows.

11.1 Tools and Software

The CC1352R device is supported by a variety of software and hardware development tools.

Development Kit

CC1352R LaunchPad™ Development Kit The CC1352R LaunchPad™ Development Kit enables development of high-performance wireless applications in the 863 - 930 MHz and 2.4 GHz frequency bands that benefit from low-power operation. The kit features the CC1352R multi-band and multiprotocol SimpleLink Wireless MCU. The kit works with the LaunchPad ecosystem, easily enabling additional functionality like sensors, display, and more. The built-in EnergyTrace™ software is an energy-based code analysis tool that measures and displays the application's energy profile and helps to optimize it for ultra-low power consumption.

Software

SimpleLink™ CC13x2-CC26x2 SDK The SimpleLink CC13x2-CC26x2 Software Development Kit (SDK) provides a complete package for the development of wireless applications on the CC13x2 / CC26x2 family of devices. The SDK includes a comprehensive software package for the CC1352R device, including the following protocol stacks:

- Bluetooth Low Energy 4 and 5.2
- Thread (based on OpenThread)
- Zigbee 3.0
- TI 15.4-Stack - an IEEE 802.15.4-based star networking solution for Sub-1 GHz and 2.4 GHz
- EasyLink - a large set of building blocks for building proprietary RF software stacks
- Multiprotocol support - concurrent operation between stacks using the Dynamic Multiprotocol Manager (DMM)

The SimpleLink CC13x2-CC26x2 SDK is part of TI's SimpleLink MCU platform, offering a single development environment that delivers flexible hardware, software and tool options for customers developing wired and wireless applications. For more information about the SimpleLink MCU Platform, visit https://www.ti.com/simplelink.

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Development Tools

Code Composer Studio™ Integrated Development Environment (IDE)

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse® software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

CCS has support for all SimpleLink Wireless MCUs and includes support for EnergyTrace™ software (application energy usage profiling). A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK.

Code Composer Studio is provided free of charge when used in conjunction with the XDS debuggers included on a LaunchPad Development Kit.

Code Composer Studio™ Cloud IDE

Code Composer Studio (CCS) Cloud is a web-based IDE that allows you to create, edit and build CCS and Energia™ projects. After you have successfully built your project, you can download and run on your connected LaunchPad. Basic debugging, including features like setting breakpoints and viewing variable values is now supported with CCS Cloud.

IAR Embedded Workbench® for Arm®

IAR Embedded Workbench® is a set of development tools for building and debugging embedded system applications using assembler, C and C++. It provides a completely integrated development environment that includes a project manager, editor, and build tools. IAR has support for all SimpleLink Wireless MCUs. It offers broad debugger support, including XDS110, IAR I-jet™ and Segger J-Link™. A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK. IAR is also supported out-of-the-box on most software examples provided as part of the SimpleLink SDK.

A 30-day evaluation or a 32 KB size-limited version is available through iar.com.

SmartRF™ Studio

SmartRF™ Studio is a Windows® application that can be used to evaluate and configure SimpleLink Wireless MCUs from Texas Instruments. The application will help designers of RF systems to easily evaluate the radio at an early stage in the design process. It is especially useful for generation of configuration register values and for practical testing and debugging of the RF system. SmartRF Studio can be used either as a standalone application or together with applicable evaluation boards or debug probes for the RF device. Features of the SmartRF Studio include:

- Link tests - send and receive packets between nodes
- Antenna and radiation tests - set the radio in continuous wave TX and RX states
- Export radio configuration code for use with the TI SimpleLink SDK RF driver
- Custom GPIO configuration for signaling and control of external switches

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Sensor Controller Studio

Sensor Controller Studio is used to write, test and debug code for the Sensor Controller peripheral. The tool generates a Sensor Controller Interface driver, which is a set of C source files that are compiled into the System CPU application. These source files also contain the Sensor Controller binary image and allow the System CPU application to control and exchange data with the Sensor Controller. Features of the Sensor Controller Studio include:

- Ready-to-use examples for several common use cases
- Full toolchain with built-in compiler and assembler for programming in a C-like programming language
- Provides rapid development by using the integrated sensor controller task testing and debugging functionality, including visualization of sensor data and verification of algorithms

CCS UniFlash

CCS UniFlash is a standalone tool used to program on-chip flash memory on TI MCUs. UniFlash has a GUI, command line, and scripting interface. CCS UniFlash is available free of charge.

11.1.1 SimpleLink™ Microcontroller Platform

The SimpleLink microcontroller platform sets a new standard for developers with the broadest portfolio of wired and wireless Arm® MCUs (System-on-Chip) in a single software development environment. Delivering flexible hardware, software and tool options for your IoT applications. Invest once in the SimpleLink software development kit and use throughout your entire portfolio. Learn more on ti.com/simplelink.

11.2 Documentation Support

To receive notification of documentation updates on data sheets, errata, application notes and similar, navigate to the device product folder on ti.com/product/CC1352R. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the MCU, related peripherals, and other technical collateral is listed as follows.

TI Resource Explorer

TI Resource Explorer

Software examples, libraries, executables, and documentation are available for your device and development board.

Errata

CC1352R Silicon Errata

The silicon errata describes the known exceptions to the functional specifications for each silicon revision of the device and description on how to recognize a device revision.

Application Reports

All application reports for the CC1352R device are found on the device product folder at: ti.com/product/CC1352R/technicaldocuments.

Technical Reference Manual (TRM)

CC13x2, CC26x2 SimpleLink™ Wireless MCU TRM

The TRM provides a detailed description of all modules and peripherals available in the device family.

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11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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11.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

12.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC1352R1F3RGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 105	CC1352 R1F3	Samples
CC1352R1F3RGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 105	CC1352 R1F3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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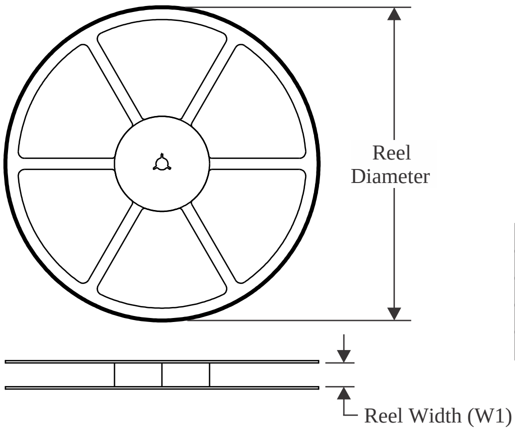
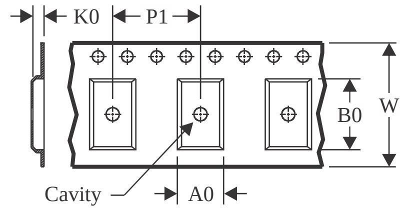
TAPE AND REEL INFORMATION

REEL DIMENSIONS

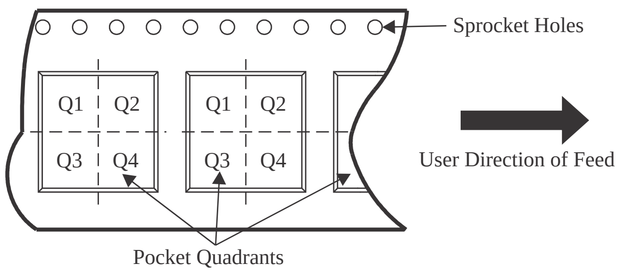


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

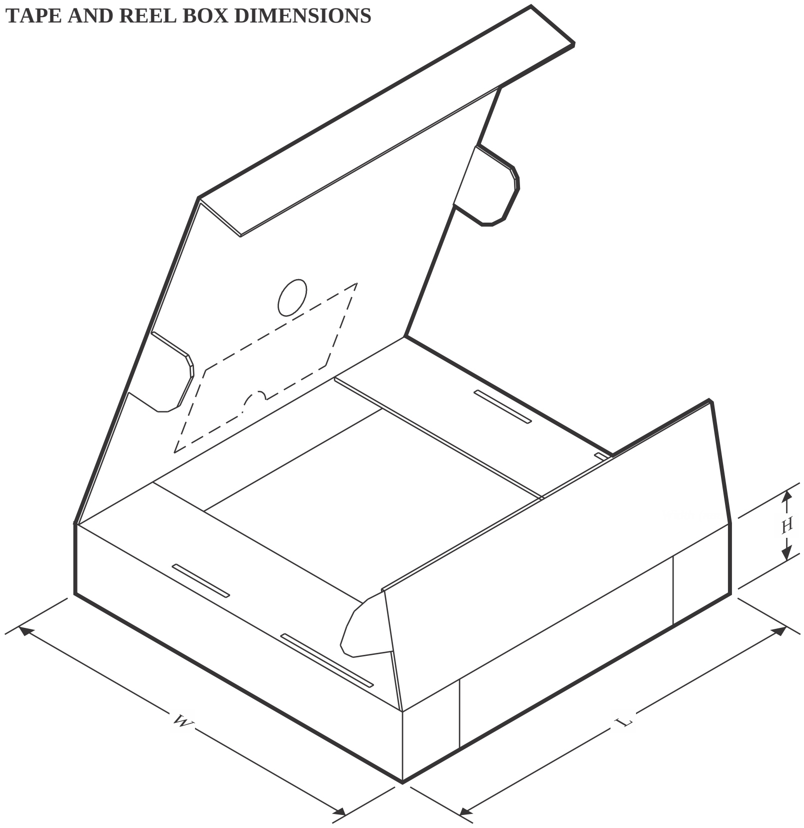
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC1352R1F3RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
CC1352R1F3RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
CC1352R1F3RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC1352R1F3RGZR	VQFN	RGZ	48	2500	367.0	367.0	35.0
CC1352R1F3RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
CC1352R1F3RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

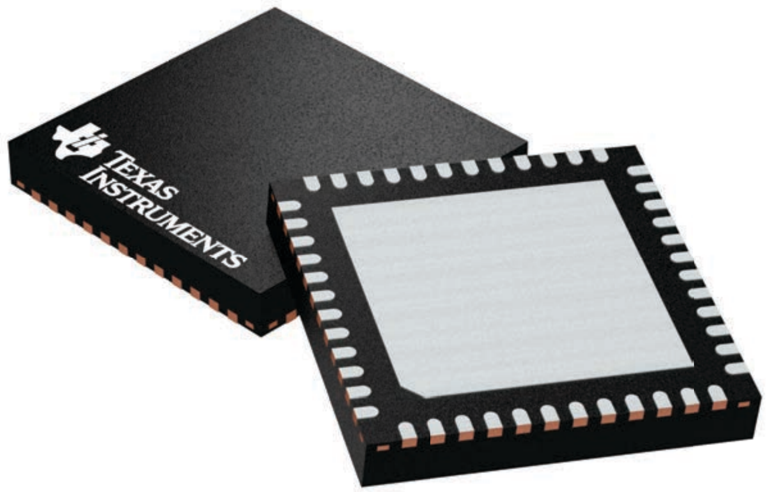
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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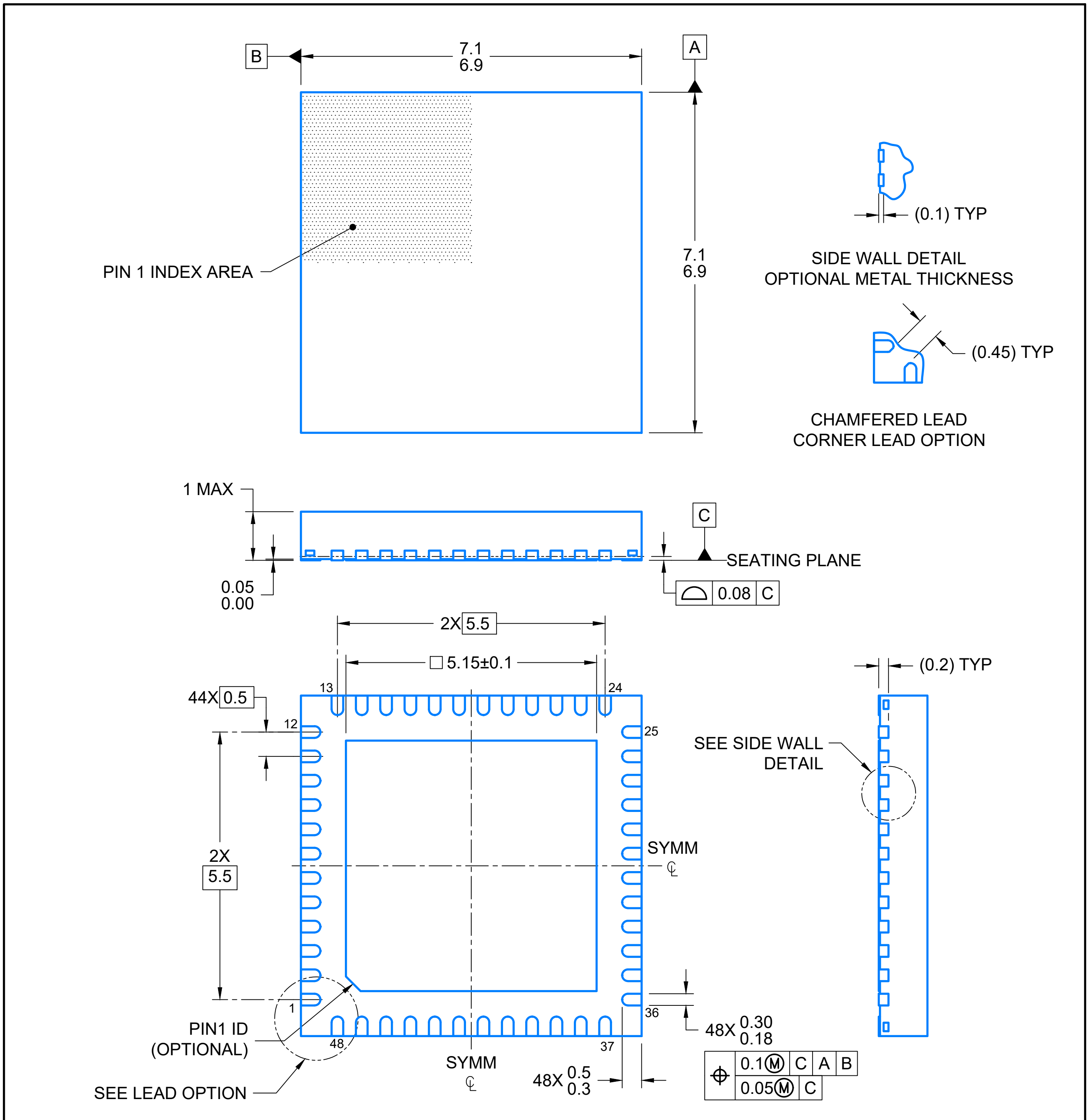
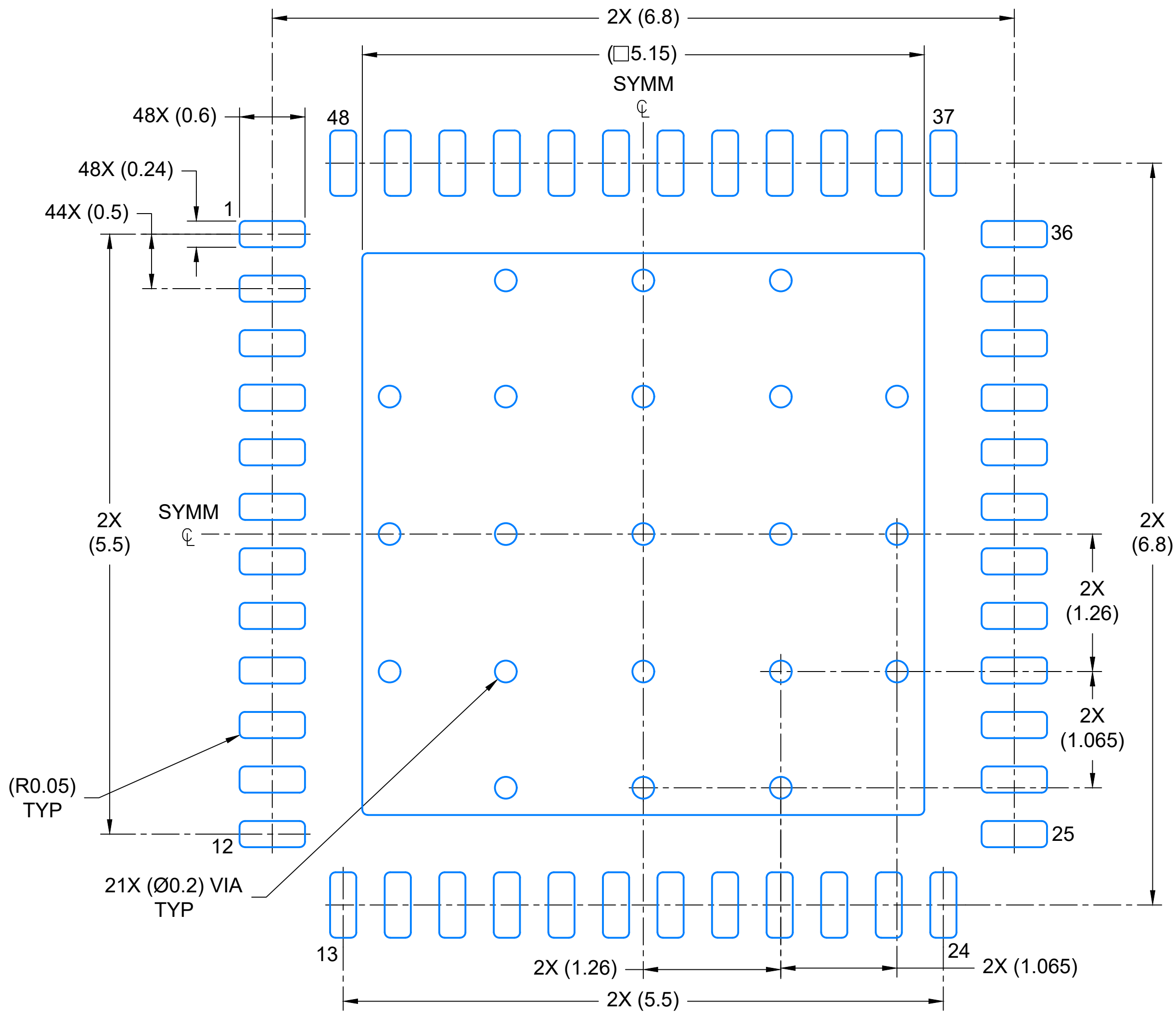
PLASTIC QUADFLAT PACK- NO LEAD



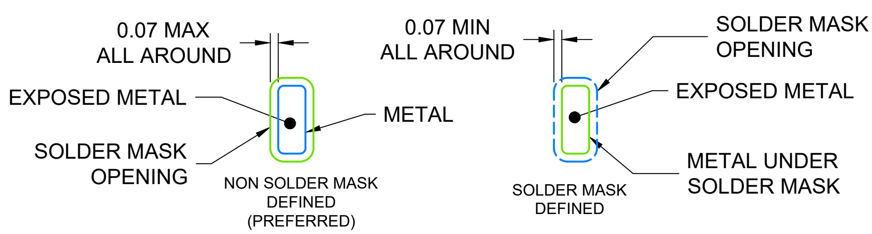
4219044/D 02/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 15X

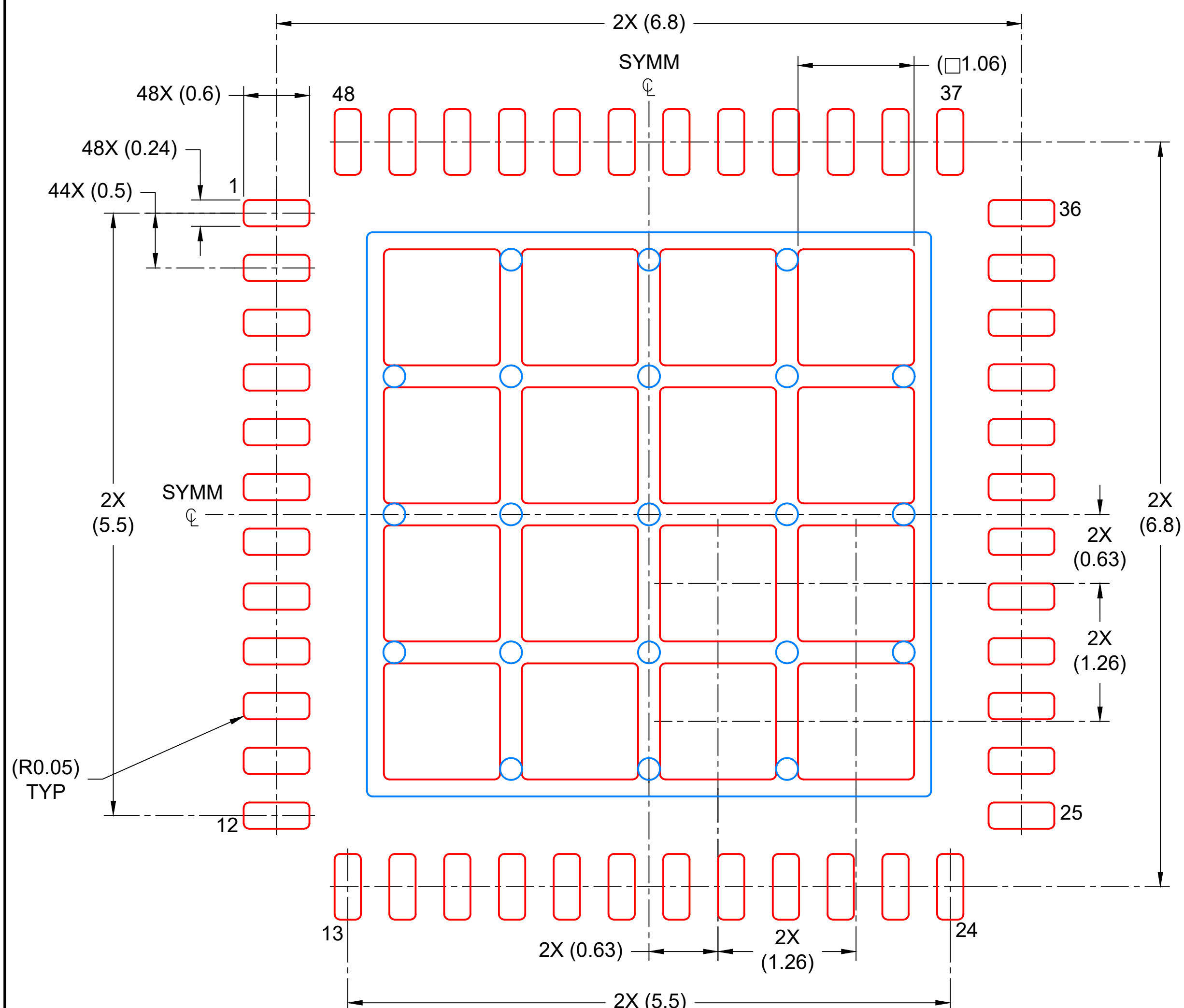


SOLDER MASK DETAILS

4219044/D 02/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
67% PRINTED COVERAGE BY AREA
SCALE: 15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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