TPSM84209 4.5V 至 28V 输入、1.2V 至 6V 输出、2.5A 电源模块

1 特性

- 完整的集成式电源解决方案可实现小尺寸的薄型设计
- 4.5mm × 4mm × 2mm QFN 封装
- 宽输出电压范围（1.2V 至 6V）
- 固定开关频率 (750kHz)
- 高级 Eco-mode™，用于提高轻负载效率
- 可编程欠压锁定 (UVLO)
- 过热热关断保护
- 过流保护（间断模式）
- 安全预偏置输出启动
- 工作 IC 结温范围：-40°C 至 +125°C
- 工作环境温度范围：-40°C 至 +85°C
- 增强的热性能：29.5°C/W
- 符合 EN55011 辐射 EMI 标准
  - 集成屏蔽电感器
- 使用 TPSM84209 并借助 WEBENCH® 电源设计器创建定制设计方案

2 应用

- 工业和电机控制
- 自动测试设备
- 医疗和成像设备
- 高密度电源系统

3 说明

TPSM84209 电源模块是一款易于使用的集成式电源，该模块由一个带屏蔽式电感的 2.5A 直流/直流转换器和无源元件组成，并且采用薄型 QFN 封装。这套整体电源解决方案仅使用了四个外部组件，同时仍能够调整关键参数以满足特定的设计要求。

TPSM84209 具有较宽的输入电压范围和较小的尺寸封装，这使得该器件非常适合用于要求输出电流高达 2.5A 的电源轨。

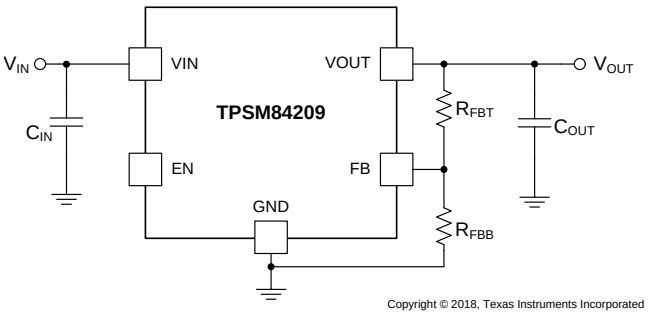
QFN 封装易于焊接到印刷电路板上，并且具有出色的功率耗散能力。TPSM84209 极具灵活性且 功能 丰富，非常适合为各类器件和系统供电。

器件信息(1)

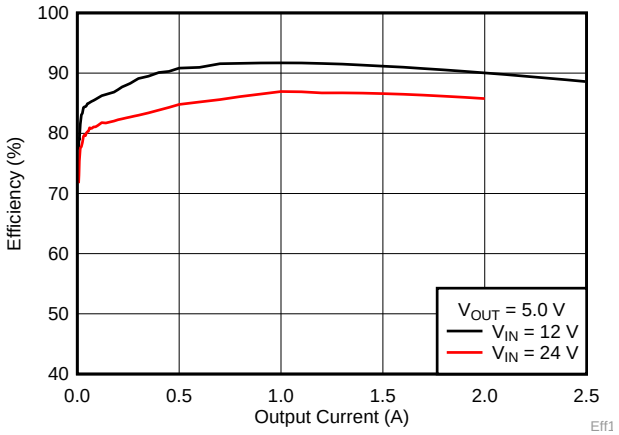
器件型号	封装	封装尺寸
TPSM84209	QFN (9)	4.50mm × 4.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化应用



效率与输出电流间的关系



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (June 2018) to Revision C **Page**

- 已更改 将“”中的“封装”列从“B3QFN (43)”更改为“QFN (9)”以更正错误 ... 1
- Changed "RVQ Package" to "RKH Package", "43-pin B3QFN" to "9-Pin QFN" ... 3

Changes from Revision A (April 2018) to Revision B **Page**

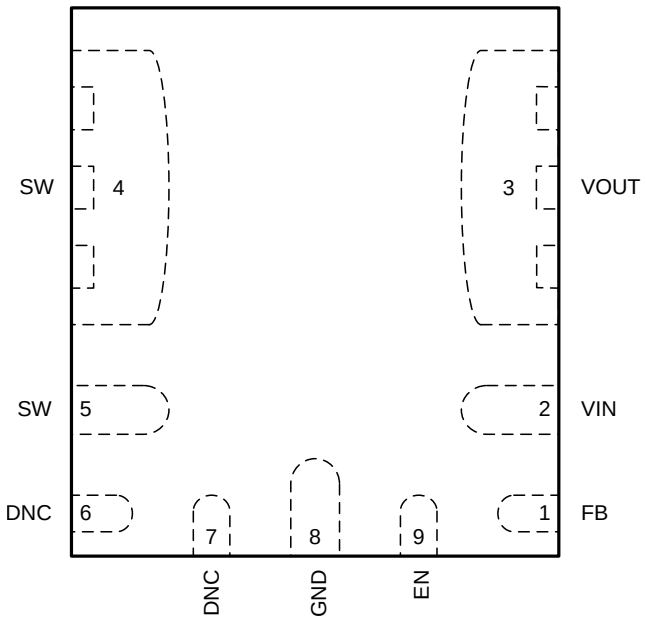
- Changed Min Storage temperature to -55°C ... 4

Changes from Original (January 2018) to Revision A **Page**

- 首次发布生产数据产品说明书 ... 1

5 Pin Configuration and Functions

RKH Package
9-Pin QFN
Top View



Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
DNC	6, 7	—	Do Not Connect. Do not connect these pins to GND or to any other voltage. These pins are connected to internal circuitry. Each pin must be soldered to an isolated pad.
EN	9	I	Enable pin. An open drain/collector device can be used to control the EN function. The module is disabled when this pin is pulled low. This pin can also be connected to an external resistor divider connected between VIN and GND to adjust the UVLO above the internal default setting. Float this pin when not used.
FB	1	I	Feedback input. To adjust the output voltage connect this pin to the center point of an external resistor divider connected between VOUT and GND.
GND	8	G	Ground pin. This is the return current path for the device. Connect this pin to the input source return, the load return, and to the ground side of the VIN and VOUT bypass capacitors using power ground planes on the PCB.
SW	4, 5	O	Switch node. These pins are connected to the input side of the internal output inductor. Do not place any external components on these pins or tie them to a pin of another function.
VIN	2	I	Input voltage. Connect this pin to the input source and connect external bypass capacitors between this pin and GND, close to the module.
VOUT	3	O	Output voltage. This pin is connected to the internal output inductor. Connect this pin to the output load and connect external bypass capacitors between this pin and GND close to the module.

(1) G = Ground, I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

Over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	30	V
	EN, FB	–0.3	7	V
Output voltage	SW	–0.3	30	V
	SW (20 ns transient)	–5	30	V
	VOUT	–0.3	7	V
Mechanical shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted		1500	G
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20 to 2000 Hz		20	G
Operating IC junction temperature, T_J (2)		–40	125	°C
Operating ambient temperature, T_A (2)		–40	85	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under the recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The ambient temperature is the air temperature of the surrounding environment. The junction temperature is the temperature of the internal power IC when the deviceis powered. Operating below the maximum ambient temperature, as shown in the safe operating area (SOA) curves in the typical characteristics sections, ensures that the maximum junction temperature of any component inside the module is never exceeded.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating ambient temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input voltage, V_{IN}	4.5(1)	28(2)	V
Output voltage, V_{OUT}	1.2	6	V
EN voltage, V_{EN}	0	6	V
Output current, I_{OUT}	0	2.5(3)	A
Operating ambient temperature, T_A	–40	85	°C
Operating IC junction temperature, T_J	–40	125	

(1) The minimum recommended input voltage is 4.5 V or (V_{OUT} × 1.3), whichever is greater.
(2) The maximum input voltage varies depending on the output voltage (see *Operating Range*).
(3) The maximum output current that the TPSM84209 can deliver is a function of input voltage, output voltage, and ambient temperature (see *Output Current Rating*).

6.4 Thermal Information

THERMAL METRIC[1]		TPSM84209 RKH (QFN) 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	32.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter[3]	2.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter[4]	17	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance, $R_{\theta JA}$, applies to devices soldered directly to a 63 mm × 50 mm, 4-layer PCB with 2 oz. copper and natural convection cooling. Additional airflow reduces $R_{\theta JA}$.
(3) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). $T_J = \psi_{JT} \times Pdis + T_T$; where Pdis is the power dissipated in the device and T_T is the temperature of the top of the device.
(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} \times Pdis + T_B$; where Pdis is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.

6.5 Electrical Characteristics

Over –40°C to +85°C ambient temperature, V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 2.5 A, (unless otherwise noted); C_{IN1} = 10 µF, 50 V, 1210 ceramic; C_{IN2} = 100-µF, 35-V, electrolytic; C_{OUT} = 2 × 47-µF, 16-V, 1210 ceramic. Minimum and maximum limits are guaranteed through production test or by design. Typical values represent the expected value for the given test conditions and may or may not be production tested.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE (V_{IN})							
V_{IN}	Input voltage	Over I_{OUT} range		4.5[1]		28[2]	V
UVLO	V_{IN} undervoltage lockout	V_{IN} increasing		3.8	4.1	4.4	V
		V_{IN} decreasing		3.3	3.6	3.9	V
I_{SHDN}	Shutdown supply current	V_{EN} = 0 V			2		µA
OUTPUT VOLTAGE (V_{OUT})							
$V_{OUT(ADJ)}$	Output voltage adjust	Over I_{OUT} range		1.2		6	V
$V_{OUT(Ripple)}$	Output voltage ripple	20-MHz bandwidth			22		mV
FEEDBACK							
V_{FB}	Feedback voltage[3]	T_A = 25°C, I_{OUT} = 0.2 A		0.581	0.596	0.611	V
	Temperature variation	–40°C ≤ T_J ≤ 125°C, I_{OUT} = 0.2 A			0.5%		
	Line regulation	T_A = 25°C, 4.5 V ≤ V_{IN} ≤ 28 V, I_{OUT} = 0.2 A			0.2		%
	Load regulation	Over I_{OUT} range, T_A = 25°C			0.5		%
CURRENT							
I_{OUT}	Output current	Natural convection, T_A = 25°C		0		2.5[4]	A
	Overcurrent threshold				4.8		A
PERFORMANCE							
η	Efficiency	V_{IN} = 24 V, I_{OUT} = 1 A	V_{OUT} = 5 V		86.5%		
			V_{OUT} = 3.3 V		82.7%		
			V_{OUT} = 2.5 V		79.3%		
		V_{IN} = 12 V, I_{OUT} = 1 A	V_{OUT} = 5 V		91.7%		
			V_{OUT} = 3.3 V		89.0%		
			V_{OUT} = 2.5 V		86.8%		
	Transient response	25% to 75% load step 1 A/µs slew rate	Over/undershoot		90		mV
			Recovery Time		125		µs

(1) The minimum recommended input voltage is 4.5 V or (V_{OUT} × 1.3), whichever is greater.
(2) The maximum input voltage varies depending on the output voltage (see *Operating Range*).
(3) The overall output voltage tolerance will be affected by the tolerance of the external R_{FBT} and R_{FBB} resistors.
(4) The maximum output current that the TPSM84209 can deliver is a function of input voltage, output voltage, and ambient temperature (see *Output Current Rating*).

Electrical Characteristics (continued)

Over –40°C to +85°C ambient temperature, V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 2.5 A, (unless otherwise noted); C_{IN1} = 10 µF, 50 V, 1210 ceramic; C_{IN2} = 100-µF, 35-V, electrolytic; C_{OUT} = 2 × 47-µF, 16-V, 1210 ceramic. Minimum and maximum limits are guaranteed through production test or by design. Typical values represent the expected value for the given test conditions and may or may not be production tested.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOFT START						
T_{SS}	Internal soft-start time			5		ms
SWITCHING FREQUENCY						
F_{SW}	Switching frequency		578	750	923	kHz
ENABLE (EN)						
$V_{EN-RISING}$	EN threshold	Rising		1.21	1.28	V
$V_{EN-FALLIN}$		Falling	1.1	1.19		V
I_{EN}	EN Input current	V_{EN} = 1 V		0.7		µA
	EN Hysteresis current	V_{EN} = 1.5 V		1.55		µA
THERMAL						
T_{SHDN}	Thermal shutdown	Shutdown temperature		165		°C
		Hysteresis		10		°C
CAPACITANCE						
C_{IN}	External input capacitance	Ceramic type	10 (5)			µF
		Non-ceramic type		47 (5)		µF
C_{OUT}	External output capacitance	Ceramic type	min (6)		500 (7)	µF
		Non-ceramic type			500 (7)	µF

(5) A minimum of 10 µF ceramic input capacitance is required for proper operation. An additional 47 µF of bulk capacitance is recommended for applications with transient load requirements.
(6) The minimum amount of required output capacitance varies depending on the output voltage (see *Output Capacitor Selection*). A minimum amount of ceramic capacitance is required. Locate the capacitance close to the device. Adding additional ceramic or non-ceramic capacitance close to the load improves the response of the regulator to load transients.
(7) The maximum output capacitance of 500 µF can be made up of all ceramic type or a combination of both ceramic and non-ceramic type.

6.6 Typical Characteristics (V_{IN} = 5 V)

T_A = 25°C, unless otherwise noted.

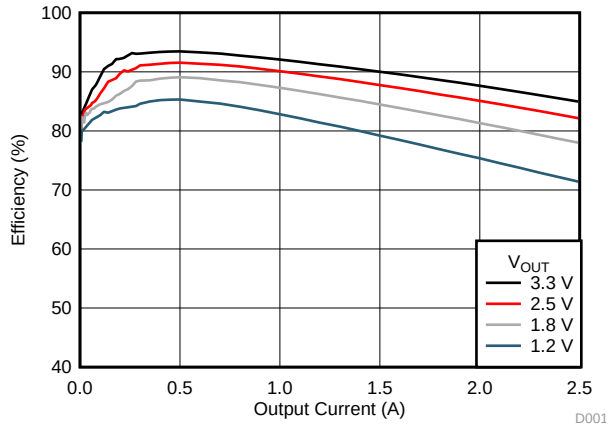


图 1. Efficiency vs Output Current

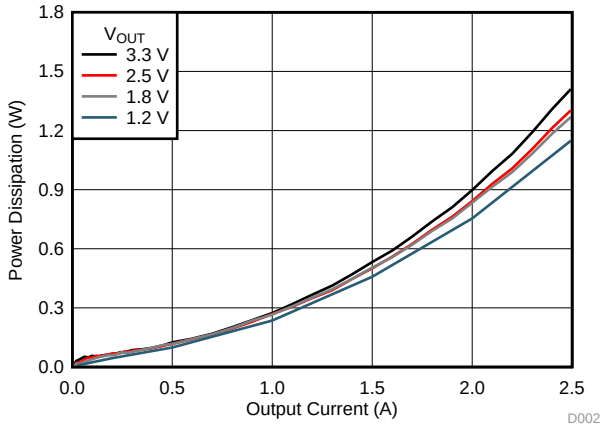
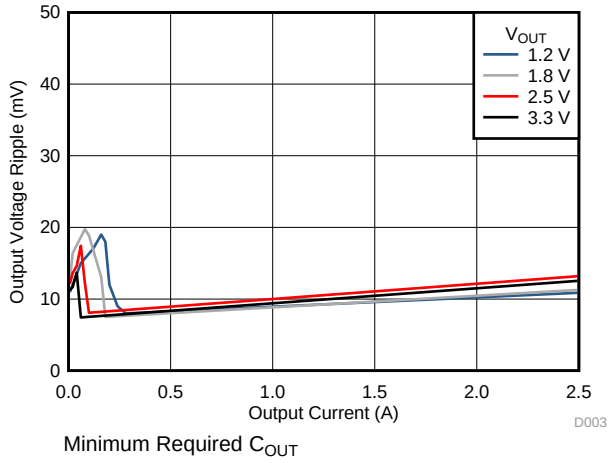
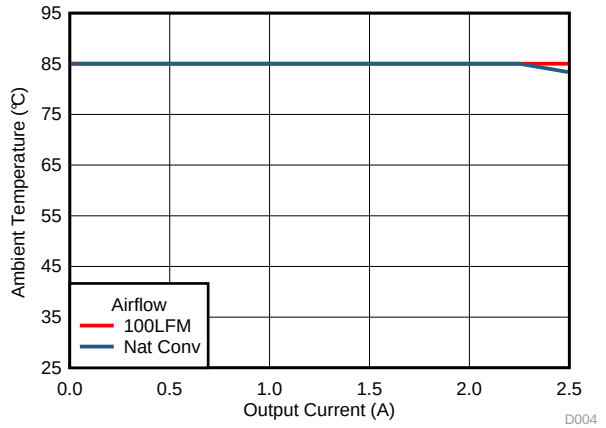


图 2. Power Dissipation vs Output Current



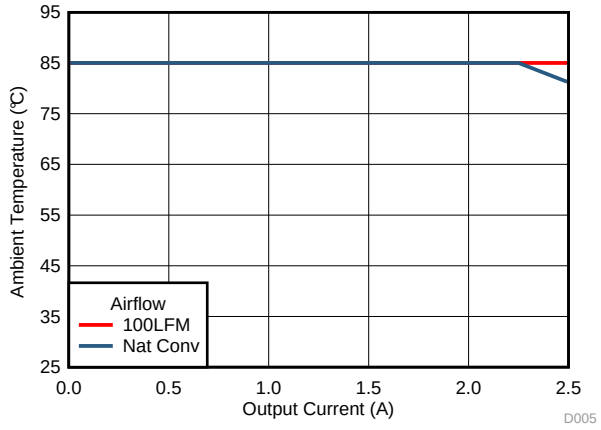
Minimum Required C_{OUT}

图 3. Voltage Ripple vs Output Current



V_{OUT} = 2.5 V

图 4. Safe Operating Area



V_{OUT} = 3.3 V

图 5. Safe Operating Area

6.7 Typical Characteristics (V_{IN} = 12 V)

T_A = 25°C, unless otherwise noted.

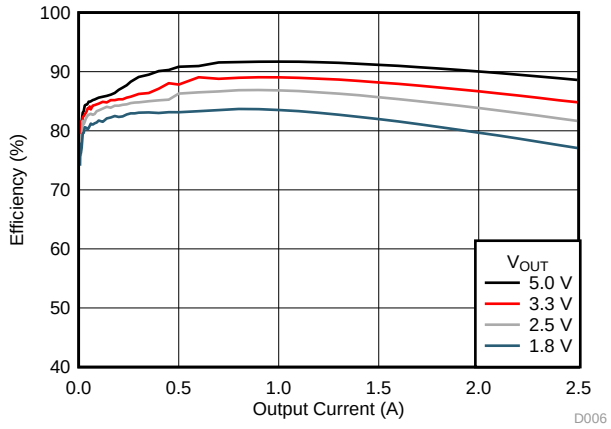


图 6. Efficiency vs Output Current

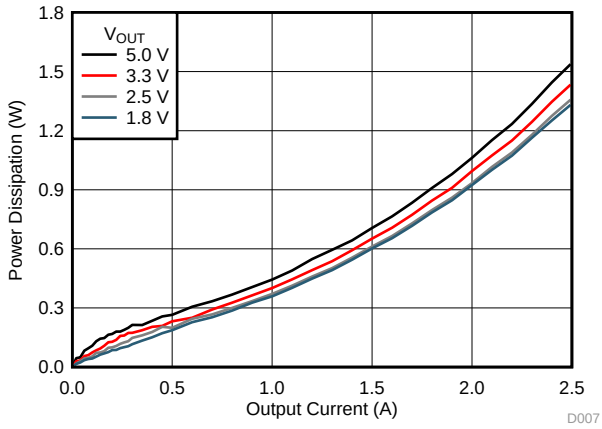


图 7. Power Dissipation vs Output Current

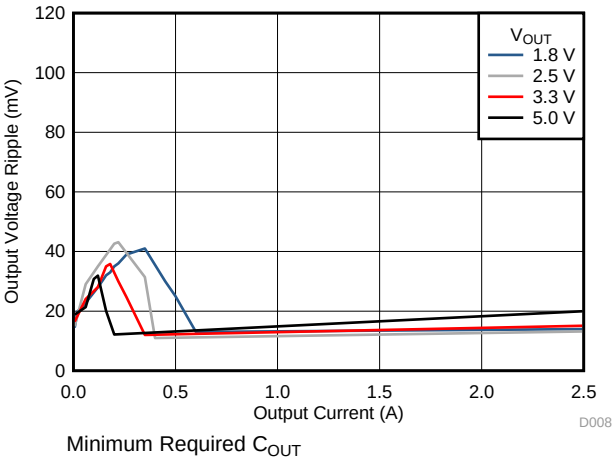


图 8. Voltage Ripple vs Output Current

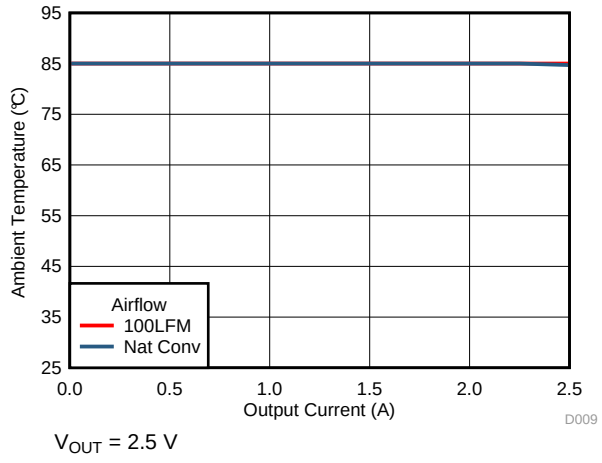


图 9. Safe Operating Area

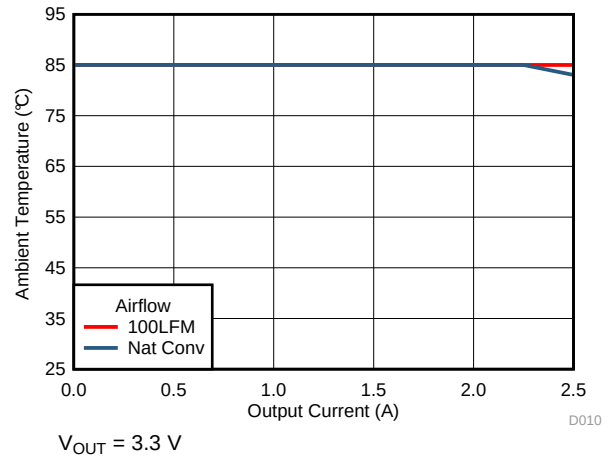


图 10. Safe Operating Area

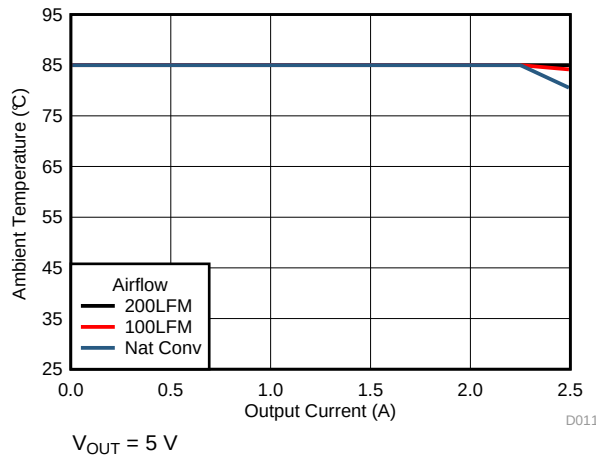


图 11. Safe Operating Area

6.8 Typical Characteristics (V_{IN} = 24 V)

T_A = 25°C, unless otherwise noted.

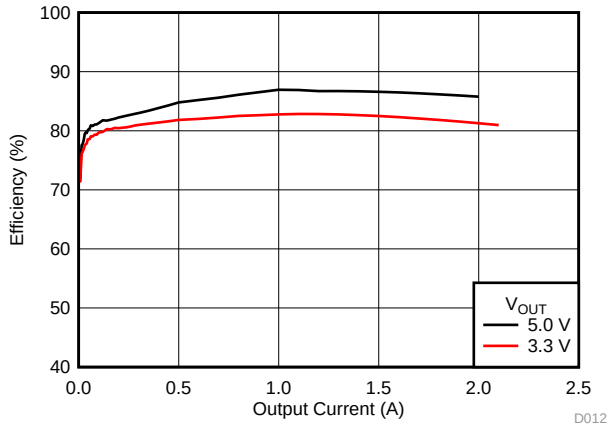


图 12. Efficiency vs Output Current

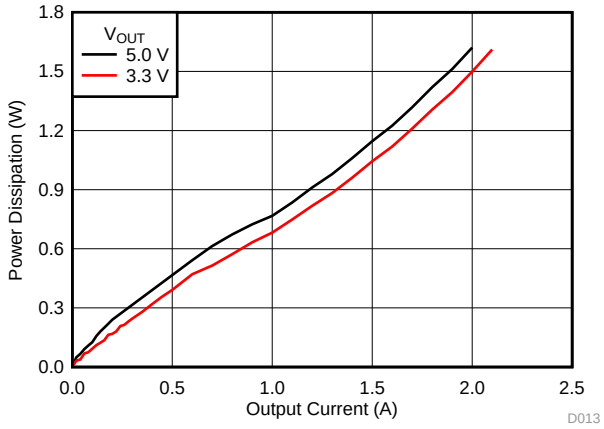
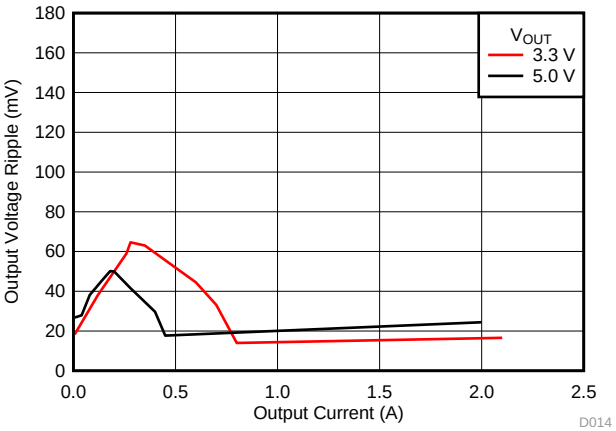
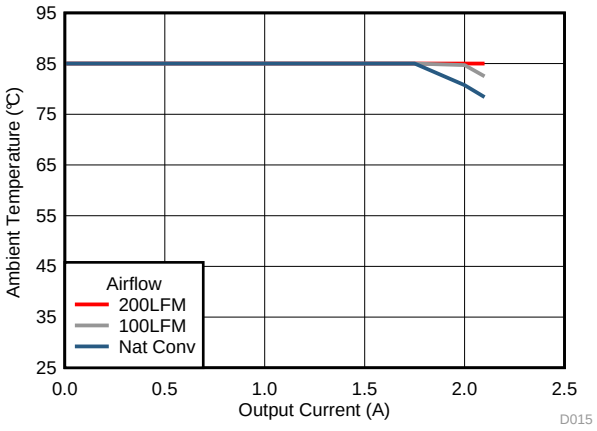


图 13. Power Dissipation vs Output Current



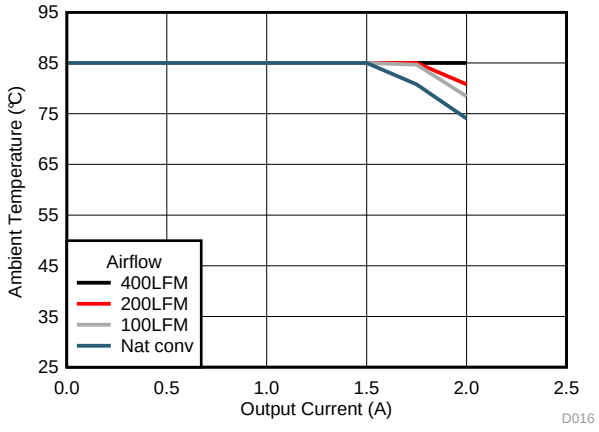
C_{OUT} = 2× 47 µF ceramic

图 14. Voltage Ripple vs Output Current



V_{OUT} = 3.3 V

图 15. Safe Operating Area



V_{OUT} = 5 V

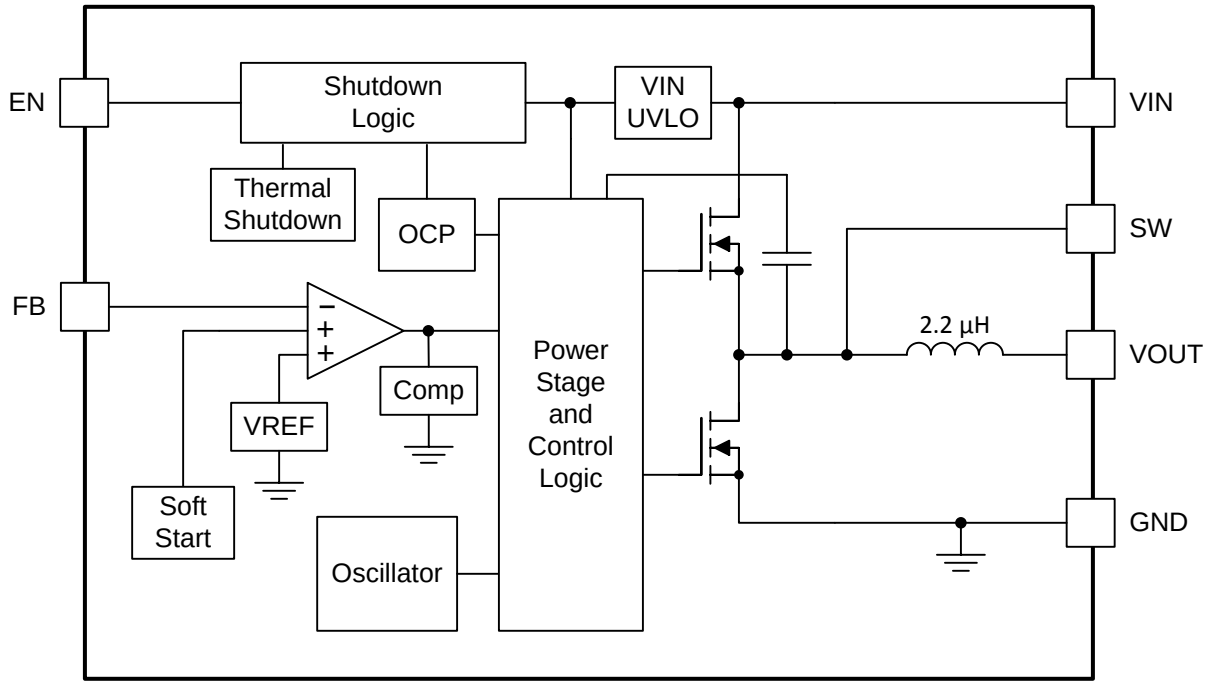
图 16. Safe Operating Area

7 Detailed Description

7.1 Overview

The TPSM84209 is a highly integrated 28-V input, 2.5-A, synchronous step-down power module with PWM, MOSFETs, inductor, and control circuitry integrated into a low-profile, overmolded, QFN package. This device enables small designs by integrating all but the input and output capacitors and voltage-setting resistor divider while keeping the ability to adjust key parameters to meet specific design requirements. The TPSM84209 operates at a 750-kHz fixed switching frequency and features advanced Eco-mode™ pulse-skip operation for improved light-load efficiency. The TPSM84209 provides an adjustable output-voltage range of 1.2 V to 6 V using a simple external-resistor divider. The TPSM84209 provides accurate voltage regulation for a variety of loads by using an internal voltage reference that is 2.5% accurate over temperature. The output-voltage rise time is controlled by a fixed 5-ms soft start. Input UVLO is internally set at 4.1 V, but can be adjusted upward using a resistor divider on the EN pin of the module. The EN pin can also be pulled low to put the module in standby mode to reduce input quiescent current. Thermal shutdown and current limit features protect the device during an overload condition. A 9-pin, 4-mm × 4.5-mm B3QFN package that includes exposed bottom pads provides a thermally enhanced solution for space-constrained applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adjusting the Output Voltage

A resistor divider connected to the FB pin (pin 1) programs the output voltage of the TPSM84209. The output voltage adjustment range is from 1.2 V to 6 V. 图 17 shows the feedback resistor connection for setting the output voltage. The recommended value of R_{FBT} is 10 kΩ. 表 1 lists the closest standard E96 value for the R_{FBB} resistor for a number of common output voltages. For other output voltages, the value of the required R_{FFB} resistor can be calculated using 公式 1.

$$R_{FBB} = \frac{6}{(V_{OUT} - 0.6)} \quad (k\Omega) \tag{1}$$

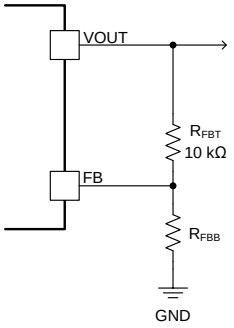


图 17. Setting the Output Voltage

表 1. Standard R_{FBB} Resistor Values

V_{OUT} (V)	R_{FBB} (kΩ)	V_{OUT} (V)	R_{FBB} (kΩ)
1.2	10.0	3.7	1.96
1.3	8.45	3.8	1.87
1.4	7.50	3.9	1.82
1.5	6.65	4.0	1.74
1.6	6.04	4.1	1.69
1.7	5.36	4.2	1.65
1.8	4.99	4.3	1.62
1.9	4.64	4.4	1.58
2.0	4.22	4.5	1.54
2.1	4.02	4.6	1.50
2.2	3.74	4.7	1.47
2.3	3.48	4.8	1.43
2.4	3.32	4.9	1.40
2.5	3.16	5.0	1.37
2.6	3.01	5.1	1.33
2.7	2.87	5.2	1.30
2.8	2.74	5.3	1.27
2.9	2.61	5.4	1.24
3.0	2.49	5.5	1.22
3.1	2.37	5.6	1.20
3.2	2.32	5.7	1.18
3.3	2.21	5.8	1.15
3.4	2.15	5.9	1.13
3.5	2.05	6.0	1.10
3.6	2.00		

7.3.2 Input Capacitor Selection

The TPSM84209 requires a ceramic input capacitor with a minimum effective capacitance of 10 µF. Use only high-quality ceramic type X5R or X7R capacitors with sufficient voltage rating. An additional 47 µF of non-ceramic capacitance is recommended for applications with transient load requirements. The voltage rating of input capacitors must be greater than the maximum input voltage. To compensate for the derating of ceramic capacitors, TI recommends a voltage rating of twice the maximum input voltage. At worst case, when operating at 50% duty cycle and maximum load, the combined ripple current rating of the input capacitors must be at least 1.25 Arms. 表 2 includes a preferred list of capacitors by vendor.

表 2. Recommended Input Capacitors(1)

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE (2) (µF)	ESR (3) (mΩ)
TDK	X5R	C3225X5R1H106K	50	10	3
Murata	X7R	GRM32ER71H106K	50	10	2
Murata	X7R	GRM32ER71J106K	63	10	2
Panasonic	ZA	EEHZA1H101P	50	100	28
Panasonic	ZA	EEHZA1J560P	63	56	30

(1) **Capacitor Supplier Verification, RoHS, Lead-free and Material Details**
Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Specified capacitance values
(3) Maximum ESR at 100 kHz, 25°C.

7.3.3 Undervoltage Lockout (UVLO)

The TPSM84209 device has an internal UVLO circuit which prevents the device from operating until the V_{IN} voltage exceeds the UVLO rising threshold, (4.1 V (typical)). The device is disabled when the VIN pin voltage falls below the internal V_{IN} UVLO threshold. The internal V_{IN} UVLO threshold has a hysteresis of 500 mV.

Applications may require a higher UVLO threshold to prevent early turnon, for sequencing requirements or to prevent input current draw at lower input voltages. An external resistor divider can be added to the EN pin to adjust the UVLO threshold higher. The external resistor divider can be configured as shown in 图 18. 表 3 lists standard values for R_{UVLO1} and R_{UVLO2} to adjust the UVLO voltage higher.

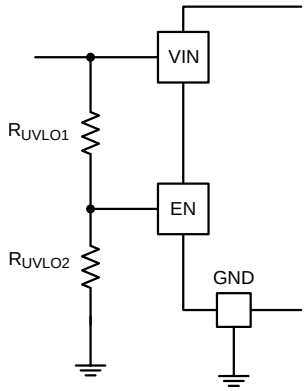


图 18. Adjustable UVLO

表 3. Standard Resistor Values for Adjusting UVLO

V_{IN} UVLO (V)	4.5	10	15	18	20
R_{UVLO1} (kΩ)	68.1	68.1	68.1	68.1	68.1
R_{UVLO2} (kΩ)	25.5	9.53	6.04	4.99	4.42

7.3.4 Output Capacitor Selection

The minimum amount of required output capacitance for the TPSM84209 varies depending on the output voltage and whether or not a feed-forward capacitor, C_{FF}, is used (see Feed-Forward Capacitor for more information on C_{FF}). 表 4 lists the minimum output capacitance for several output voltage ranges when not using C_{FF}. The required output capacitance must be comprised of all ceramic capacitors or a combination of ceramic and polymer-type capacitors. The effects of temperature and capacitor voltage rating must be considered when selecting capacitors to meet the minimum required capacitance.

When adding additional output capacitance, ceramic capacitors or a combination of ceramic and polymer-type capacitors can be used. The required capacitance above the minimum is determined by actual transient deviation requirements. See 表 5 for a preferred list of output capacitors by vendor.

表 4. Minimum Required Output Capacitance

V_{OUT} RANGE (V)		Minimum Required C_{OUT}
MIN	MAX	
1.2	< 1.5	188 µF (4 x 47 µF ceramic)(1)
1.5	< 2.5	141 µF (3 x 47 µF ceramic)(1)
2.5	< 5	94 µF (2 x 47 µF ceramic)
5	6	47 µF (1 x 47 µF ceramic)

(1) The minimum required output capacitance can also be made up of 1 x 47 µF ceramic + 1 x 100 µF polymer-type capacitor.

表 5. Recommended Output Capacitors(1)

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE(2) (µF)	ESR(3) (mΩ)
TDK	X5R	C3225X5R1C106K	16	10	2
Murata	X5R	GRM32ER61C106K	16	10	2
TDK	X5R	C3225X5R1C226M	16	22	2
Murata	X5R	GRM32ER61C226K	16	22	2
TDK	X5R	C3225X5R1A476M	10	47	2
Murata	X5R	GRM32ER61C476K	16	47	3
TDK	X5R	C3225X5R0J107M	6.3	100	2
Murata	X5R	GRM32ER60J107M	6.3	100	2
Murata	X5R	GRM32ER61A107M	10	100	2
Kemet	X5R	C1210C107M4PAC7800	16	100	2
Panasonic	POSCAP	6TPE100MI	6.3	100	18
Panasonic	POSCAP	6TPF220M9L	6.3	220	9
Panasonic	POSCAP	6TPE220ML	6.3	220	12

(1) **Capacitor Supplier Verification, RoHS, Lead-free and Material Details**
Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Specified capacitance values.
(3) Maximum ESR at 100 kHz, 25°C.

7.3.5 Feed-Forward Capacitor

The TPSM84209 is internally compensated to be stable over the operating range of the device. However, depending on the output voltage and amount of output capacitance, an additional feed-forward capacitor, C_{FF}, may be added for optimum performance. Adding additional output capacitance above the minimum reduces the output voltage ripple of the device. However, adding additional output capacitance also reduces the cross-over frequency of the device, slowing the response to load transients. Adding a feed-forward capacitor when adding more output capacitance helps to restore cross-over frequency of the device, restoring the transient response.

The external feed-forward capacitor must be placed in parallel with the top resistor divider, R_{FBT}. The placement of C_{FF} is shown in 图 19. 表 6 lists the required C_{FF} values for different amounts of output capacitance. For output voltages < 2.5 V, it is not recommended to add a C_{FF} capacitor.

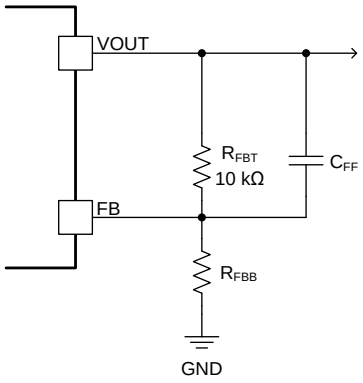


图 19. Feed-Forward Capacitor

表 6. C_{FF} Values(1)

V_{OUT} RANGE (V)		Amount of C_{OUT}			
MIN	MAX	47 µF (1 x 47 µF)	94 µF (2 x 47 µF)	141 µF (3 x 47 µF)	≥ 188 µF (4 x 47 µF)
2.5	< 3.3	Not applicable	C_{FF} = 100 pF	C_{FF} = 220 pF	C_{FF} = 330 pF
3.3	< 5	Not applicable	C_{FF} = 100 pF	C_{FF} = 330 pF	C_{FF} = 330 pF
5	6	C_{FF} = 100 pF	C_{FF} = 330 pF	C_{FF} = 330 pF	C_{FF} = 330 pF

(1) The C_{FF} values listed in this table apply when R_{FBT} = 10 kΩ. To calculate the value of C_{FF} when using another R_{FBT} value, multiply the C_{FF} value listed in the table by 10 kΩ / R_{FBT}.

7.3.6 Operating Range

The TPSM84209 operates over a wide input voltage and output voltage range; however, not all output voltages can operate over the entire input voltage range. The maximum and minimum input voltage limits are shown in 图 20. The TPSM84209 can be operated between the Maximum and Minimum V_{IN} limit lines.

Operating above the Maximum V_{IN} line may cause the device to skip pulses in order to maintain the regulated output voltage.

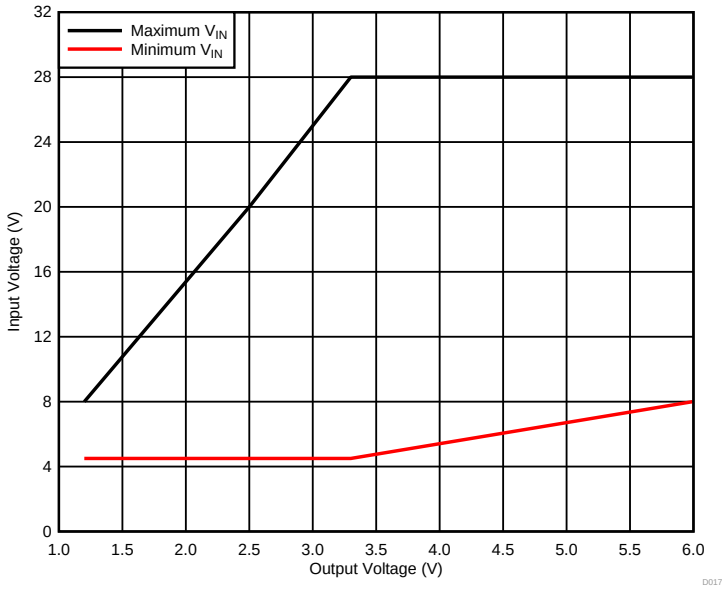


图 20. Input Voltage vs Output Voltage

7.3.7 Output Current Rating

The maximum output current that the TPSM84209 can deliver is a function of input voltage, output voltage, and ambient temperature. The TPSM84209 is capable of delivering up to 2.5 A of output current; however refer to 图 21 and 图 22 for maximum current ratings based on operating conditions of the specific application.

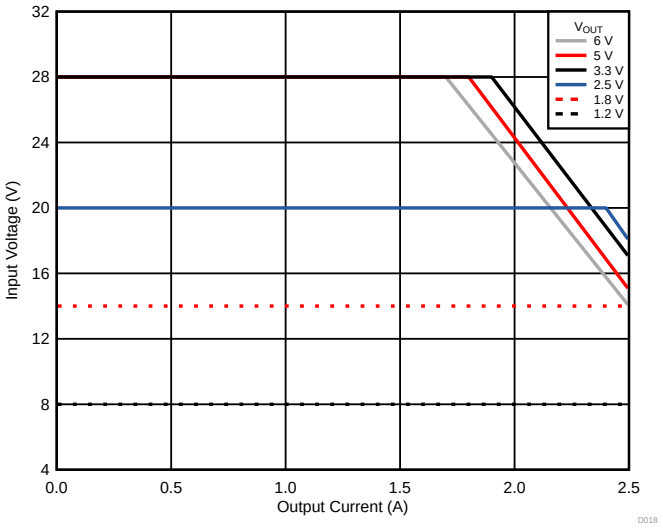


图 21. Output Current Derating T_A = 25°C

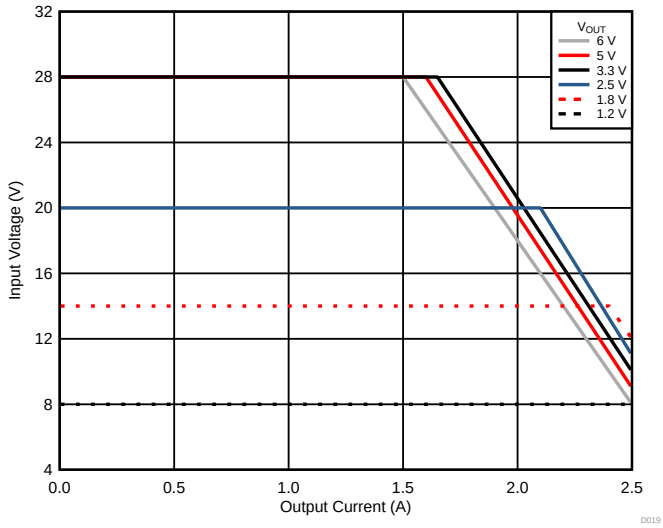


图 22. Output Current Derating T_A = 85°C

7.3.8 Enable (EN)

The EN pin provides electrical ON and OFF control of the device. When the EN pin voltage exceeds the threshold voltage, the device begins operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters the low-quiescent current state.

The EN pin has an internal pullup-current source, which allows the user to float the EN pin to enable the device. If an application requires control of the EN pin, use open-drain or open-collector output logic to interface with the pin.

图 23 shows the typical application of the enable function. Turning Q1 on applies a low voltage to the enable control pin and disables the output of the supply, shown in 图 24. If Q1 is turned off, the supply executes a soft-start power-up sequence, as shown in 图 25.

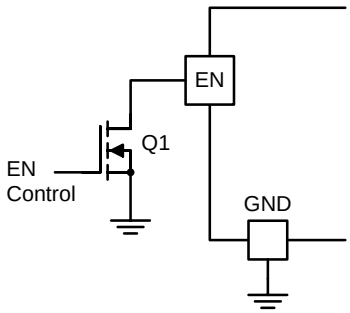


图 23. Typical Enable Control

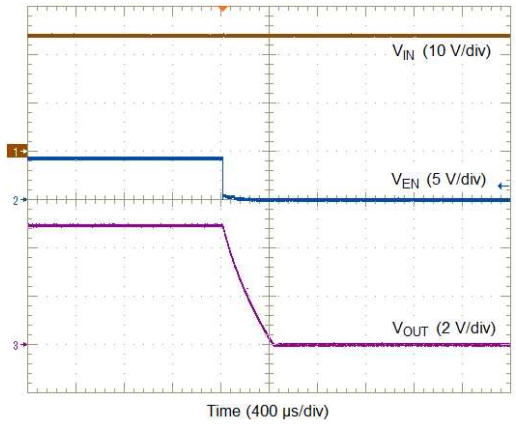


图 24. Enable Turnoff

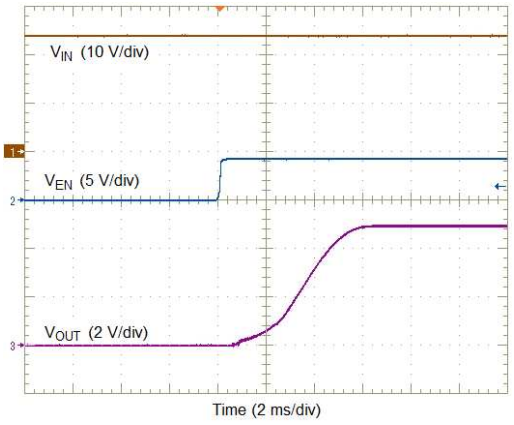


图 25. Enable Turnon

7.3.9 Internal Soft Start

The TPSM84209 device uses the internal soft-start function. The internal soft-start time is set to 5 ms typically.

7.3.10 Safe Start-Up Into Prebiased Outputs

The device has been designed to prevent the low-side MOSFET from discharging a prebiased output. During monotonic prebiased start-up, both high-side and low-side MOSFETs are not allowed to be turned on until the internal soft-start voltage is higher than FB pin voltage.

7.3.11 Light Load Efficiency / Eco-Mode

The TPSM84209 device is designed to operate in high-efficiency, pulse-skipping mode under light load conditions. As the load current on the output is decreased, a point is reached where the energy delivered by a single switching pulse is more than the load can absorb. This causes the output voltage to rise slightly. This rise in output voltage is sensed by the feedback loop, and the device responds by skipping one or more switching cycles until the output voltages falls back to the setpoint. At very light loads or no load, many switching cycles are skipped. The observed effect during this pulse-skipping mode of operation is an increase in the peak-to-peak ripple voltage and a decrease in the ripple frequency. The load current where pulse skipping begins is a function of the input voltage and output voltage. 图 26 is a plot of the pulse-skipping threshold current as a function of input voltage for a number of popular output voltages.

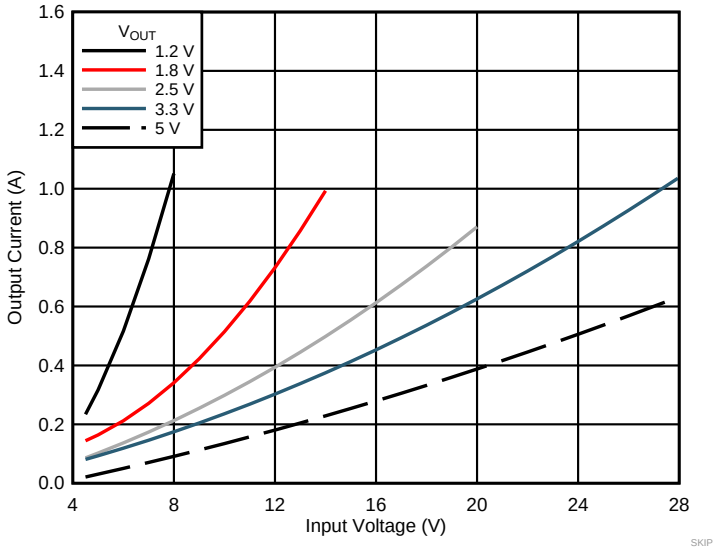


图 26. Pulse-Skipping Threshold

7.3.12 Voltage Dropout

Voltage dropout is the difference between the input voltage and output voltage that is required to maintain output voltage regulation while providing the rated output current.

To ensure the TPSM84209 maintains output voltage regulation over the recommended operating range, the minimum recommended input voltage is 4.5 V or (V_{OUT} × 1.3), whichever is greater. However, the TPSM84209 does produce an output voltage when operated below the recommended input voltage range. 图 27 shows the typical dropout voltage curves for 5-V output at T_A = 25°C. (Note: As ambient temperature increases, dropout voltage and frequency foldback occur at higher input voltage.)

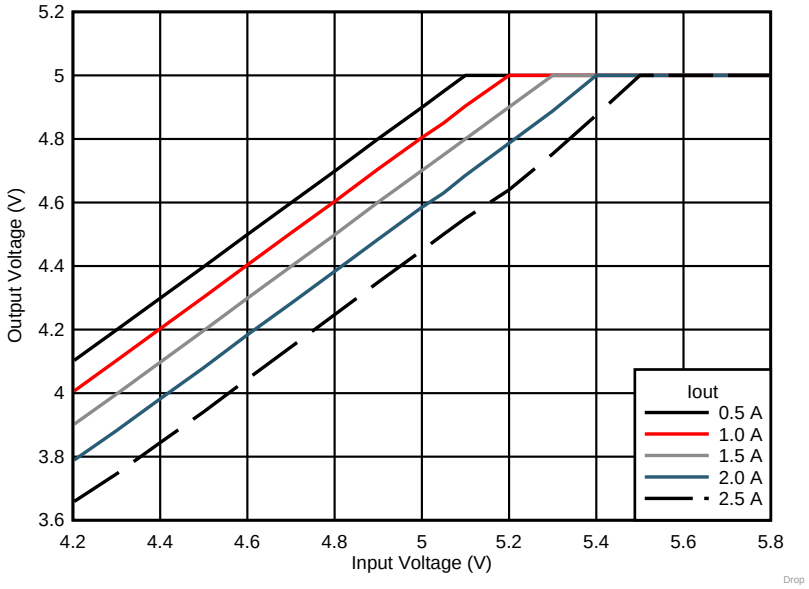


图 27. Voltage Dropout

7.3.13 Overcurrent Protection

For protection against load faults, the TPSM84209 incorporates output overcurrent protection. Applying a load that exceeds the overcurrent threshold of the regulator causes the output to shut down. Following shutdown, the module periodically attempts to recover by initiating a soft-start power-up as shown in 图 28. This is described as a hiccup mode of operation, where the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced which reduces power dissipation. Once the fault is removed, the module automatically recovers and returns to normal operation as shown in 图 29.

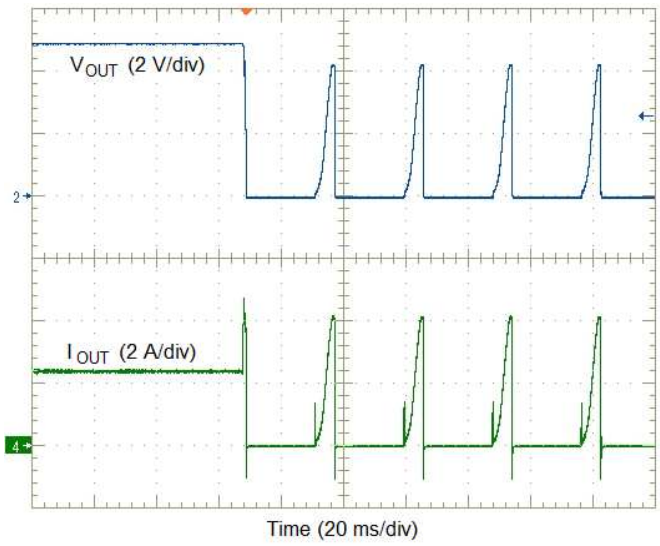


图 28. Overcurrent Limiting

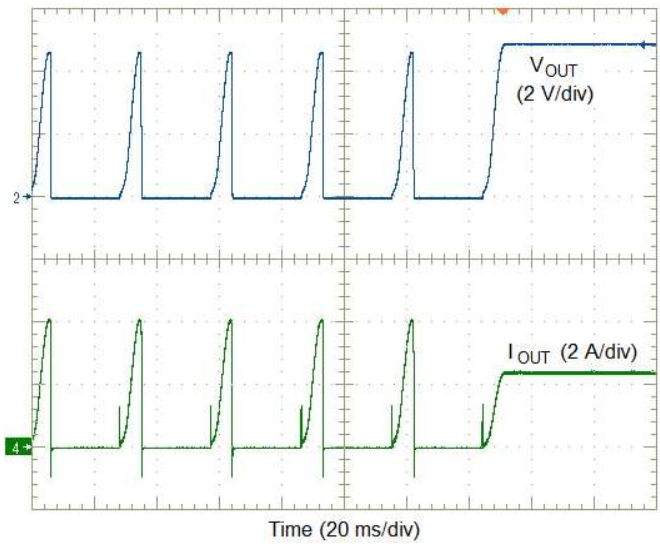


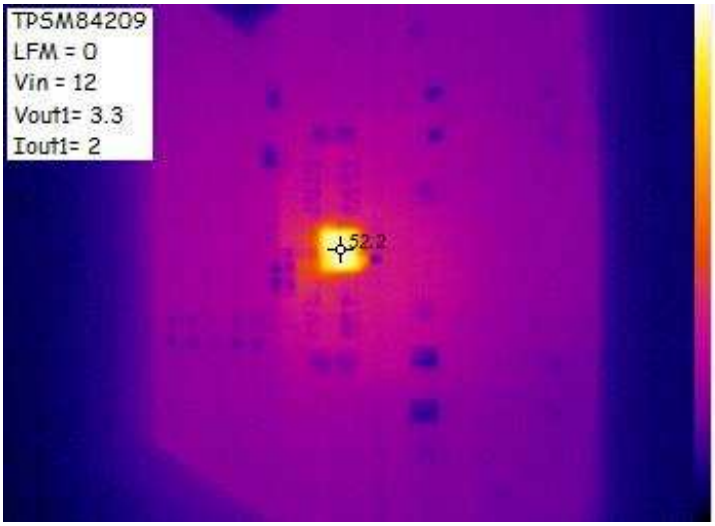
图 29. Removal of Overcurrent

7.3.14 Output Overvoltage Protection (OVP)

The TPSM84209 incorporates an overvoltage transient protection (OVTP) circuit to minimize output voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP circuit includes an overvoltage comparator to compare the FB pin voltage and internal thresholds. When the FB pin voltage goes above 108% × Vref, the high-side MOSFET is forced off. When the FB pin voltage falls below 104% × Vref, the high-side MOSFET is enabled again.

7.3.15 Thermal Performance

The typical thermal performance of the TPSM84209 is shown in 图 30. The thermal image shows the typical temperature rise of TPSM84209 is 27.2°C above ambient when operated at V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 2 A, with no airflow (LFM = 0).



T_A = 25°C

图 30. Thermal Image

7.3.16 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 165°C (typ). The device reinitiates the power-up sequence when the junction temperature drops below 155°C (typ).

7.4 Device Functional Modes

7.4.1 Active Mode

When V_{IN} is above the UVLO threshold and the EN pin voltage is above the EN high threshold, the TPSM84209 operates in the active mode. Normal continuous conduction mode (CCM) occurs when inductor peak current is above 0 A. In CCM, the TPSM84209 operates at a fixed frequency.

7.4.2 Eco-Mode Operation

The TPSM84209 device is designed to operate in high-efficiency, pulse-skipping mode under light load conditions. Pulse skipping initiates when the high-side FET current is less than 500 mA typically. During pulse skipping, the low-side FET turns off when the switch current falls to 0 A. The switching node (SW pin) waveform takes on the characteristics of discontinuous conduction mode (DCM) operation and the apparent switching frequency decreases. As the output current decreases, the perceived time between switching pulses increases.

7.4.3 Shutdown Mode

The EN pin provides electrical ON and OFF control for the TPSM84209. When the EN pin voltage is below the EN threshold, the device is in shutdown mode. In shutdown mode the standby current is 2 μA, typically. The TPSM84209 also employs UVLO protection. If V_{IN} is below the UVLO level, the output of the regulator turns off.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPSM84209 is a synchronous, step-down DC/DC power module. It is used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 2.5 A. The following design procedure can be used to select components for the TPSM84209. Alternately, the WEBENCH® software may be used to generate complete designs. When generating a design, the WEBENCH software utilizes an iterative design procedure and accesses comprehensive databases of components. See www.ti.com/webench for more details.

8.2 Typical Application

The TPSM84209 requires only a few external components to convert from a wide input-voltage-supply range to a wide range of output voltages. 图 31 shows a basic TPSM84209 schematic with only the minimum required components.

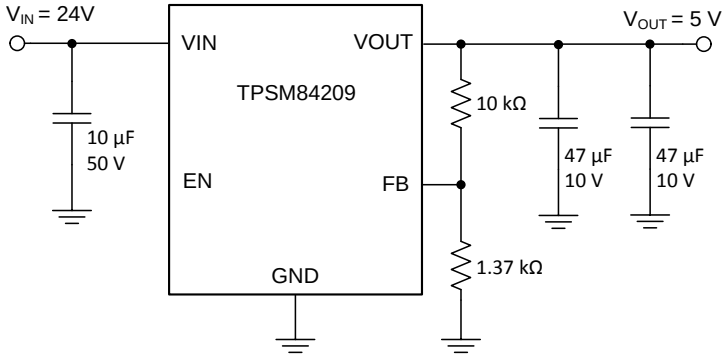


图 31. TPSM84209 Typical Application

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 7 and the following design procedures.

表 7. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage V_{IN}	24 V typical
Output voltage V_{OUT}	5 V
Output current rating	2 A

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM84209 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Setpoint

The output voltage of the TPSM84209 device is externally adjustable using a resistor divider (R_{FBT} and R_{FBB}) between VOUT, FB, and GND. With a fixed value of 10 kΩ for R_{FBT}, select the value of R_{FBB} from 表 1 or calculate using 公式 2:

$$R_{FBB} = \frac{6}{(V_{OUT} - 0.6)} \quad (k\Omega) \tag{2}$$

For a output voltage of 5 V, the formula yields a value of 1.36 kΩ. Choose the closest available value of 1.37 kΩ for R_{FBB}.

8.2.2.3 Input Capacitors

For this design, a 10-µF, X7R dielectric ceramic capacitor rated for 50 V is used for the input decoupling capacitor.

8.2.2.4 Output Capacitors

The minimum required output capacitance for a 5-V output is two 47-µF ceramic capacitors. For this design, two 47-µF, X5R dielectric ceramic capacitors rated for 16 V is used for the output capacitance.

8.2.2.5 Enable Control

The EN pin provides electrical ON/OFF control of the device. If an application requires control of the EN pin, use open-drain or open-collector output logic to interface with the pin. For this design, a small-signal, low-leakage MOSFET (BSS138) was used.

8.2.3 Application Waveforms

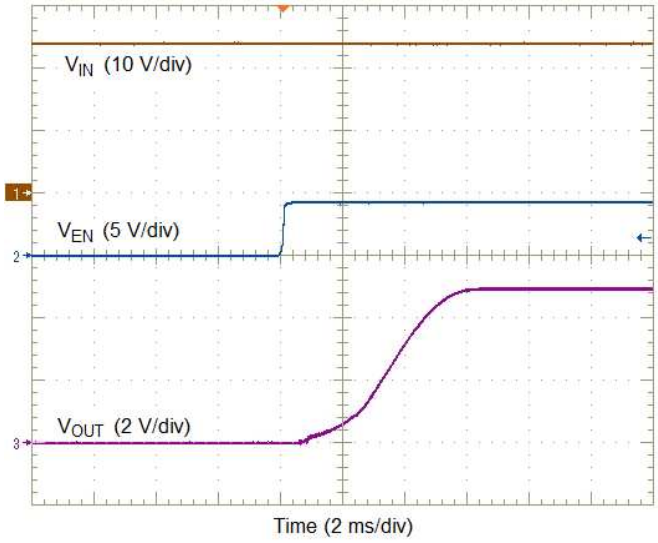
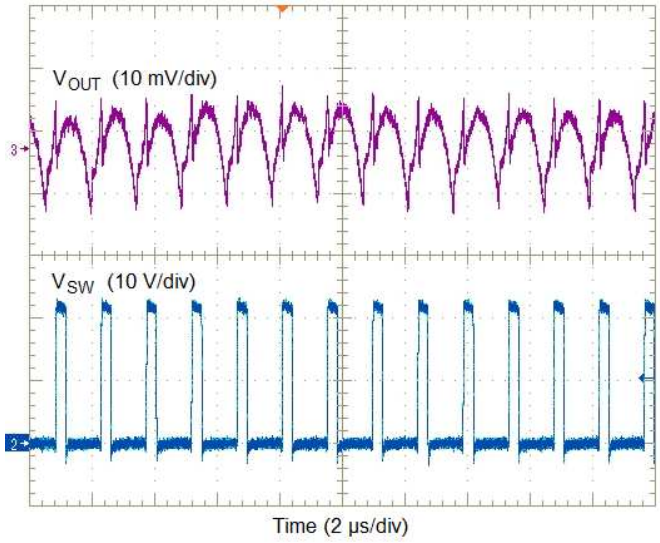


图 32. Start-Up Waveforms



V_{IN} = 24 V V_{OUT} = 5 V I_{OUT} = 2 A

图 33. Output Ripple and PH Node Waveforms

9 Power Supply Recommendations

The TPSM84209 is designed to operate from an input-voltage-supply range between 4.5 V and 28 V. This input supply must be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the TPSM84209 supply voltage that can cause a false UVLO fault triggering and system reset.

If the input supply is located more than a few inches from the TPSM84209 additional bulk capacitance may be required in addition to the ceramic bypass capacitors. Typically, a 47-µF or 100-µF electrolytic capacitor is sufficient.

10 Layout

The performance of any switching power supply depends as much upon the layout of the PCB as the component selection. See the following guidelines to design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

10.1 Layout Guidelines

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. 图 34 and 图 35, shows a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (VIN, VOUT, and GND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Place the output voltage feedback resistors, R_{FBT} and R_{FBB}, as close as possible to their respective pins.
- Use multiple vias to connect the power planes to internal layers.

10.2 Layout Examples

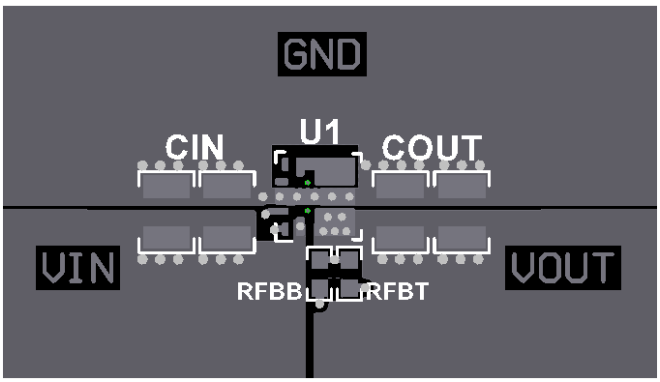


图 34. Typical Top-Layer Layout

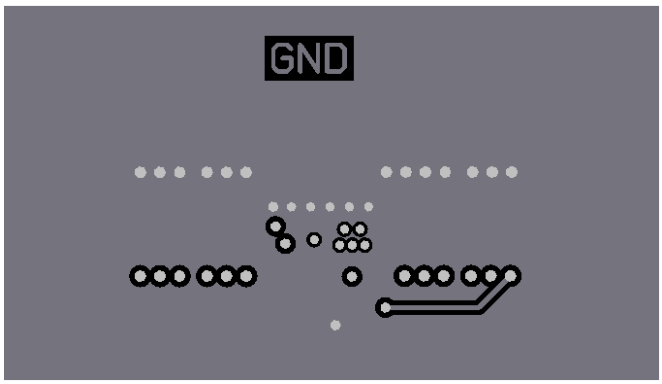


图 35. Typical GND Layer

10.3 EMI

The TPSM84209 is compliant with EN55011 radiated emissions. 图 36, 图 37, and 图 38 show typical examples of radiated emissions plots for the TPSM84209. The graphs include the plots of the antenna in the horizontal and vertical positions.

10.3.1 EMI Plots

EMI plots were measured using the standard TPSM84209EVM with no input filter.

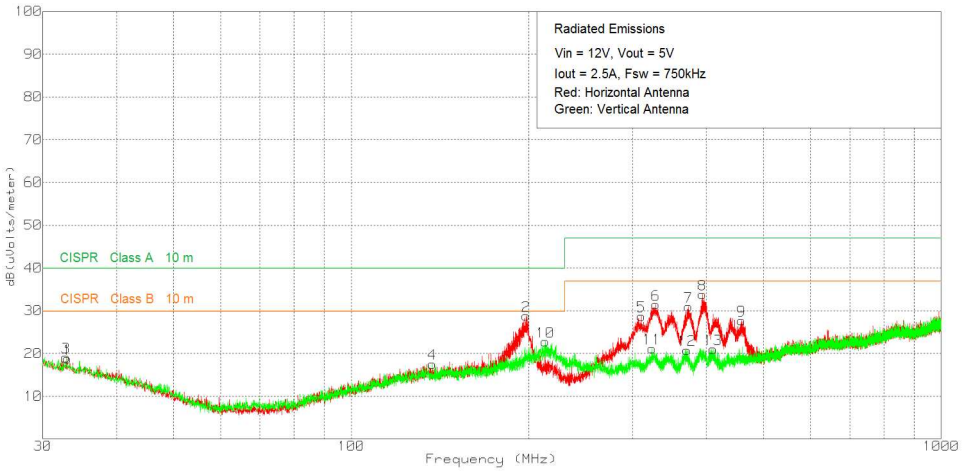


图 36. Radiated Emissions 12-V Input, 5-V Output, 2.5-A Load (EN55011 Class B)

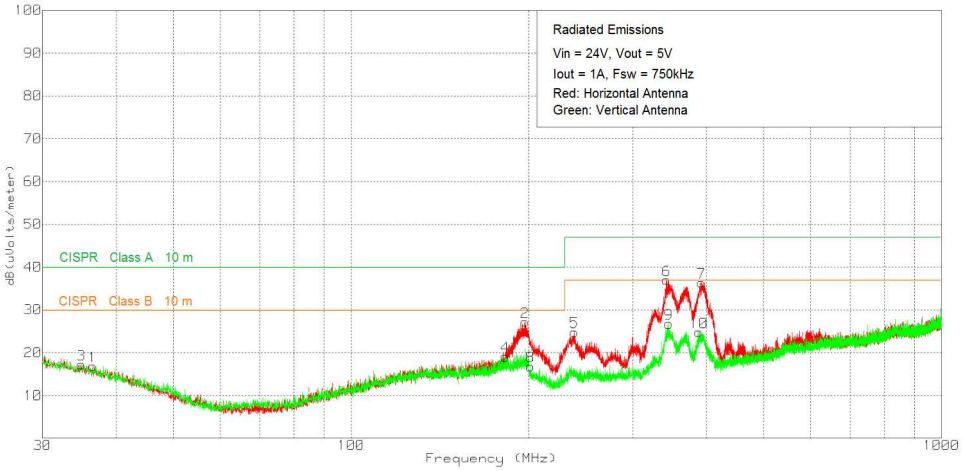


图 37. Radiated Emissions 24-V Input, 5-V Output, 1-A Load (EN55011 Class B)

EMI (接下页)

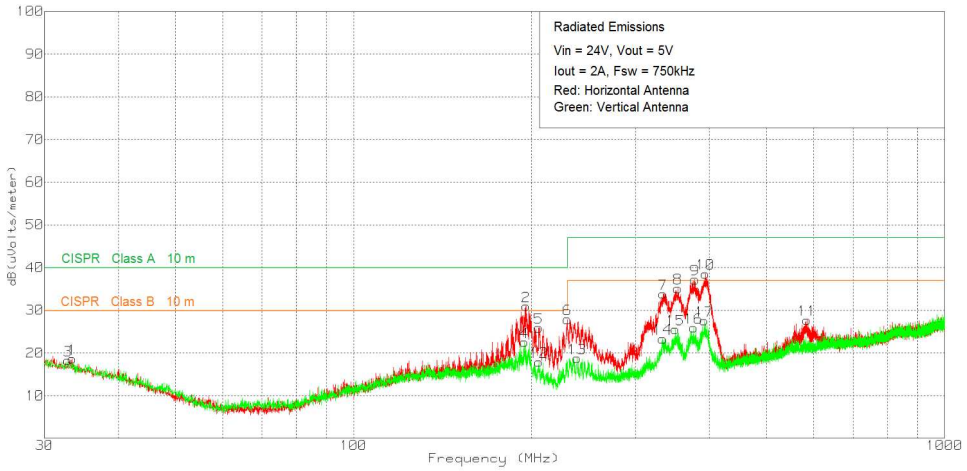


图 38. Radiated Emissions 24-V Input, 5-V Output, 2-A Load (EN55011 Class A)

10.4 Package Specifications

表 8. Package Specifications Table

TPSM84209		VALUE	UNIT
Weight		107	mg
Flammability	Meets UL 94 V-O		
MTBF Calculated Reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign	123	MHrs

11 器件和文档支持

11.1 器件支持

11.1.1 第三方产品免责声明

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11.2 使用 WEBENCH® 工具创建定制设计方案

请单击此处，借助 WEBENCH® Power Designer 并使用 TPSM84209 器件创建定制设计方案。

1. 首先输入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化该设计的关键参数，如效率、尺寸和成本。
3. 将生成的设计与德州仪器 (TI) 的其他可行的解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案以常用 CAD 格式导出
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com.cn/WEBENCH。

11.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.5 商标

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WEBENCH is a registered trademark of Texas Instruments.
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11.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

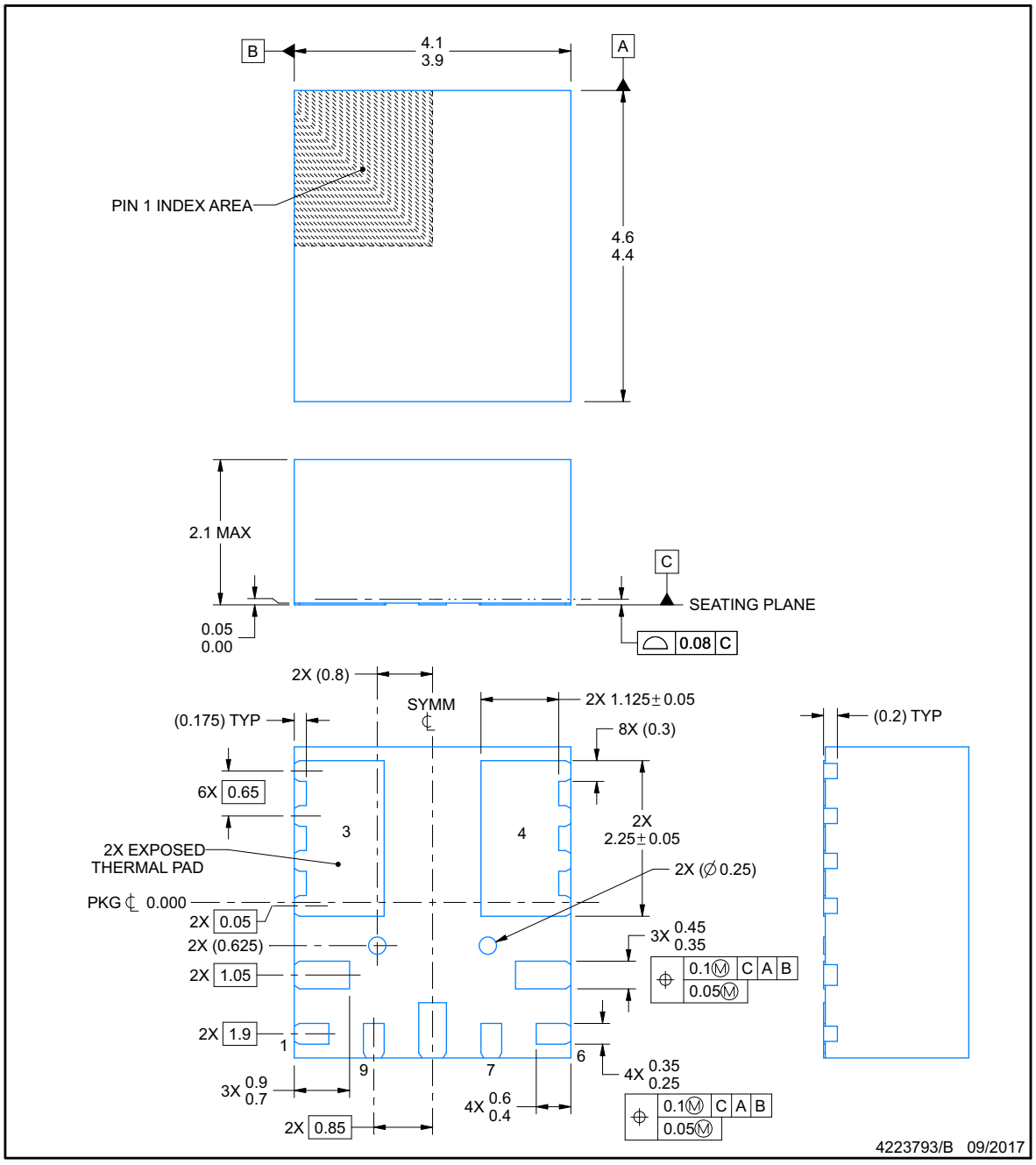
以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

PACKAGE OUTLINE

RKH0009A

QFN - 2.1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



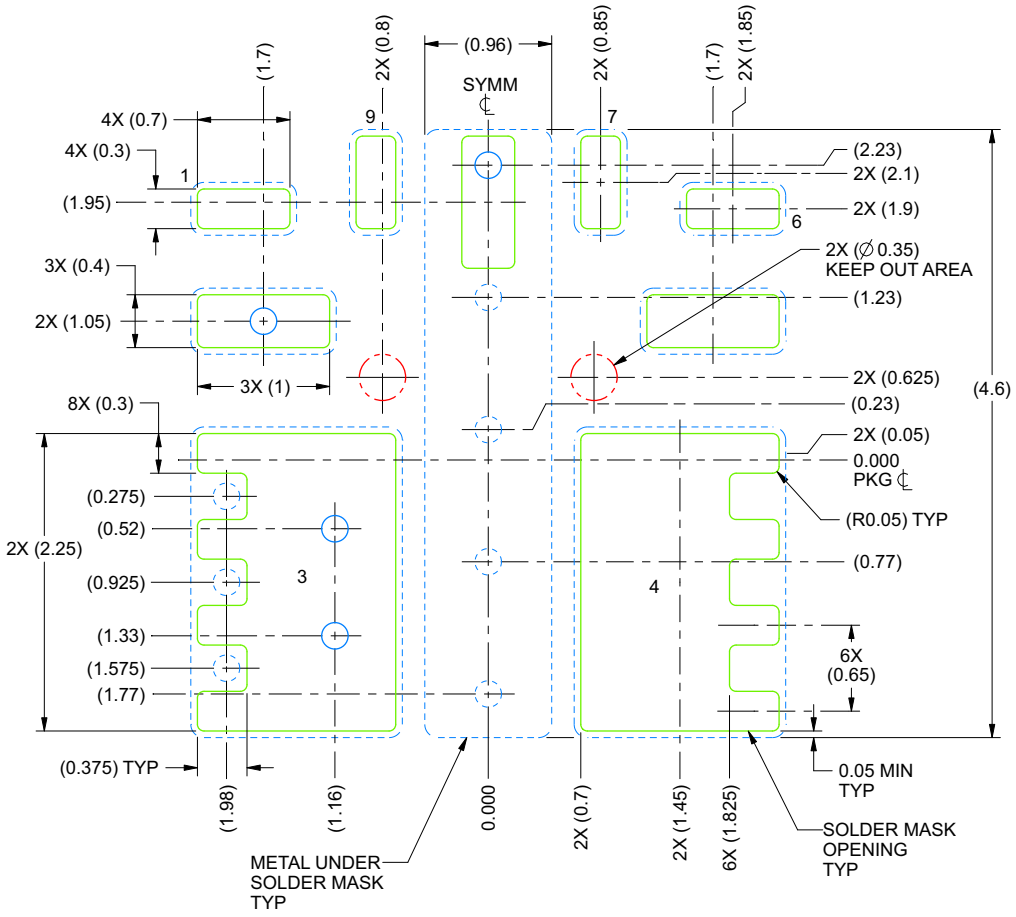
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RKH0009A — **QFN - 2.1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:20X

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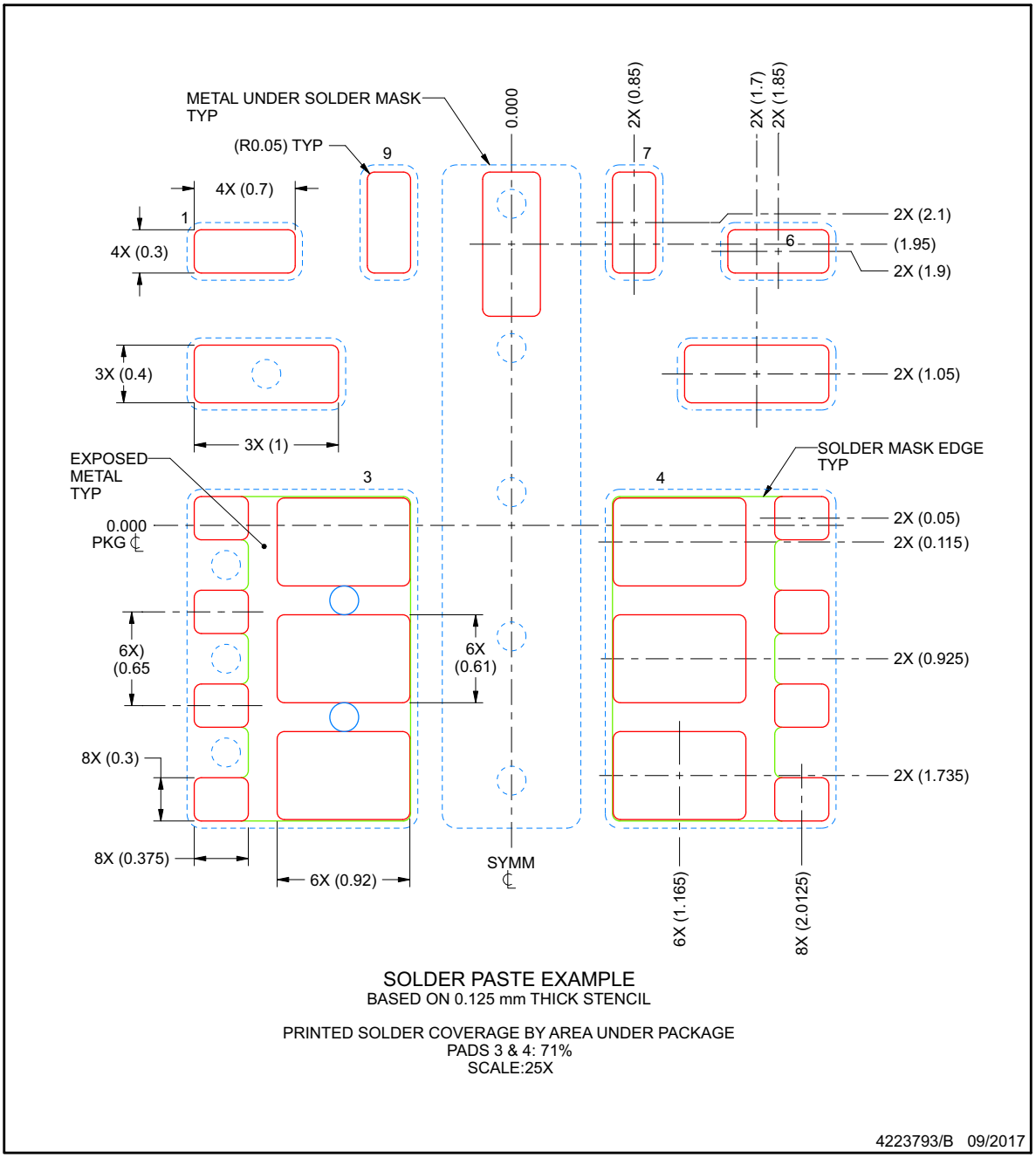
NOTES: (continued)

4. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RKH0009A — **QFN - 2.1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 3 & 4: 71%
SCALE:25X

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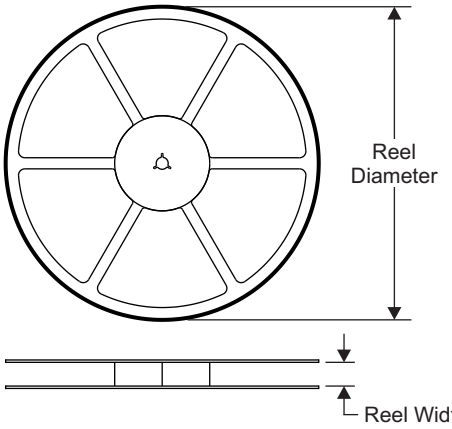
NOTES: (continued)

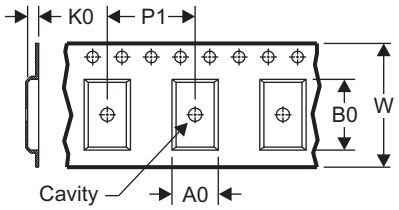
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

12.1 Tape and Reel Information

REEL DIMENSIONS

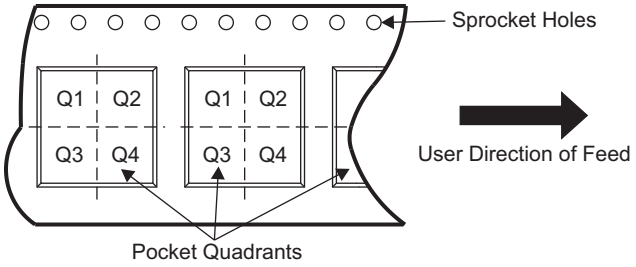


TAPE DIMENSIONS



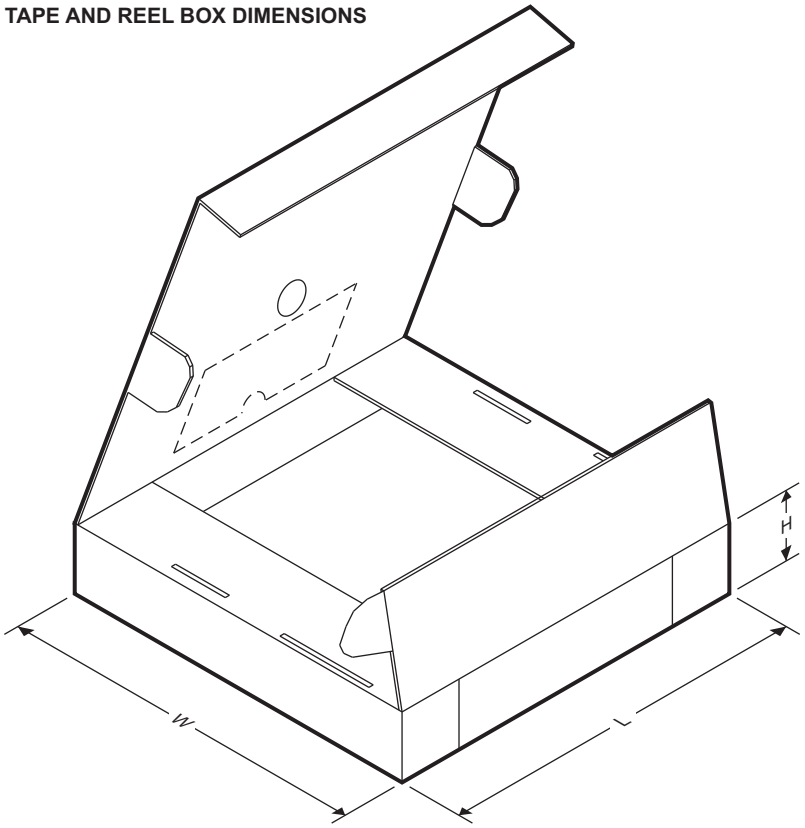
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM84209RKHT	QFN-FCMOD	RKH	9	3000	330.0	12.4	4.3	4.8	2.25	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM84209RKHT	QFN-FCMOD	RKH	9	3000	383.0	353.0	58.0

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPSM84209RKHR	ACTIVE	QFN-FCMOD	RKH	9	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	TPSM84209	Samples
TPSM84209RKHT	ACTIVE	QFN-FCMOD	RKH	9	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	TPSM84209	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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