TEXAS INSTRUMENTS
TS3USB221E
ZHCSK77E – SEPTEMBER 2009 – REVISED JULY 2024

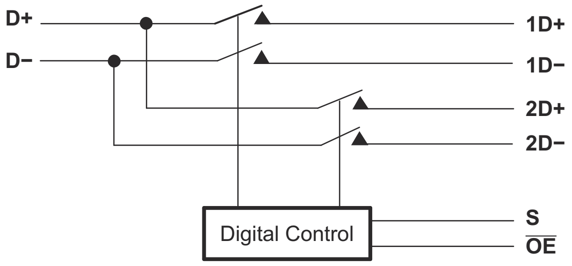
TS3USB221E 具有单使能端和 IEC 3 级 ESD 保护的高速 USB 2.0 (480Mbps) 1:2 多路复用器 – 多路信号分离器开关

1 特性

- V_{CC} 工作范围为 2.3V 至 3.6V
- 开关 I/O 支持高达 5.5V 的信号
- 1.8V 兼容控制引脚输入
- $\overline{OE}$ 禁用时采用低功耗模式 (1μA)
- r_{ON} = 6Ω（最大值）
- Δr_{ON} = 0.2Ω（典型值）
- $C_{IO(ON)}$ = 7pf（最大值）
- 低功耗（最大值为 30μA）
- 经测试的 ESD 性能：
  - 7000V 人体放电模型，符合 JEDEC JS-001 标准
  - 1000V 充电器件模型，符合 JEDEC JS-002 标准
- ESD 性能 I/O 端口接地：
  - 12kV 人体放电模型 (JEDEC JS-001)
  - ±7kV 接触放电 (IEC 61000-4-2)
- 高带宽（典型值为 1GHz）

2 应用

- 为 USB 1.0、1.1 和 2.0 路由信号
- 手机
- 数码相机
- 笔记本电脑
- USB I/O 扩展
- MHL 1.0



方框图

3 说明

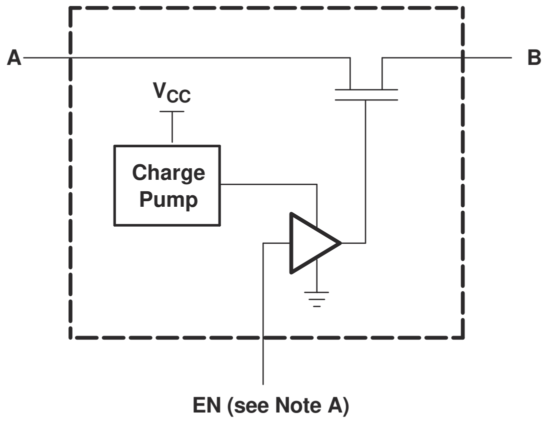
TS3USB221E 是一款高带宽开关，专为手持和消费类应用（例如手机、数码相机和具有集线器的笔记本电脑或具有受限 USB I/O 的控制器）中的高速 USB 2.0 信号切换而设计。此开关具有较宽的带宽 (1GHz)，这一特性使得信号传递具有最少的边缘失真和相位失真。该器件将 USB 主机器件差动输出复用到一个相应的输出（共两个输出）。此开关为双向开关，输出端高速信号具有极少或零衰减。TS3USB221E 经过精心设计，可实现低位间偏移和高通道间噪声隔离，并且与高速 USB 2.0 (480Mbps) 等各种标准兼容。

TS3USB221E 在所有引脚上集成了 ESD 保护单元，采用 SON 封装 (3mm × 3mm) 和微型 μQFN 封装 (2mm × 1.5mm)，在自然通风条件下的额定工作温度范围为 –40°C 至 85°C。

封装信息

器件型号	封装(1)	封装尺寸(2)
TS3USB221E	DRC（VSON，10）	3mm × 3mm
	RSE（UQFN，10）	2mm × 1.5mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



A. EN 是应用于开关的内部启用信号。

每个 FET 开关 (SW) 的简化版原理图)

English Data Sheet: SCDS263

Table of Contents

4 Pin Configuration and Functions

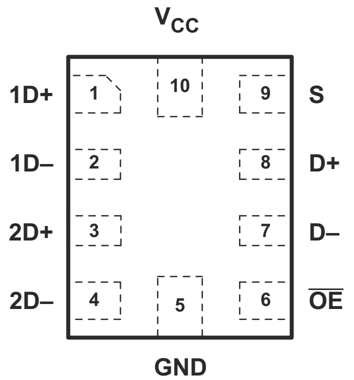


图 4-1. RSE Package, 10-Pin UQFN (Top View)

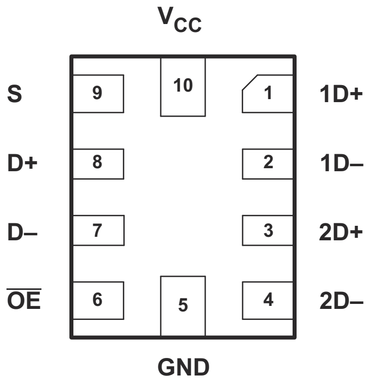


图 4-2. RSE Package, 10-Pin UQFN (Bottom View)

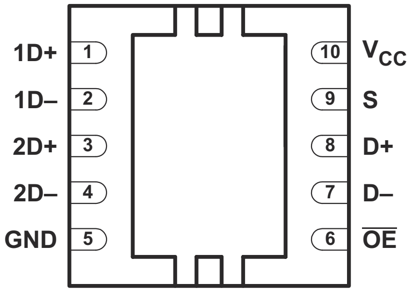


图 4-3. DRC Package, 10-Pin VSON (Top View)

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1D+	1	I/O	USB port 1
1D–	2	I/O	
2D+	3	I/O	USB port 2
2D–	4	I/O	
GND	5	—	Ground
$\overline{OE}$	6	I	Bus-switch enable
D–	7	I/O	Common USB port
D+	8	I/O	
S	9	I	Select input
V_{CC}	10	—	Supply voltage

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	4.6	V
V_{IN}	Control input voltage(2) (2) (3)		–0.5	7	V
$V_{I/O}$	Switch I/O voltage(2) (3) (4)		–0.5	7	V
I_{IK}	Control input clamp current	$V_{IN} < 0$		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$		–50	mA
$I_{I/O}$	ON-state switch current(5)			±120	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance(6)	DRC package		48.7	°C/W
		RSE package		243	
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ ESDA/JEDEC JS-001(1)	I/O pins to GND	±12000	V
			Pins GND, $\overline{OE}$, S and V_{CC}	±7000	
		Contact discharge (IEC 61000-4-2)	I/O pins to GND	±7000	
		Charged-device model (CDM), per JEDEC specification JESD-002(2)		±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

See (1).

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltages	V_{CC} = 2.3 V to 2.7 V	0.46 × V_{CC}		V
		V_{CC} = 2.7 V to 3.6 V	0.46 × V_{CC}		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.25 × V_{CC}	V
		V_{CC} = 2.7 V to 3.6 V		0.25 × V_{CC}	
$V_{I/O}$	Data input/output voltage(2)		0	5.5	V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the *Implications of Slow or Floating CMOS Inputs* application note.
(2) The I/O pins are 5.5V tolerant and functional for the entire range. However, for VI/O >3.6V, channel R_{ON} will be high. Use 3.3V power supply for best results.

5.4 Thermal Information

THERMAL METRIC(1)		TS3USB221E		UNIT
		DRC (VSON)	RSE (UQFN)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	57.7	204.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	87.7	118.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	32.6	121.5	
ψ_{JT}	Junction-to-top characterization parameter	8.2	13.9	
ψ_{JB}	Junction-to-board characterization parameter	32.8	121.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	18.5	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS			MIN	TYP(2)	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V, 2.7 V,	I_I = –18 mA		–1.8			V
I_{IN}	Control inputs	V_{CC} = 3.6 V, 2.7 V, 0 V,	V_{IN} = 0 V to 3.6 V				±1	μA
I_{OZ} (3)		V_{CC} = 3.6 V, 2.7 V, V_O = 0 V to 5.25 V, V_I = 0 V,	V_{IN} = V_{CC} or GND, Switch OFF				±1	μA
I_{OFF}		V_{CC} = 0 V	$V_{I/O}$ = 0 V to 5.25 V				±2	μA
			$V_{I/O}$ = 0 V to 3.6 V				±2	
			$V_{I/O}$ = 0 V to 2.7 V				±1	
I_{CC}		V_{CC} = 3.6 V, 2.7 V, V_{IN} = V_{CC} or GND,	$I_{I/O}$ = 0 V, Switch ON or OFF				30	μA
I_{CC} (low power mode)		V_{CC} = 3.6 V, 2.7 V, V_{IN} = V_{CC} or GND	Switch disabled ($\overline{OE}$ in high state)				1	μA
I_{CC} (4)	Control inputs	One input at 1.8 V, Other inputs at V_{CC} or GND	V_{CC} = 3.6 V				20	μA
			V_{CC} = 2.7 V				0.5	
C_{in}	Control inputs	V_{CC} = 3.3 V, 2.5 V,	V_{IN} = 3.3 V or 0 V			1.5	2.5	pF
$C_{io(OFF)}$		V_{CC} = 3.3 V, 2.5 V,	$V_{I/O}$ = 3.3 V or 0 V,	Switch OFF		3.5	5	pF
$C_{io(ON)}$		V_{CC} = 3.3 V, 2.5 V,	$V_{I/O}$ = 3.3 V or 0 V,	Switch ON		6	7.5	pF
r_{ON} (5)		V_{CC} = 3 V, 2.3 V	V_I = 0 V,	I_O = 30 mA		3	6	Ω
			V_I = 2.4 V,	I_O = –15 mA		3.4	6	
Δr_{ON}		V_{CC} = 3 V, 2.3 V	V_I = 0 V,	I_O = 30 mA		0.2		Ω
			V_I = 1.7,	I_O = –15 mA		0.2		
$r_{ON(flat)}$		V_{CC} = 3 V, 2.3 V	V_I = 0 V,	I_O = 30 mA		1		Ω
			V_I = 1.7,	I_O = –15 mA		1		

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

5.6 Dynamic Electrical Characteristics, V_{CC} = 3.3 V ±10%

over operating range, T_A = – 40°C to 85°C, V_{CC} = 3.3 V ±10%, GND = 0 V

PARAMETER		TEST CONDITIONS	TYP(1)	UNIT
X_{TALK}	Crosstalk	R_L = 50 , f = 250 MHz	– 40	dB
O_{IRR}	OFF isolation	R_L = 50 , f = 250 MHz	– 40	dB
BW	Bandwidth (– 3 dB)	R_L = 50	1	GHz

(1) For Maximum or Minimum conditions, use the appropriate value specified under *Electrical Characteristics* for the applicable device type.

5.7 Dynamic Electrical Characteristics, V_{CC} = 2.5 V ±10%

over operating range, T_A = – 40°C to 85°C, V_{CC} = 2.5 V ±10%, GND = 0 V

PARAMETER		TEST CONDITIONS	TYP(1)	UNIT
X_{TALK}	Crosstalk	R_L = 50 , f = 250 MHz	-39	dB
O_{IRR}	OFF isolation	R_L = 50 , f = 250 MHz	-40	dB
BW	Bandwidth (3 dB)	R_L = 50	1	GHz

(1) For Maximum or Minimum conditions, use the appropriate value specified under *Electrical Characteristics* for the applicable device type.

5.8 Switching Characteristics, V_{CC} = 3.3 V ±10%

over operating range, T_A = – 40°C to 85°C, V_{CC} = 3.3 V ±10%, GND = 0 V

PARAMETER			MIN	TYP(1)	MAX	UNIT
t_{pd}	Propagation delay(2) (3)			0.25		ns
t_{ON}	Line enable time	S to D, nD			30	ns
		$\overline{OE}$ to D, nD			17	
t_{OFF}	Line disable time	S to D, nD			12	ns
		$\overline{OE}$ to D, nD			10	
$t_{SK(O)}$	Output skew between center port to any other port(2)			0.1	0.2	ns
$t_{SK(P)}$	Skew between opposite transitions of the same output (t_{PHL} – t_{PLH})(2)			0.1	0.2	ns

(1) For Maximum or Minimum conditions, use the appropriate value specified under *Electrical Characteristics* for the applicable device type.
(2) Specified by design
(3) The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. Because this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

5.9 Switching Characteristics, V_{CC} = 2.5 V ±10%

over operating range, T_A = – 40°C to 85°C, V_{CC} = 2.5 V ±10%, GND = 0 V

PARAMETER			MIN	TYP(1)	MAX	UNIT
t_{pd}	Propagation delay(2) (3)			0.25		ns
t_{ON}	Line enable time	S to D, nD			50	ns
		$\overline{OE}$ to D, nD			32	
t_{OFF}	Line disable time	S to D, nD			23	ns
		$\overline{OE}$ to D, nD			12	
$t_{SK(O)}$	Output skew between center port to any other port(2)			0.1	0.2	ns
$t_{SK(P)}$	Skew between opposite transitions of the same output (t_{PHL} – t_{PLH})(2)			0.1	0.2	ns

(1) For Maximum or Minimum conditions, use the appropriate value specified under *Electrical Characteristics* for the applicable device type.

(2) Specified by design

(3) The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. This time constant is much smaller than the rise/fall times of typical driving signals, therefore the time adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

5.10 Typical Characteristics

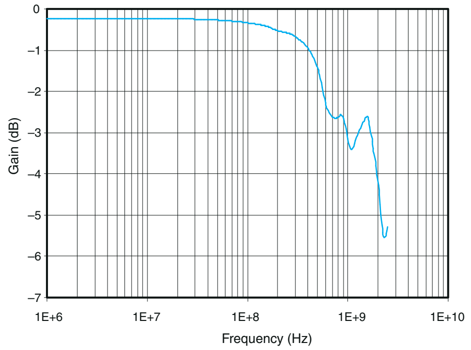


图 5-1. Gain vs Frequency

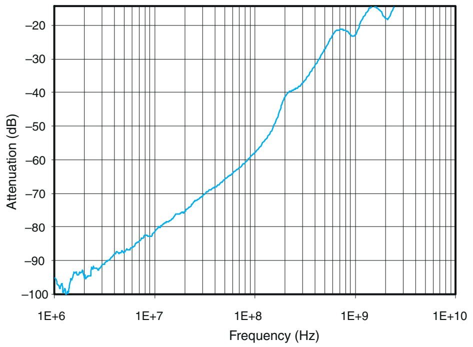


图 5-2. OFF Isolation vs Frequency

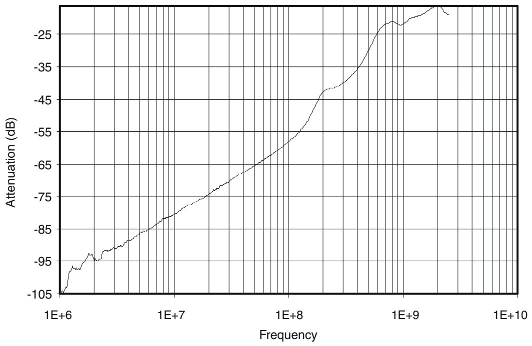


图 5-3. Crosstalk vs Frequency

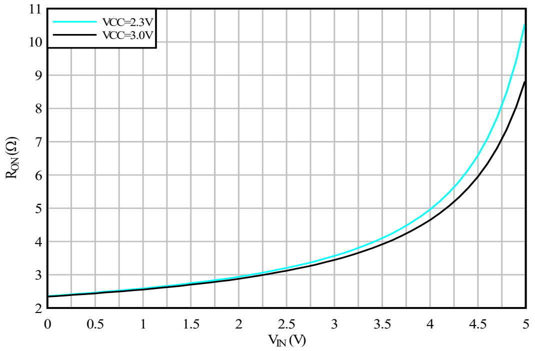
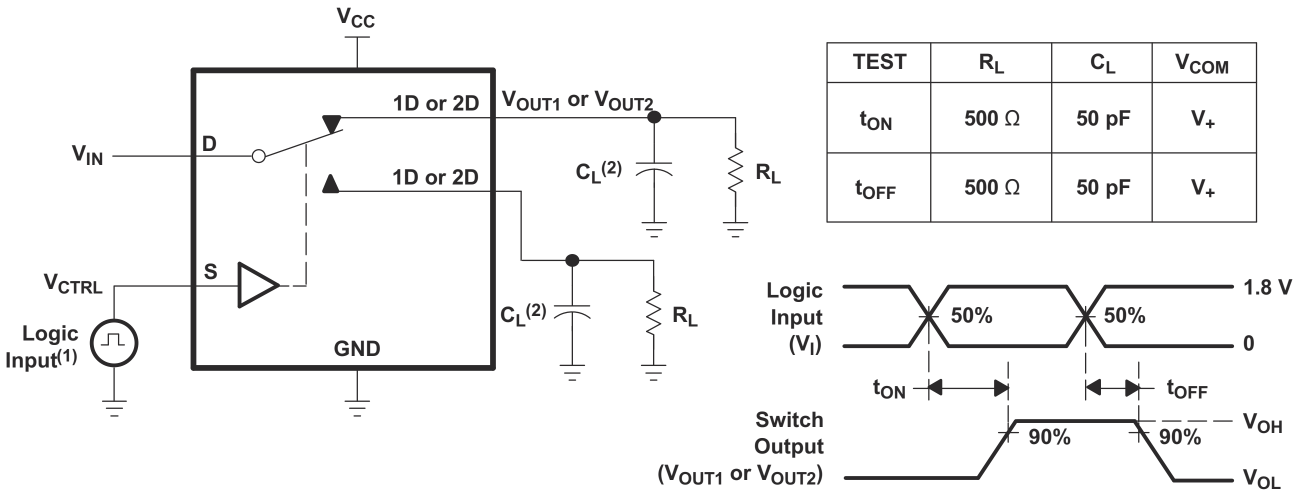


图 5-4. R_{on} vs V_{IN} (I_{OUT} = – 30 mA)

Parameter Measurement Information



TEST	R_L	C_L	V_{COM}
t_{ON}	500 Ω	50 pF	V_+
t_{OFF}	500 Ω	50 pF	V_+

(1) All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50W, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

图 6-1. Turnon (T_{ON}) and Turnoff Time (T_{OFF})

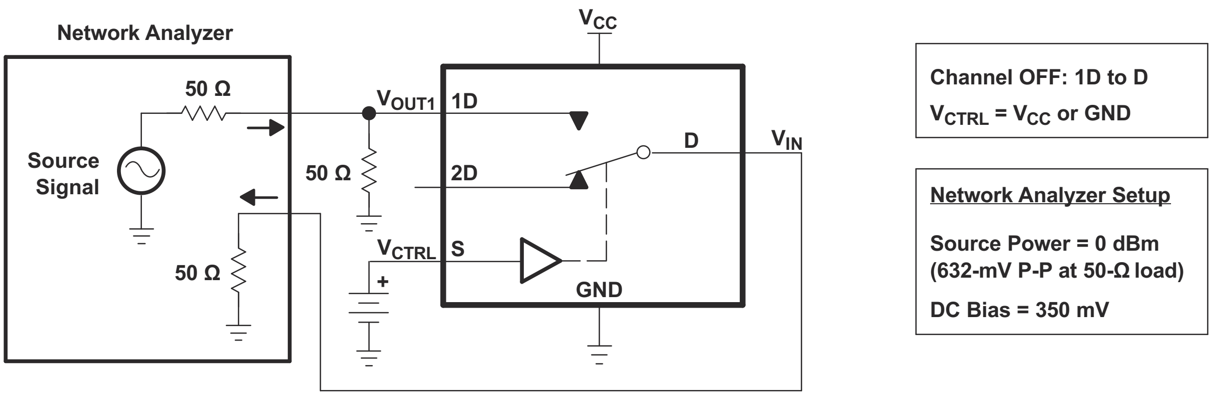


图 6-2. OFF Isolation (O_{ISO})

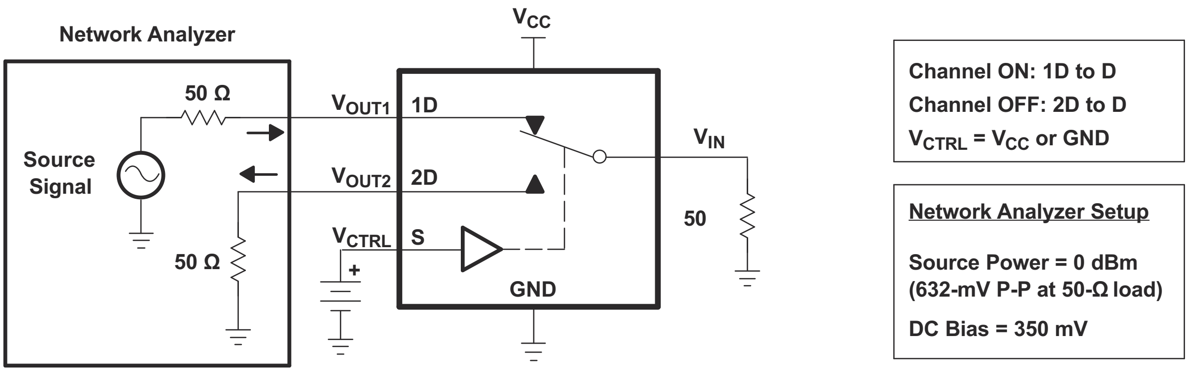


图 6-3. Crosstalk (X_{TALK})

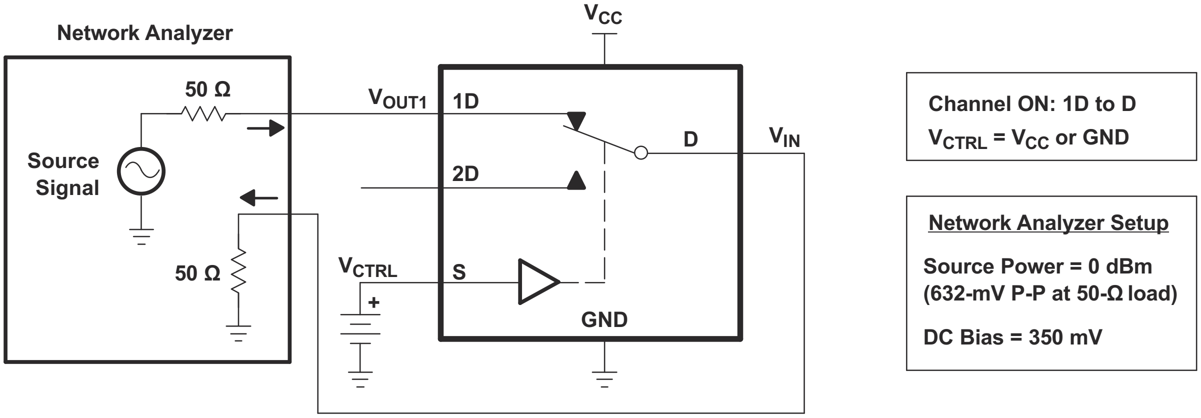


图 6-4. Bandwidth (BW)

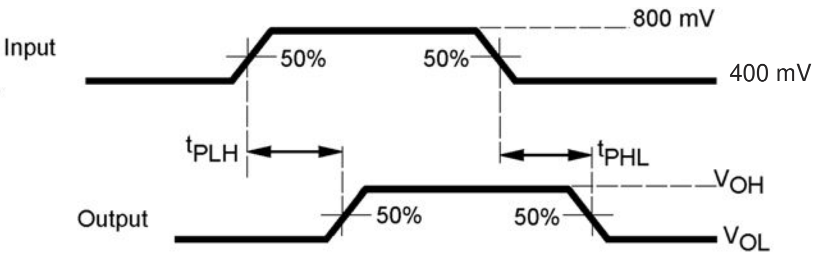


图 6-5. Propagation Delay

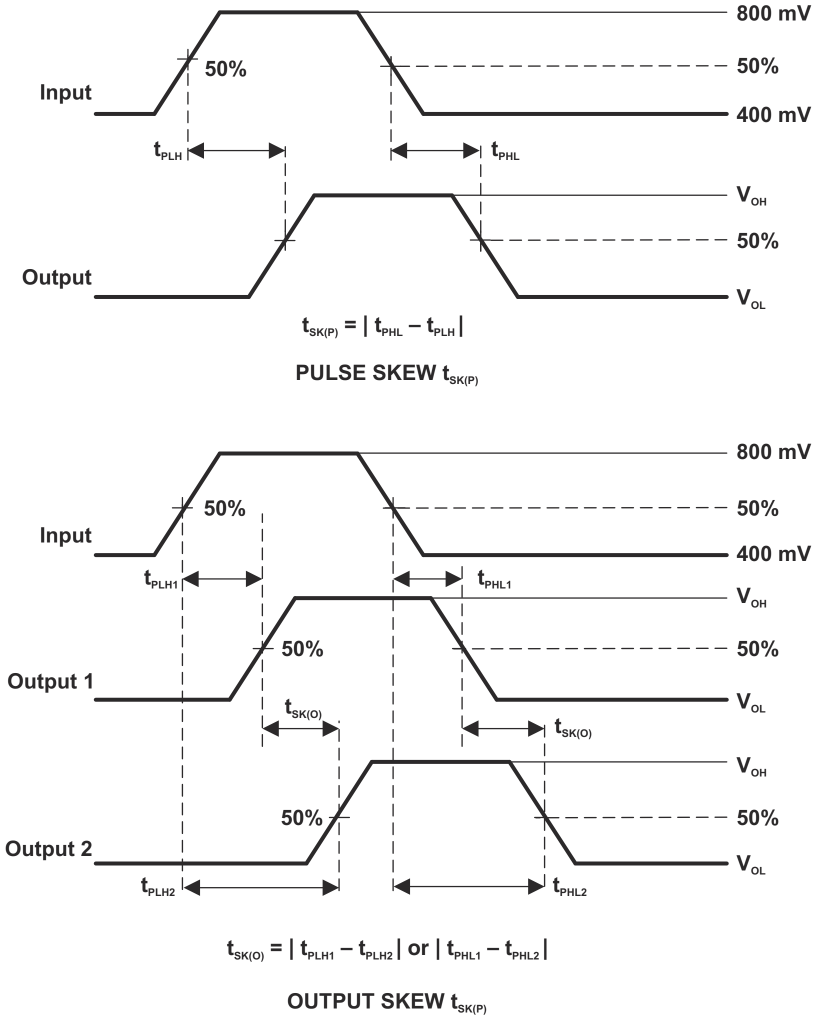


图 6-6. Skew Test

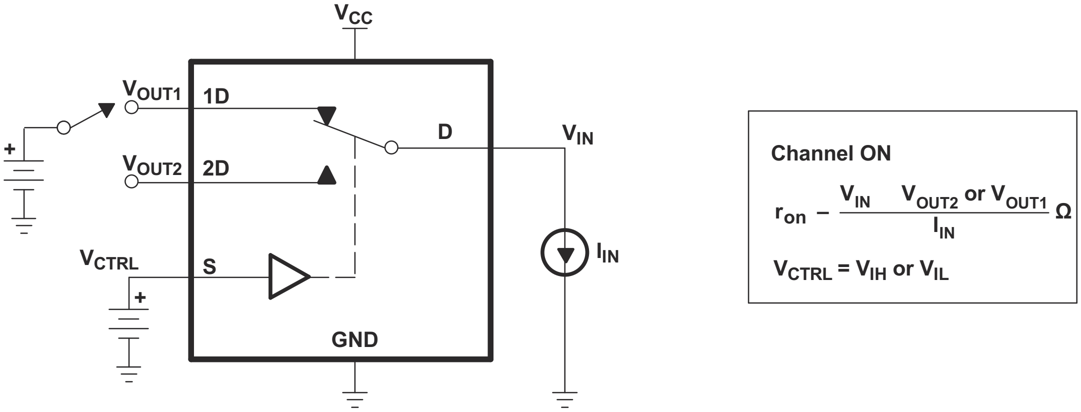
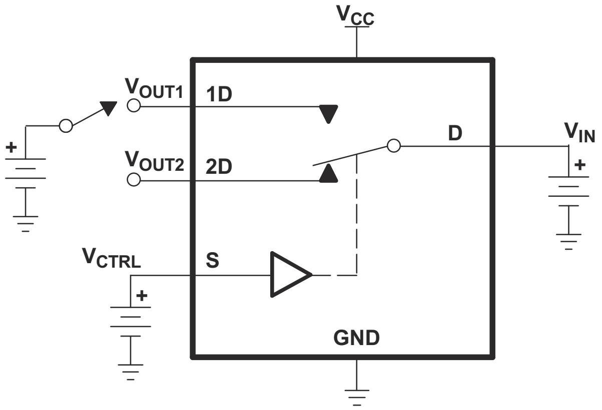
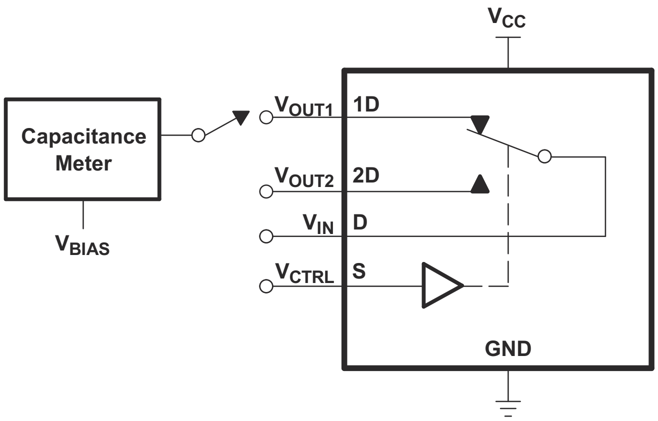


图 6-7. ON-State Resistance (R_{on})



OFF-State Leakage Current
Channel OFF
$V_{CTRL} = V_{IH}$ or V_{IL}

图 6-8. OFF-State Leakage Current



$V_{BIAS} = V_{CC}$ or GND
$V_{CTRL} = V_{CC}$ or GND
Capacitance is measured at 1D, 2D, D, and S inputs during ON and OFF conditions.

图 6-9. Capacitance

6 Detailed Description

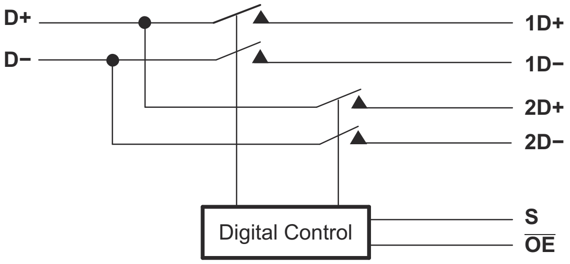
6.1 Overview

The TS3USB221E device is a 2-channel SPDT switch specially designed for the switching of high-speed USB 2.0 signals in handset and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB I/Os. The wide bandwidth (1 GHz) of this switch allows signals to pass with minimum edge and phase distortion. The device multiplexes differential outputs from a USB host device to one of two corresponding outputs. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. The device also has a low power mode that reduces the power consumption to 1 µA for portable applications with a battery or limited power budget.

The device is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

The TS3USB221E device integrates ESD protection cells on all pins, is available in a SON package (3mm × 3mm) as well as in a tiny µQFN package (2mm × 1.5mm) and is characterized over the free-air temperature range from –40°C to 85°C.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Low Power Mode

The TS3USB221E has a low power mode that reduces the power consumption to 1 µA when the device is not in use. To put the device in low power mode and disable the switch, the bus-switch enable pin $\overline{OE}$ must be supplied with a logic high signal.

6.4 Device Functional Modes

表 6-1. Truth Table

S	$\overline{OE}$	FUNCTION
X	H	Disconnect
L	L	D = 1D
H	L	D = 2D

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

There are many USB applications in which the USB hubs or controllers have a limited number of USB I/Os. The TS3USB221E can effectively expand the limited USB I/Os by switching between multiple USB buses to interface them to a single USB hub or controller. The TS3USB221E can also be used to connect a single controller to two USB connectors.

7.2 Typical Application

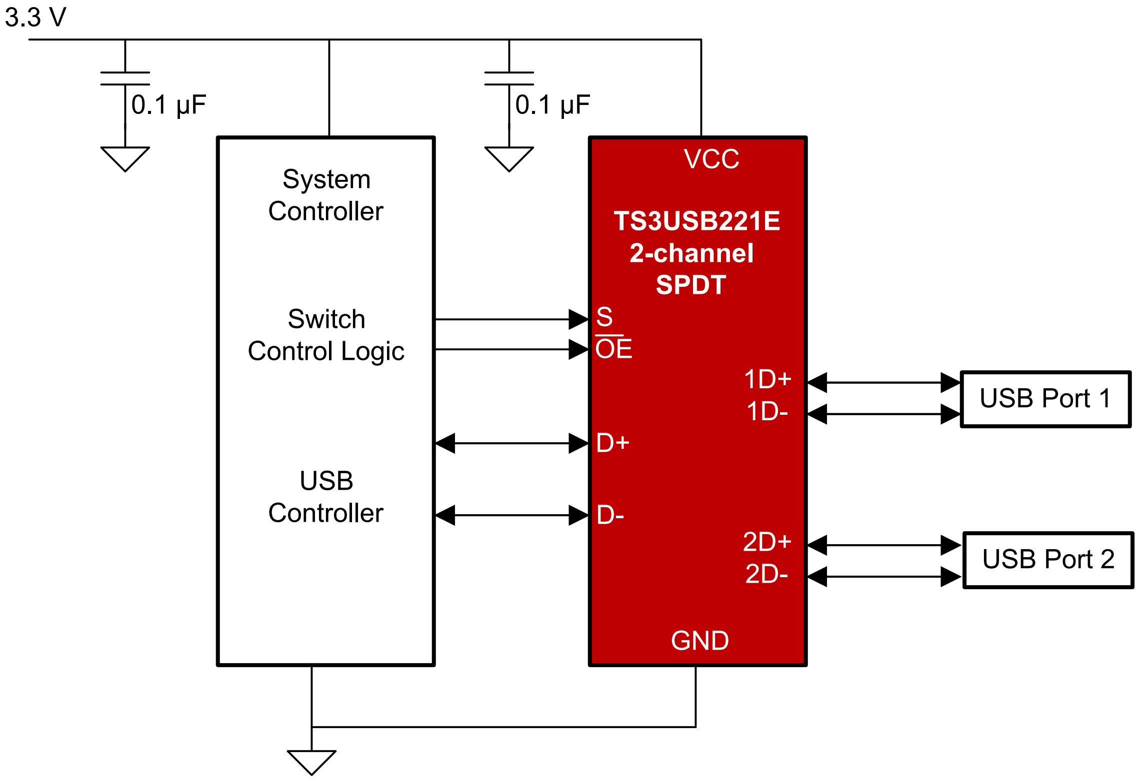


图 7-1. Simplified Schematic

7.2.1 Design Requirements

Follow the design requirements of the USB 1.0, 1.1, and 2.0 standards.

TI recommends that the digital control pins S and $\overline{OE}$ be pulled up to V_{CC} or down to GND to avoid undesired switch positions that could result from the floating pin.

7.2.2 Detailed Design Procedure

The TS3USB221E can be properly operated without any external components. However, TI recommends to connect any unused pins to ground through a 50-Ω resistor to prevent signal reflections back into the device.

7.2.3 Application Curves

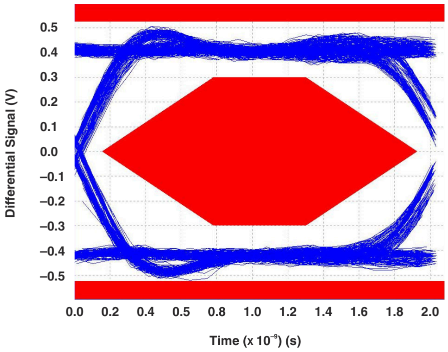


图 7-2. Eye Pattern: 480-Mbps USB Signal With No Switch (Through Path)

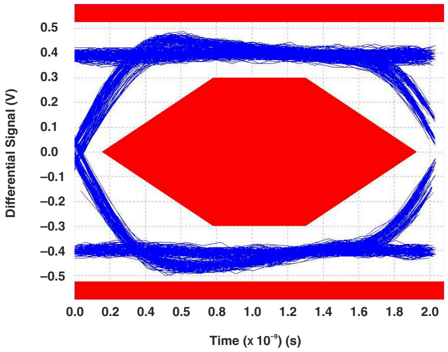


图 7-3. Eye Pattern: 480-Mbps USB Signal With Switch 1D Path

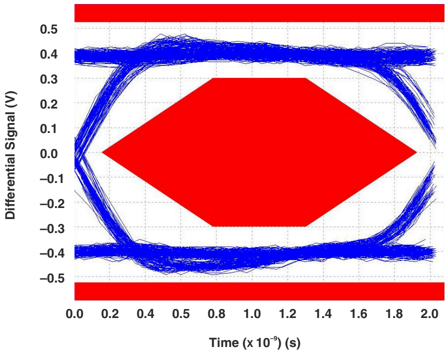


图 7-4. Eye Pattern: 480-Mbps USB Signal With Switch 2D Path

7.3 Power Supply Recommendations

Make sure that the power to the device supplied through the V_{CC} pin follows the USB 1.0, 1.1, and 2.0 standards. TI recommends placing a bypass capacitor as close as possible to the supply pin V_{CC} to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

7.4 Layout

7.4.1 Layout Guidelines

Place supply bypass capacitors as close to V_{CC} pin as possible and avoid placing the bypass caps near the D+/D – traces.

The high speed D+/D – traces should always be matched lengths and must be no more than 4 inches; otherwise, the eye diagram performance can be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In layout, the impedance of D+ and D – traces should match the cable characteristic differential impedance for optimal performance.

Route the high-speed USB signals using a minimum of vias and corners to reduce signal reflections and impedance changes. When a via must be used, increase the clearance size around the via to minimize the capacitance. Each via introduces discontinuities in the transmission line of the signal and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.

Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub should be less than 200 mm.

Route all high-speed USB signal traces over continuous planes (V_{CC} or GND), with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in 图 7-5.

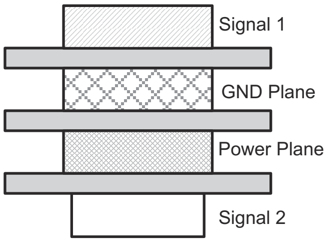


图 7-5. Four-Layer Board Stack-Up

The majority of signal traces should run on a single layer, preferably Signal 1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies. For more information on layout guidelines, see *High Speed Layout Guidelines* and *USB 2.0 Board Design and Layout Guidelines* .

7.4.2 Layout Example

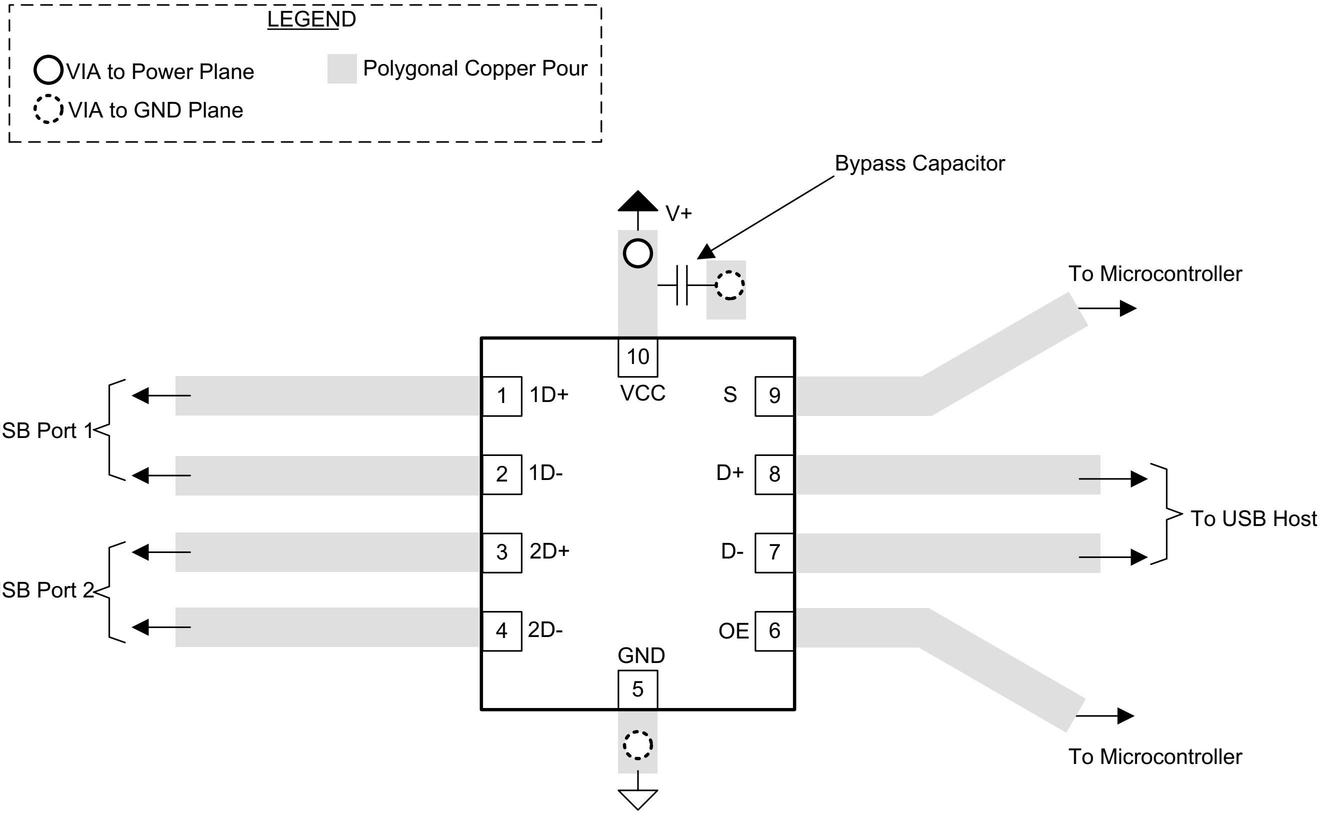


图 7-6. Package Layout Diagram

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note
- Texas Instruments, *High Speed Layout Guidelines*
- Teas Instruments, *USB 2.0 Board Design and Layout Guidelines*

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (September 2019) to Revision E (July 2024) **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式 1
- Changed ESD HBM performance testing standard from: JESD 22 to: JEDEC JS-001 4
- Changed ESD CDM performance testing standard from: JESD22-C101 to: JEDEC JS-002 4
- Added tablenote to the Data input/output voltage parameter 4
- Changed RSE (UQFN) junction-to-ambient thermal resistance value from: 169.8°C/W to: 204.8°C/W 5
- Changed RSE (UQFN) junction-to-case (top) thermal resistance value from: 84.7°C/W to: 118.1°C/W 5
- Changed RSE (UQFN) junction-to-board thermal resistance value from: 94.9°C/W to: 121.5°C/W 5
- Changed RSE (UQFN) junction-to-top characterization parameter value from: 5.7°C/W to: 13.9°C/W 5
- Changed RSE (UQFN) junction-to-board characterization parameter value from: 94.9°C/W to: 121.2°C/W 5
- Changed the V_{IK} value in the *Electrical Characteristics* table from: –1.8V maximum to: –1.8V minimum 5
- Changed the graphs in the *Typical Characteristics* section 7

Changes from Revision C (April 2015) to Revision D (September 2019)	Page
• 将 V_{CC} 工作范围从 2.5V 至 3.3V 更改为 2.3V 至 3.6V	1

Changes from Revision B (July 2012) to Revision C (April 2015)	Page
• 添加了 *引脚配置和功能* 部分、*ESD 等级* 表、*热性能信息* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分	1
• 删除了 *订购信息* 表	1

Changes from Revision A (February 2010) to Revision B (July 2012)	Page
• 更新了 *订购信息* 表中 RSE 封装的顶部标记	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3USB221EDRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZVM	Samples
TS3USB221ERSER	ACTIVE	UQFN	RSE	10	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(LGH, LGO, LGR, LG V)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

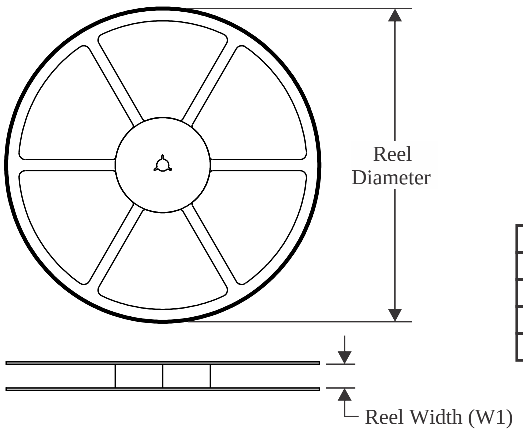
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

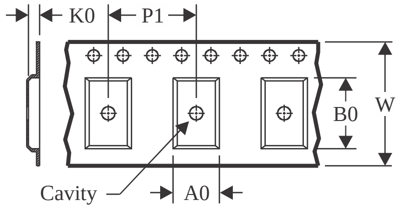
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

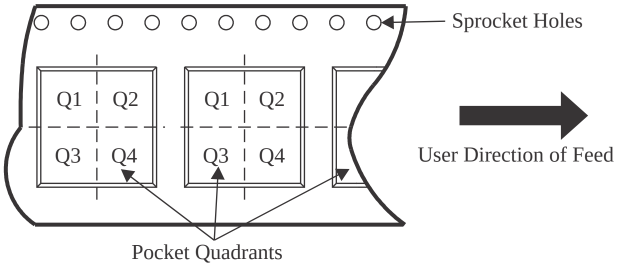


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

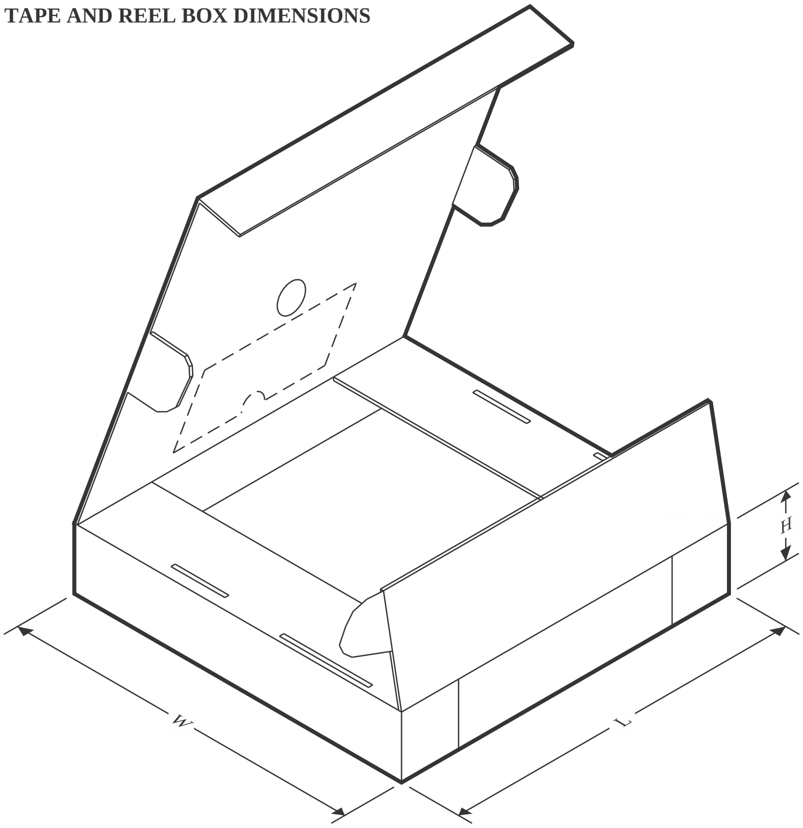
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

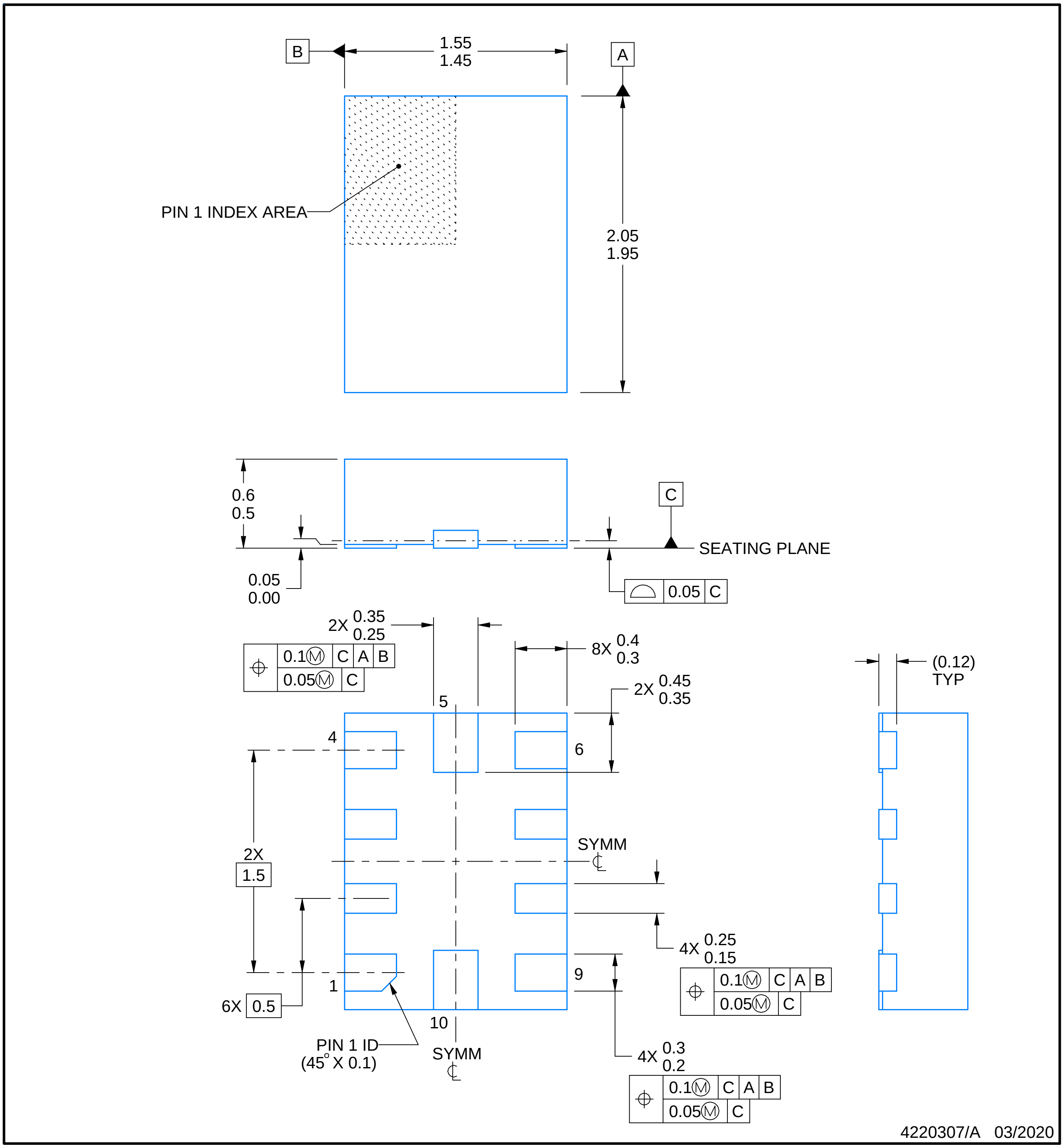
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3USB221EDRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TS3USB221ERSER	UQFN	RSE	10	3000	180.0	9.5	1.7	2.2	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3USB221EDRCR	VSON	DRC	10	3000	356.0	356.0	35.0
TS3USB221ERSER	UQFN	RSE	10	3000	189.0	185.0	36.0

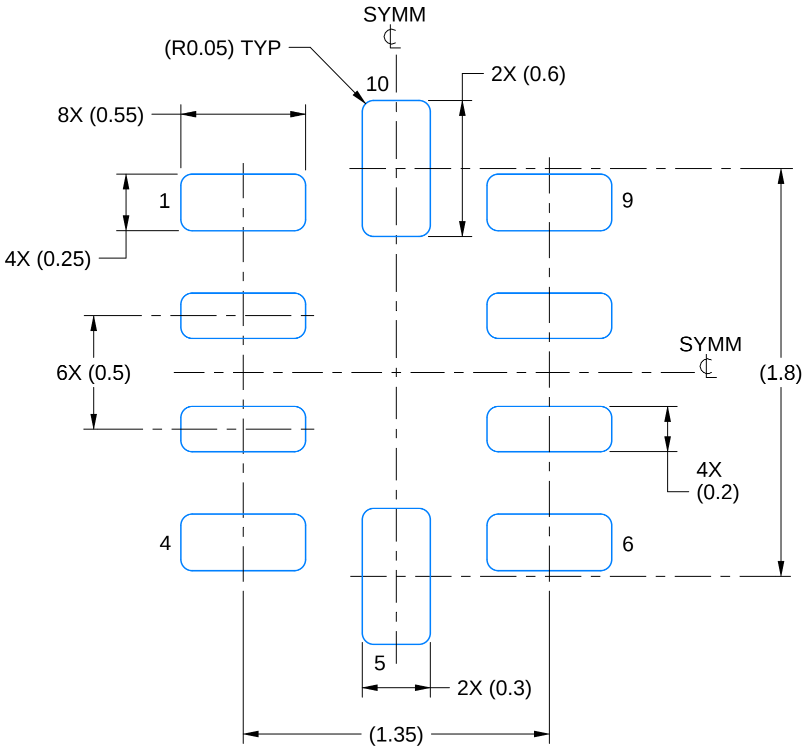


4220307/A 03/2020

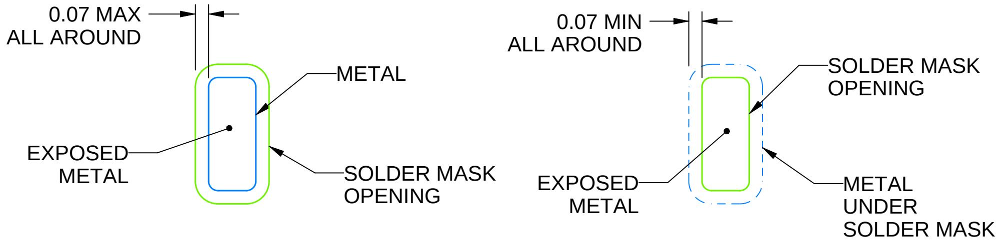
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



NON SOLDER MASK
DEFINED
(PREFERRED)

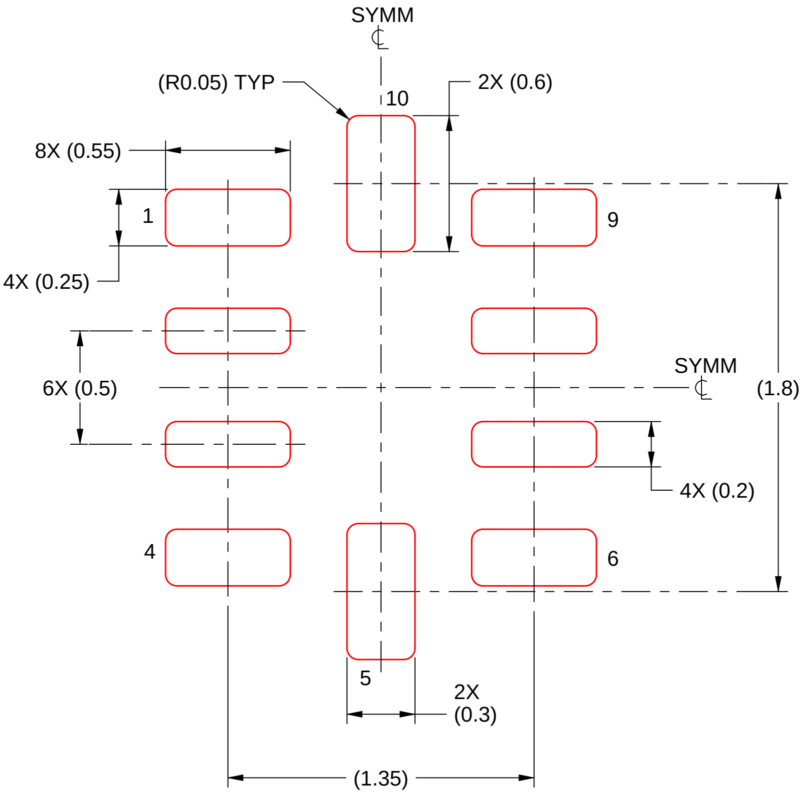
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4220307/A 03/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

4220307/A 03/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

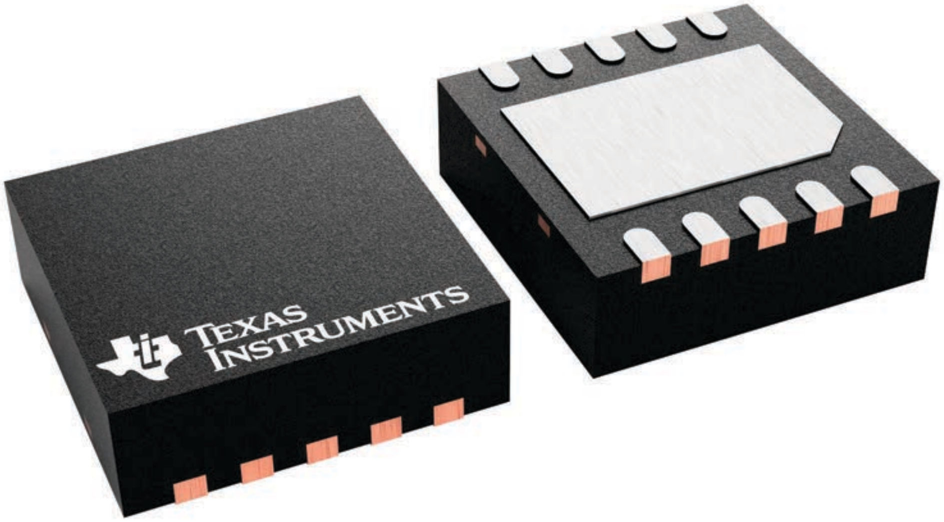
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

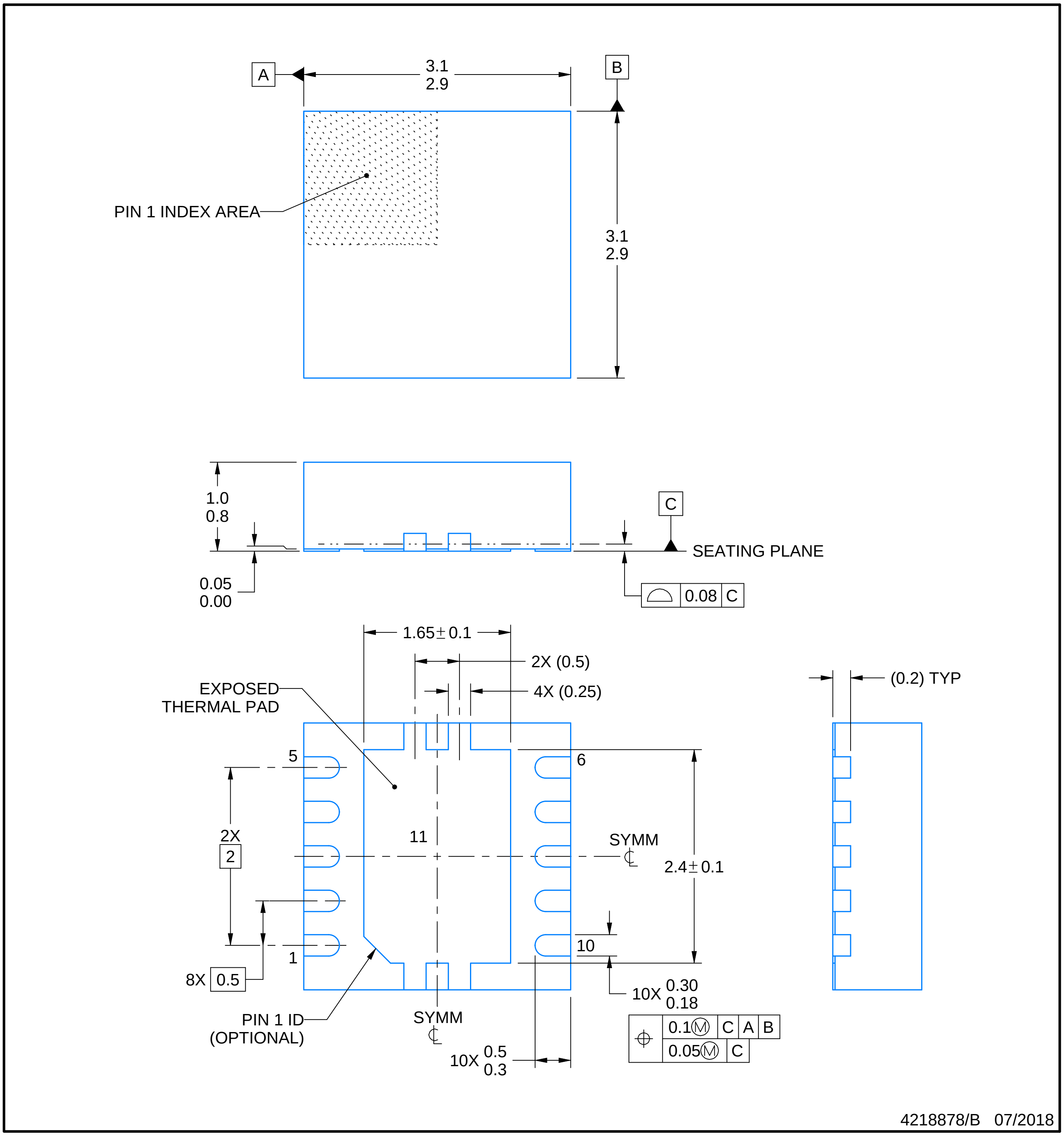


DRC0010J

PACKAGE OUTLINE

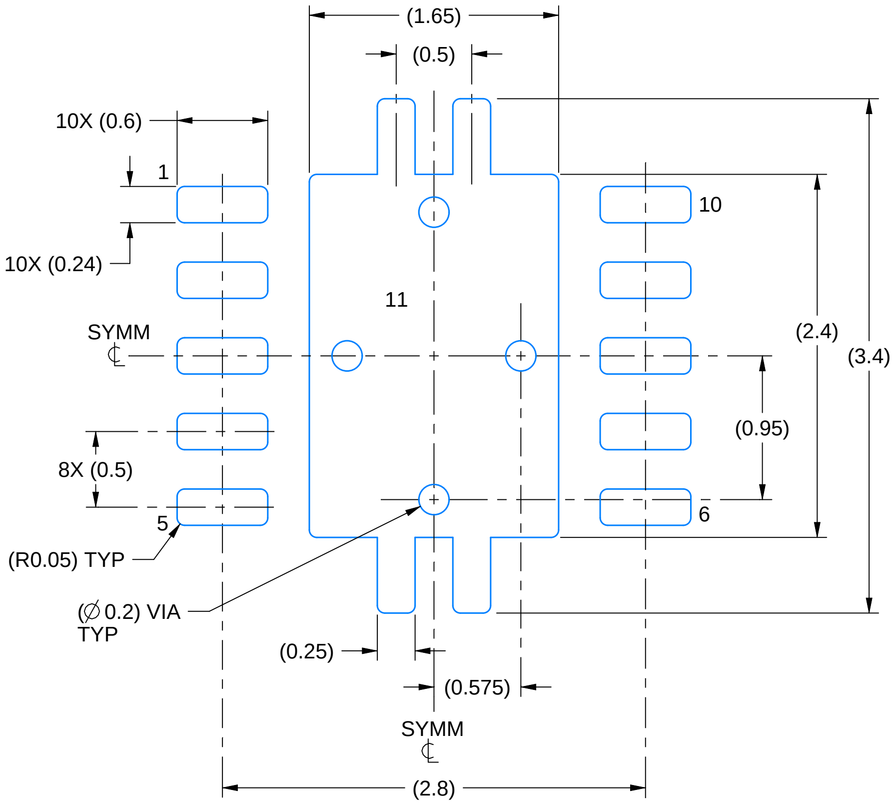
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

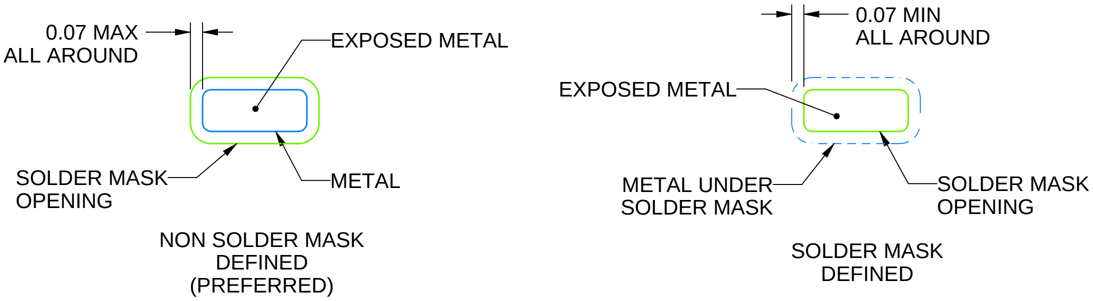


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



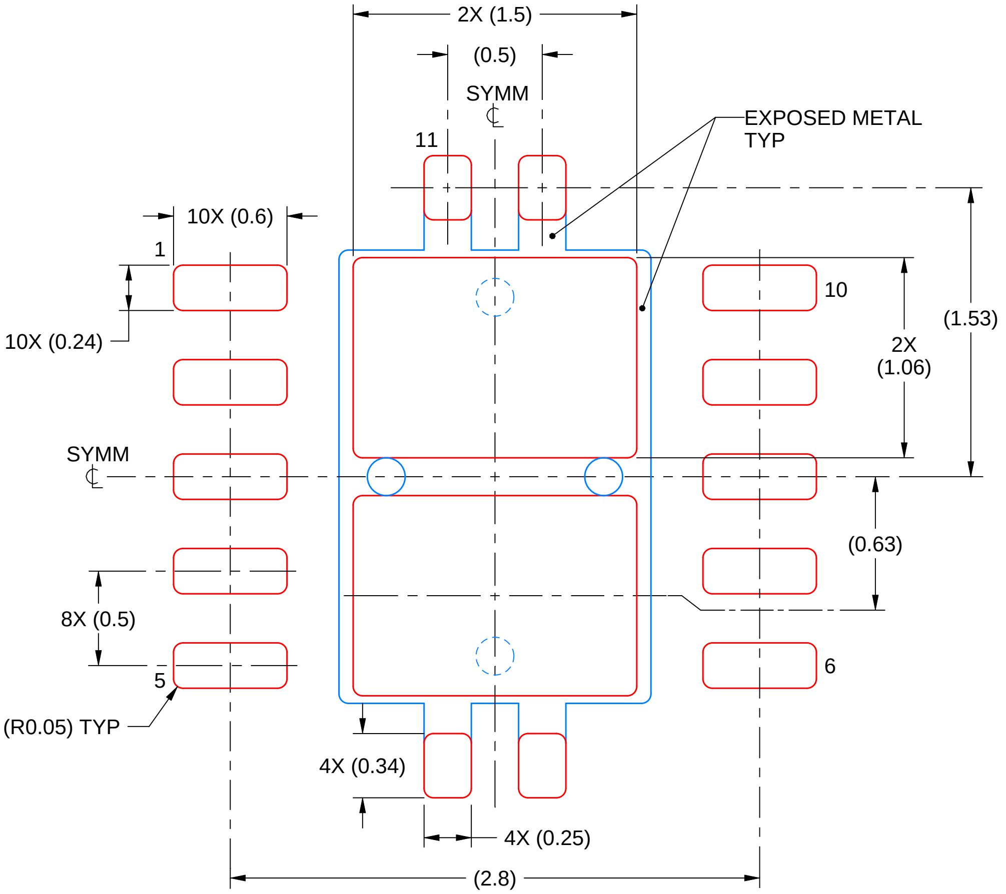
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265