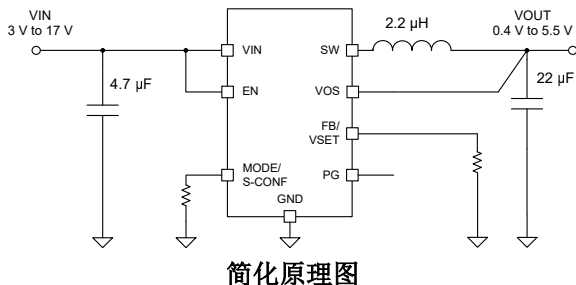


TPS629210-Q1 1A、3V 至 17V 汽车类低 I_Q 降压转换器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
 - -40°C 至 150°C 的工作结温范围
 - 器件 HBM ESD 分类等级 2
 - CDM ESD 分级等级 C4B
- 提供功能安全
 - 有助于进行功能安全系统设计的文档
- 高效率 DCS-Control 拓扑
 - 内部补偿
 - 无缝 PWM/PFM 转换
- 4 μA (典型值) 低静态电流
- 输出电流高达 1A
- 250m Ω 高侧/85m Ω 低侧 $R_{\text{DS(on)}}$
- $\pm 1\%$ 的输出电压精度
- 可配置的输出电压选项：
 - 0.6V 至 5.5V V_{FB} 外部分压器：
 - VSET 内部分压器：
 - 18 个电压选项 (0.4V 至 5.5V)
- 通过 MODE/S-CONF 引脚提高了灵活性
 - 2.5 MHz 或 1.0 MHz 开关频率
 - 具有动态模式更改选项的强制 PWM 或自动 (PFM) 省电模式
 - 输出放电开/关
- 无需外部自举电容器
- 过流和过热保护
- 100% 占空比模式
- 精密使能输入
- 电源正常状态输出
- 与 TPS629206-Q1 和 TPS629203-Q1 器件引脚对引脚兼容
- 0.5mm 间距、8 引脚 SOT-5X3 封装



2 应用

- 高级驾驶辅助系统 (ADAS)
- 汽车信息娱乐系统与仪表组
- 汽车车身电子装置和照明
- 混合动力、电动和动力总成系统

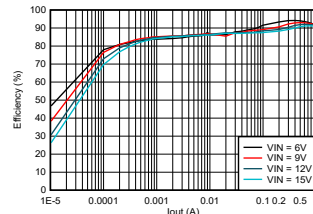
3 说明

符合汽车标准的 TPS6292xx-Q1 系列器件是高效、小巧、高度灵活且易于使用的同步降压直流/直流转换器。3V 至 17V 的宽输入电压范围支持各种由 12V、5V 或 3.3V 电源轨或者单节或多节锂离子电池供电的系统。可将 TPS629210-Q1 配置为以强制 PWM 模式或可变频率 (自动 PFM) 模式在 2.5 MHz 或 1 MHz 频率下运行。在自动 PFM 模式下, 器件在轻负载时自动转换为省电模式, 以保持高效率。此外, 借助 4 μA 的低典型静态电流, 可在极小的负载下实现高效率。TI 的自动效率增强 (AEE) 模式可根据输入和输出电压自动调整开关频率, 从而无需使用不同的电感器即可在整个工作范围内保持高转换效率。除选择开关频率的行为之外, MODE/S-CONF 输入引脚还可用于在外部和内部反馈分压器和启用/禁用输出电压放电功能的不同组合之间进行选择。在内部反馈配置中, FB/VSET 引脚和 GND 之间的电阻器可用于在 18 种不同的输出电压选项之间进行选择 (请参阅表 8-2)。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
TPS629210-Q1	DRL (SOT-5X3, 8)	1.60mm × 2.10mm (包括引脚)
TPS629210-Q1	DYC (SOT-5X3, 8)	1.60mm × 2.10mm (包括引脚)

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



效率与输出电流间的关系 (频率为 2.5MHz, $V_{\text{OUT}} = 3.3\text{V}$, 自动 PFM/PWM)



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (December 2021) to Revision C (March 2023)	Page
• 添加了 DYC 封装.....	1
• Added the DYC package.....	3
• Added the DYC package.....	3
• Added the DYC package.....	41

Changes from Revision A (September 2021) to Revision B (December 2021)	Page
• 将器件状态从“预告信息”更改为“量产数据”.....	1

5 Device Comparison Table

Device Number	Output Current	Input Voltage	Operating Temperature Range	Switching Frequency	PWM Mode	V _O Adjust	Package Options
TPS629203-Q1	0 A - 0.3 A	3 V - 17 V	- 40°C to 150°C	Selectable 1-MHz or 2.5-MHz options	Selectable auto PWM/PFM or forced PWM	Externally programmable or 18 internal options	DRL
TPS629206-Q1	0 A - 0.6 A						DRL and DYC
TPS629210-Q1	0 A - 1 A						

6 Pin Configuration and Functions

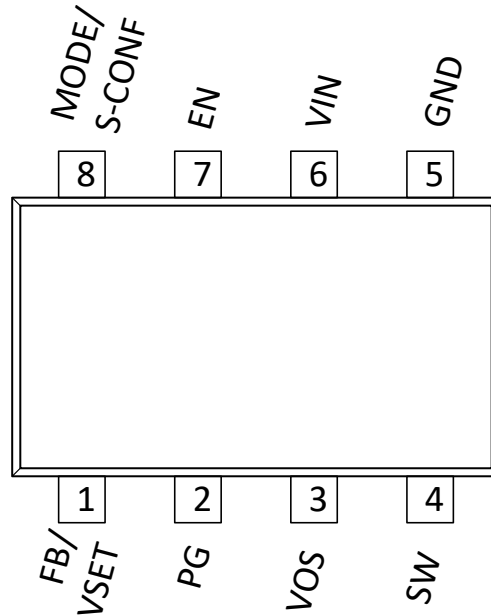


图 6-1. TPS629210-Q1 8-Pin DRL SOT-5X3 Pinout (TOP)

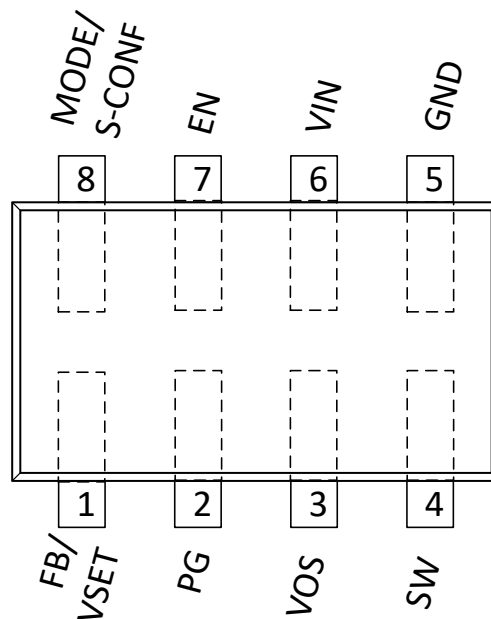


图 6-2. TPS629210-Q1 8-Pin DYC SOT-5X3 Pinout (TOP)

表 6-1. Pin Functions

Pin		I/O	Description
Name	NO.		
FB/VSET	1	I	Dependent upon device configuration (see 节 8.3.1) <ul style="list-style-type: none"> • FB: Voltage feedback input. Connect a resistive output voltage divider to this pin. • VSET: Output voltage setting pin. Connect a resistor to GND to choose the output voltage according to 表 8-2.
PG	2	O	Open-drain power-good output
VOS	3	I	Output voltage sense pin. Connect directly to the positive pin of the output capacitor.
SW	4		Switch pin of the converter. Connected to the internal power switches
GND	5		Ground pin
VIN	6	I	Power supply input. Make sure the input capacitor is connected as close as possible between the VIN pin and GND.
EN	7	I	Enable/disable pin including a threshold comparator. Connect to logic low to disable the device. Pull high to enable the device. Do not leave this pin unconnected.
MODE/S-CONF	8	I	Device mode selection (auto PFM/PWM or forced PWM operation) and Smart-CONFIG pin. Connect a resistor to configure the device according to 表 8-1 .

7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage ⁽²⁾	VIN, EN, PG, MODE/S-CONF	-0.3	18	V
Voltage ⁽²⁾	SW ⁽³⁾	-0.3	V _{IN} + 0.3	V
Voltage ⁽²⁾	SW (AC, less than 10ns) ⁽³⁾	-3.0	23	V
Voltage ⁽²⁾	FB/VSET, VOS	-0.3	6	V
Current	PG		10	mA
T _{stg}	Storage temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to network ground terminal.
- (3) While switching.

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD classification level 2	±2000	V
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C4B	±750	V

- (1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _I	Input voltage range	3.0		17	V
V _O	Output voltage range	0.4		5.5	V
C _I	Effective input capacitance	3	4.7		µF
C _O	Effective output capacitance ⁽¹⁾	10	22	100	µF
L	Output inductance ⁽²⁾	1.0 ⁽³⁾	2.2	4.7 ⁽⁴⁾	µH
I _{OUT}	Output current	0		1	A
I _{SINK_PG}	Sink current at PG-Pin			1	mA
T _J	Junction temperature ⁽⁵⁾	-40		150	°C

- (1) This is for capacitors directly at the output of the device. More capacitance is allowed if there is a series resistance associated to the capacitor.
- (2) Nominal inductance value.
- (3) Not recommended for 1 MHz operation
- (4) Larger values of inductance may be used to reduce the ripple current, but they may have a negative impact on efficiency and the overall transient response.
- (5) Operating lifetime is derated at junction temperatures greater than 150°C.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS629210-Q1		UNIT
		SOT583 8-Pin (DRL)		
		JEDEC PCB	TPS6292xx EVM	
R _{θJA}	Junction-to-ambient thermal resistance	120	60	°C/W

THERMAL METRIC ⁽¹⁾		TPS629210-Q1		UNIT
		SOT583 8-Pin (DRL)		
		JEDEC PCB	TPS6292xx EVM	
$R_{\theta_{JC(top)}}$	Junction-to-case (top) thermal resistance	45	n/a	°C/W
$R_{\theta_{JB}}$	Junction-to-board thermal resistance	25	n/a	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1	n/a	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Thermal Information - DYC Package

THERMAL METRIC ⁽¹⁾		TPS629210-Q1		UNIT
		SOT583 8-Pin (DYC)		
		JEDEC PCB	TPS6292xx DYC EVM	
$R_{\theta_{JA}}$	Junction-to-ambient thermal resistance	105	55	°C/W
$R_{\theta_{JC(top)}}$	Junction-to-case (top) thermal resistance	45	n/a	°C/W
$R_{\theta_{JB}}$	Junction-to-board thermal resistance	22	n/a	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1	n/a	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	18	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.6 Electrical Characteristics

$V_I = 3\text{ V to }17\text{ V}$, $T_J = -40\text{ °C to }+150\text{ °C}$, Typical values at $V_I = 12\text{ V}$ and $T_A = 25\text{ °C}$, unless otherwise noted

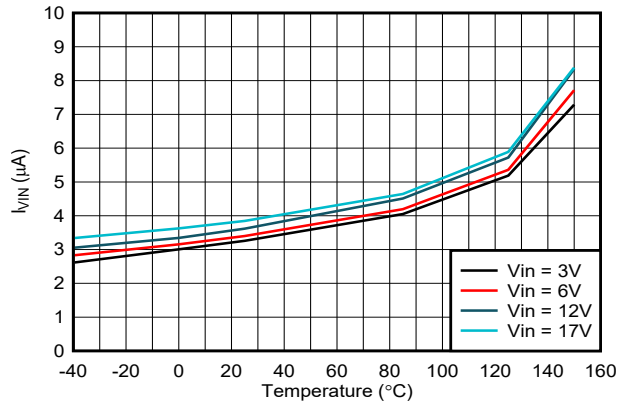
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Operating Quiescent Current, (Power Save Mode)	Iout = 0 mA, device not switching		4		μA
$I_{Q,PWM}$	Operating Quiescent Current (PWM Mode)	VIN=12V, VOUT=1.2V; Iout = 0 mA, device switching		5		mA
I_{SD}	Shutdown current into VIN pin	EN = 0 V		0.25	3	μA
V_{UVLO}	Under Voltage Lock-Out	VIN rising	2.85	2.95	3.0	V
	Under Voltage Lock-Out	VIN falling	2.65	2.75	2.85	V
V_{UVLO}	Under Voltage Lock-Out Hysteresis			200		mV
CONTROL & INTERFACE						
I_{LKG}	EN Input leakage current	EN=VIN		3	300	nA
$V_{IH,MODE}$	High-Level Input Voltage at MODE/S-CONF Pin		1.0			V
$V_{IL,MODE}$	Low-level input voltage at MODE/S-CONF Pin				0.15	V
V_{IH}	High-level input voltage at EN-Pin		0.97	1.0	1.03	V
V_{IL}	Low-level input voltage at EN-Pin		0.87	0.9	0.93	V
V_{PG}	Power good threshold	VFB rising, referenced to VFB nominal	93%	96%	99%	
		VFB falling, referenced to VFB nominal	89%	93%	96%	
$V_{PG,HYS}$	Power good threshold hysteresis	hysteresis		3%		
$t_{PG,DLY}$	Power good delay time			32		μs
$t_{PG,DLY}$	Power good pull down resistance			10		Ω
$V_{PG,OL}$	Low-level output voltage at PG pin	ISINK = 1 mA			0.1	V

7.6 Electrical Characteristics (continued)

$V_I = 3\text{ V to }17\text{ V}$, $T_J = -40\text{ }^\circ\text{C to }+150\text{ }^\circ\text{C}$, Typical values at $V_I = 12\text{ V}$ and $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{PG,LKG}$	Input leakage current into PG pin	$V_{PG} = 5\text{ V}$		0.01	1	μA
POWER SWITCHES						
$R_{DS,ON}$	High-side FET on resistance			250		$\text{m}\Omega$
	Low-side FET on resistance			85		
I_{LIM}	High-side FET current limit		1.5	1.8	2.1	A
	Low-side FET current limit		1.3	1.6	1.9	A
$I_{LIM,SINK}$	Low-side FET sink current limit		0.8	1	1.2	A
T_{SD}	Thermal Shutdown Threshold	T_J rising		170		$^\circ\text{C}$
	Thermal Shutdown Hysteresis	T_J falling		20		
f_{SW}	Switching frequency	2.5-MHz selection (FPWM Mode)		2.5		MHz
f_{SW}	Switching frequency	1.0-MHz selection (FPWM Mode)		1.0		MHz
$T_{ON(MIN)}$	Minimum On-time			40		ns
$I_{LKG,SW}$	Leakage current into SW-Pin	$EN = 0\text{V}$, $V_{SW} = V_{OS} = 5.5\text{V}$		0.1	5	μA
OUTPUT						
V_O	Output Voltage Regulation	VSET Configuration selected, $0^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$	-1%		+1%	
V_O	Output Voltage Regulation	VSET Configuration selected, $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$ (DRL Package)	-1.4%		+1.1%	
V_O	Output Voltage Regulation	VSET Configuration selected, $V_{OUT} \leq 3.8\text{V}$, $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$ (DYC Package)	-1.4%		+1.1%	
V_O	Output Voltage Regulation	VSET Configuration selected, $V_{OUT} \geq 5.0\text{V}$, $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$ (DYC Package)	-1.6%		+1.1%	
V_{FB}	Feedback Regulation Voltage	Adjustable Configuration selected		0.6		V
V_{FB}	Feedback Voltage Regulation	FB-Option selected, $0^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$	-0.75%		+0.75%	
V_{FB}	Feedback Voltage Regulation	FB-Option selected, $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$	-1.2%		+0.75%	
I_{FB}	Input leakage current into FB pin	Adjustable configuration, $V_{FB} = 0.6\text{ V}$		1	100	nA
T_{delay}	Start-up delay time	$I_O = 0\text{ mA}$, time from EN rising edge until start switching, External FB Configuration selected		700	1500	μs
	Start-up delay time	$I_O = 0\text{ mA}$, time from EN rising edge until start switching, VSET Configuration selected		1000	1800	μs
T_{SS}	Soft-Start time	$I_O = 0\text{ mA}$ after T_{delay} , from 1 st switching pulse until target V_O		600	700	μs
R_{DISCH}	Active Discharge Resistance	Discharge = ON - Option Selected, EN = LOW,		7.5	20	Ω

7.7 Typical Characteristics



Measured with the device not switching

图 7-1. Typical Quiescent Current vs Temperature

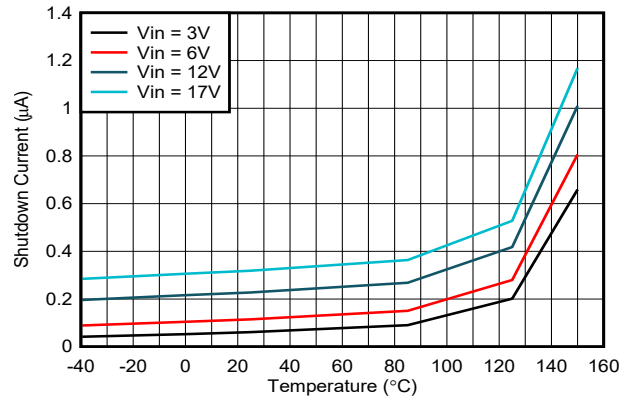


图 7-2. Typical Shutdown Current vs Temperature

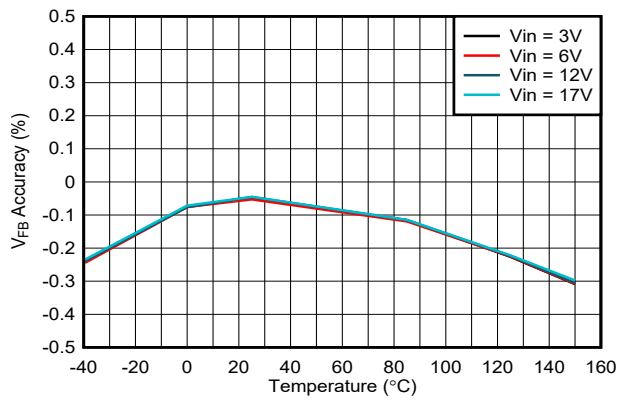


图 7-3. Output Voltage Accuracy - External Feedback

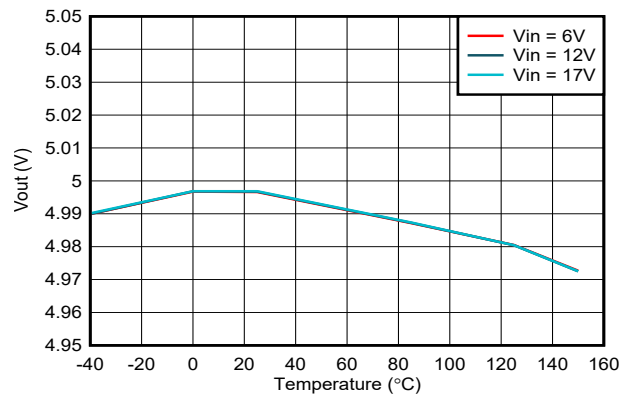


图 7-4. Output Voltage Accuracy - VSET Selected

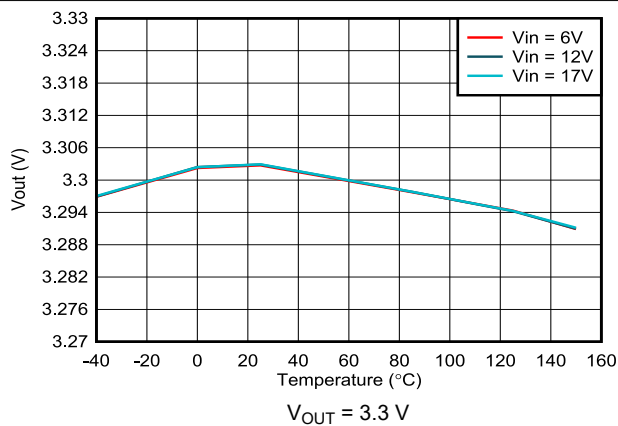


图 7-5. Output Voltage Accuracy - VSET Selected

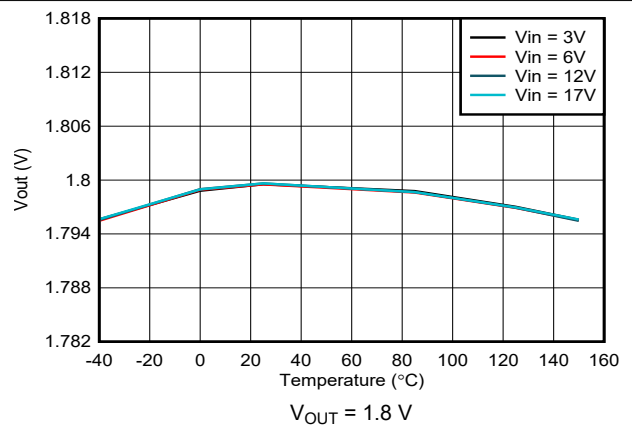


图 7-6. Output Voltage Accuracy - VSET Selected

7.7 Typical Characteristics (continued)

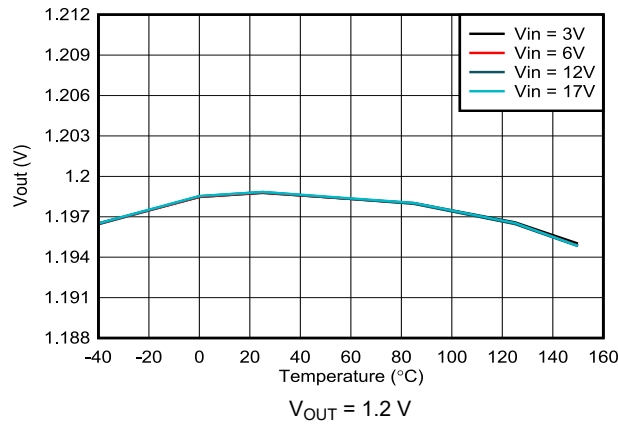


图 7-7. Output Voltage Accuracy - VSET Selected

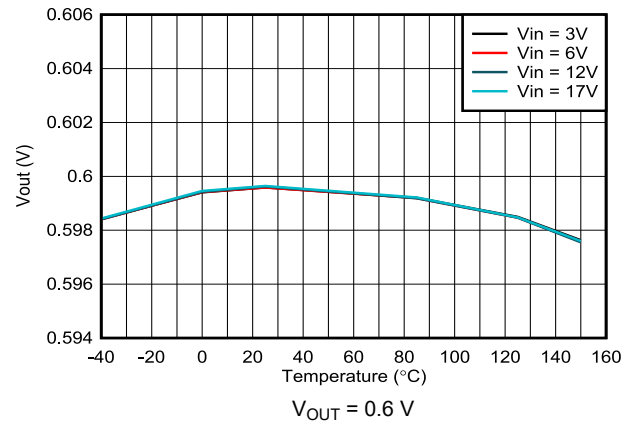


图 7-8. Output Voltage Accuracy - VSET Selected

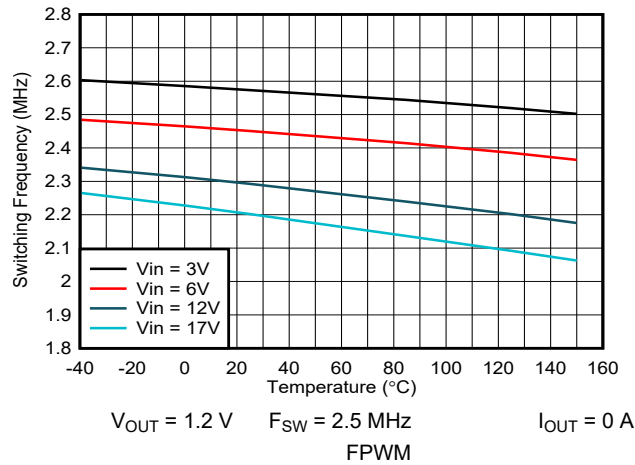


图 7-9. Switching Frequency vs Temperature

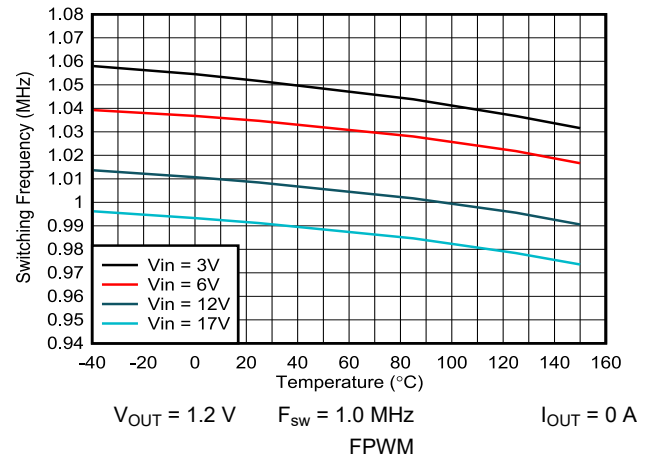


图 7-10. Switching Frequency vs Temperature

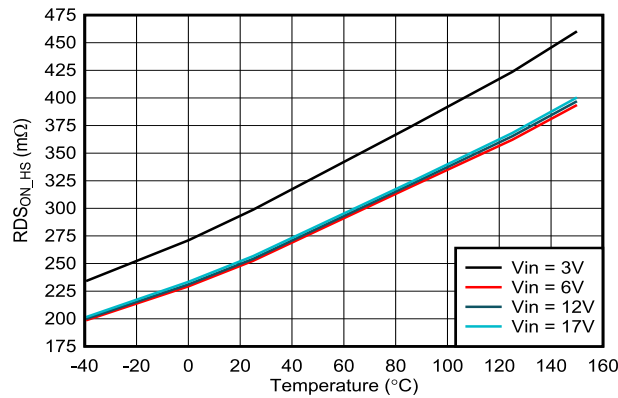


图 7-11. High-Side RDS_{ON} vs Temperature

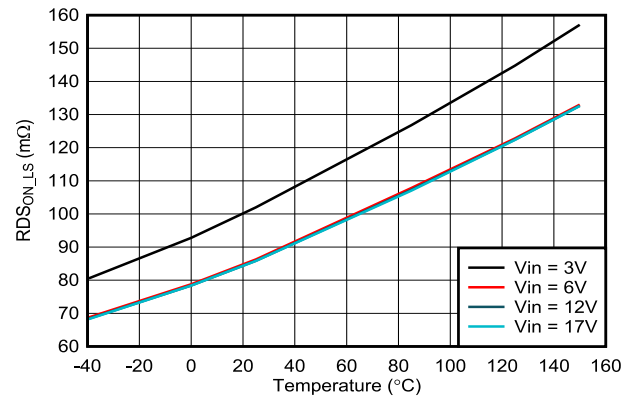


图 7-12. Low-Side RDS_{ON} vs Temperature

7.7 Typical Characteristics (continued)

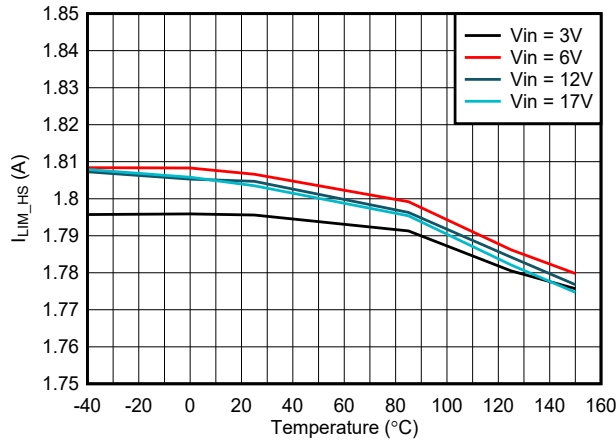


图 7-13. High-Side I_{LIM} vs Temperature

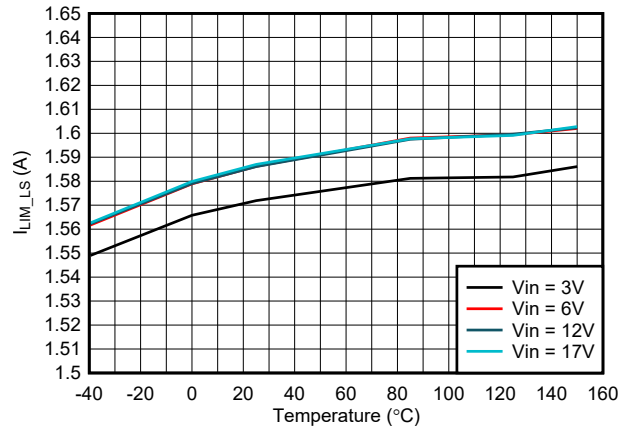


图 7-14. Low-Side I_{LIM} vs Temperature

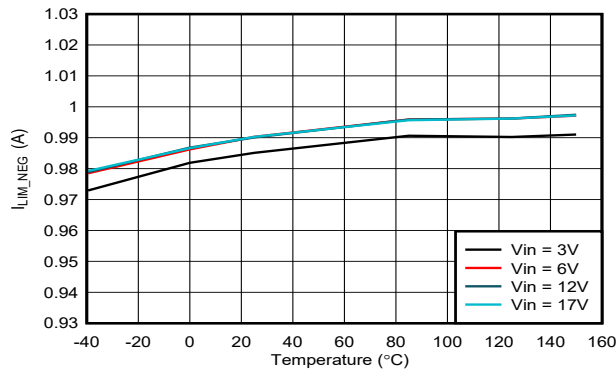


图 7-15. Low-Side I_{NEG} vs Temperature

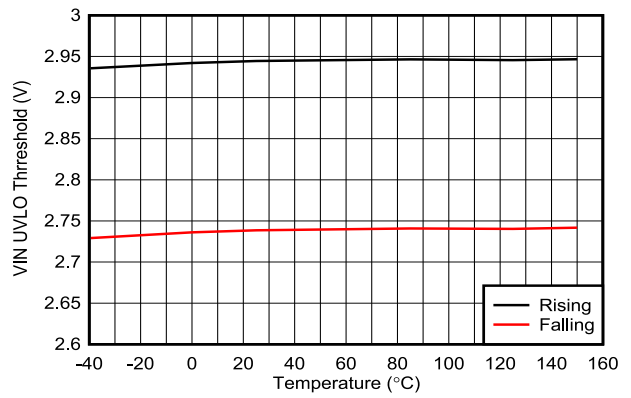


图 7-16. V_{IN} UVLO Thresholds vs Temperature

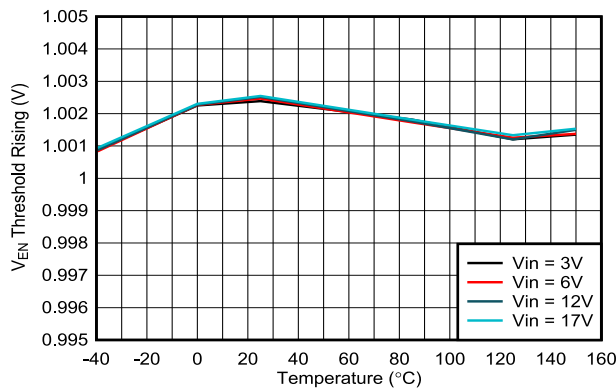


图 7-17. Precision Enable Threshold vs Temperature

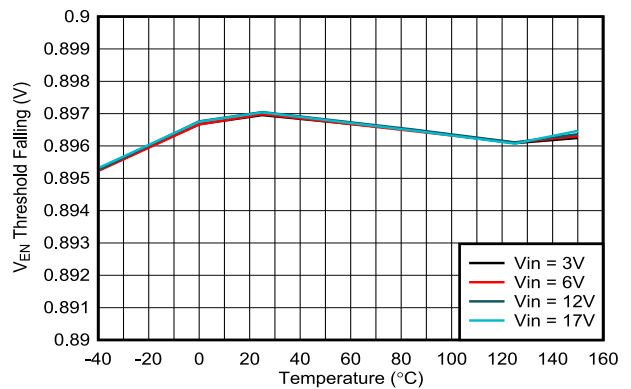


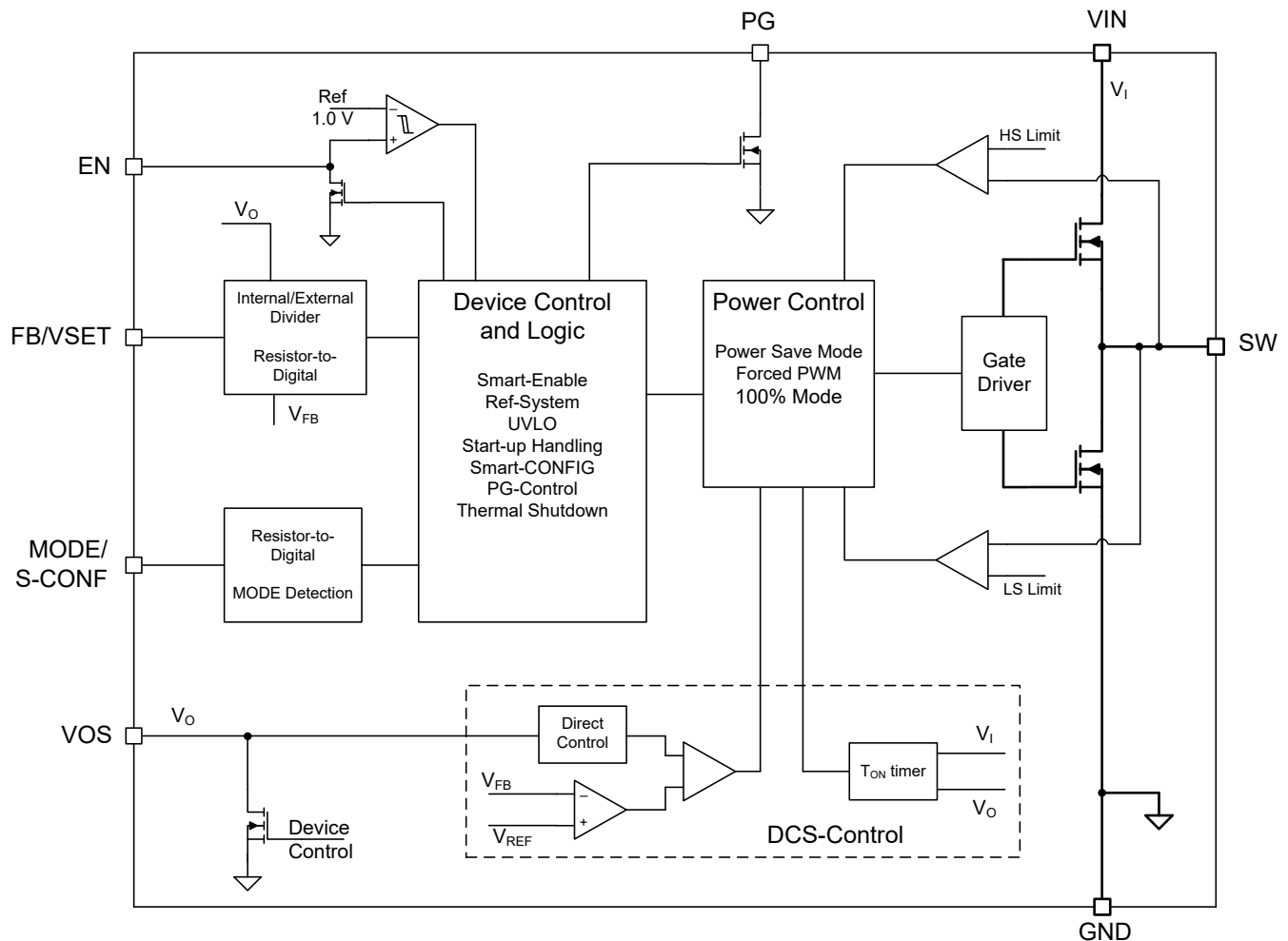
图 7-18. Precision Enable Threshold vs Temperature

8 Detailed Description

8.1 Overview

The TPS629210-Q1 synchronous switched mode power converter is based on DCS-Control (Direct Control with Seamless Transition into power save mode), an advanced regulation topology that combines the advantages of hysteretic, voltage mode, and current mode control. This control loop takes information about output voltage changes and feeds it directly to a fast comparator stage, and sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To get accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low-ESR capacitors.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Mode Selection and Device Configuration (MODE/S-CONF Pin)

The MODE/S-CONF pin is an input with two functions, which can be used to customize the device behavior in two ways:

- Select the device mode (forced PWM or auto PFM/PWM operation) traditionally with a HIGH or LOW level.
- Select the device configuration (switching frequency, internal and external feedback, output discharge, and PFM/PWM mode) by connecting a single resistor to this pin.

The device interprets this pin during its start-up sequence after the internal OTP readout and before it starts switching in soft start. If the device reads a HIGH or LOW level, dynamic mode change is active and PFM/PWM mode can be changed during operation. If the device reads a resistor value, there is no further interpretation during operation and the device mode or other configurations cannot be changed afterward.

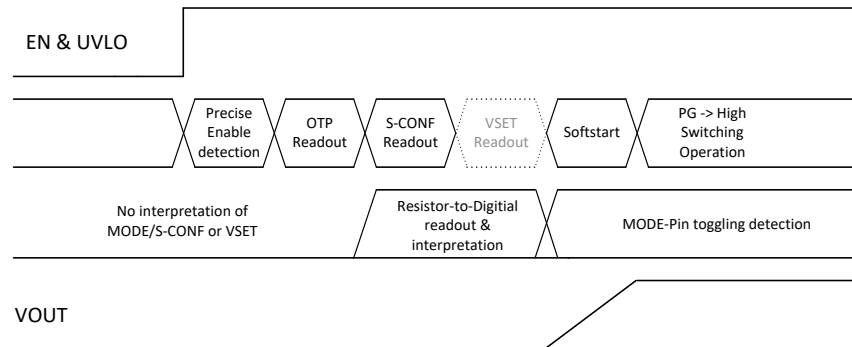


图 8-1. Interpretation of S-CONF and VSET Flow

表 8-1. Smart-CONFIG Setting Table

#	M ODE/S-CONF Level Or Resistor Value [Ω] ⁽¹⁾	FB/VSET Pin	F _{sw} (MHz)	Output Discharge	Mode (Auto Or Forced PWM)	Dynamic Mode Change
Setting Options by Level						
1	GND	external FB	up to 2.5 ⁽²⁾	yes	Auto PFM/PWM with AEE	Active
2	HIGH (> 1.8 V)	external FB	2.5	yes	Forced PWM	
Setting Options by Resistor						
3	7.50 k	external FB	up to 2.5 ⁽²⁾	no	Auto PFM/PWM with AEE	not active
4	9.31 k	external FB	2.5	no	Forced PWM	
5	11.50 k	external FB	1	yes	Auto PFM/PWM	
6	14.30 k	external FB	1	yes	Forced PWM	
7	17.80 k	external FB	1	no	Auto PFM/PWM	
8	22.10 k	external FB	1	no	Forced PWM	
9	27.40 k	VSET	up to 2.5 ⁽²⁾	yes	Auto PFM/PWM with AEE	
10	34.00 k	VSET	2.5	yes	Forced PWM	
11	42.20 k	VSET	up to 2.5 ⁽²⁾	no	Auto PFM/PWM with AEE	
12	52.30 k	VSET	2.5	no	Forced PWM	
13	64.90 k	VSET	1	yes	Auto PFM/PWM	
14	80.60 k	VSET	1	yes	Forced PWM	
15	100.00 k	VSET	1	no	Auto PFM/PWM	
16	124.00 k	VSET	1	no	Forced PWM	

(1) E96 Resistor Series, 1% accuracy, temperature coefficient better or equal than ± 200 ppm/ $^{\circ}$ C

(2) F_{sw} varies based on V_{IN} and V_{OUT}. See 节 8.4.3 for more details.

8.3.2 Adjustable V_O Operation (External Voltage Divider)

If the device is configured to operate in classical adjustable V_O operation, the FB/VSET pin is used as the feedback pin and must sense V_O through an external divider network. 图 8-2 shows the typical schematic for this configuration.

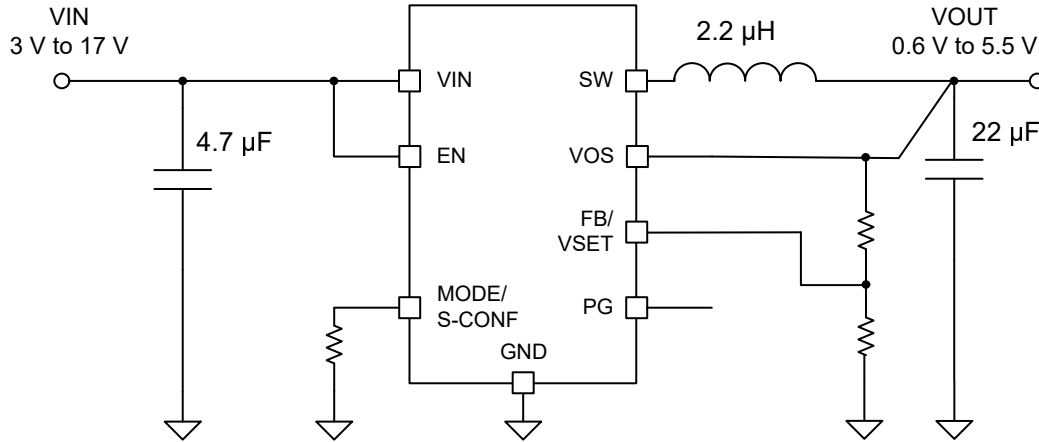


图 8-2. Adjustable V_O Operation Schematic

8.3.3 Selectable V_O Operation (VSET and Internal Voltage Divider)

If the device is configured to VSET operation, the device interprets the VSET pin value following the MODE/S-CONF readout (see 图 8-3). There is no further interpretation of the VSET pin during operation and the output voltage cannot be changed afterward without toggling the EN pin.

图 8-3 shows the typical schematic for this configuration, where V_O is directly sensed at the VOS pin of the device. V_O is sensed only through the VOS pin by an internal resistor divider. The target V_O is programmed by an external resistor connected between VSET and GND (see 表 8-2).

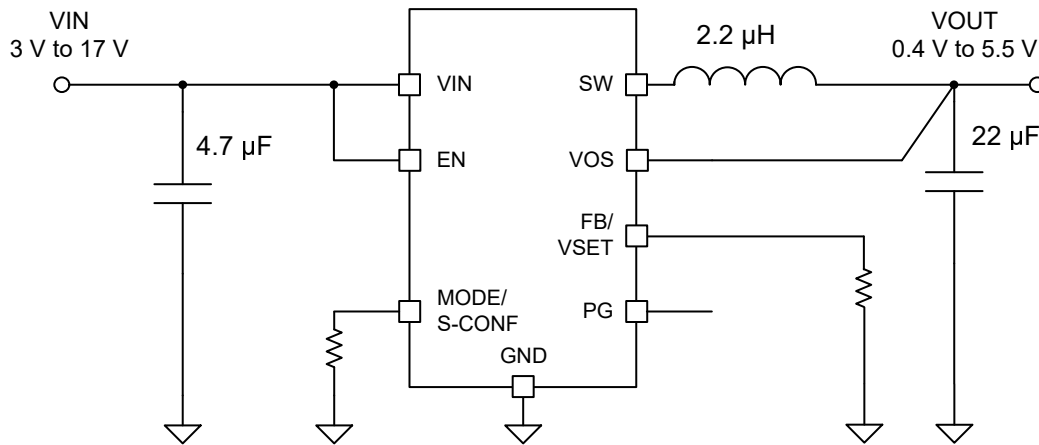


图 8-3. Selectable V_O Operation Schematic

表 8-2. VSET Selection Table

VSET #	Resistor Value [Ω] ⁽¹⁾	Target V _O [V]
1	GND	1.2
2	4.87 k	0.4
3	6.04 k	0.6
4	7.50 k	0.8
5	9.31 k	0.85
6	11.50 k	1.0
7	14.30 k	1.1
8	17.80 k	1.25
9	22.10 k	1.3
10	27.40 k	1.35
11	34.00 k	1.8
12	42.20 k	1.9
13	52.30 k	2.5
14	64.90 k	3.8
15	80.60 k	5.0
16	100.00 k	5.1
17	124.00 k	5.5
18	249.00 k or larger/open	3.3

(1) E96 Resistor Series, 1% accuracy, temperature coefficient better or equal to ± 200 ppm/ $^{\circ}$ C

8.3.4 Smart Enable with Precise Threshold

The voltage applied at the EN pin of the TPS629210-Q1 is compared to a fixed threshold rising voltage. This allows the user to drive the pin by a slowly changing voltage and enables the use of an external RC network to achieve a power-up delay.

The precise enable input allows the use of a user-programmable undervoltage lockout by adding a resistor divider to the input of the EN pin.

The enable input threshold for a falling edge is lower than the rising edge threshold. The TPS629210-Q1 starts operation when the rising threshold is exceeded. For proper operation, the EN pin must be terminated and must not be left floating. Pulling the EN pin low forces the device into shutdown. In this mode, the internal high-side and low-side MOSFETs are turned off and the entire internal control circuitry is switched off.

An internal resistor pulls the EN pin to GND and avoids the pin to be floating. This prevents an uncontrolled start-up of the device in case the EN pin cannot be driven to a low level safely. With EN low, the device is in shutdown mode. The device is turned on with EN set to a high level. The pulldown control circuit disconnects the pulldown resistor on the EN pin after the internal control logic and the reference have been powered up. With EN set to a low level, the device enters shutdown mode and the pulldown resistor is activated again.

8.3.5 Power Good (PG)

The TPS629210-Q1 has a built-in power-good (PG) feature to indicate whether the output voltage has reached its target and the device is ready. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor to any voltage up to the recommended input voltage level. PG is low when the device is turned off due to EN, UVLO (undervoltage lockout), or thermal shutdown. V_{IN} must remain present for the PG pin to stay low.

If the power-good output is not used, it is recommended to tie to GND or leave open.

表 8-3. Power-Good Indicator Functional Table

Logic Signals				PG Status
V_I	EN Pin	Thermal Shutdown	V_O	
$V_{VIN} > UVLO$	HIGH	No	V_O on target	High Impedance
			$V_O < target$	LOW
		Yes	x	LOW
	LOW	x	x	LOW
$1.8 V < V_{VIN} < UVLO$	x	x	x	LOW
$V_I < 1.8 V$	x	x	x	Undefined

8.3.6 Output Discharge Function

The purpose of the discharge function is to make sure there is a defined down-ramp of the output voltage when the device is being disabled but also to keep the output voltage close to 0 V when the device is off. The output discharge feature is only active after the TPS629210-Q1 has been enabled at least after since the supply voltage was applied. The internal discharge resistor is connected to the VOS pin. The discharge function is enabled as soon as the device is disabled (EN pin = low), in thermal shutdown, or in undervoltage lockout. The minimum supply voltage required for the discharge function to remain active typically is 2 V.

8.3.7 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents mis-operation of the device by switching off both the power FETs. The device is fully operational for voltages above the rising UVLO threshold and turns off if the input voltage trips below the threshold for a falling supply voltage.

8.3.8 Current Limit and Short Circuit Protection

The TPS629210-Q1 is protected against overload and short circuit events. If the inductor current exceeds the current limit, I_{LIM_HS} , the high-side switch is turned off and the low-side switch is turned on to ramp down the inductor current. The high-side FET turns on again only if the current in the low-side FET has decreased below the low-side current limit threshold, I_{LIM_LS} .

Due to internal propagation delay, the actual current can exceed the static current limit during that time. The dynamic current limit is given in [方程式 1](#).

$$I_{peak(typ)} = I_{LIMH} + \frac{V_L}{L} \times t_{pd} \quad (1)$$

where:

- I_{LIMH} is the static current limit as specified in the electrical characteristics.
- L is the effective inductance at the peak current.
- V_L is the voltage across the inductor ($V_{IN} - V_{OUT}$).
- t_{PD} is the internal propagation delay of typically 50 ns.

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. The dynamic high-side switch peak current can be calculated as follows:

$$I_{peak(typ)} = I_{LIMH} + \frac{V_{IN} - V_{OUT}}{L} \times 50ns \quad (2)$$

The TPS629210-Q1 also includes a low-side negative current limit ($I_{LIM:SINK}$) to protect against excessive negative currents that can occur in forced PWM mode under heavy to light load transient conditions. If the negative current in the low-side switch exceeds the $I_{LIM:SINK}$ threshold, the low-side switch is disabled. Both the low-side and high-side switches remain off until an internal timer re-enables the high-side switch based on the selected PWM switching frequency.

CAUTION

TI recommends that the inductor be sized such that the inductor ripple current, ΔI_L (see [方程式 9](#)), does not exceed 1.6 A to avoid the potential for continuous operation of the negative current limit with no output load ($I_O = 0$ A).

8.3.9 Thermal Shutdown

The junction temperature of the device, T_J , is monitored by an internal temperature sensor. If T_J rises and exceeds the thermal shutdown threshold, T_{SD} , the device shuts down. Both the high-side and low-side power FETs are turned off and PG goes low. When T_J decreases below the hysteresis, the converter resumes normal operation, beginning with soft start. During a PFM skip pause, the thermal shutdown feature is not active. A shutdown or restart is only triggered during a switching cycle. See [节 8.4.2](#).

8.4 Device Functional Modes

8.4.1 Forced Pulse Width Modulation (PWM) Operation

The TPS629210-Q1 has two operating modes: forced PWM mode discussed in this section and auto PFM/PWM mode as discussed in [节 8.4.2](#).

With the MODE/S-CONF pin set to forced PWM mode, the device operates with pulse width modulation in continuous conduction mode (CCM) with a nominal switching frequency of either 1.0 MHz or 2.5 MHz. The frequency variation in PWM is controlled and depends on V_{IN} , V_{OUT} , and the inductance. The on time in forced PWM mode is given by [方程式 3](#).

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} \quad (3)$$

For very small output voltages, an absolute minimum on time of approximately 40 ns is kept to limit switching losses. The operating frequency is thereby reduced from its nominal value, which keeps efficiency high.

8.4.2 Power Save Mode Operation (Auto PFM/PWM)

When the MODE/S-CONF pin is configured for auto PFM/PWM mode, power save mode is allowed. The device operates in PWM mode as long the output current is higher than half the ripple current of the inductor. To maintain high efficiency at light loads, the device enters power save mode at the boundary to discontinuous conduction mode (DCM). This happens if the output current becomes smaller than half the ripple current of the inductor. Power save mode is entered seamlessly to make sure there is high efficiency in light-load operation. The device remains in power save mode as long as the inductor current is discontinuous.

In power save mode, the switching frequency decreases linearly with the load current maintaining high efficiency. The transition into and out of power save mode is seamless in both directions.

The TPS629210-Q1 adjusts the on time (TON) in power save mode, depending on the input voltage and the output voltage to maintain highest efficiency. The on time in steady-state operation can be estimated as:

With the MODE/S-CONF pin set to 1.0-MHz operation:

$$T_{ON} (\mu s) = \frac{V_{OUT}}{V_{IN}} \quad (4)$$

With the MODE/S-CONF pin set to 2.5-MHz operation:

$$T_{ON} (ns) = 100 \times \frac{V_{IN}}{V_{IN} - V_{OUT}} \quad (5)$$

Using TON, the typical peak inductor current in power save mode is approximated by:

$$ILPSM_{peak} = \frac{V_{IN} - V_{OUT}}{L} \times T_{ON} \quad (6)$$

The output voltage ripple in power save mode is given by [方程式 7](#):

$$\Delta V = \frac{L \times V_{IN}^2}{200 \times C} + \left(\frac{1}{V_{IN} - V_{OUT}} + \frac{1}{V_{OUT}} \right) \quad (7)$$

备注

When V_{IN} decreases to typically 15% above V_{OUT} , the device does not enter power save mode regardless of the load current. The device maintains output regulation in PWM mode.

8.4.3 AEE (Automatic Efficiency Enhancement)

When the MODE/S-CONF pin is configured for auto PFM/PWM with AEE mode, the TPS629210-Q1 provides the highest efficiency over the entire input voltage and output voltage range by automatically adjusting the switching frequency of the converter (see [方程式 8](#)). To keep the efficiency high over the entire duty cycle range, the switching frequency is adjusted while maintaining the ripple current amplitudes. This feature compensates for the very small duty cycles of high V_{IN} to low V_{OUT} conversions, which can limit the control range in other topologies.

$$F_{SW} (MHz) = 10 \times V_{OUT} \times \frac{V_{IN} - V_{OUT}}{V_{IN}^2} \quad (8)$$

Traditionally, the efficiency of a switched mode converter decreases if V_{OUT} decreases, V_{IN} increases, or both. By decreasing the switching losses at lower V_{OUT} values or higher V_{IN} values, the AEE feature provides an efficiency enhancement across various duty cycles, especially for the lower V_{OUT} values, where fixed frequency converters suffer from a significant efficiency drop. Furthermore, when used with the recommended 2.2- μ H

inductor, the ripple current amplitudes remains low enough to deliver the full output current without reaching current limit across the entire range of input and output voltages (see 图 8-4).

By using the same TON configuration (see 方程式 9) across the entire load range in AEE mode, the inductor ripple current in AEE mode becomes effectively independent of the output voltage and can be approximated by 方程式 9:

$$\Delta I_L (\text{mA}) = T_{ON} \times \frac{V_{IN} - V_{OUT}}{L} = 0.1 \times \frac{V_{IN} (\text{V})}{L (\mu\text{H})} \quad (9)$$

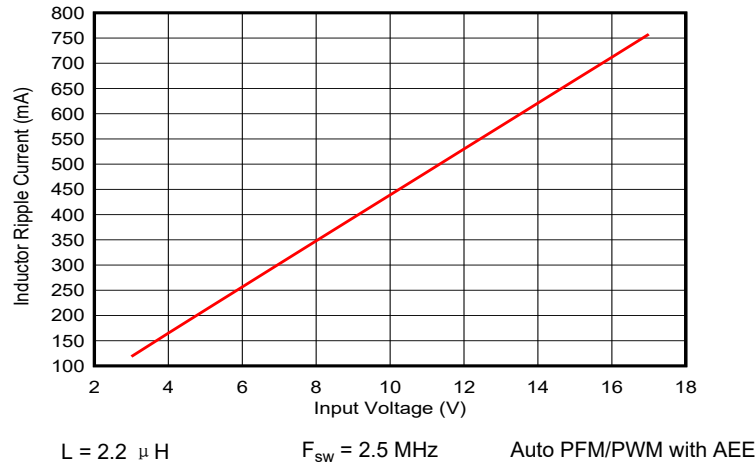


图 8-4. Typical Inductor Ripple Current Versus Input Voltage in AEE Mode

The TPS629210-Q1 operates in AEE mode as long as the output current is higher than half the ripple current of the inductor. To maintain high efficiency at light loads, the device enters power save mode at the boundary to discontinuous mode (DCM), which happens when the output current becomes smaller than half the inductor ripple current.

8.4.4 100% Duty-Cycle Operation

The duty cycle of the buck converter operated in PWM mode is given in 方程式 10.

$$D = \frac{V_{OUT}}{V_{IN}} \quad (10)$$

The duty cycle increases as the input voltage comes close to the output voltage and the off time of the high-side switch gets smaller. When the minimum off time of typically 80 ns is reached, the TPS629210-Q1 scales down its switching frequency while it approaches 100% mode. In 100% mode, the device keeps the high-side switch on continuously as long as the output voltage is below the internal set point. This allows the conversion of small input to output voltage differences. For example, getting the longest operation time of battery-powered applications. In 100% duty cycle mode, the low-side FET is switched off.

The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, can be calculated as:

$$V_{IN (MIN)} = V_{OUT} + I_{OUT} \times (R_{DS(ON)} + R_L) \quad (11)$$

where:

- I_{OUT} is the output current.
- $R_{DS(on)}$ is the on-state resistance of the high-side FET.
- R_L is the DC resistance of the inductor used.

8.4.5 Starting into a Prebiased Load

The TPS629210-Q1 is capable of starting into a prebiased output. The device only starts switching when the internal soft-start ramp is equal or higher than the feedback voltage. If the voltage at the feedback pin is biased to a higher voltage than the nominal value, the TPS629210-Q1 does not start switching unless the voltage at the feedback pin drops to the target. Performance is the same for devices configured for VSET operation (internal feedback), however, the switching is delayed until the soft-start ramp reaches the internal feedback voltage.

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS629210-Q1 device is a highly efficient, small, and highly-flexible synchronous step-down DC-DC converter that is easy to use. A wide input voltage range of 3 V to 17 V supports a wide variety of inputs like 12-V supply rails, single-cell or multi-cell Li-Ion, and 5-V or 3.3-V rails.

9.2 Typical Application

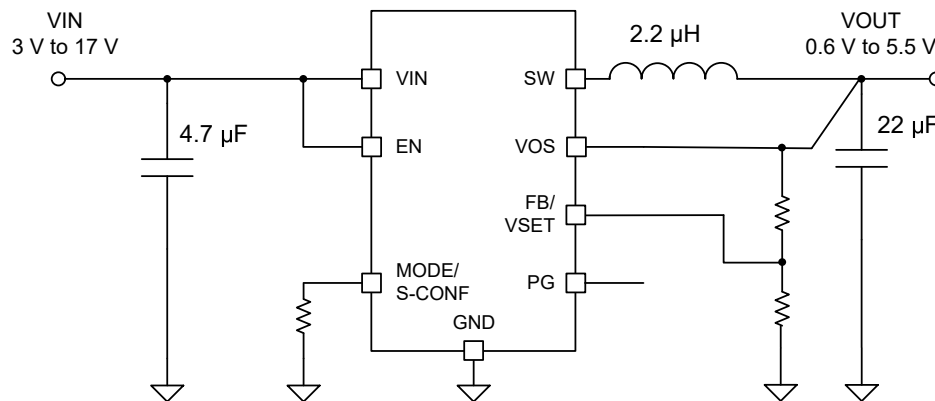


图 9-1. Typical Application Setup

表 9-1. List of Components

Reference	Description	Manufacturer
IC	17-V, 1-A Step-Down Converter	TPS629210-Q1; Texas Instruments
L1	2.2-µH inductor	XGL3530-222; Coilcraft
C1	4.7 µF, 25 V, Ceramic, 1206	CGA5L1X7R1E475K160AC, TDK
C2	22 µF, 6.3 V, Ceramic, 0805	GCM21BD70J226ME36L, MuRata
R1	Depending on V_{OUT} ; see 节 9.2.2.2 .	Standard 1% metal film
R2	Depending on V_{OUT} ; see 节 9.2.2.2 .	Standard 1% metal film
R3	Depending on device setting, see 节 8.3.1 .	Standard 1% metal film

9.2.1 Design Requirements

The design guidelines provide a component selection to operate the device within the recommended operating conditions.

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the TPS629210-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Programming the Output Voltage

The output voltage of the TPS629210-Q1 is adjustable and can be programmed for output voltages from 0.6 V to 5.5 V, using a resistor divider from VOUT to GND. The voltage at the FB pin is regulated to 600 mV. The value of the output voltage is set by the selection of the resistor divider from [表 9-2](#). TI recommends to size R2 to be less than 300 k Ω to allow for a feedback current of at least 2 μ A. Lower resistor values are recommended for highest accuracy and most robust design.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (12)$$

where

- VFB is 0.6 V.

表 9-2. Setting the Output Voltage

Nominal Output Voltage	R1	R2	Exact Output Voltage
0.8 V	51 k Ω	150 k Ω	0.804 V
1.2 V	130 k Ω	130 k Ω	1.200 V
1.5 V	150 k Ω	100 k Ω	1.500 V
1.8 V	475 k Ω	237 k Ω	1.803 V
2.5 V	523 k Ω	165 k Ω	2.502 V
3.3 V	619 k Ω	137 k Ω	3.311 V
5 V	619 k Ω	84.5 k Ω	4.995 V

9.2.2.3 External Component Selection

The external components have to fulfill the needs of the application, but also the stability criteria of the control loop of the device. The TPS629210-Q1 is optimized to work within a range of external components.

9.2.2.3.1 Output Filter and Loop Stability

The TPS629210-Q1 is internally compensated to be stable with a range of LC filter combinations. The LC output filters inductance and capacitance have to be considered together, creating a double pole, responsible for the corner frequency of the converter using 方程式 13.

$$f_{LC} = \frac{1}{2\pi\sqrt{L \times C}} \quad (13)$$

表 9-3 can be used to simplify the output filter component selection. The values in 表 9-3 are nominal values, and the effective capacitance was considered to be +20% and - 50%. Different values can work, but care has to be taken on the loop stability which is affected. More information on the sizing of the LC filter of a DCS-Control regulator can be found in the [Optimizing the TPS62130/40/50/60 Output Filter Application Note](#).

表 9-3. Recommended LC Output Filter Combinations

	4.7 μ F	10 μ F	22 μ F	47 μ F	100 μ F	200 μ F
1 μ H ^{(3) (4)}			✓	✓	✓	✓ ⁽²⁾
1.5 μ H		✓	✓	✓	✓ ⁽²⁾	
2.2 μ H		✓	✓ ⁽¹⁾	✓	✓ ⁽²⁾	
3.3 μ H	✓	✓	✓	✓		
4.7 μ H	✓	✓	✓	✓ ⁽²⁾		

- (1) This LC combination is the standard value and recommended for most applications.
- (2) Output capacitance must have an ESR of $\geq 10 \text{ m}\Omega$ for stable operation. See 节 9.3.1.
- (3) Not recommended for 1-MHz operation
- (4) At full load, $I_{L\text{peak}}$ can exceed I_{LIM_HS} at higher input or output voltages.

Although the TPS629210-Q1 is stable without the pole and zero being in a particular location, an external feedforward capacitor can also be added to adjust their location based on the specific needs of the application. This can provide better performance in power save mode, improved transient response, or both.

A more detailed discussion on the optimization for stability versus transient response can be found in the [Optimizing Transient Response of Internally Compensated DC-DC Converters Application Note](#) and [Feedforward Capacitor to Improve Stability and Bandwidth of TPS621/821-Family Application Note](#).

9.2.2.3.2 Inductor Selection

The TPS629210-Q1 is designed for a nominal 2.2- μ H inductor. Larger values can be used to achieve a lower inductor current ripple but they can have a negative impact on efficiency and transient response. Smaller values than 2.2 μ H cause larger inductor current ripple, which cause larger negative inductor currents in forced PWM mode and higher peak currents at full load. Therefore, they are not recommended at larger voltages across the inductor as it is the case for high input voltages and low output voltages. With low output current in forced PWM mode, this causes a larger negative inductor current peak that can exceed the negative current limit. At low or no output current and small inductor values, the output voltage can therefore not be regulated any more. More detailed information on further LC combinations can be found in the [Optimizing the TPS62130/40/50/60 Output Filter Application Note](#).

The inductor selection is affected by several effects like the following:

- Inductor ripple current
- Output ripple voltage
- PWM-to-PFM transition point
- Efficiency

In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). 方程式 14 calculates the maximum inductor current.

$$I_{L(MAX)} = I_{OUT(MAX)} + \frac{\Delta I_{L(MAX)}}{2} \quad (14)$$

$$\Delta I_{L(MAX)} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN(MAX)}}}{L_{(MIN)} \times f_{SW}} \quad (15)$$

where:

- $I_L(\max)$ is the maximum inductor current.
- ΔI_L is the peak-to-peak inductor ripple current.
- $L(\min)$ is the minimum effective inductor value.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. It is recommended to add a margin of approximately 20%. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well. The following inductors have been used with the TPS629210-Q1 and are recommended for use:

表 9-4. List of Inductors

Type	Inductance [μH]	DCR [$\text{m}\Omega$]	Current [A] ⁽¹⁾	Dimensions [L×W×H] mm	Manufacturer
DFE252012PD-2R2M ⁽²⁾	2.2 μH , $\pm 20\%$	84	2.8	2.5 × 2.0 × 1.2	muRata
XGL3530-222ME	2.2 μH , $\pm 20\%$	20	4.0	3.5 × 3.2 × 3	Coilcraft
XGL4020-222ME	2.2 μH , $\pm 20\%$	19.5	6.2	4 × 4 × 2.1	Coilcraft
XGL3530-332ME	3.3 μH , $\pm 20\%$	33	3.3	3.5 × 3.2 × 3	Coilcraft
XGL4020-472ME	4.7 μH , $\pm 20\%$	43	4.1	4 × 4 × 2.1	Coilcraft

(1) I_{SAT} at 30% drop

(2) For smaller size solutions that do not require maximum efficiency at the full output current

The inductor value also determines the load current at which power save mode is entered:

$$I_{Load(PSM)} = \frac{1}{2} \times \Delta I_L \quad (16)$$

9.2.2.3.3 Capacitor Selection

9.2.2.3.3.1 Output Capacitor

The recommended value for the output capacitor is 22 μF . The architecture of the TPS629210-Q1 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends to use X7R or X5R dielectric. Using a higher value has advantages like smaller voltage ripple and a tighter DC output accuracy in power save mode (see [Optimizing the TPS62130/40/50/60 Output Filter Application Note](#) for more information).

In power save mode, the output voltage ripple depends on the following:

- Output capacitance
- ESR
- ESL
- Peak inductor current

Using ceramic capacitors provides small ESR, ESL, and low ripple.

The output capacitor must be as close as possible to the device, and TI recommends to have the VOS signal and feedback resistors (if used) must be connected to the positive terminal of the output capacitor.

For large output voltages, the DC bias effect of ceramic capacitors is large and the effective capacitance has to be observed.

9.2.2.3.3.2 Input Capacitor

For most applications, 4.7- μ F nominal is sufficient and is recommended, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low-ESR multilayer ceramic capacitor (MLCC) is recommended for best filtering and must be placed as close as possible to the VIN and GND pins.

表 9-5. List of Capacitors

Type	Nominal Capacitance [μ F]	Voltage Rating [V]	Size	Manufacturer
CGA5L1X7R1E475K160AC	4.7	25	1206 ⁽¹⁾	TDK
CGA5L1X7R1E106K160AC	10	25	1206 ⁽¹⁾	TDK

(1) Smaller (0805 or 0603) options may be used and are available from various manufacturers.

9.2.3 Application Curves

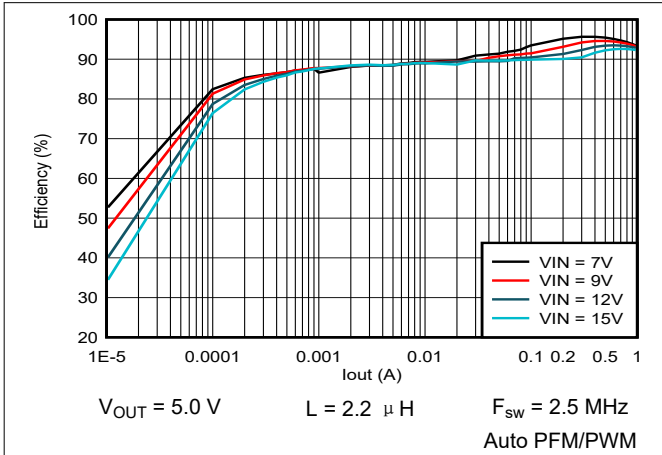


图 9-2. Efficiency vs Output Current

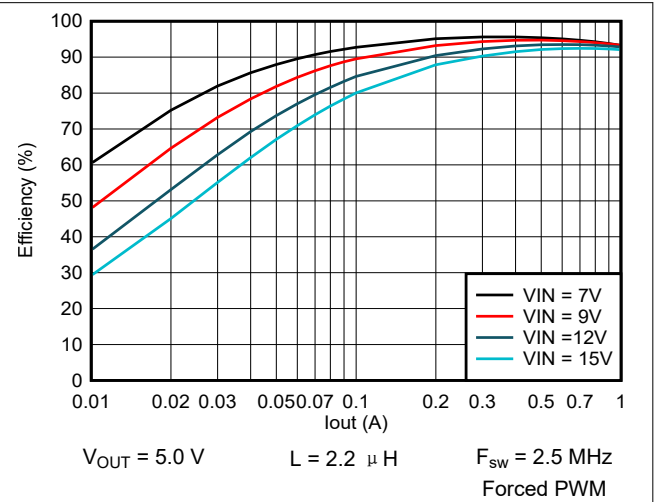


图 9-3. Efficiency vs Output Current

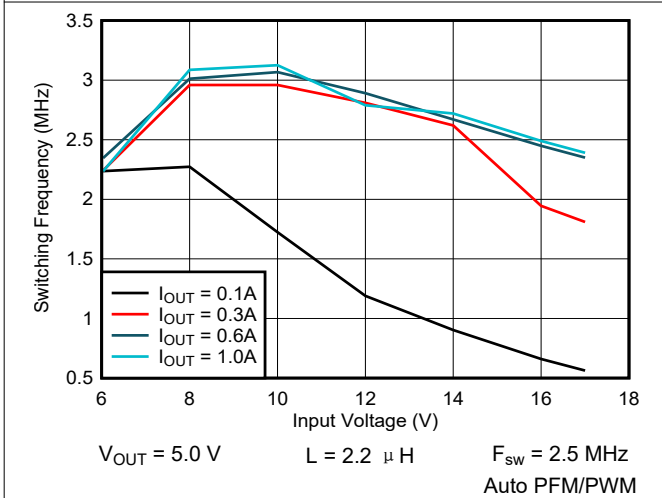


图 9-4. Switching Frequency vs Input Voltage

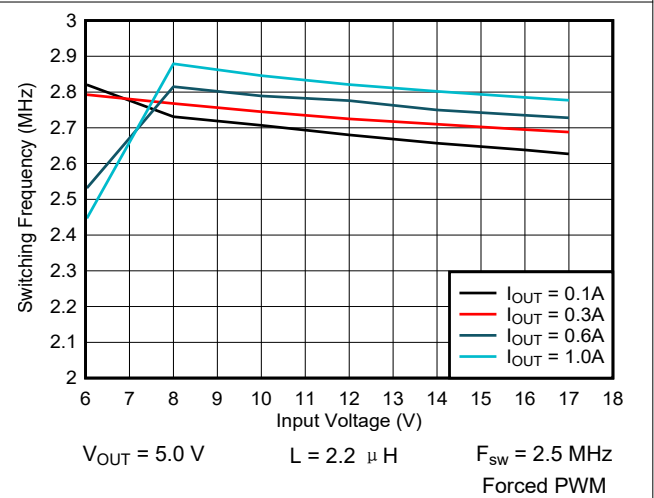


图 9-5. Switching Frequency vs Input Voltage

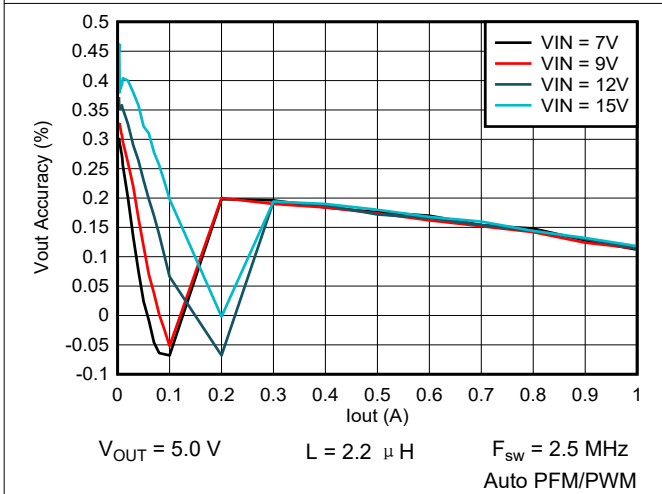


图 9-6. Output Voltage vs Output Current

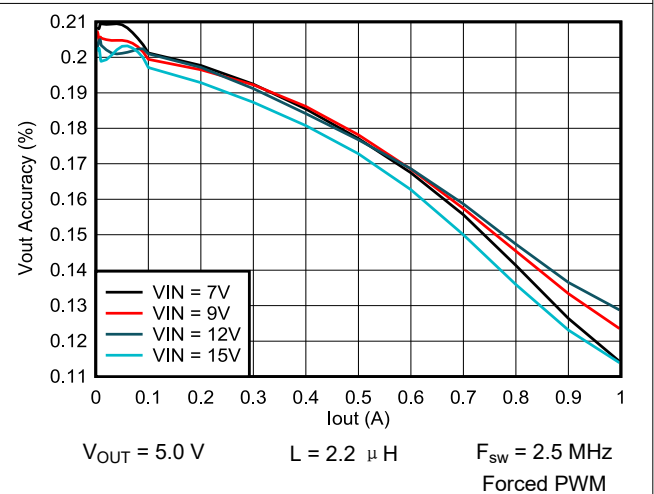


图 9-7. Output Voltage vs Output Current

9.2.3 Application Curves (continued)

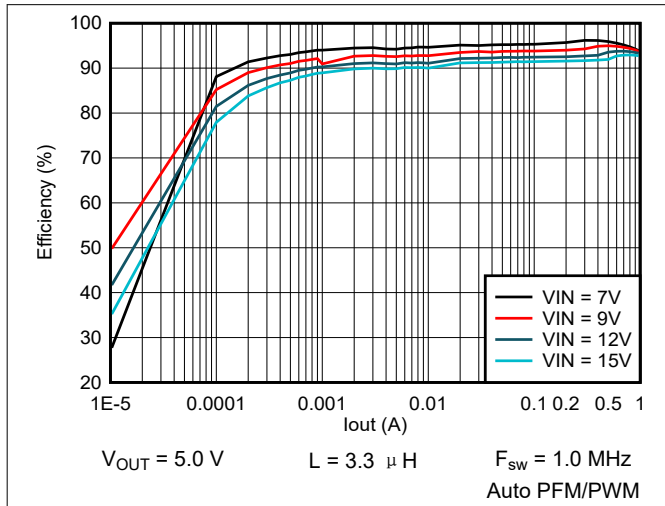


图 9-8. Efficiency vs Output Current

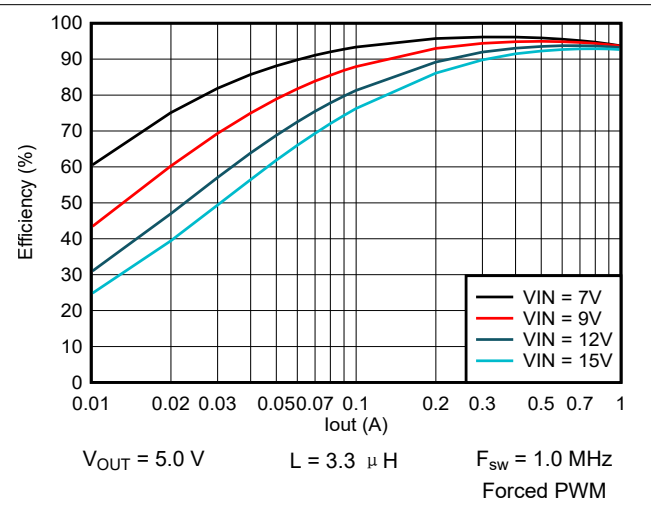


图 9-9. Efficiency vs Output Current

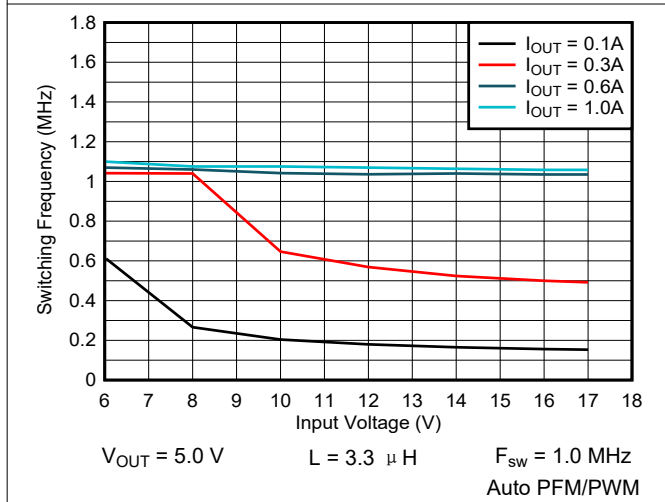


图 9-10. Switching Frequency vs Input Voltage

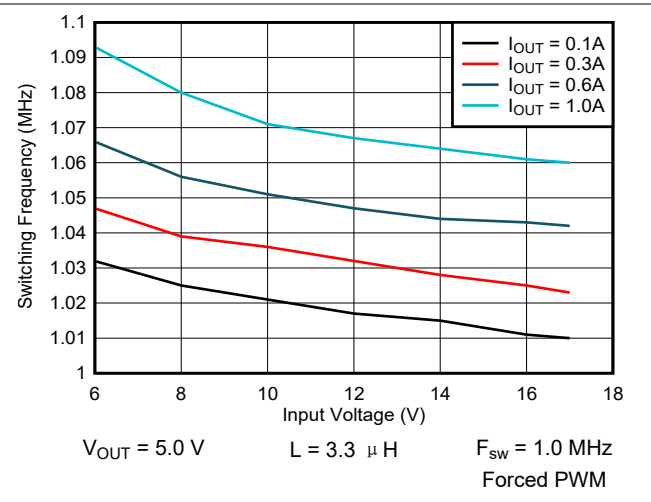


图 9-11. Switching Frequency vs Input Voltage

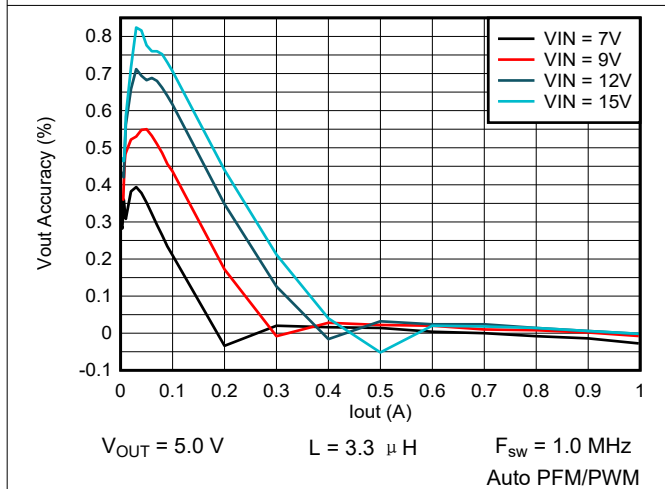


图 9-12. Output Voltage vs Output Current

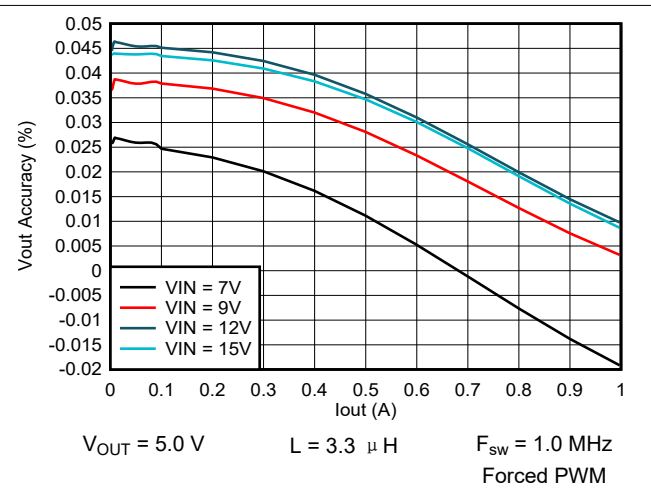


图 9-13. Output Voltage vs Output Current

9.2.3 Application Curves (continued)

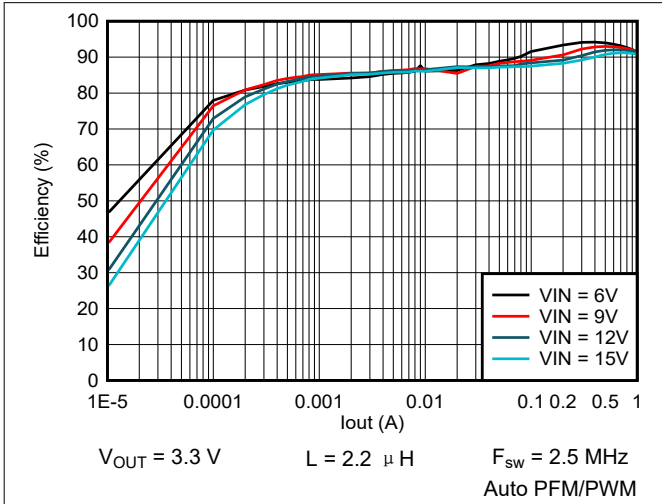


图 9-14. Efficiency vs Output Current

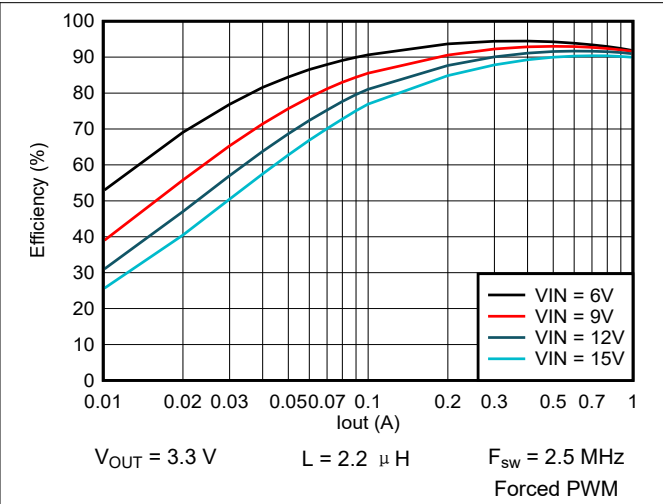


图 9-15. Efficiency vs Output Current

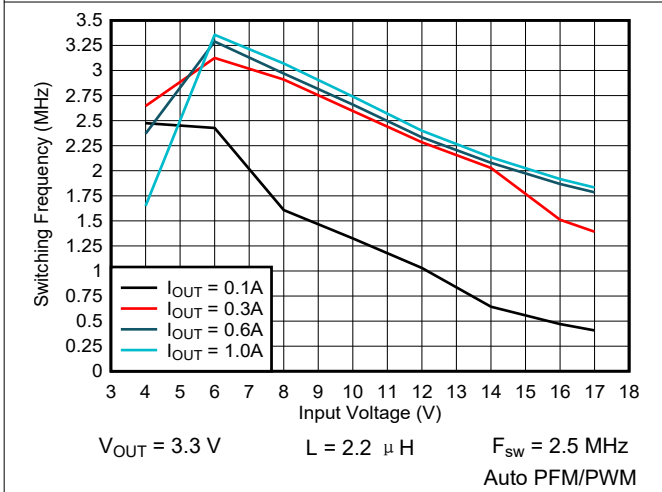


图 9-16. Switching Frequency vs Input Voltage

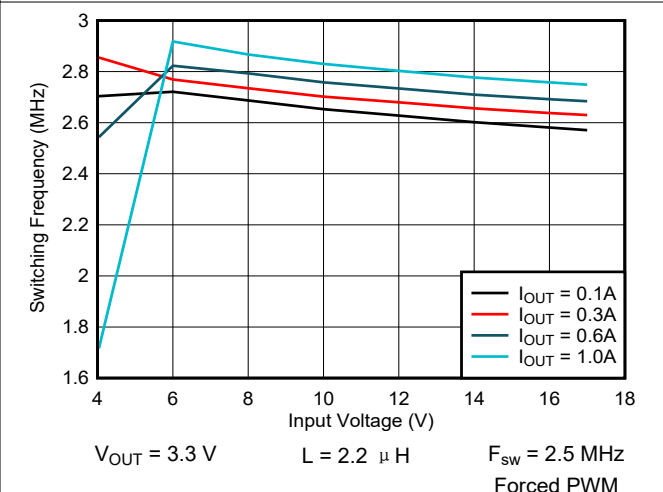


图 9-17. Switching Frequency vs Input Voltage

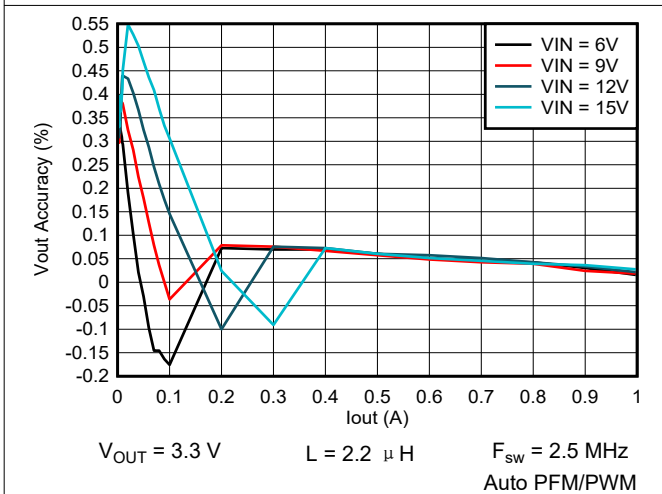


图 9-18. Output Voltage vs Output Current

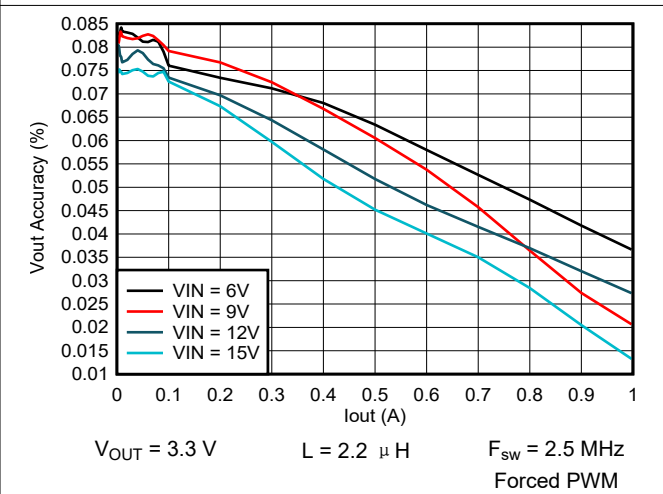


图 9-19. Output Voltage vs Output Current

9.2.3 Application Curves (continued)

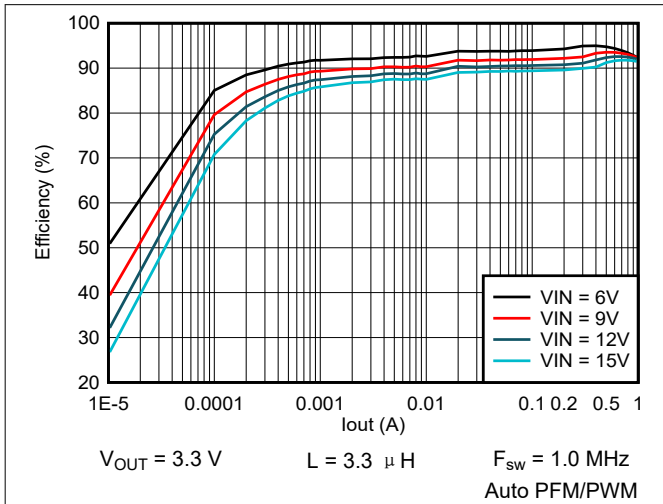


图 9-20. Efficiency vs Output Current

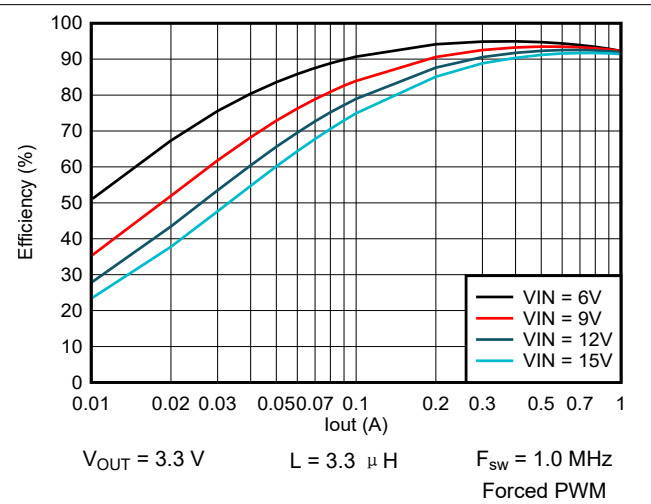


图 9-21. Efficiency vs Output Current

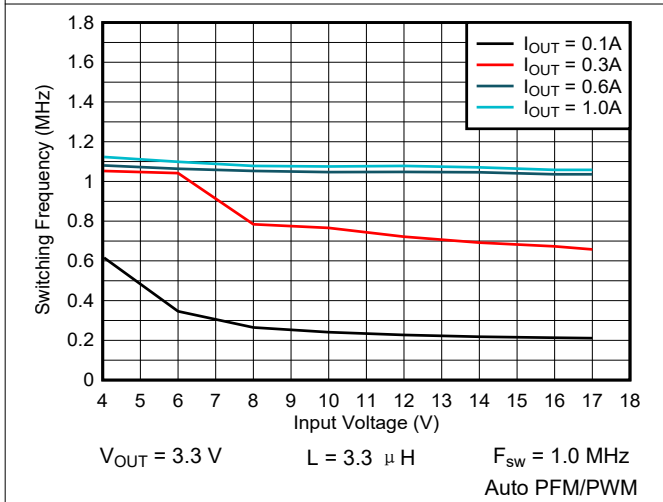


图 9-22. Switching Frequency vs Input Voltage

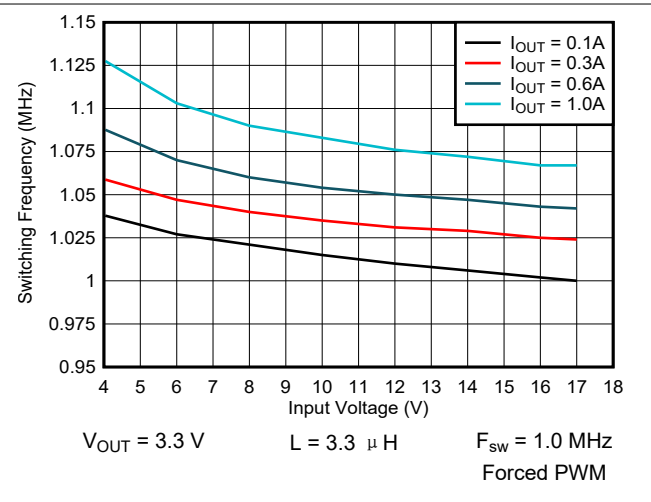


图 9-23. Switching Frequency vs Input Voltage

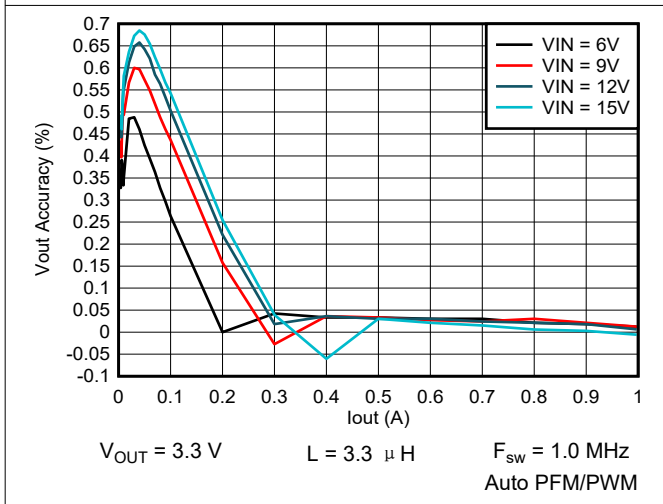


图 9-24. Output Voltage vs Output Current

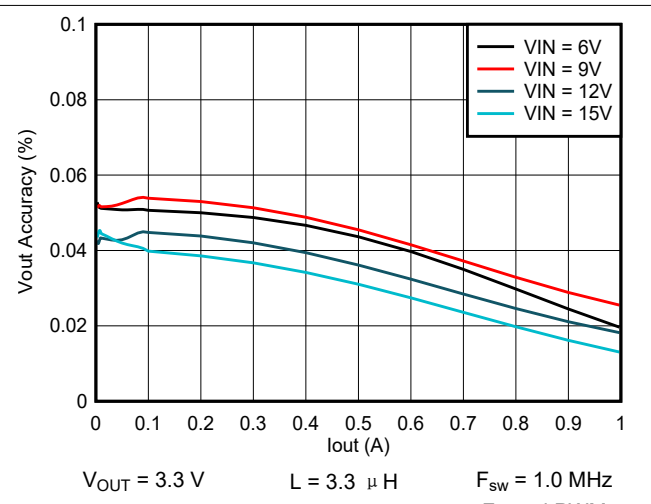


图 9-25. Output Voltage vs Output Current

9.2.3 Application Curves (continued)

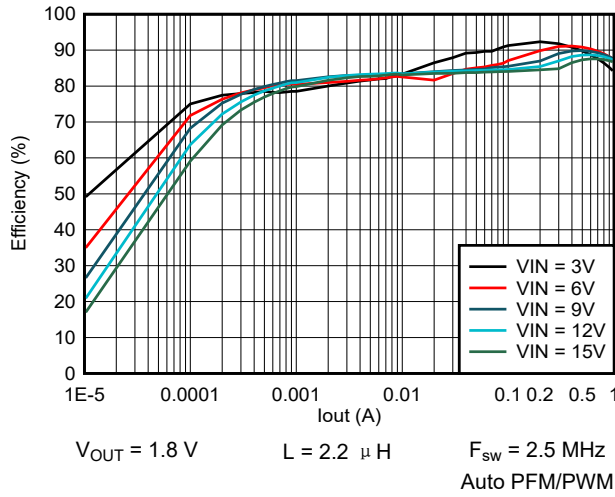


图 9-26. Efficiency vs Output Current

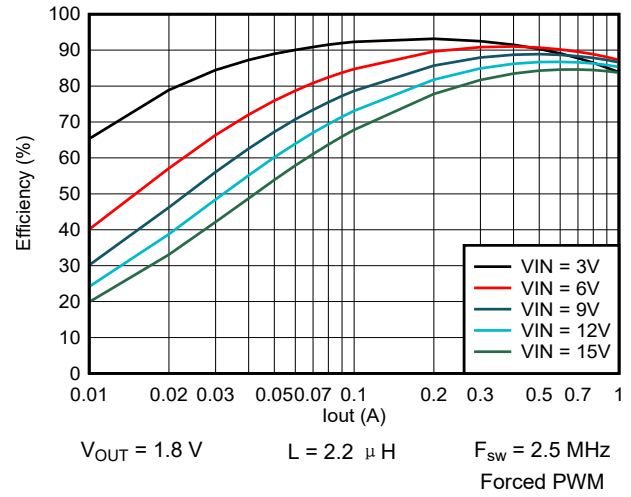


图 9-27. Efficiency vs Output Current

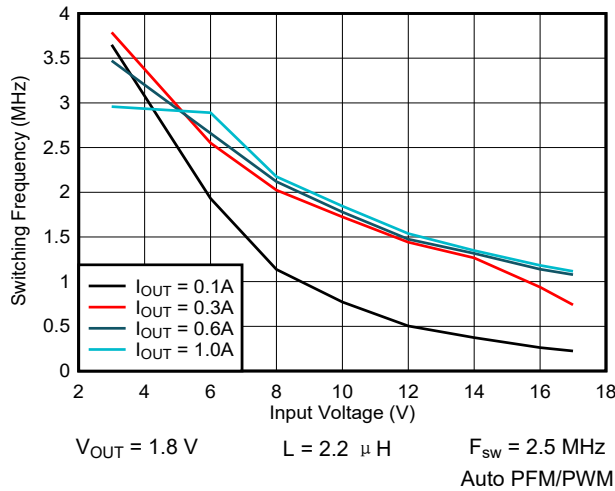


图 9-28. Switching Frequency vs Input Voltage

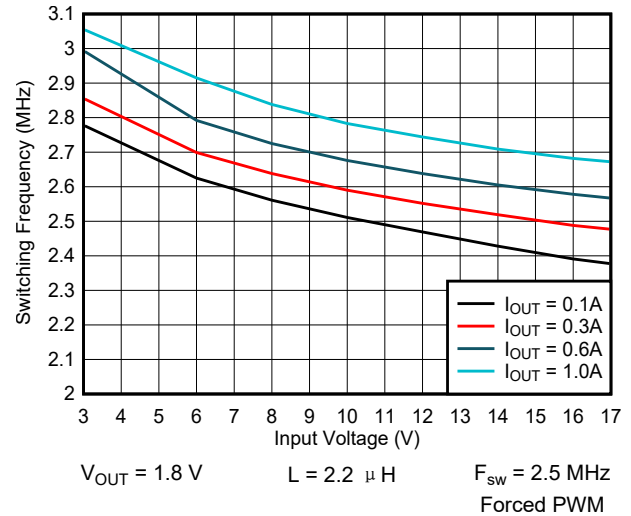


图 9-29. Switching Frequency vs Input Voltage

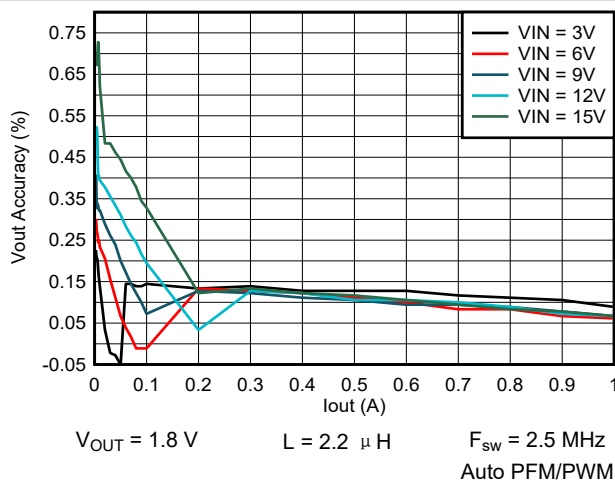


图 9-30. Output Voltage vs Output Current

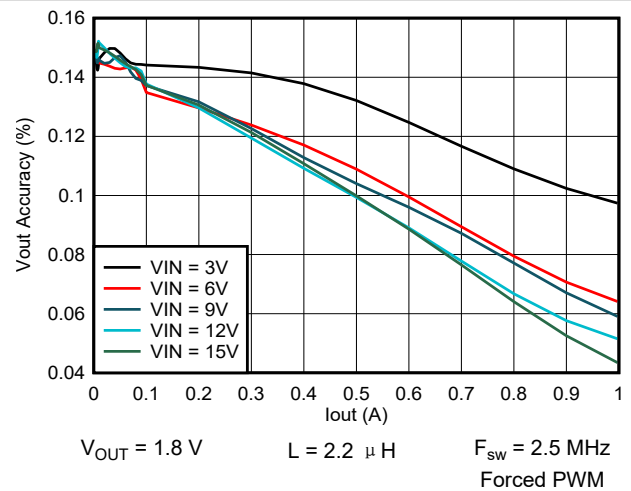


图 9-31. Output Voltage vs Output Current

9.2.3 Application Curves (continued)

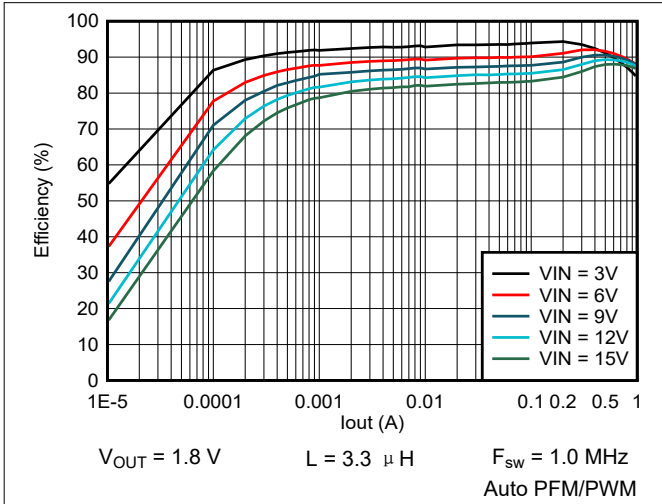


图 9-32. Efficiency vs Output Current

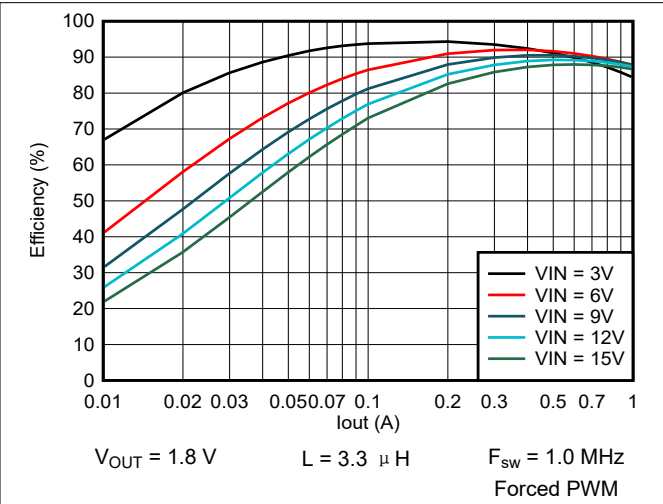


图 9-33. Efficiency vs Output Current

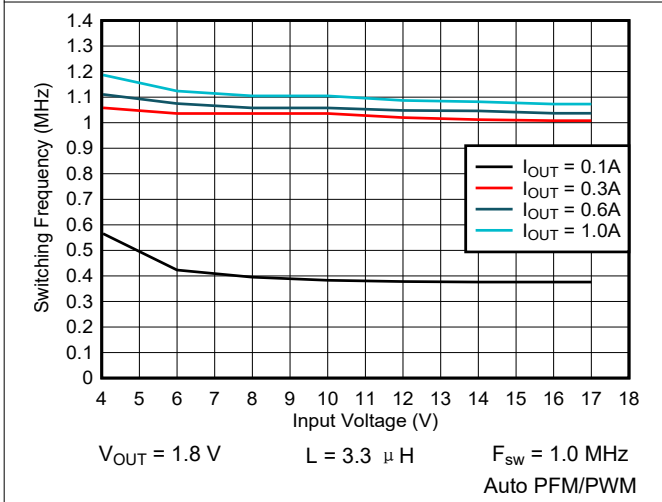


图 9-34. Switching Frequency vs Input Voltage

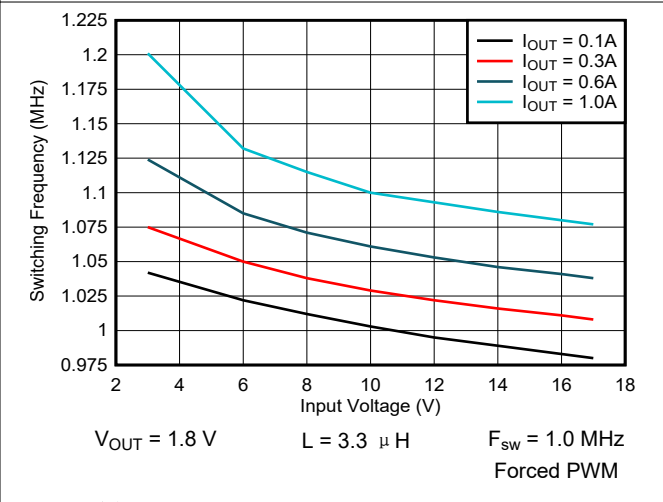


图 9-35. Switching Frequency vs Input Voltage

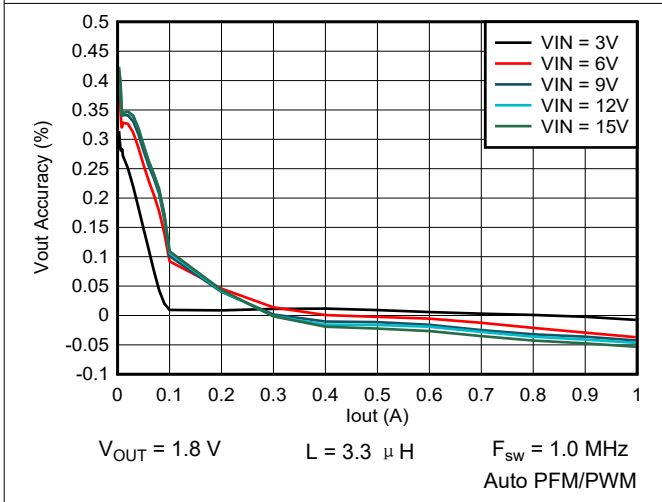


图 9-36. Output Voltage vs Output Current

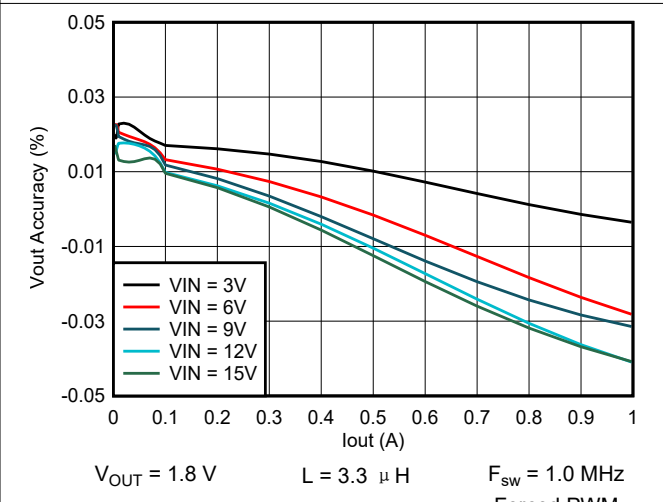


图 9-37. Output Voltage vs Output Current

9.2.3 Application Curves (continued)

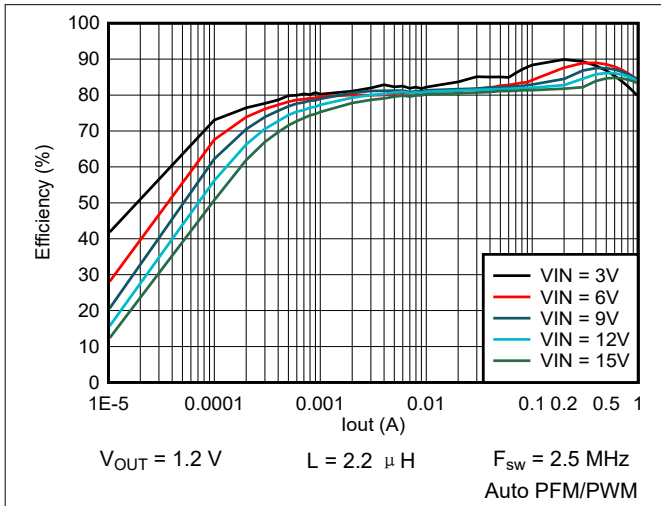


图 9-38. Efficiency vs Output Current

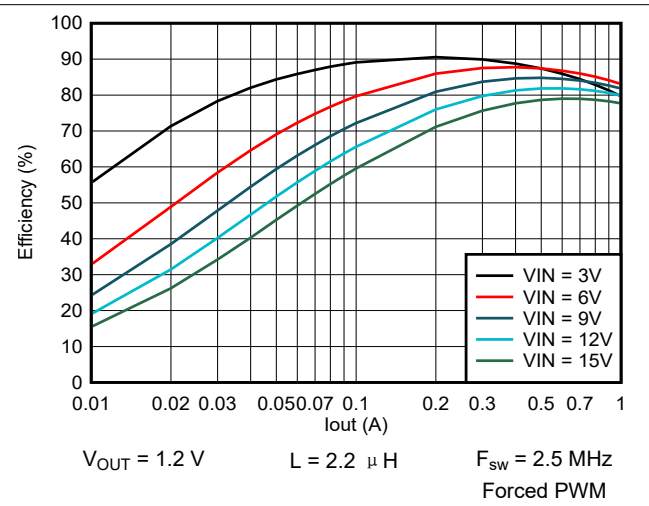


图 9-39. Efficiency vs Output Current

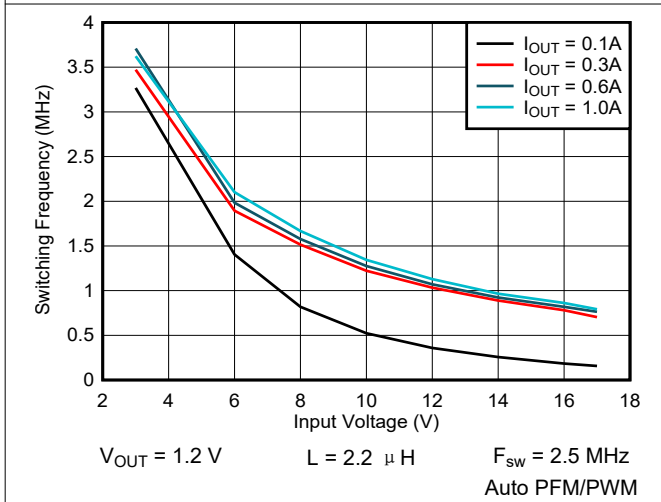


图 9-40. Switching Frequency vs Input Voltage

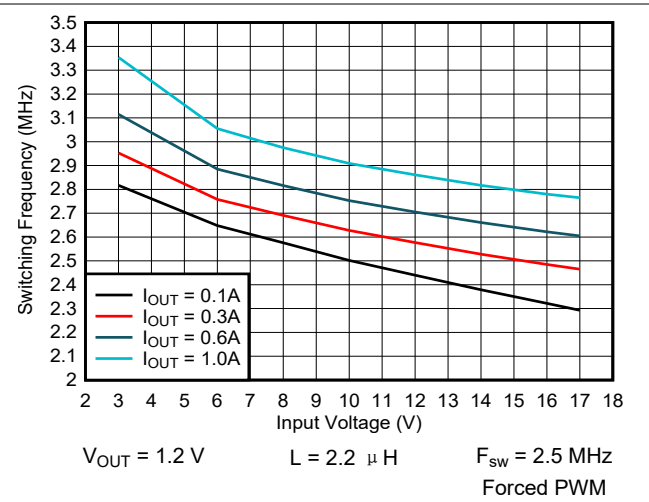


图 9-41. Switching Frequency vs Input Voltage

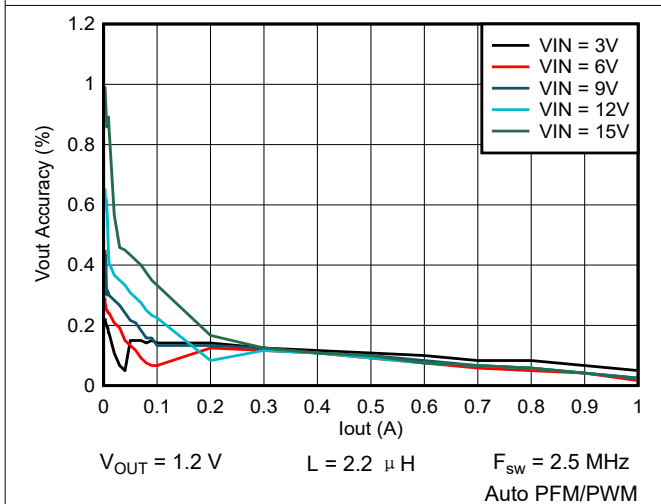


图 9-42. Output Voltage vs Output Current

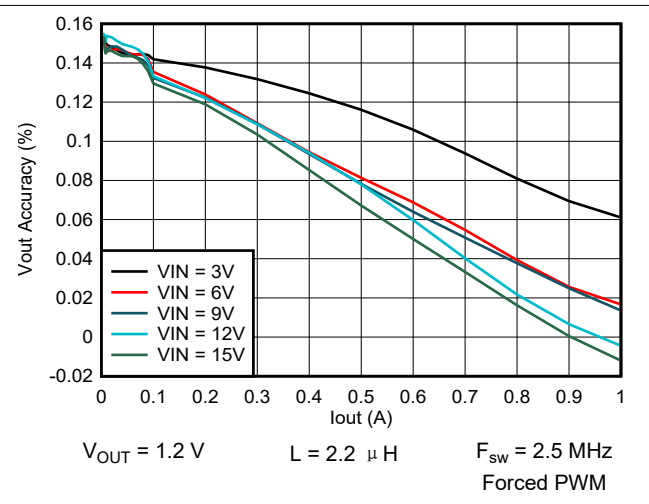


图 9-43. Output Voltage vs Output Current

9.2.3 Application Curves (continued)

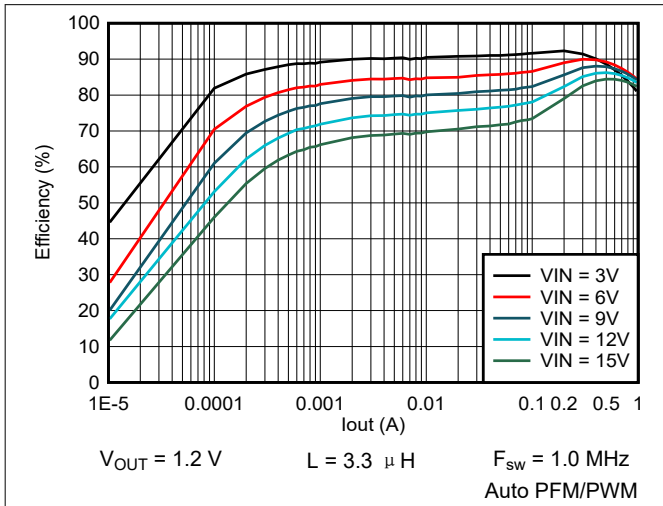


图 9-44. Efficiency vs Output Current

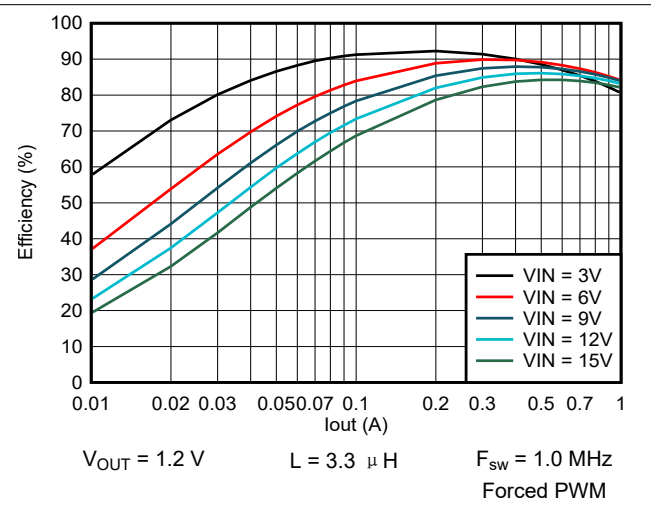


图 9-45. Efficiency vs Output Current

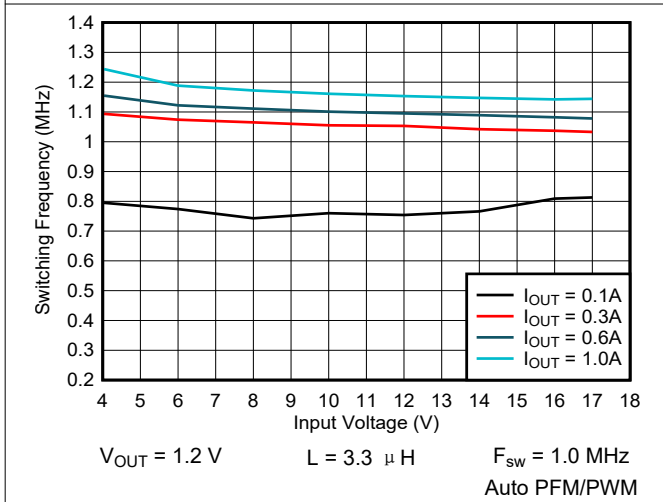


图 9-46. Switching Frequency vs Input Voltage

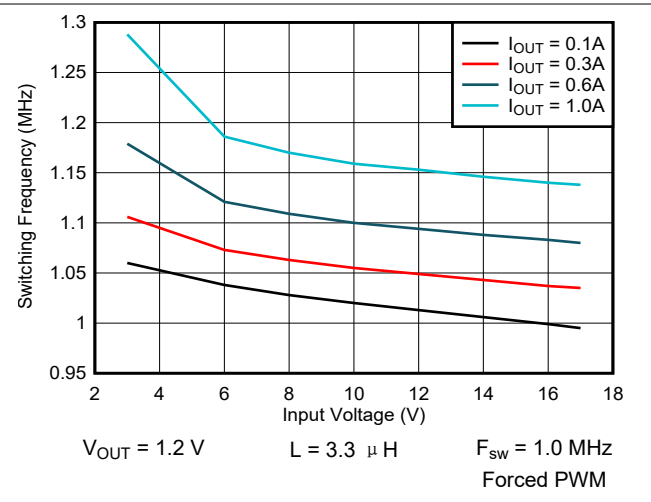


图 9-47. Switching Frequency vs Input Voltage

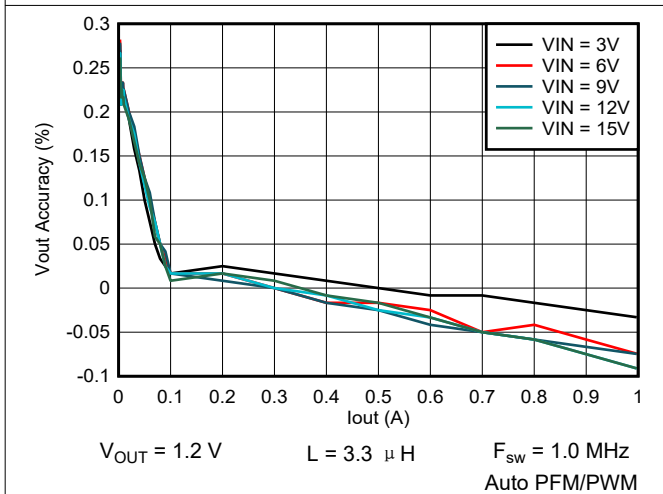


图 9-48. Output Voltage vs Output Current

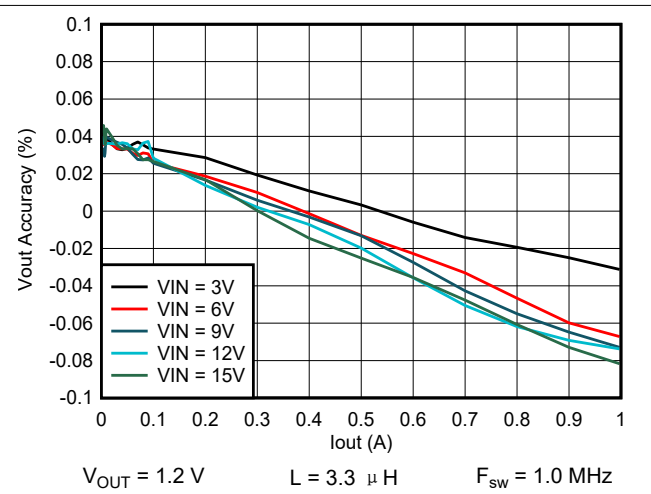


图 9-49. Output Voltage vs Output Current

9.2.3 Application Curves (continued)

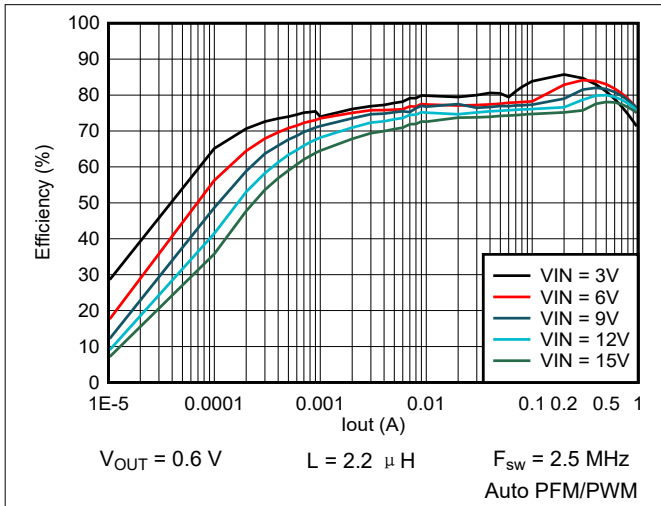


图 9-50. Efficiency vs Output Current

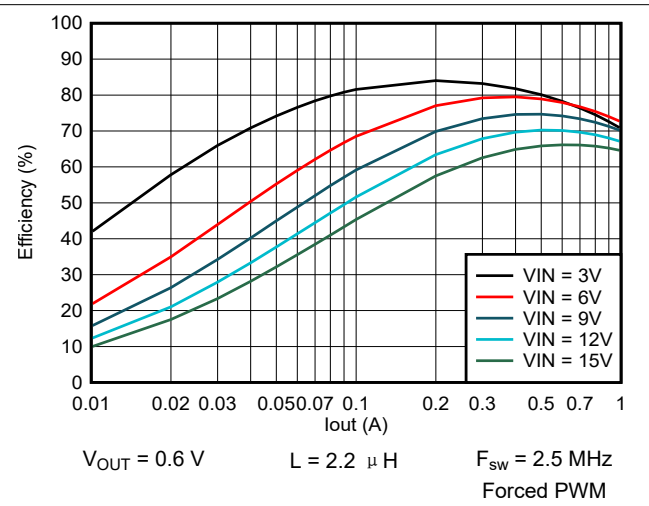


图 9-51. Efficiency vs Output Current

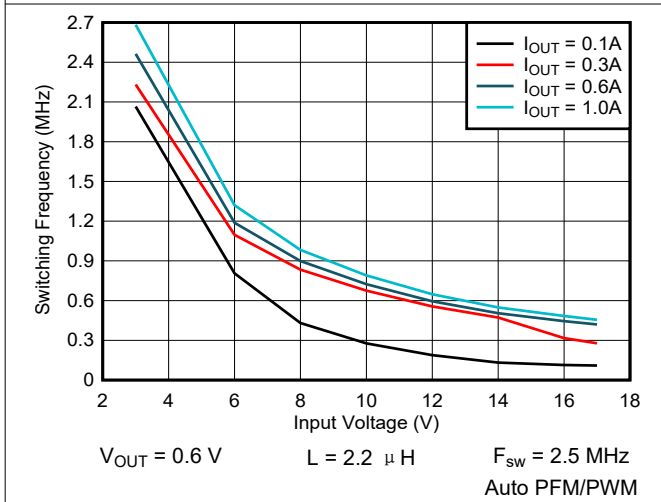


图 9-52. Switching Frequency vs Input Voltage

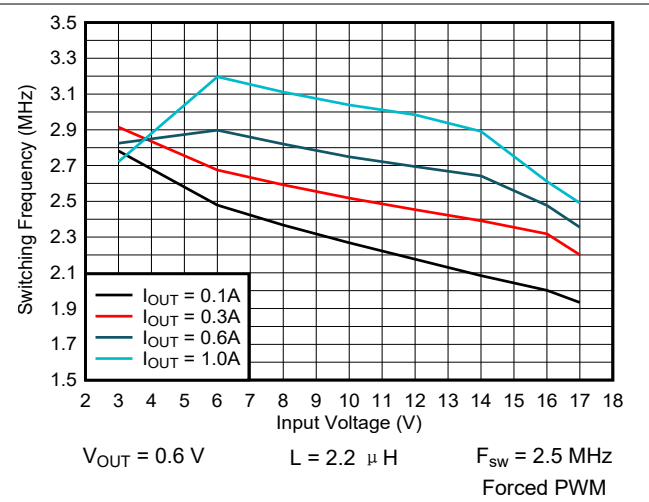


图 9-53. Switching Frequency vs Input Voltage

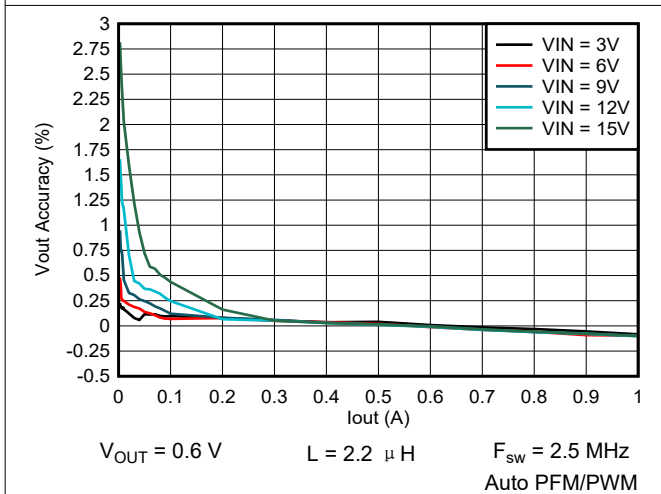


图 9-54. Output Voltage vs Output Current

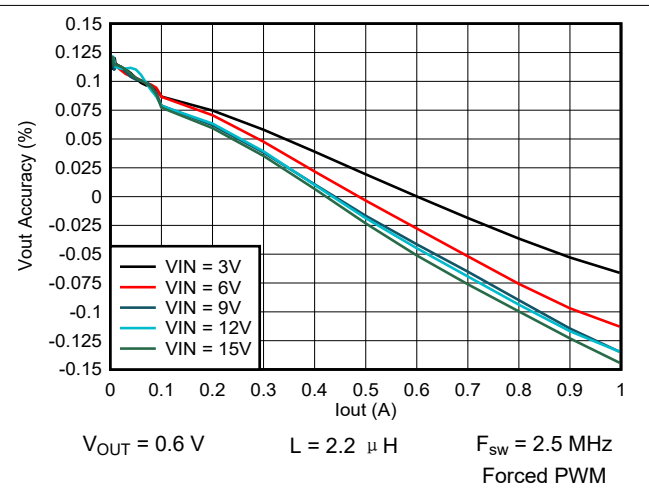
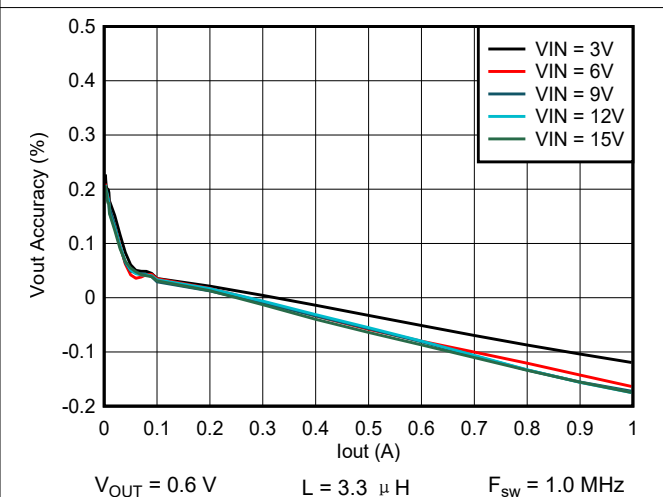
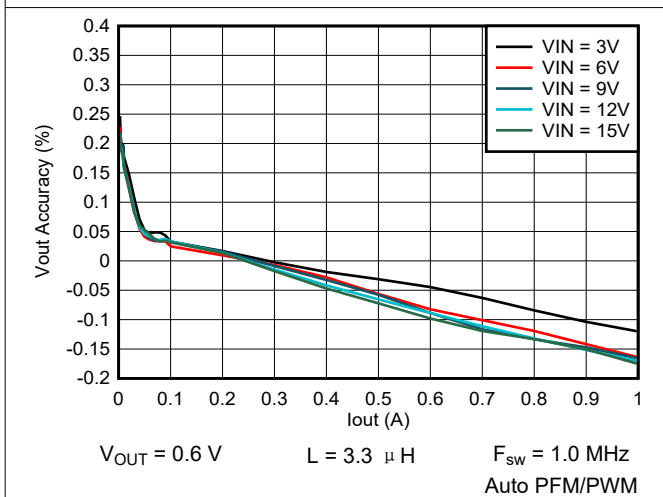
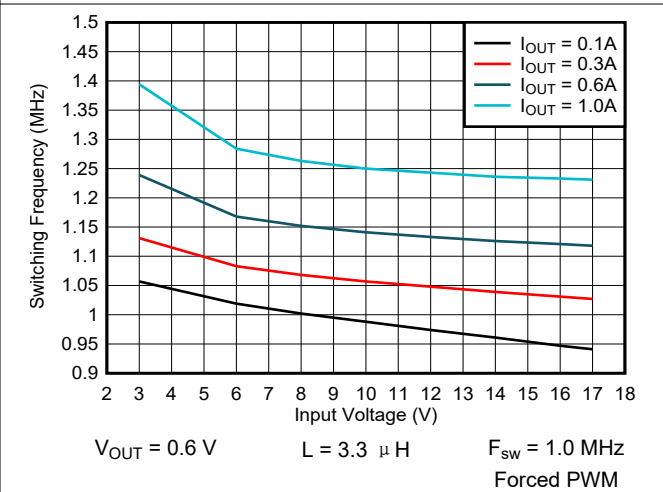
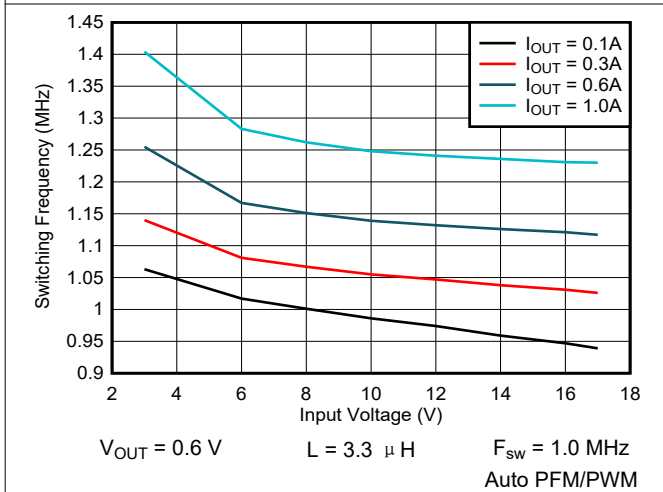
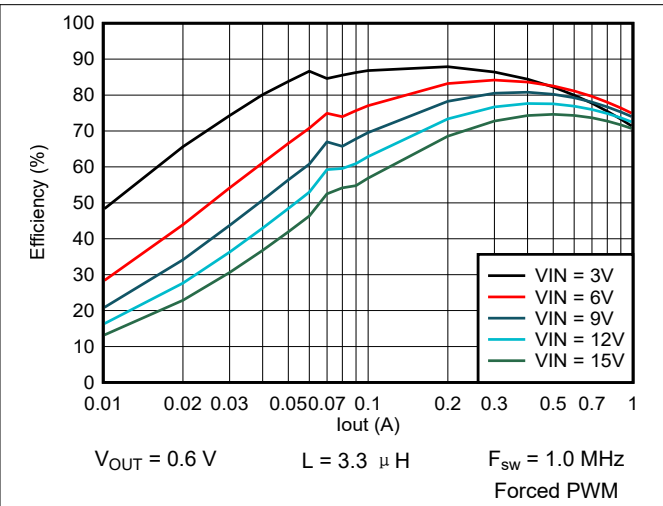
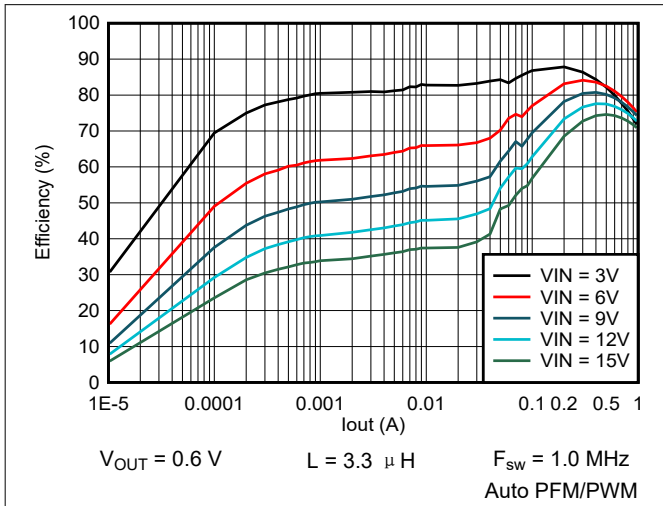
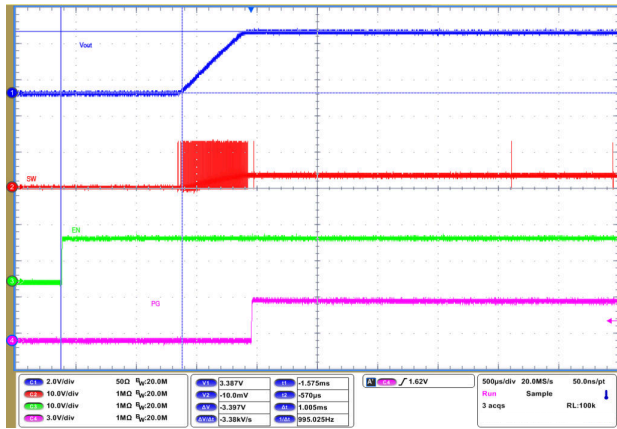


图 9-55. Output Voltage vs Output Current

9.2.3 Application Curves (continued)

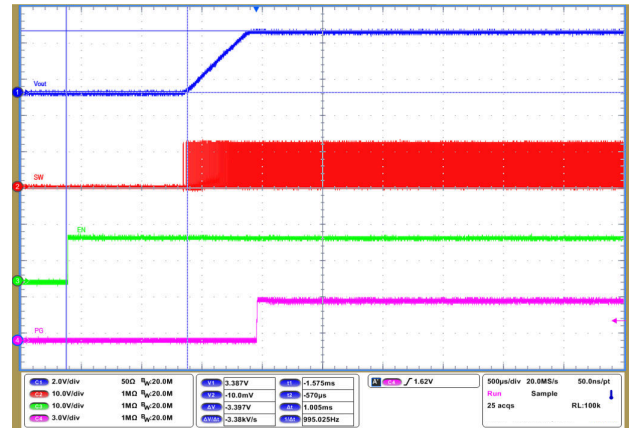


9.2.3 Application Curves (continued)



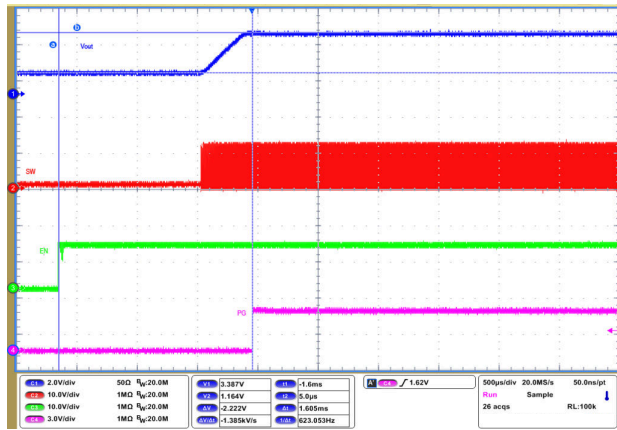
$V_{IN} = 12$ V $L = 2.2$ μ H $F_{SW} = 2.5$ MHz
 $V_{OUT} = 3.3$ V $I_O = 0$ A Auto PFM/PWM

图 9-62. Start-Up Timing



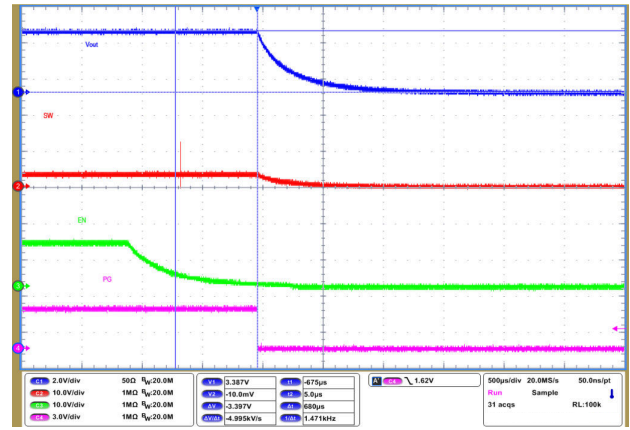
$V_{IN} = 12$ V $L = 2.2$ μ H $F_{SW} = 2.5$ MHz
 $V_{OUT} = 3.3$ V $I_O = 1$ A Forced PWM

图 9-63. Start-Up Timing



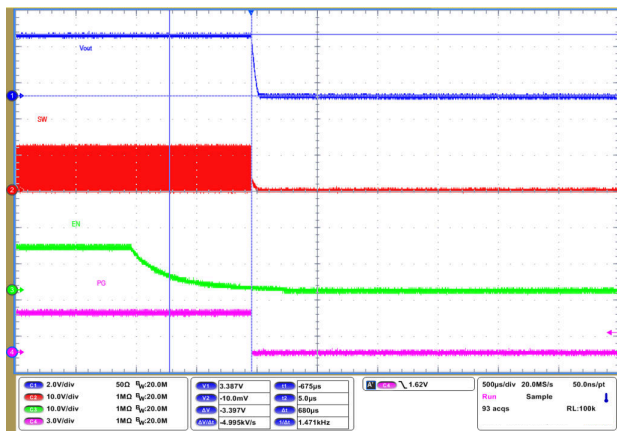
$V_{IN} = 12$ V $L = 2.2$ μ H $F_{SW} = 2.5$ MHz
 $V_{OUT} = 3.3$ V $I_O = 0$ A Forced PWM

图 9-64. Start-Up into Prebiased Output



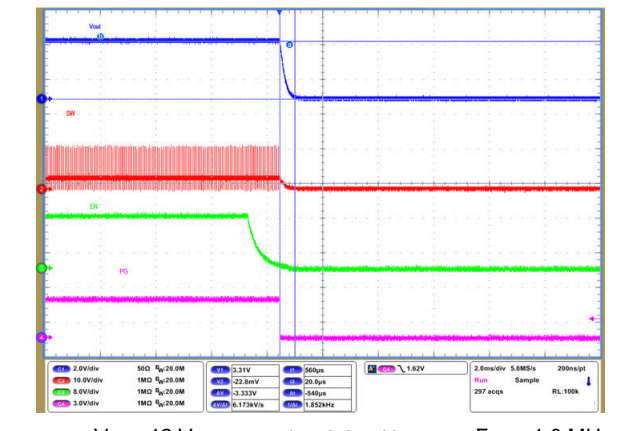
$V_{IN} = 12$ V $L = 2.2$ μ H $F_{SW} = 2.5$ MHz
 $V_{OUT} = 3.3$ V $I_O = 0$ A Auto PFM/PWM

图 9-65. Shutdown Timing with Output Discharge Enabled



$V_{IN} = 12$ V $L = 2.2$ μ H $F_{SW} = 2.5$ MHz
 $V_{OUT} = 3.3$ V $I_O = 1$ A Forced PWM

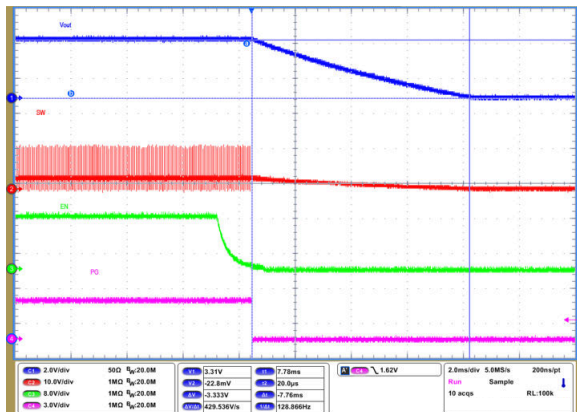
图 9-66. Shutdown Timing with Output Discharge Disabled



$V_{IN} = 12$ V $L = 3.3$ μ H $F_{SW} = 1.0$ MHz
 $V_{OUT} = 3.3$ V $I_O = 10$ mA Auto PFM/PWM

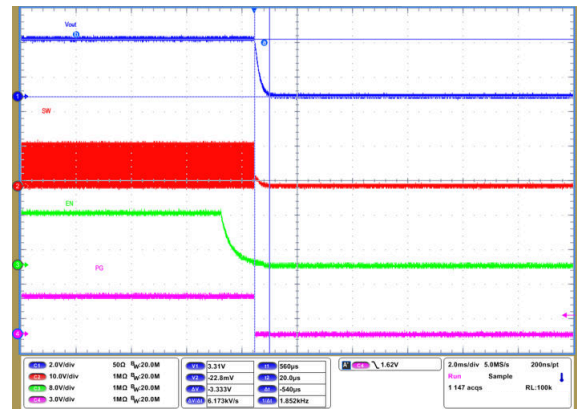
图 9-67. Shutdown Timing with Output Discharge Enabled

9.2.3 Application Curves (continued)



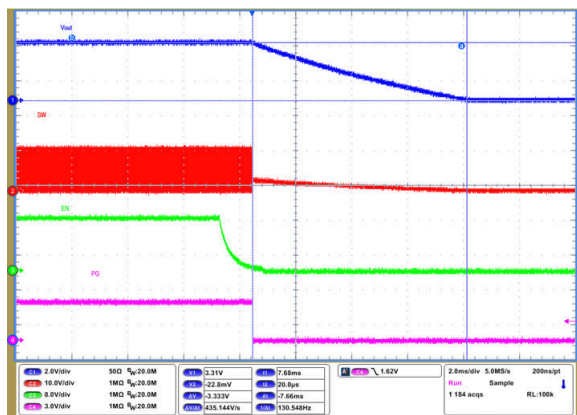
$V_{IN} = 12\text{ V}$ $L = 3.3\ \mu\text{ H}$ $F_{SW} = 1.0\text{ MHz}$
 $V_{OUT} = 3.3\text{ V}$ $I_O = 10\text{ mA}$ Auto PFM/PWM

图 9-68. Shutdown Timing with Output Discharge Disabled



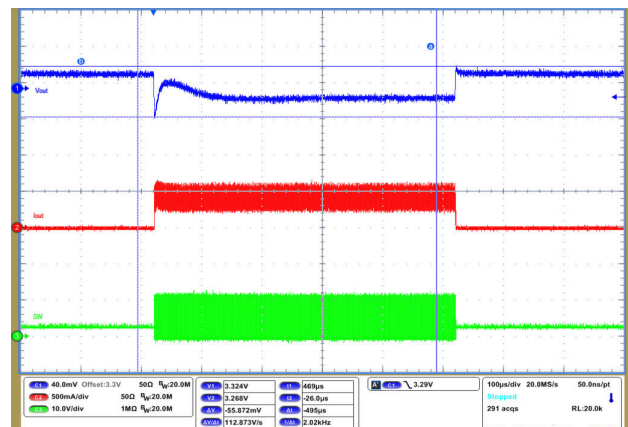
$V_{IN} = 12\text{ V}$ $L = 3.3\ \mu\text{ H}$ $F_{SW} = 1.0\text{ MHz}$
 $V_{OUT} = 3.3\text{ V}$ $I_O = 10\text{ mA}$ Forced PWM

图 9-69. Shutdown Timing with Output Discharge Enabled



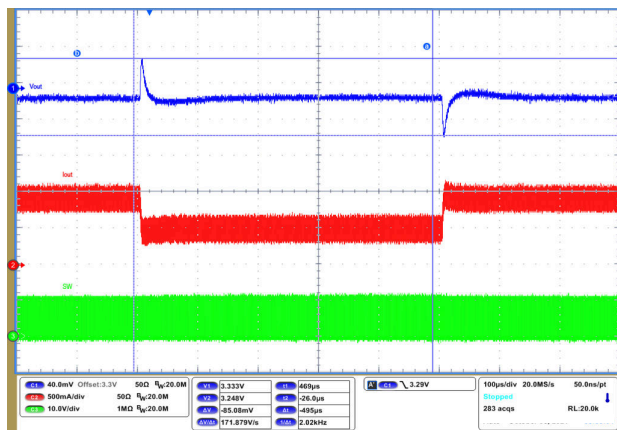
$V_{IN} = 12\text{ V}$ $L = 3.3\ \mu\text{ H}$ $F_{SW} = 1.0\text{ MHz}$
 $V_{OUT} = 3.3\text{ V}$ $I_O = 10\text{ mA}$ Forced PWM

图 9-70. Shutdown Timing with Output Discharge Disabled



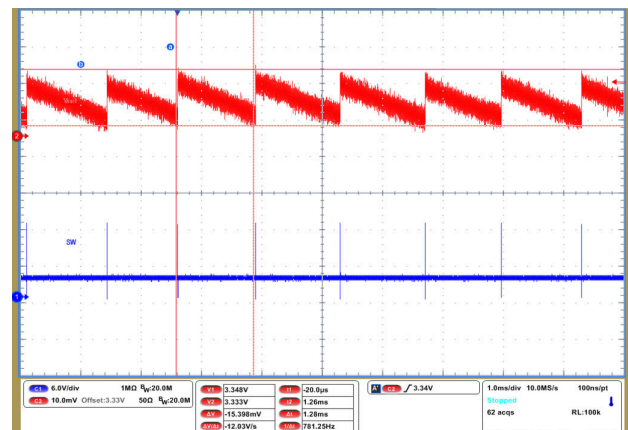
$V_{IN} = 12\text{ V}$ $L = 2.2\ \mu\text{ H}$ $F_{SW} = 2.5\text{ MHz}$
 $V_{OUT} = 3.3\text{ V}$ $I_O = 0\text{ A to }0.5\text{ A}$ Auto PFM/PWM

图 9-71. Load Transient Response



$V_{IN} = 12\text{ V}$ $L = 2.2\ \mu\text{ H}$ $F_{SW} = 2.5\text{ MHz}$
 $V_{OUT} = 3.3\text{ V}$ $I_O = 0.5\text{ A to }1\text{ A}$ Auto PFM/PWM

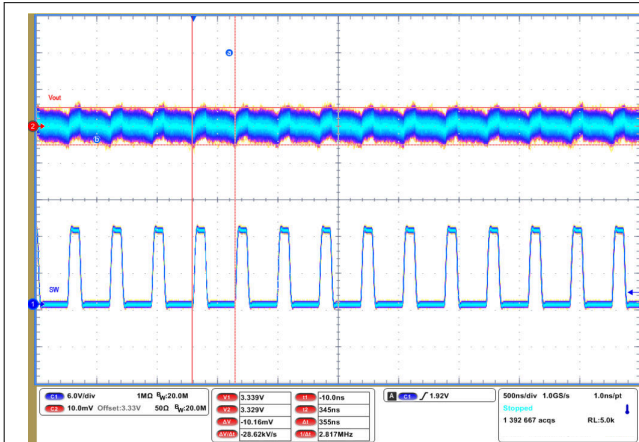
图 9-72. Load Transient Response



$V_{IN} = 12\text{ V}$ $L = 2.2\ \mu\text{ H}$ $F_{SW} = 2.5\text{ MHz}$
 $V_{OUT} = 3.3\text{ V}$ $I_O = 0\text{ A}$ Auto PFM/PWM

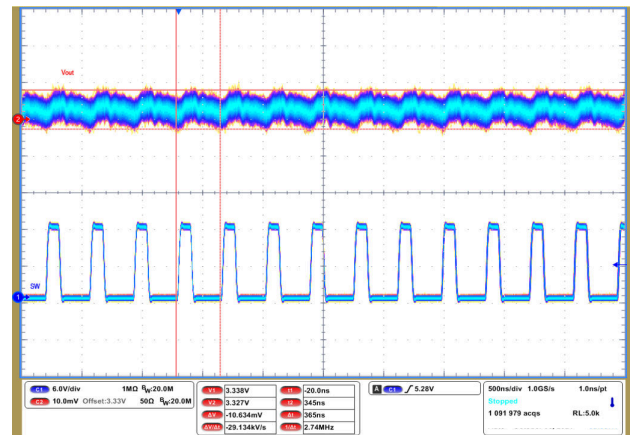
图 9-73. Output Voltage Ripple

9.2.3 Application Curves (continued)



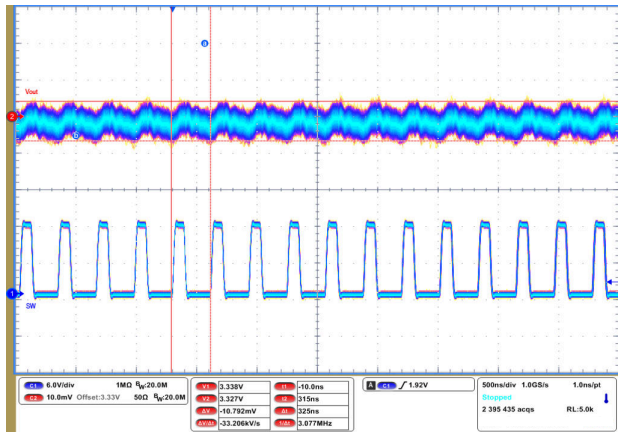
$V_{IN} = 12\text{ V}$ $L = 2.2\ \mu\text{H}$ $F_{SW} = 2.5\text{ MHz}$
 $V_{OUT} = 3.3\text{ V}$ $I_O = 0\text{ A}$ Forced PWM

图 9-74. Output Voltage Ripple



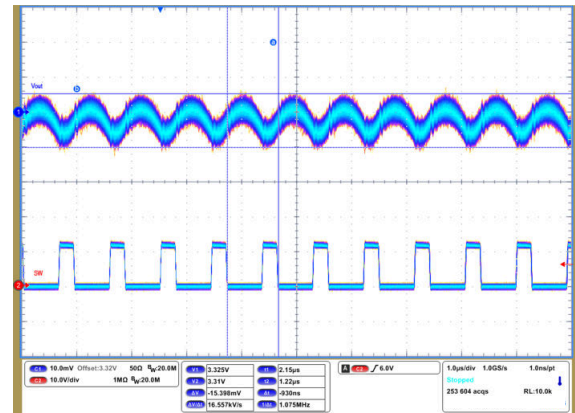
$V_{IN} = 12\text{ V}$ $L = 2.2\ \mu\text{H}$ $F_{SW} = 2.5\text{ MHz}$
 $V_{OUT} = 3.3\text{ V}$ $I_O = 1\text{ A}$ Auto PFM/PWM

图 9-75. Output Voltage Ripple



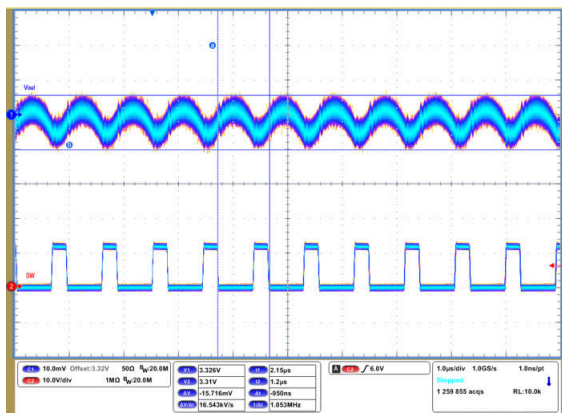
$V_{IN} = 12\text{ V}$ $L = 2.2\ \mu\text{H}$ $F_{SW} = 2.5\text{ MHz}$
 $V_{OUT} = 3.3\text{ V}$ $I_O = 1\text{ A}$ Forced PWM

图 9-76. Output Voltage Ripple



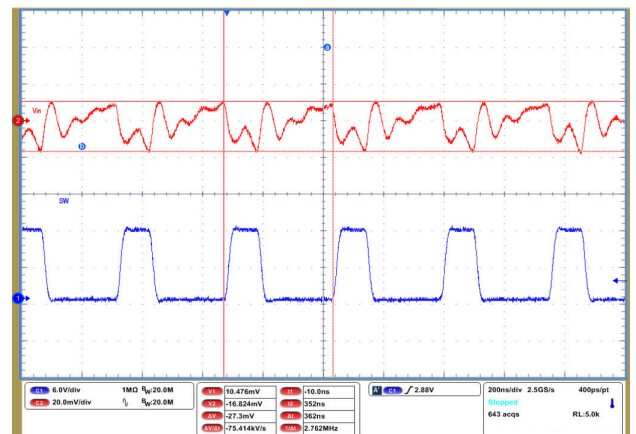
$V_{IN} = 12\text{ V}$ $L = 3.3\ \mu\text{H}$ $F_{SW} = 1.0\text{ MHz}$
 $V_{OUT} = 3.3\text{ V}$ $I_O = 1\text{ A}$ Auto PFM/PWM

图 9-77. Output Voltage Ripple



$V_{IN} = 12\text{ V}$ $L = 3.3\ \mu\text{H}$ $F_{SW} = 1.0\text{ MHz}$
 $V_{OUT} = 3.3\text{ V}$ $I_O = 1\text{ A}$ Forced PWM

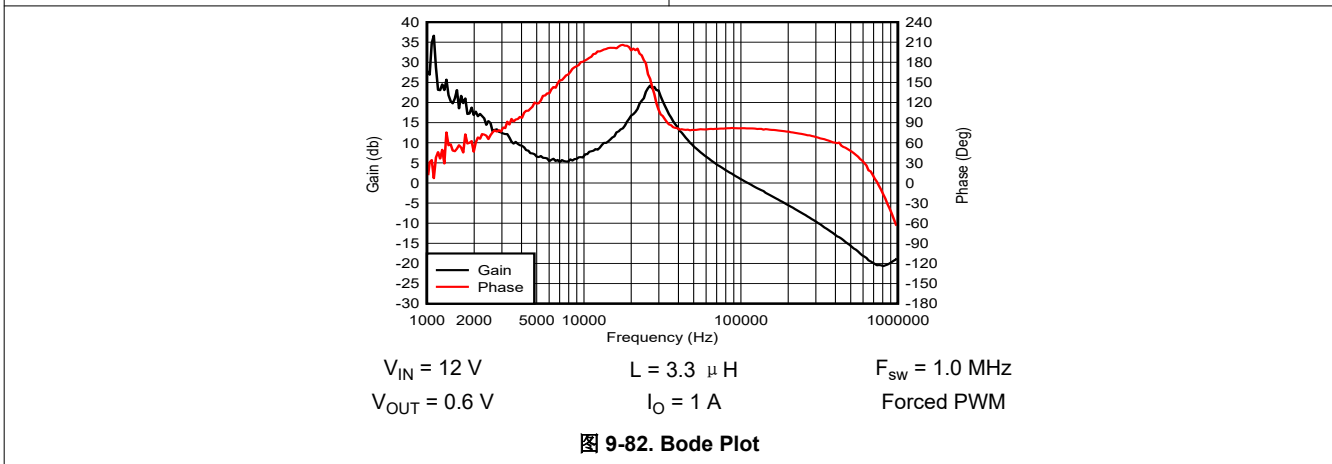
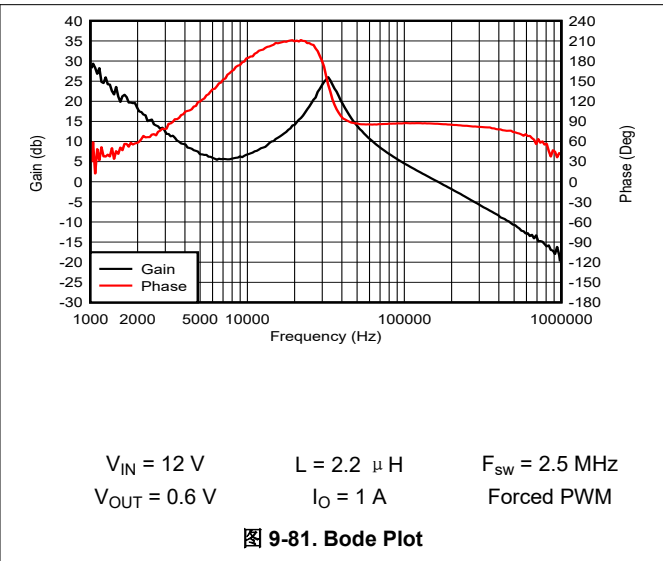
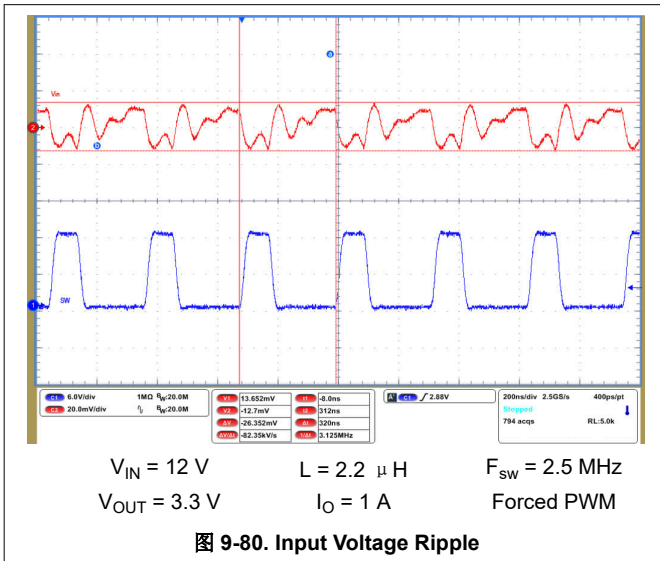
图 9-78. Output Voltage Ripple



$V_{IN} = 12\text{ V}$ $L = 2.2\ \mu\text{H}$ $F_{SW} = 2.5\text{ MHz}$
 $V_{OUT} = 3.3\text{ V}$ $I_O = 1\text{ A}$ Auto PFM/PWM

图 9-79. Input Voltage Ripple

9.2.3 Application Curves (continued)



9.3 System Examples

9.3.1 Powering Multiple Loads

In applications where the TPS629210-Q1 is used to power multiple load circuits, it is possible that the total capacitance on the output is very large. To properly regulate the output voltage, there must be an appropriate AC signal level on the VOS pin. Tantalum capacitors have a large enough ESR to keep output voltage ripple sufficiently high on the VOS pin. With low-ESR ceramic capacitors, the output voltage ripple can get very low, so it is not recommended to use a large capacitance directly on the output of the device. If there are several load circuits with their associated input capacitor on a PCB, these loads are typically distributed across the board. This adds enough trace resistance (R_{trace}) to keep a large enough AC signal on the VOS pin for proper regulation.

The minimum total trace resistance on the distributed load is $10 \text{ m}\Omega$. The total capacitance $n \times C_{\text{IN}}$ in [图 9-83](#) was $32 \times 47 \text{ }\mu\text{F}$ of ceramic X7R capacitors.

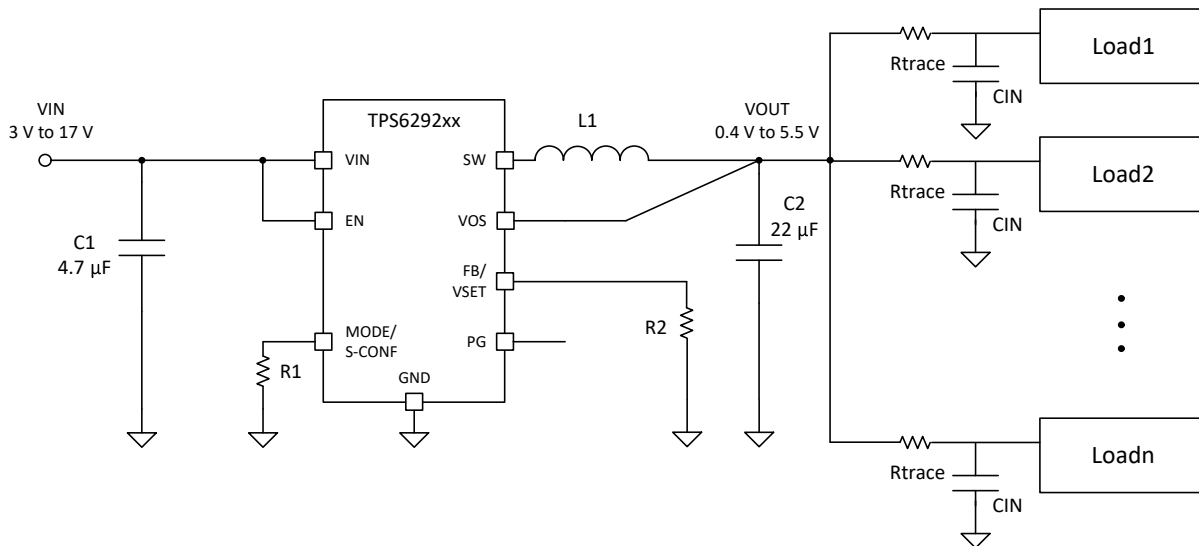


图 9-83. Multiple Loads Example

9.3.2 Inverting Buck-Boost (IBB)

The must generate negative voltage rails for electronic designs is a common challenge. The wide 3-V to 17-V input voltage range of the TPS629210-Q1 makes it ideal for an inverting buck-boost (IBB) circuit, where the output voltage is inverted or negative with respect to ground.

The circuit operation in the IBB topology differs from that in the traditional buck topology. Though the components are connected the same as with a traditional buck converter, the output voltage terminals are reversed. See [图 9-84](#) and [图 9-85](#).

The maximum input voltage that can be applied to an IBB converter is less than the maximum voltage that can be applied to the TPS629210-Q1 in a typical buck configuration. This is because the ground pin of the IC is connected to the (negative) output voltage. Therefore, the input voltage across the device is V_{IN} to V_{OUT} , and not V_{IN} to ground. Thus, the input voltage range of the TPS629210-Q1 in an IBB configuration becomes 3 V to 17 V + V_{OUT} , where V_{OUT} is a negative value.

The output voltage range is the same as when configured as a buck converter, but only negative. Thus, the output voltage for a TPS629210-Q1 in an IBB configuration can be set between -0.4 V and -5.5 V .

The maximum output current for the TPS629210-Q1 in an IBB topology is normally lower than a traditional buck configuration due to the average inductor current being higher in an IBB configuration. Traditionally, lower input or (more negative) output voltages results in a lower maximum output current. However, using a larger inductor

value or the higher 2.5-MHz frequency setting can be used to recover some or all of this lost maximum current capability.

When implementing an IBB design, it is important to understand that the IC ground is tied to the negative voltage rail, and in turn, the electrical characteristics of the TPS629210-Q1 device are referenced to this rail. During power up, as there is no charge in the output capacitor, the IC GND pin (and V_{OUT}) are effectively 0 V, thus parameters such as the V_{IN} UVLO and EN thresholds are the same as in a typical buck configuration. However, after the output voltage is in regulation, due to the negative voltage on the IC GND pin, the device traditionally continues to operate below what can appear to be the normal UVLO/EN falling thresholds relative to the system ground. Thus, special care must be taken if the user is using the dynamic mode change feature on the MODE pin of the TPS629210-Q1 or driving the EN pin from an upstream microcontroller as the high and low thresholds are relative to the negative rail and not the system ground.

More information on using a DCS regulator in an IBB configuration can be found in the [Description Compensating the Current Mode Boost Control Loop Application Note](#) and [Using the TPS6215x in an Inverting Buck-Boost Topology Application Note](#).

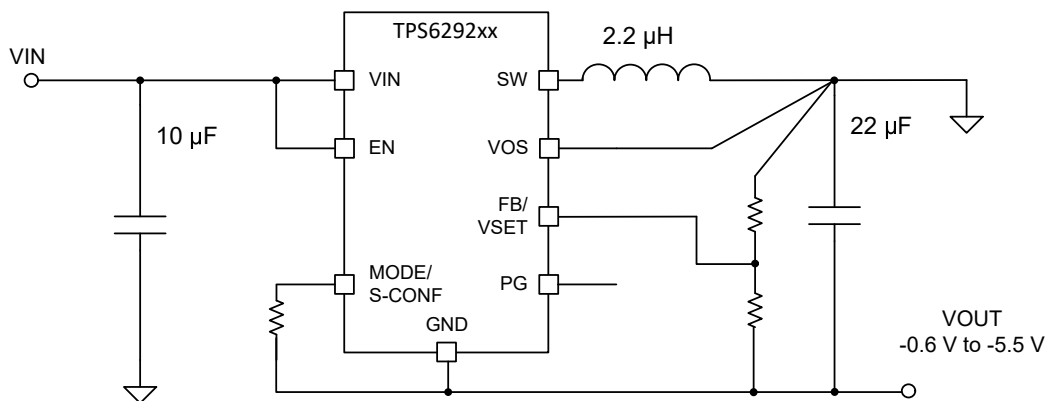


图 9-84. IBB Example with Adjustable Feedback

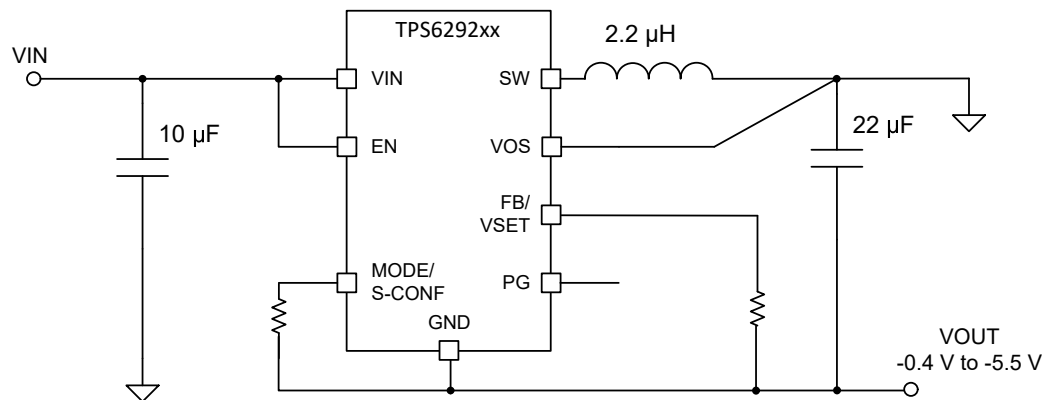


图 9-85. IBB Example with Internal Feedback

9.4 Power Supply Recommendations

The power supply to the TPS629210-Q1 must have a current rating according to the supply voltage, output voltage, and output current of the TPS629210-Q1.

9.5 Layout

9.5.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more so at high switching frequencies. Therefore, the PCB layout of the TPS629210-Q1 demands careful attention to make sure proper operation and to get the performance specified. A poor layout can lead to issues like the following:

- Poor regulation (both line and load)
- Stability and accuracy weaknesses
- Increased EMI radiation
- Noise sensitivity

See [Figure 9-86](#) for the recommended layout of the TPS629210-Q1, which is designed for common external ground connections. The input capacitor must be placed as close as possible between the VIN and GND pin of the TPS629210-Q1.

Provide low inductive and resistive paths for loops with high di/dt. Therefore, paths conducting the switched load current must be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high dv/dt. Therefore, the input and output capacitance must be placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces must be avoided. Loops that conduct an alternating current must outline an area as small as possible, as this area is proportional to the energy radiated.

Sensitive nodes like FB and VOS must be connected with short wires and not nearby high dv/dt signals (for example, SW). As they carry information about the output voltage, they also must be connected as close as possible to the actual output voltage (at the output capacitor). The FB resistors, R1 and R2, must be kept close to the IC and connect directly to those pins and the system ground plane. The same applies for the S-CONFIG/MODE and VSET programming resistors.

The package uses the pins for power dissipation. Thermal vias on the VIN, GND, and SW pins help to spread the heat through the PCB.

In case any of the digital inputs (EN or S-CONF/MODE pins) must be tied to the input supply voltage at VIN, the connection must be made directly at the input capacitor as indicated in the schematics.

The recommended layout is implemented on the EVM and shown in the [TPS629210-Q1 EVM User's Guide](#).

9.5.2 Layout Example

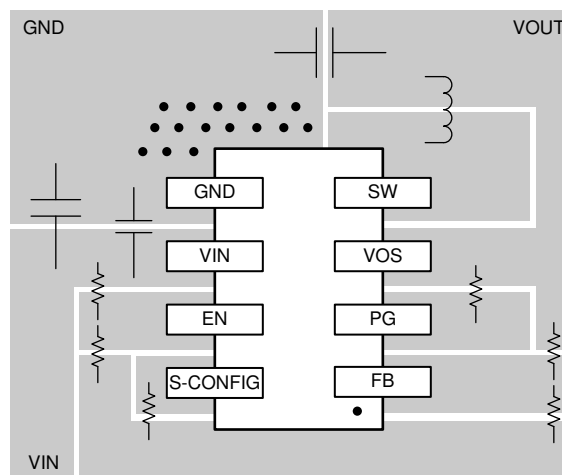


图 9-86. TPS629210-Q1 Layout

9.5.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added

heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

The following are basic approaches for enhancing thermal performance:

- Improving the power dissipation capability of the PCB design (for example, increasing copper thickness, thermal vias, number of layers)
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the [Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs Application Note](#) and [Semiconductor and IC Package Thermal Metrics Application Note](#).

The TPS629210-Q1 is designed for a maximum operating junction temperature (T_J) of 150°C. Therefore, the maximum output power is limited by the power losses that can be dissipated over the actual thermal resistance, given by the package and the surrounding PCB structures. If the thermal resistance of the package is given, the size of the surrounding copper area and a proper thermal connection of the IC can reduce the thermal resistance. To get an improved thermal behavior, TI recommends to use top layer metal to connect the device with wide and thick metal lines. Internal ground layers can connect to vias directly under the IC for improved thermal performance. Additionally, the DYC package option (see [图 6-2](#)) with extended leads can also be used to further reduce the thermal resistance of a design.

If short circuit or overload conditions are present, the device is protected by limiting internal power dissipation.

10 Device and Documentation Support

10.1 Device Support

10.1.1 第三方产品免责声明

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10.1.2 Development Support

10.1.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the TPS629210-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs Application Note](#)
- Texas Instruments, [Semiconductor and IC Package Thermal Metrics Application Note](#)
- Texas Instruments, [TPS629210-Q1EVM User's Guide](#)
- Texas Instruments, [Description Compensating the Current Mode Boost Control Loop Application Note](#)
- Texas Instruments, [Using the TPS6215x in an Inverting Buck-Boost Topology Application Note](#)
- Texas Instruments, [Optimizing the TPS62130/40/50/60 Output Filter Application Note](#)
- Texas Instruments, [Optimizing Transient Response of Internally Compensated DC-DC Converters Application Note](#)
- Texas Instruments, [Description Compensating the Current Mode Boost Control Loop Application Note](#)

10.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.4 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

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10.6 静电放电警告



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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.7 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS629210QDRLRQ1	ACTIVE	SOT-5X3	DRL	8	4000	RoHS & Green	Call TI SN	Level-1-260C-UNLIM	-40 to 150	T210	Samples
TPS629210QDYCRQ1	ACTIVE	SOT-5X3	DYC	8	4000	RoHS & Green	Call TI SN	Level-1-260C-UNLIM	-40 to 150	T10Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS629210-Q1 :

- Catalog : [TPS629210](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS629210QDRLRQ1	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3
TPS629210QDYCRQ1	SOT-5X3	DYC	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS629210QDRLRQ1	SOT-5X3	DRL	8	4000	210.0	185.0	35.0
TPS629210QDYCRQ1	SOT-5X3	DYC	8	4000	210.0	185.0	35.0

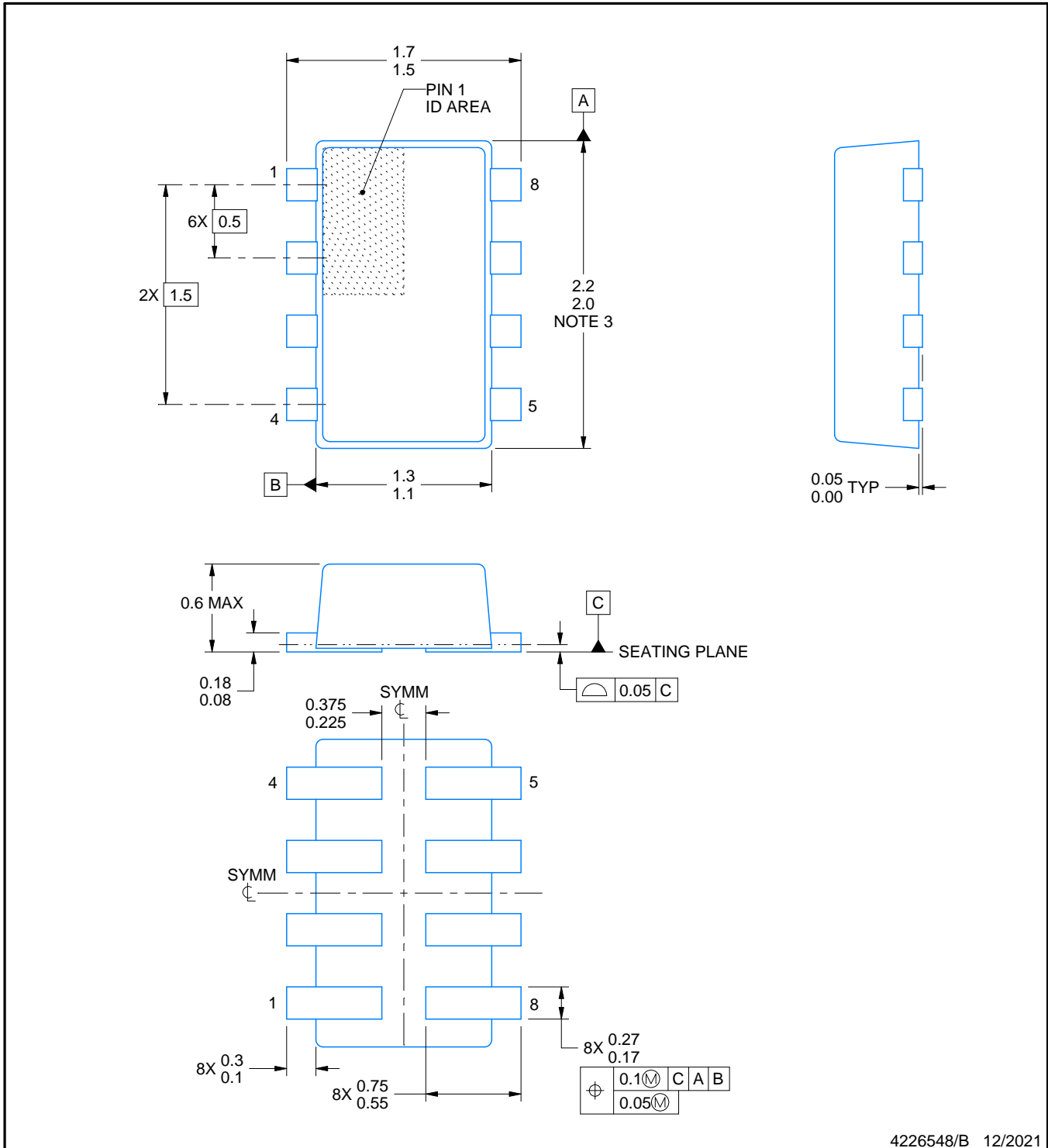
DYC0008A



PACKAGE OUTLINE

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



4226548/B 12/2021

NOTES:

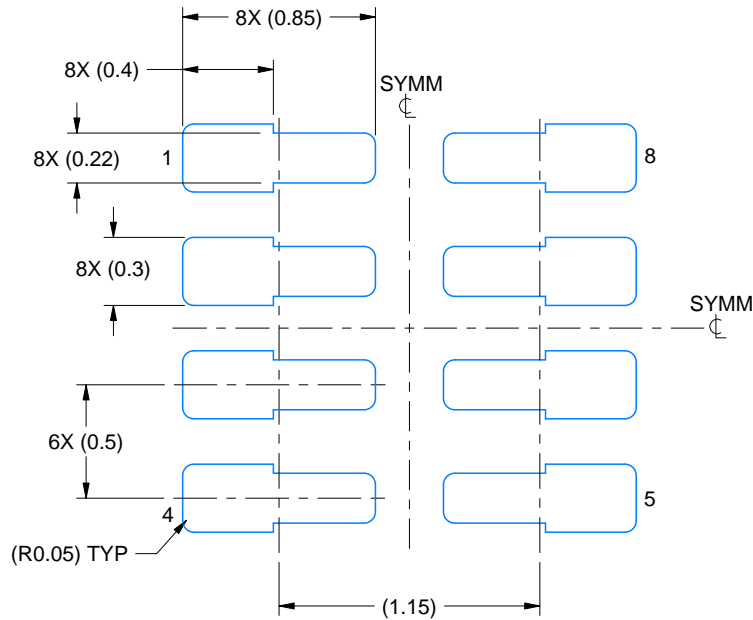
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

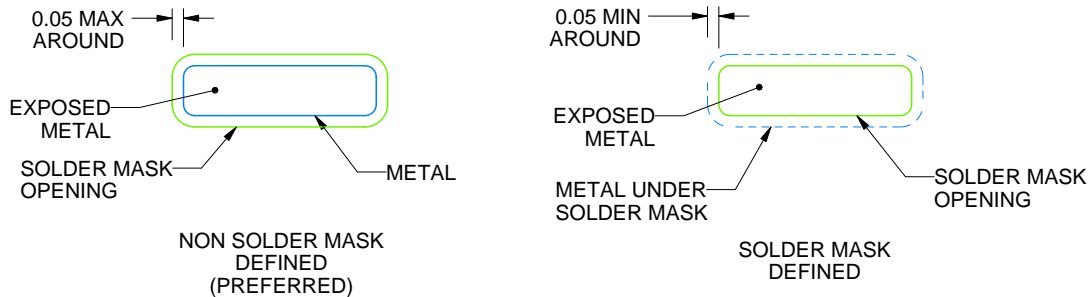
DYC0008A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDERMASK DETAILS

4226548/B 12/2021

NOTES: (continued)

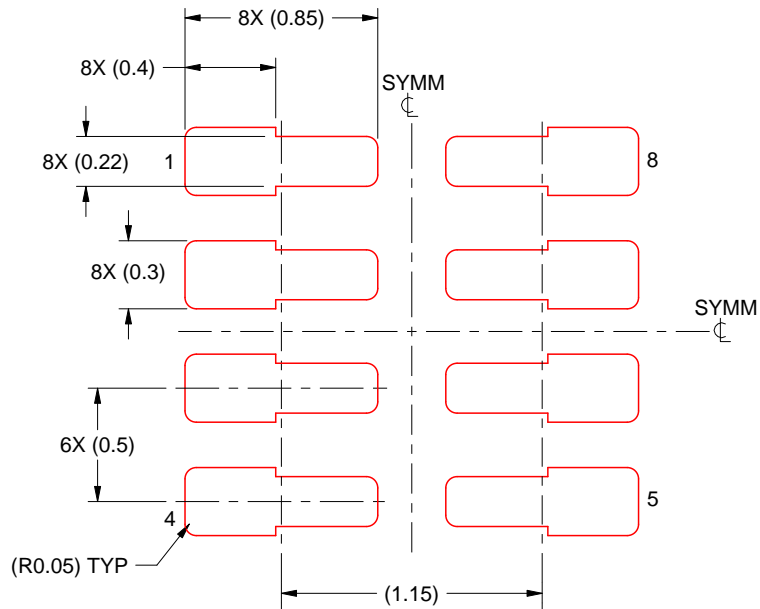
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DYC0008A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4226548/B 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

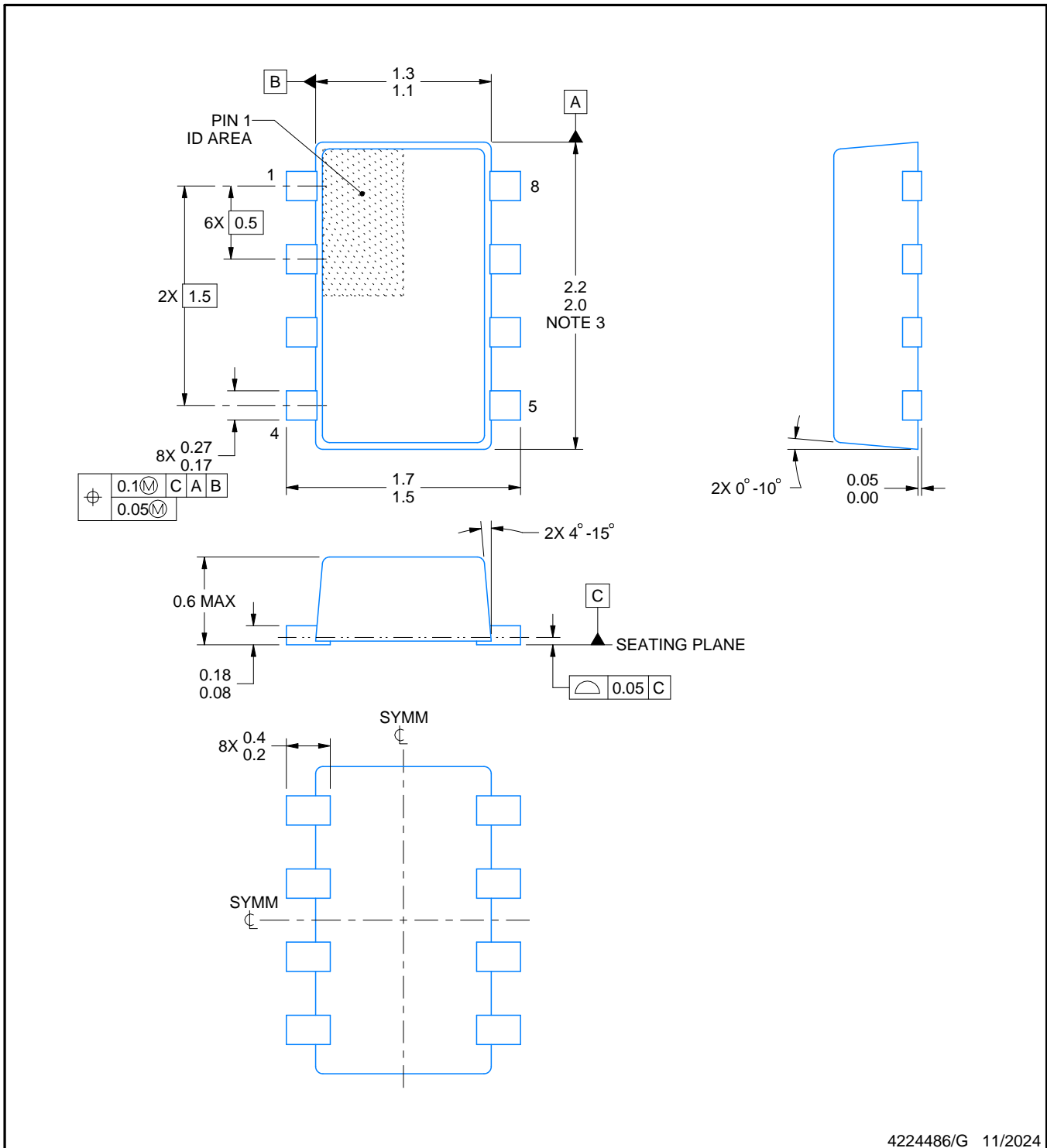
DRL0008A



PACKAGE OUTLINE

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



4224486/G 11/2024

NOTES:

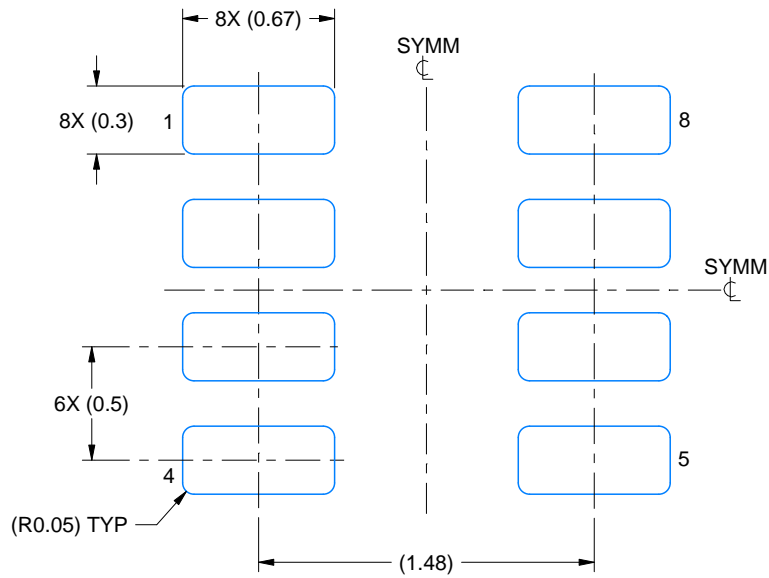
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

EXAMPLE BOARD LAYOUT

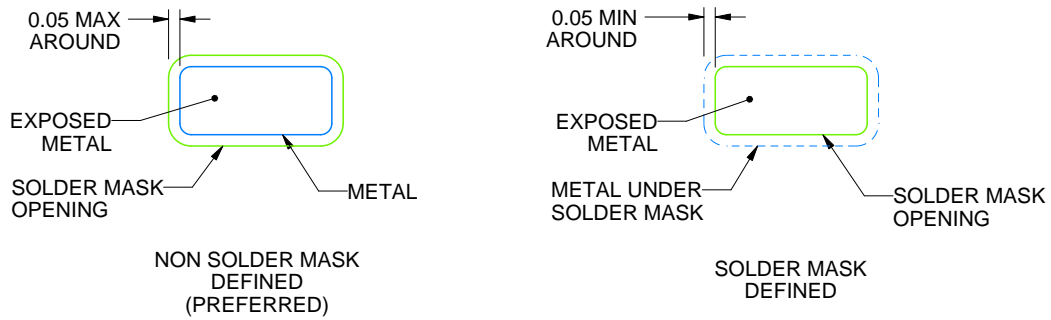
DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDERMASK DETAILS

4224486/G 11/2024

NOTES: (continued)

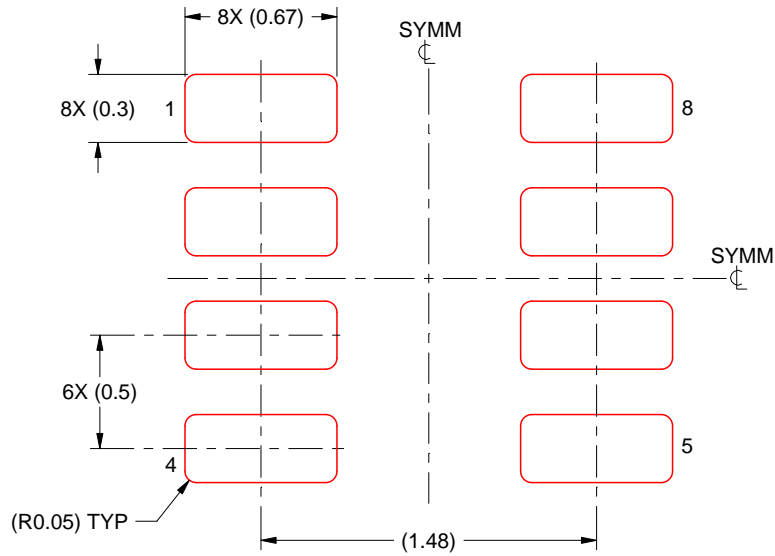
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4224486/G 11/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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