TI Designs：TIPD173
适用于单端多路复用器应用的 16 位 1MSPS 数据采集 参考设计

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资源

TIPD173	设计文件夹
TINA-TI™	产品文件夹
ADS8860	产品文件夹
OPA320	产品文件夹
OPA333	产品文件夹
THS4281	产品文件夹
REF5040	产品文件夹
REF6040	产品文件夹

电路 描述

TIPD173 TI 设计描述了 16 位 1MSPS 单端数据采集 (DAQ) 块的系统性设计方法。该设计 采用了 一个 16 位高精度逐次逼近型寄存器 (SAR) 模数转换器 (ADC)；用于驱动 ADC 输入的低噪声、低功耗和宽带宽电路；以及用于驱动 ADC 参考输入的外部极低漂移参考驱动器电路。该设计经过优化，可在多路复用 应用中实现出色的趋稳时间、功耗、静态性能和动态性能。

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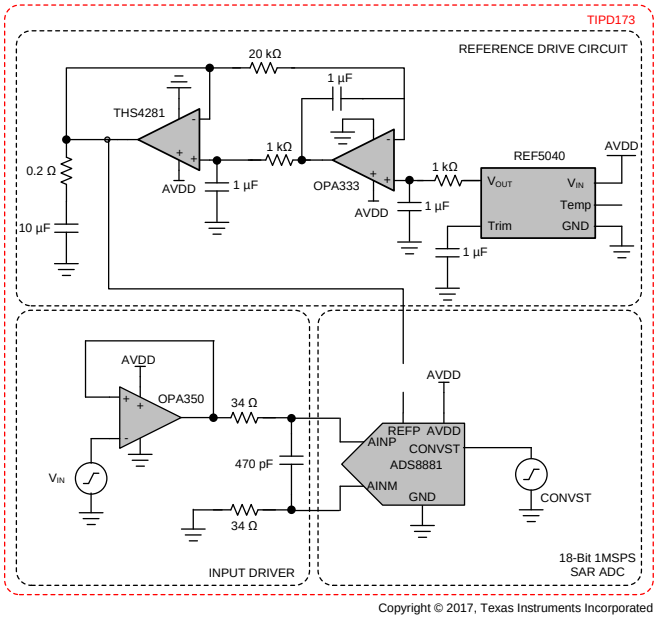

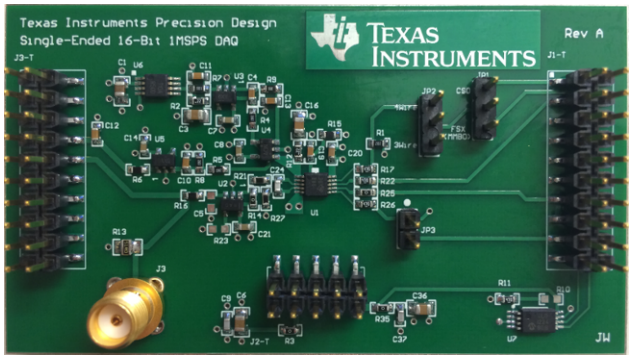

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1 System Overview

1.1 Design Summary

The primary objective for this design is to create a 16-bit, 1-MSPS, single-ended DAQ system that is optimized to achieve excellent transient settling performance for a full-scale step input signal. The design requirements for this block design are as follows:

- System supply voltage: 5-V DC
- ADC supply voltage: 3.3-V DC
- ADC sampling rate: 1 MSPS
- ADC reference voltage: 4.096-V DC
- ADC input signal range: A step input range from 0.1 V to V_{REF}. The system does not utilize a negative supply; therefore, the minimum input signal is limited by the input output limitation of the operational amplifier (op amp) to avoid any signal distortion.

1.2 Key System Specifications

表 1 summarizes the design goals and performance. 图 1 shows the system specification containing the low power, fast settling time, static performance, and dynamic performance.

表 1. Comparison of Design Goals, Simulation, and Measured Performance

PARAMETERS	SPECIFICATION	SIMULATION	MEASURED
Total power	≤ 25 mW	—	21.5 mW
16-bit settling time(1)	≤ 900 ns	852 ns	850 ns
Effective resolution$_{SYS}$	16 bits	—	16 bits
Linearity error	< ±2 LSB	—	< ±0.5 LSB
Signal-to-noise ratio$_{SYS}$ (SNR$_{SYS}$)(2)	> 90 dB	—	90.5 dB
Total harmonic distortion$_{SYS}$ (THD$_{SYS}$)	< –104 dB	—	–105.4 dB
Effective number of bits$_{SYS}$ (ENOB$_{SYS}$)	> 14.5 bits	—	14.58 dB

(1) The 16-bit settling time starts when the multiplexer changes the channel.

(2) The signal-to-noise ratio (SNR) and settling time are the most important performance trade-offs addressed in this design. If a low-cutoff-frequency input filter is implemented to achieve lower noise, the large RC time constant results in longer settling time and vice versa.

图 1 shows the resulting measured data for the worst-case scenario, which is the multiplexer switching channels having the input swing form the negative rail to the positive, and vice versa.

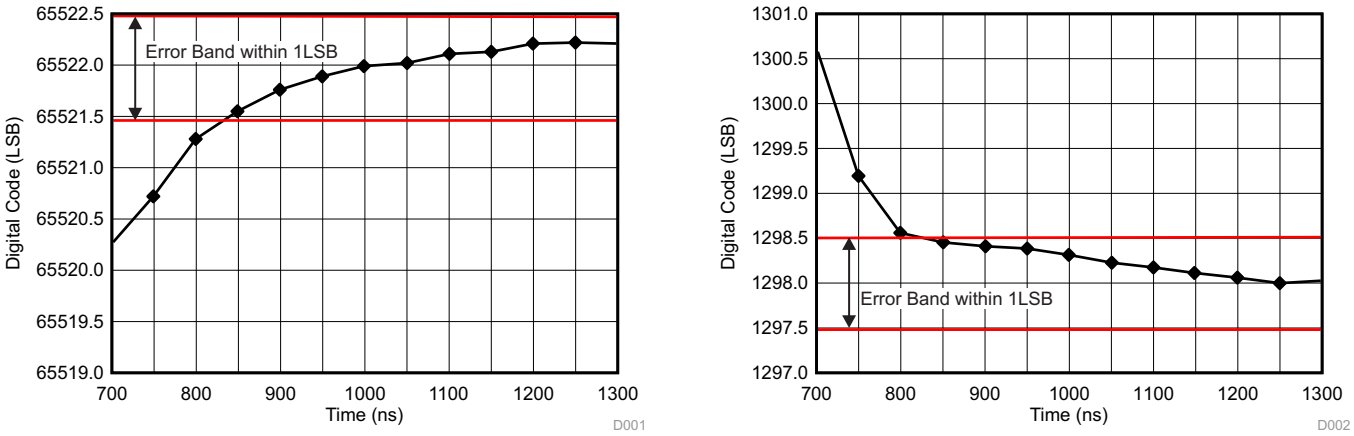


图 1. Measurement Result of Settling Time Plot for Multiplexed Data Acquisition Block(1) Rising Full-Scale Input and Falling Full-Scale Input

(1) Each test measurement in 图 1 includes an average of 1000 data points to reduce the noise.

2 System Design Theory

2.1 Theory of Operation

The TIPD173 TI Precision Design discusses the design methodology for a 16-bit, 1-MSPS single-ended DAQ block. Common applications for this design are temperature, pressure, biopotential measurements, and power measurement. The DAQ system can be broken into three parts: the reference driver, input driver, and ADC. The combined performance of these three parts determine the overall system performance. The theoretical design method, which this section explains, uses the specifications to optimize the design.

- **Step 1: Choose the appropriate ADC that meets the system specification**

  This system uses a SAR ADC with excellent AC performance for very low power consumption to meet the specifications for this TI design. The SAR ADC architecture meets the total power budget of this design and provides fast settling. Some other alternatives are delta-sigma ($\Delta\Sigma$) and pipeline ADCs. Although the $\Delta\Sigma$ ADC has very high resolution due to oversampling and noise shaping, the high power consumption does not fit the system specification when operating at 1 MSPS. However, the pipeline ADC can easily obtain a very high sample rate, but 16-bit resolution is not easily attainable.

- **Step 2: Select the proper input driving amplifier and charge bucket**

  For a high sampling rate, the input amplifier must be designed to perform the sample-and-hold function quickly and accurately. If the ADC input signal cannot settle to the specified error during the acquisition time, the performance is extremely degraded. A well-designed charge bucket attenuates the noise and provides high precision. Because the charge bucket constitutes a capacitive load, the stability of the input driving amplifier must also be considered during the design of the input driver circuit.

- **Step 3: Design a high-precision reference driver**

  A well-designed reference driver provides low offset, low drift, and a low-noise reference voltage. A poorly-designed reference driver can seriously impact system performance. 图 2 summarizes the important design criteria for each circuit block used in the design of a complete DAQ system.

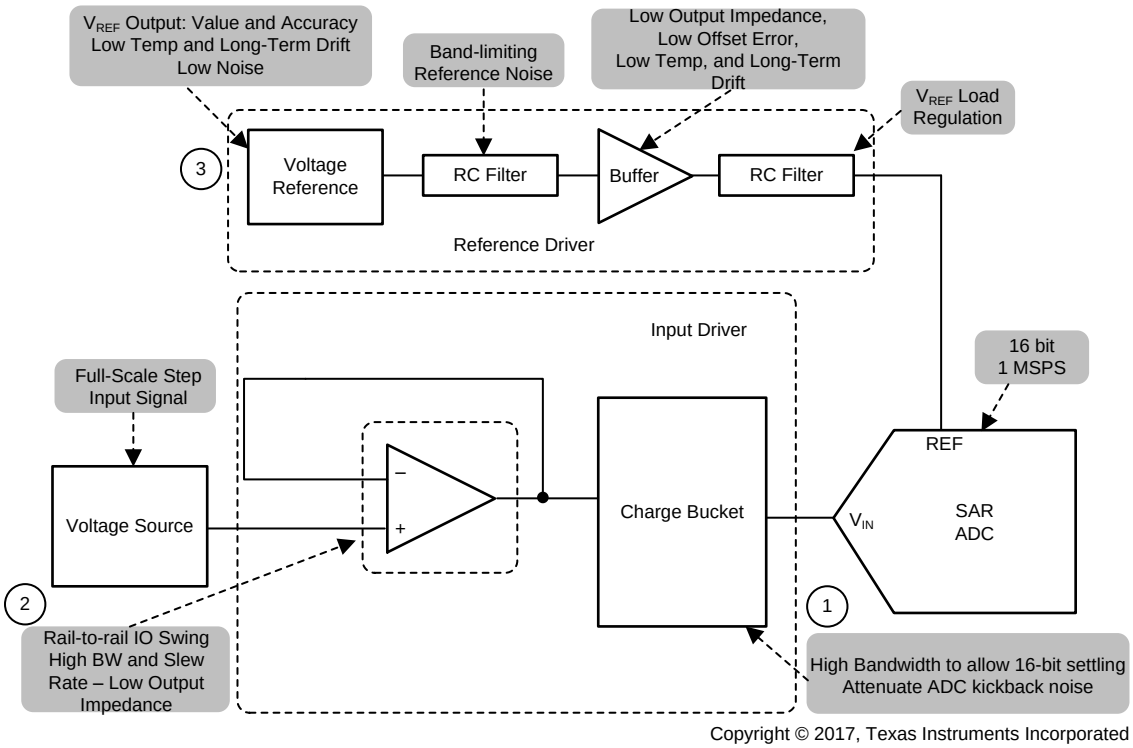


图 2. System Block Diagram Highlighting Primary Design Criteria

2.2 Understanding DAQ Performance

The main system specifications for this design are settling time, INL, effective resolution, signal-to-noise ratio (SNR), total harmonic distortion (THD), signal-to-noise distortion ratio (SINAD), and effective number of bits (ENOB). These specifications can be categorized into three groups: settling time, static performance, and dynamic performance. These specifications are not independent of each other and every DAQ design involves a balance between these parameters. This performance trade-off during design is based on the system requirements of a particular application. For example, static performance is the key parameter for systems that are designed to test DC input signals such as temperature measurement. In audio applications, achieving good dynamic performance is critical. The application described in this design is a multiplexed application. In such applications, settling time is the key parameter to influence static and dynamic performance. If the input signal does not settle within the required accuracy, the result is degradation of the linearity and distortion performance of the system.

2.2.1 Settling Time

Settling time is the time required for an output to reach and remain within an error band from an ideal instantaneous step input. The error band is usually set within 1 LSB for good accuracy. Higher system resolution requires narrow error bands. Settling time is determined by the slew rate and recovery of the input driving amplifier, as 图 3 shows.

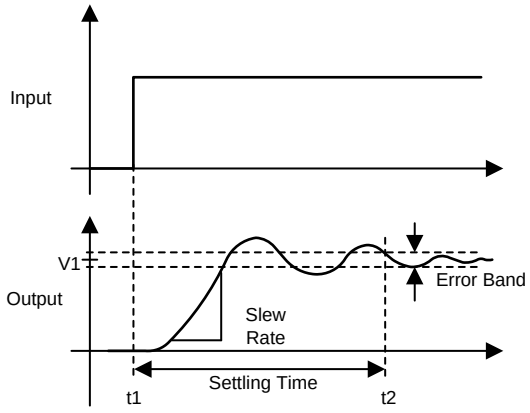
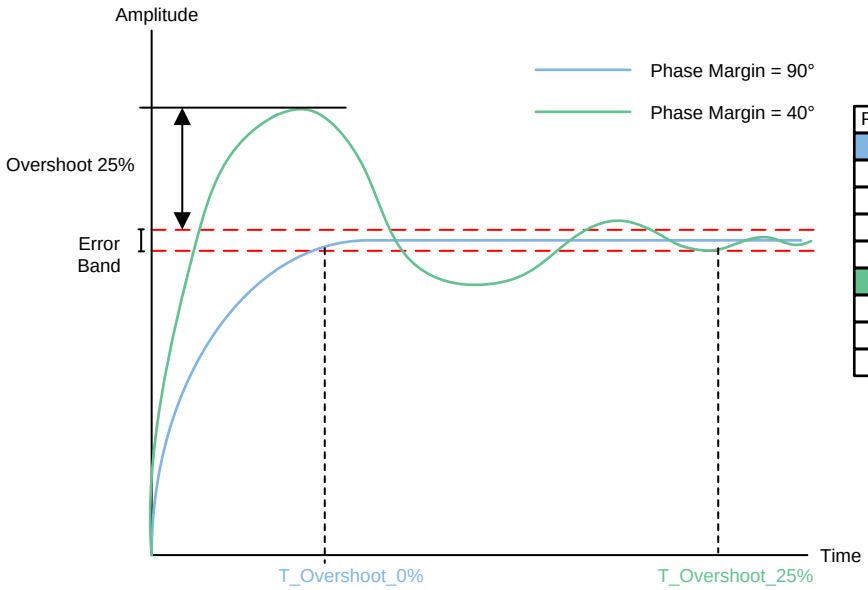


图 3. Definition of Settling Time

The recovery time for an amplifier output is most important for fast input settling. If the amplifier has a low phase margin, this causes the overshoot to increase and hence, increases the time to settle. 图 4 shows the effect of variable phase margins on the output overshoot and step response of the amplifier. The blue line shows the output signal for a 90º phase margin system with a much lower settling time (see T_Overshoot_0%). Comparing the response of the two signals, the signal with 40° phase margin (see green trace) has a much longer settling time (see T_overshoot_25%). Therefore, designing a high-phase margin system is important to settle the input signal rapidly. This design uses the method of increasing the Riso for phase compensation; however, increasing the phase margin results in a larger RC time constant, which adversely affects the input settling performance. This trade-off is the most important consideration that requires optimization in this design.



Phase Margin	Overshoot
90°	0
80°	2%
70°	5%
60°	10%
50°	16%
40°	25%
30°	37%
20°	53%
10°	73%

图 4. Overshoot versus Phase Margin

2.2.2 Static Performance

Static performance is a measure of the DAQ accuracy for a DC input signal. In this application, the DC performance is important if the signals that are connected to the multiplexer are DC.

2.2.2.1 Effective Resolution

Effective resolution$_{SYS}$ is a measurement of the static performance of a DAQ. For constant DC inputs, the output error of the ADC is a result of the combination of noise from the input drivers, ADC, reference voltage, power supplies, and so forth. System noise produces an approximate Gaussian code distribution at the ADC output, as 图 5 shows.

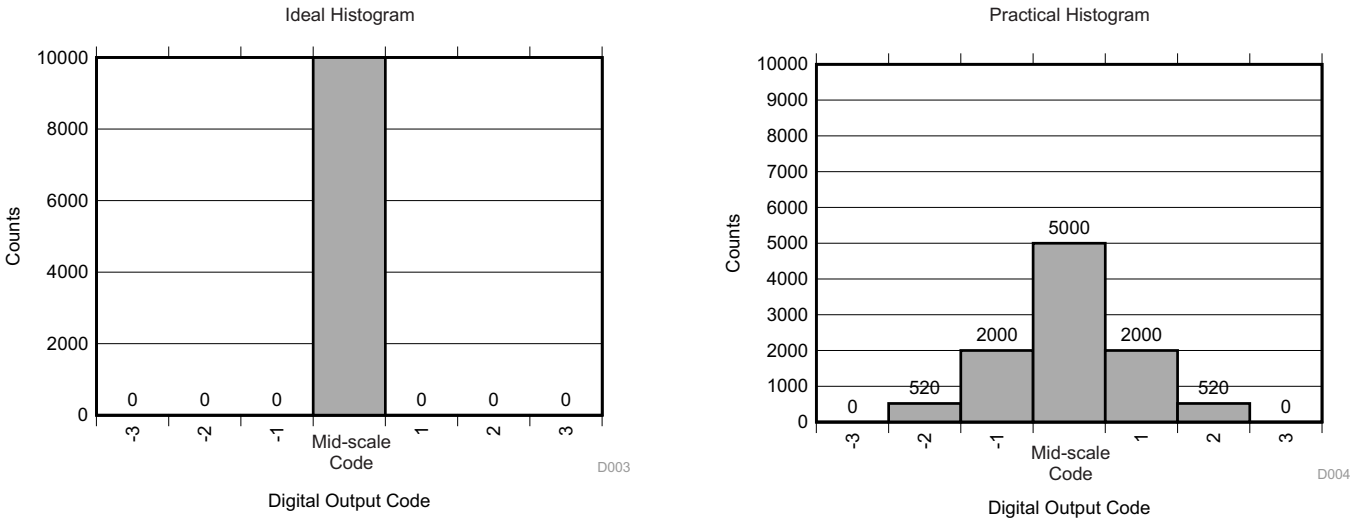


图 5. Histogram of ADC Output Codes for Constant Midscale DC Input

The effective resolution is calculated using 公式 1, which shows how noise decreases the effective resolution:

$$\text{Effective Resolution}_{SYS} = N - \log_2(\sigma_{HISTO\_SYS\_NOISE}) \quad (1)$$

where,

- Effective resolution$_{SYS}$ = DC measurement of the system resolution including the effect of noise
- N = ADC resolution
- $\sigma_{HISTO\_SYS\_NOISE}$ = the standard deviation of the measured system noise in fractions of LSB.

Directly using the ADC resolution to evaluate the total system performance is insufficient. The overall system accuracy decreases because there is additional noise contribution by the input driver, reference voltage, and ADC. The effective resolution accurately reflects the static resolution. Note that $\sigma_{HISTO\_SYS\_NOISE}$ is measured and varies for different driver and reference schemes

2.2.2.2 Linearity

Integral nonlinearity (INL, also known as relative accuracy error) is the maximum deviation between an actual code transition point (dashed line) and its corresponding ideal transition point (solid line) after gain and offset error have been removed (see 图 6). Even though the ADC has a specific INL, the INL degrades if the sampling capacitor has not settled to a 16-bit accuracy.

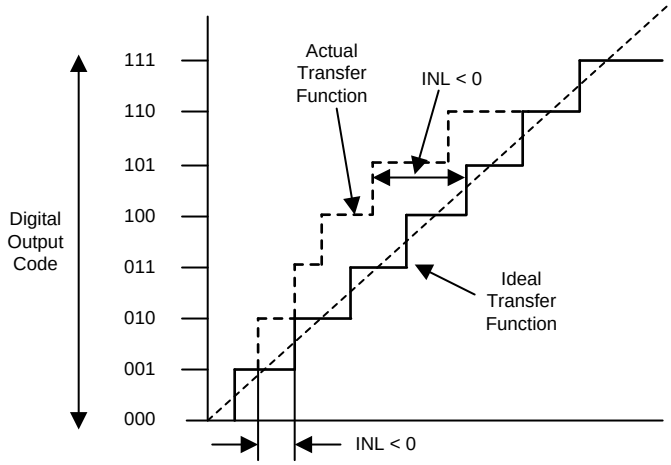


图 6. Definition of Integral Nonlinearity (INL)

2.2.3 Dynamic Performance

Dynamic performance is the measure of the DAQ accuracy for an AC input signal. The most important metrics to assess the dynamic performance of the system are SNR, THD, SINAD, and ENOB. 图 7 shows a comparison of an ideal and digitized sine wave after the spectrum analysis. The pure sine wave goes through the amplifier, ADC, and fast Fourier transform (FFT) to obtain the digitized sine wave. The harmonic distortion and noise floor result in a deviation of the input signal from the ideal waveform.

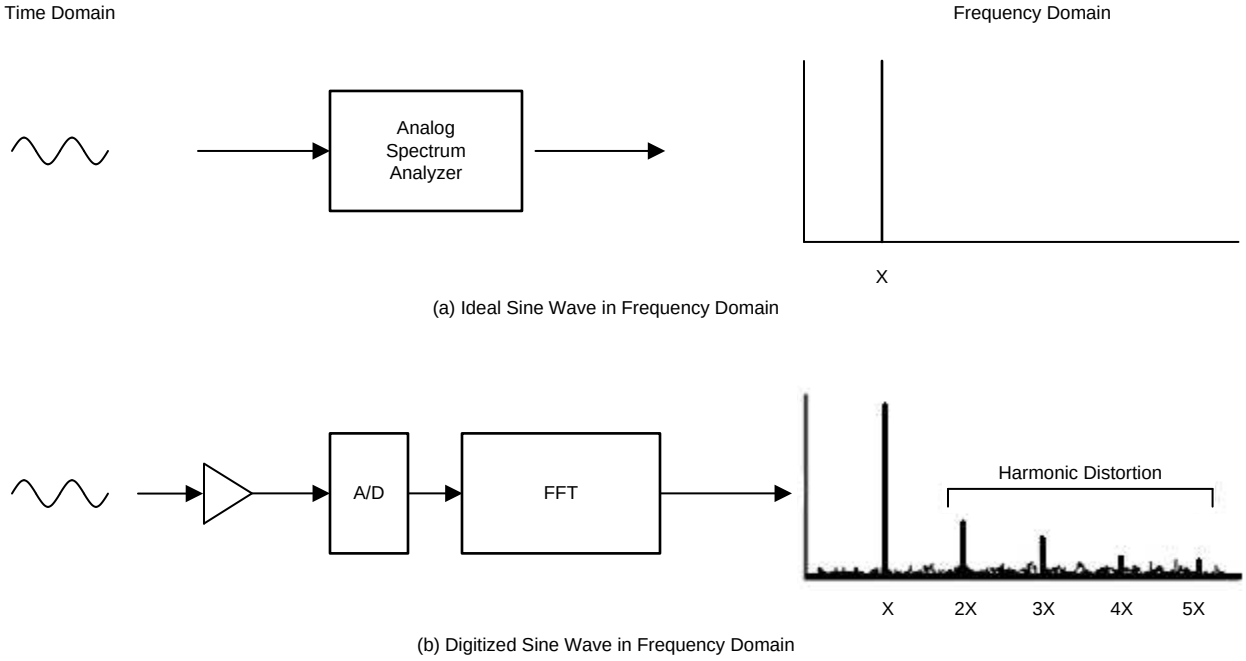


图 7. Comparison of (A) Ideal and (B) Digitized Sine Wave in Frequency Domain

The dynamic performance of a DAQ can be analyzed considering the harmonic distortion and noise separately. The frequency domain plot in 图 8 shows the meaning of each AC parameter.

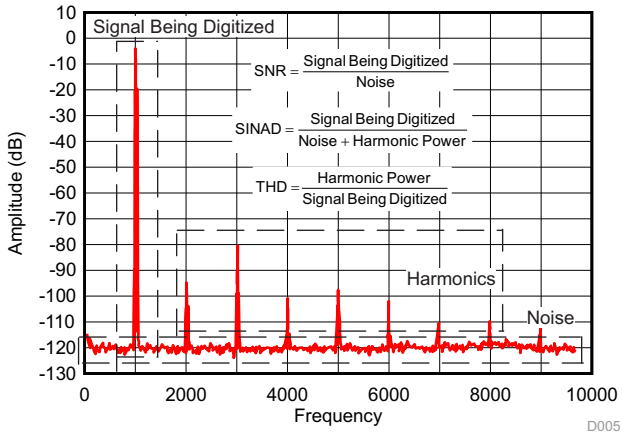


图 8. Dynamic Specifications of ADC

2.2.3.1 Signal-to-Noise Ratio (SNR)

SNR_{SYS} provides an insight into the total noise of the system. The total noise of the DAQ is the root sum square (RSS) of the input driver noise ($V_{n\_AMP\_RMS}$) and the ADC noise ($V_{n\_ADC\_RMS}$), as 公式 2 shows. The ADC noise includes the quantization noise as well as the noise contributed by the ADC internal circuitry. The total noise ($V_{n\_TOT\_RMS}$) referred to the input of the ADC is used for calculating the total SNR of the system (SNR_{SYS}), as 公式 3 shows:

$$V_{n\_TOT\_RMS} = \sqrt{V_{n\_AMP\_RMS}^2 + V_{n\_ADC\_RMS}^2} \tag{2}$$

where,

- Vn_TOT_RMS = system total noise
- Vn_AMP_RMS = input driver noise
- Vn_ADC_RMS = ADC noise including reference noise

$$SNR_{SYS}(dB) = 20\log\frac{V_{SIG\_RMS}}{V_{n\_TOT\_RMS}} \tag{3}$$

where,

- SNR_{SYS} = system signal-to-noise ratio
- V_{SIG_RMS} = RMS value of input signal
- $V_{n\_TOT\_RMS}$ = system total noise.

2.2.3.2 Total Harmonic Distortion (THD)

Total harmonic distortion (THD) is defined as the ratio of the RSS of all harmonic components (generally nine harmonics are used) to the power of the fundamental signal frequency. THD is generally specified with an input signal near full scale (FS). If the RMS value of an input signal is denoted as V_{SIG_RMS} and the power in N^{th} harmonic is denoted by $V_{HAR\_n\_RMS}$, then the total harmonic distortion ($V_{HAR\_TOT\_RMS}$) and THD can be calculated as shown in 公式 4 and 公式 5:

$$V_{HAR\_TOT\_RMS} = \sqrt{V_{HAR\_1\_RMS}^2 + V_{HAR\_2\_RMS}^2 + \ldots\ldots + V_{HAR\_9\_RMS}^2} \tag{4}$$

where,

- $V_{HAR\_TOT\_RMS}$ = total harmonic distortion
- $V_{HAR\_n\_RMS}$ = power in N^{th} harmonics

$$THD_{SYS}(dB) = 20\log\frac{V_{HAR\_TOT\_RMS}}{V_{SIG\_RMS}} \tag{5}$$

where,

- THD_{SYS} = ratio of all harmonic component to the power of the fundamental signal frequency
- $V_{HAR\_TOT\_RMS}$ = total harmonic distortion
- V_{SIG_RMS} = RMS value of input signal.

2.2.3.3 Signal-to-Noise and Distortion Ratio (SINAD)

$SINAD_{SYS}$ combines the effect of distortion and noise to provide a cumulative measure of the overall dynamic performance of the system, as 公式 6 shows:

$$SINAD_{SYS}(dB) = 20\log\frac{V_{SIG\_RMS}}{\sqrt{V_{n\_TOT\_RMS}^2 + V_{HAR\_TOT\_RMS}^2}} \quad (6)$$

where,

- $SINAD_{SYS}$ = system signal-to-noise and distortion ratio
- V_{SIG_RMS} = RMS value of input signal
- $V_{HAR\_TOT\_RMS}$ = total harmonic distortion.

2.2.3.4 Effective Number of Bits (ENOB)

$ENOB_{SYS}$ is an effective measurement of the quality of a digitized signal from an ADC by specifying the number of bits above the noise floor (see 公式 7):

$$ENOB_{SYS} = \frac{SINAD_{SYS} - 1.76}{6.02} \quad (7)$$

where,

- $SINAD_{SYS}$ = system signal-to-noise and distribution ratio
- $ENOB_{SYS}$ = effective number of bits.

2.3 Design Consideration of DAQ for Multiplexed Application

The primary design consideration for a multiplexed application is settling time. If the settling time is too large such that the signal cannot converge within the specified error band, then errors occur that are greater than the expected device errors. The error affects both static and dynamic performance. This design is based on the worst-case scenario which is switching between different channels, where one channel is at the negative full-scale (NFS) voltage and the other channel is at the positive full-scale (PFS) voltage. In this case, the step size is the full-scale range (FSR); therefore, the input driver requires the longest time to settle within the error band. The time it takes to change channels also affects the settling time of the system.

In this design, the time for a multiplexer to switch channels and settle to a full-scale step at the amplifiers input is assumed to be less than 100 ns. This is a constraint of the multiplexer transition time and input settling that work for this design. The NFS and PFS levels are the lowest and highest voltage inputs that do not violate the input and output limitations. A voltage of 3.3 V and 5 V is used to supply the digital and analog circuit. 图 9 shows the signal path and timing diagram of operation for a multiplexed application. Conversion of an SAR ADC can be broken into the sampling and conversion phase. In the conversion phase, the S1 switch opens and S2 switch closes. While the ADC is converting, the system spends multiplexer switching time (t_{MUX}) to switch the channels and a quiet time period (t_{QT}) for signal slewing and recovery. In the sampling phase, the S1 switch closes and the S2 switch opens the spending acquisition time (t_{ACQ}), 图 9 shows.

The settling time must be divided into three parts: slew region, recovery region, and settling region. The importance of the recovery region is already discussed in 节 2.2.1. One important thing is the voltage drop (ΔV) between the period of conversion and sampling due to the kickback caused by the classic SAR architecture. This is caused by the charging and discharging of the internal capacitor when the SAR ADC starts to sample and hold the signal. Therefore, the ADC requires time to recover within the specified error band. The time for settling depends on the ΔV and RC time constant. If the ΔV and RC time constant are too big, t_{ACQ} may not allow sufficient time to guarantee settling within the specified error band. Different ADCs have varied timing constraints for sampling and conversion. Multiplexer switching, buffer transition,

and charge bucket settling must be completed within 1 μs for the 1-MSPS design target of this DAQ. Each part of the sample and conversion cycle is sequential, so the delay at any stage affects the overall timing. For example, if a slower multiplexer is used, then less time is available for the amplifier to slew and settle. Hence, the amplifier requires a higher slew rate and gain bandwidth product to reduce the time to settle. However, the high slew rate and gain bandwidth product correlates with higher power consumption. Each part of the design affects the system performance. Realizing the trade-offs between varied component selections for this specific application is important.

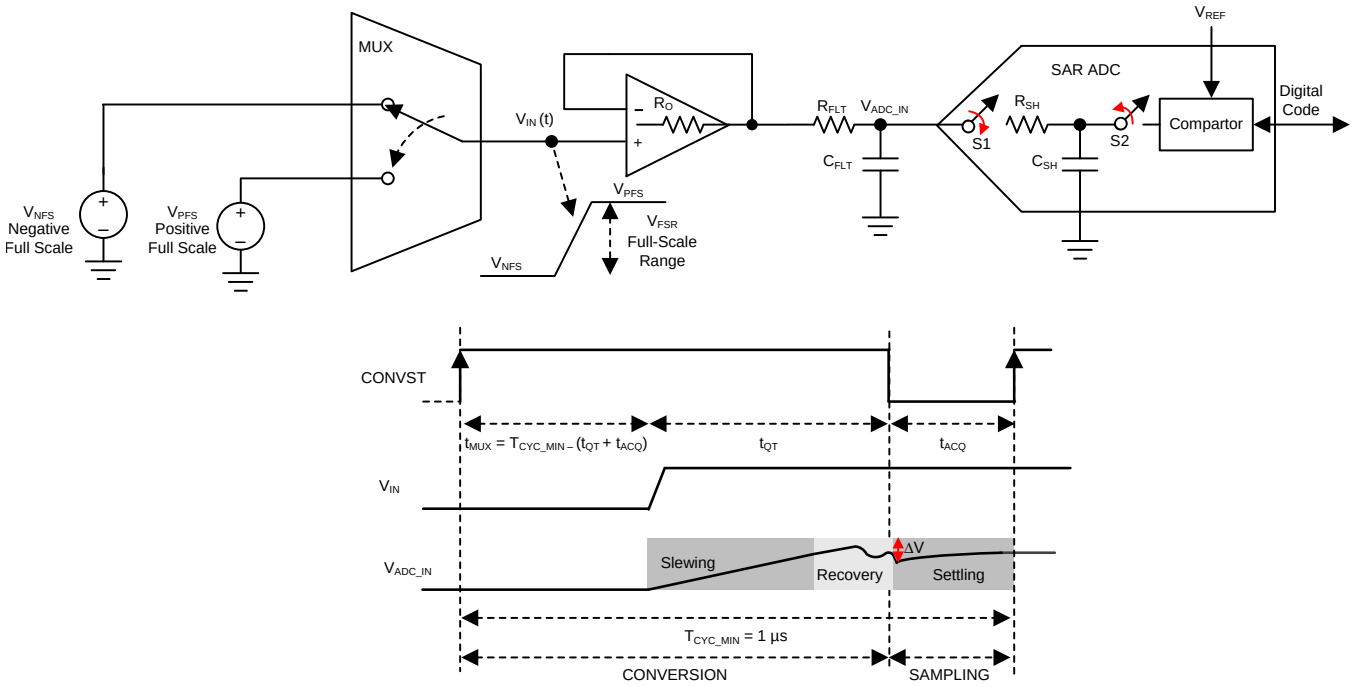


图 9. Timing Diagram of Settling Time in DAQ

2.4 Input Driver

An ADC input driver is composed of a driving amplifier and charge bucket. The driving amplifier provides the high driving capability for fast settling in a specified error band. The charge bucket is used for reducing the noise to prevent the aliasing and reduce the kickback noise during switching. The capacitor of the charge bucket also acts as a good charge reservoir to quickly charge the internal sample-and-hold capacitor during the acquisition process. Timing can roughly be calculated as t_{QT} and t_{ACQ} using the slew rate and RC first-order equation, as 图 10 shows. However, the phase margin must be high to increase the accuracy of the calculated timing. The practical circuit is a second-order system; therefore, when the phase margin is low, the V_{ADC_IN} will have the overshoot during settling and cause a longer recovery time. Hence, the different combination of amplifier and RC filter affects the varied time for settling.

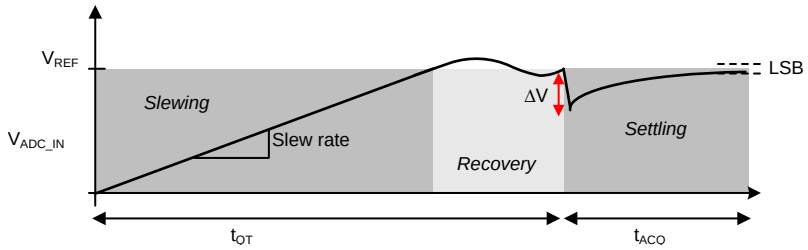


图 10. Typical Input Settling Time Response

2.4.1 Charge Bucket Design

A good charge bucket design must provide sufficient charge to replenish the internal SAR sampling capacitor. The charge bucket design must also maintain amplifier stability and settling time. The schematic in 图 11 shows the simplified behavior of a single-ended ADC input stage. The purpose of C_{FLT} is to replenish the charge on the internal sampling capacitor CSH when S1 is closed. R_{FLT} must be large enough to allow the amplifier to maintain stability, but must be small enough to allow settling during the settling period. The charge bucket design involves selecting C_{FLT} and R_{FLT}, which must meet the criteria for charge replenishment, stability, and settling time.

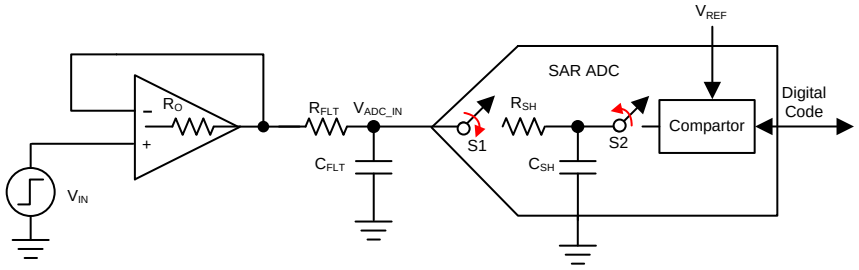


图 11. Simplified Schematic of Single-Ended ADC Input Stage

2.4.1.1 Reducing Charge Kickback—Replenish Charge on C_{SH}

The capacitor C_{FLT} helps to reduce the kickback noise at the ADC input and provides a charge bucket to quickly charge the input capacitor C_{SH} during the sampling process. The ideal value to select for the capacitor C_{FLT} is the largest possible. The usual basic guideline is that, when the S1 switch closes, the voltage droop (ΔV) on C_{FLT} is less than 5% of the input voltage. 公式 8 shows the charge required for an ADC sampling capacitor from zero to full scale in the worst-case scenario.

$$Q_{IN} = C_{SH} \times V_{REF} \tag{8}$$

公式 9 calculates the charge supplied by a filter cap:

$$Q_{FLT} = C_{FLT} \times \Delta V \leq C_{FLT} \times (0.05\ V_{REF}) \tag{9}$$

By the principle of charge conservation, the charge required by the sampling capacitor must be equal to the charge provided by the filter capacitor, as 公式 10 shows.

$$Q_{FLT} = Q_{IN} \tag{10}$$

$$C_{FLT} \times (0.05\ V_{REF}) \geq C_{SH} \times V_{REF} \tag{11}$$

$$C_{FLT} \geq 20 \times C_{SH} \tag{12}$$

Therefore, the capacitor C_{FLT} can be chosen according to the size of input capacitor C_{SH}, as the previous 公式 12 shows. In this design, the charge contributed by C_{FLT} must be reduced for a higher value of an isolation resistor based on the same RC time constant to increase the phase margin (as discussed in 2.4 节).

2.4.1.2 Stability

Understanding the trade-offs involved in selecting the values of C_{FLT} and R_{FLT} is important. If the value of C_{FLT} is high, it provides better attenuation against the kickback noise when the sampling switch closes. However, C_{FLT} cannot be made arbitrarily high because it degrades the phase margin of the driving amplifier, thus making it unstable. The series resistor R_{FLT} acts as an isolation resistor, which helps to stabilize the driving amplifier. A higher value of R_{FLT} is helpful from the amplifier stability perspective, but degrades AC performance and should be balanced with the amplifier stability to ensure that the distortion

does not exceed the required specifications. The distortion occurs because of the non-linear input impedance of the ADC and it increases with source impedance, input signal frequency, and amplitude. The minimum value for R_{FLT} is dependent on the output impedance of the amplifier based on stability considerations. If the open-loop output impedance of the driving amplifier is equal to R_O, its stability can be analyzed by evaluating the effect of R_{FLT} and C_{FLT} on the open-loop response (A_{OL}) of the amplifier (see 图 12). The combination of R_O, R_{FLT}, and C_{FLT} introduces one pole, f_P (see 公式 13), and one zero, f_Z (see 公式 14), in the open-loop response of the amplifier, for which the corner frequencies are given as follows:

$$f_P = \frac{1}{2\pi (R_O + R_{FLT}) C_{FLT}} \tag{13}$$

$$f_Z = \frac{1}{2\pi R_{FLT} C_{FLT}} \tag{14}$$

To ensure that the phase change from the zero negates the phase change that the pole initiates, it is important that the frequency distance between the pole and zero must be less than or equal to one decade, as shown in . In this condition, the phase margin is larger than 45° (see 图 12).

$$\log\left(\frac{f_Z}{f_P}\right) \leq 1 \tag{15}$$

Use 公式 13 and 公式 14 to derive the minimum value for R_{FLT} in 公式 16:

$$R_{FLT} \geq \frac{R_O}{9} \tag{16}$$

In the interest of stability, the effects of f_Z must occur at a frequency lower than the closed-loop gain bandwidth of the amplifier (f_{CL}). The closure rate between the open- and closed-loop gain curves should not be greater than 20 dB/decade for stability of the amplifier circuit.

Therefore, the lower bound of R_{FLT} has been determined for a stable input driver.

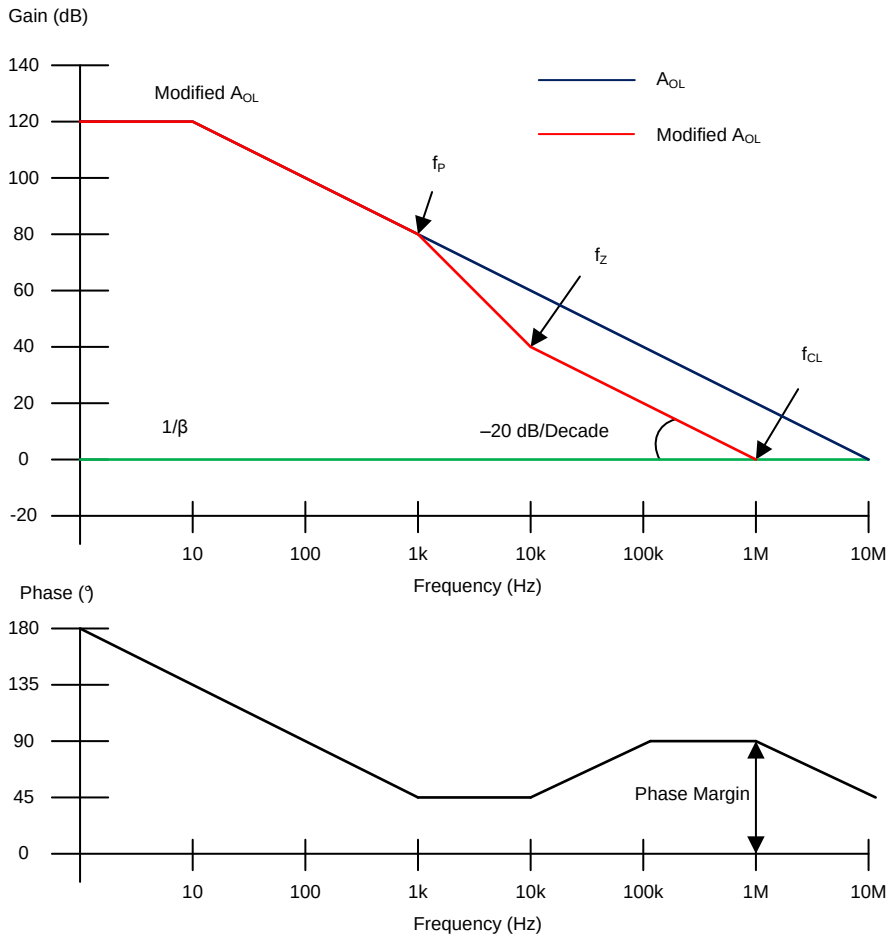


图 12. Analyzing Effect of RC-Filter on Op Amp Stability Using A_{OL} Response

2.4.1.3 Settling Time

A fast settling time with inputs settling within 1 LSB is necessary to maintain good linearity. The worst case is that the input voltage V_{IN} changes by a full-scale step from 0.1 V to V_{REF}, but the C_{FLT} provides a charge bucket. The voltage drop can be calculated using 公式 9. Therefore, the behavior of the input voltage is represented by 公式 17:

$$V_{ADC\_IN}(t) = V_{REF} - \Delta V \times e^{-\left(\frac{t}{\tau}\right)} \tag{17}$$

where,

- $\tau = R_{FLT} \times C_{FLT}$
- $t = t_{ACQ}$ = acquisition time
- $\Delta V = C_{SH} \times V_{REF} / C_{FLT}$.

For a specific sampling time, the RC time constant must be designed to meet the timing and accuracy constraint as 公式 18 shows. The following equation can be derived from 公式 18 to 公式 23:

$$V_{REF} - V_{ADC\_IN}(t) \le 1LSB \tag{18}$$

$$V_{REF} - (V_{REF} - \Delta V \times e^{-(\frac{t}{\tau})}) \le 1LSB \tag{19}$$

$$\Delta V \times e^{-\frac{t}{\tau}} \le 1LSB \tag{20}$$

$$\frac{\Delta V}{1LSB} \le e^{\frac{t}{\tau}} \tag{21}$$

$$R_{FLT} \times C_{FLT} \times \ln(\frac{\Delta V}{1LSB}) \le t \tag{22}$$

$$R_{FLT} \le \frac{t}{\ln\left(\frac{\Delta V}{1LSB}\right) \times C_{FLT}} \tag{23}$$

where,

- 1 LSB = $V_{REF} / 2^N$.

Therefore, the upper bound of R_{FLT} has been determined for the settling time as shown in 公式 23.

Notice that 公式 18 is based on the assumption that the ADC input has already settled to V_{REF} (see 图 10). In this design, to satisfy the assumption, R_{FLT} needs to increase the phase margin and must be selected close to the upper bound to ensure settling to V_{REF}, because the selected input driver only has sufficient bandwidth for a low power specification. If the ADC input has not settled before the sampling-and-hold region, the $V_{\_ADC\_IN}$ must be adjusted to other values.

2.4.1.4 Final Selection of R_{FLT} and C_{FLT}—Check Stability and Settling Time Criteria

The value of the charge bucket can be summarized by checking stability and settling time, as 公式 24 and 公式 25 show.

$$C_{FLT} \ge 20 \times C_{SH} \tag{24}$$

$$\frac{R_O}{9} \le R_{FLT} \le \frac{t}{\ln\left(\frac{\Delta V}{1LSB}\right) \times C_{FLT}} \tag{25}$$

The first step is to select the C_{FLT} based on 公式 24. Then choose the lower bound R_{FLT} value and check the settling time and phase margin. If the settling time is too long because of phase margin, select the upper bound value of R_{FLT} and recheck the settling time and phase margin. If the phase margin is still not enough, C_{FLT} must be adjusted to a smaller value due to the higher value of R_{FLT}, which increases the phase margin based on the same RC time constant.

Notice that the practical circuit is the second-order system; therefore, increasing R_{FLT} does not mean that the settling time will increase.

2.4.2 Input Amplifier Design

Another key aspect in designing the input driver circuit for high-resolution SAR ADCs is the selection of an appropriate driving amplifier. The amplifier selection process is highly dependent on the input signal and throughput of the ADC. This design is optimized for a full-scale step input signal, so the key amplifier specifications for the selection criteria are as follows.

2.4.2.1 Slew Rate

The minimum slew rate for the driving amplifier is dependent on the type and amplitude of the input signal (see 公式 26):

$$\text{Slew Rate} = \text{MAX}\left(\frac{\Delta V_{OUT}}{\Delta t}\right) \tag{26}$$

where,

- $\Delta t = t_{QT}$ = quiet time period
- $\Delta V_{OUT} = V_{REF}$ = reference voltage.

2.4.2.2 Bandwidth

This bandwidth must be much higher than the bandwidth of the ADC input circuit to ensure that there is no attenuation of the input signal resulting from the bandwidth limitation of the amplifier. In general, select the amplifier based on the calculation in 公式 27.

$$\text{Unity} - \text{Gain Bandwidth} \geq 4 \times \frac{1}{2\pi R_{FLT} C_{FLT}} \tag{27}$$

2.4.2.3 Rail-to-Rail Input and Output Swing

This application uses an input signal with a full-scale voltage swing; therefore, an amplifier with support for a rail-to-rail input and output (RRIO) swing is required.

2.4.2.4 Open-Loop Output Impedance

The output impedance must be as low as possible to efficiently drive the switched capacitor inputs of the SAR ADC as well as to maintain the op amp stability under high capacitive load conditions.

2.4.2.5 Max Output Current

The output peak current drive requirement for the amplifier is dependent on the values of R_{FLT} and C_{FLT}. This dependency is due to the fact that, during sampling, the capacitor C_{FLT} charges the internal sampling capacitor (C_{SH}), which causes a voltage drop across C_{FLT}. The recharge current for capacitor C_{FLT} is provided by the output stage of the amplifier, thus imposing a minimum condition on the output drive capability of the amplifier as calculated by 公式 28 and 公式 29.

$$I_{OUT} \geq \frac{\Delta V_{FLT}}{R_{FLT}} \quad (28)$$

$$I_{OUT} \geq \frac{C_{SH} \times V_{REF}}{C_{FLT} \times R_{FLT}} \quad (29)$$

2.4.2.6 Offset Drift

The offset drift is an important parameter used to influence the accuracy. The output error is caused by temperature variation. In industrial applications, the wide temperature range environment is common; therefore, the amplifier drift must be as low as possible to ensure good performance.

2.4.2.7 Noise

Noise can be defined as an unwanted signal that combines with a desired signal to result in an error. In this design, the cutoff frequency cannot be arbitrarily low because it influences the settling time; therefore, choose a low-noise amplifier as one of the solutions to reduce the noise.

The input amplifier noise can be categorized into two basic groups: extrinsic and intrinsic. Extrinsic noise is noise produced from some external circuit or natural phenomena. 60-Hz power line noise and interference from mobile phones are common examples of extrinsic noise. Cosmic radiation is another example of a natural phenomenon that causes extrinsic noise. Shielding and filtering can be used to reduce extrinsic noise. Intrinsic noise is caused by components within a circuit, which means that intrinsic noise can be predicted with hand calculations and simulations. 图 13 shows how intrinsic amplifier noise is modeled.

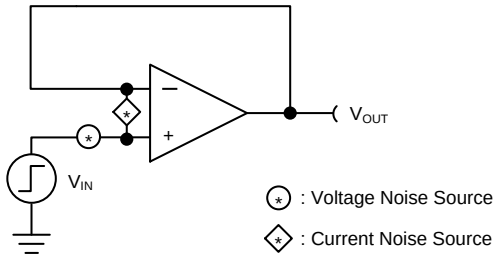


图 13. Intrinsic Noise of Input Driver

公式 30 shows how to calculate the total RMS noise for this amplifier topology. Other amplifier topologies require different calculations. For example, an inverting amplifier has a different gain and also includes the effects of current noise and resistor noise.

$$V_{n\_AMP\_RMS} = \text{Noise Gain} \times V_{n\_AMP\_RTI\_RMS}$$
$$= \text{Noise Gain} \times \sqrt{1.57 \times BW_{FLT}} \times V_{n\_AMP\_DENSITY}$$
$$= \sqrt{1.57 \times BW_{FLT}} \times V_{n\_AMP\_DENSITY} \quad (30)$$

where,

- Noise gain = gain of non-inverting configuration = 1
- $V_{n\_AMP\_RTI\_RMS}$ = amplifier noise referred to the input
- $V_{n\_AMP\_RMS}$ = amplifier noise referred to the output
- BW_{FLT} = cutoff frequency of filter
- $V_{n\_AMP\_DENSITY}$ = amplifier voltage noise density.

For a system specification of the effective resolution and SNR, the voltage noise density of the amplifier can be defined based on the determined cutoff frequency for settling time and stability.

To obtain the N-bit effective resolution$_{SYS}$ as shown in 公式 1, the total system noise containing the input driver and ADC noise must be lower than 1 LSB. See the following derivation in 公式 31.

To achieve the target effective resolution, the $\sigma_{HISTO\_AMP\_NOISE}$ must be lower than specified noise; therefore, after rearranging the equation, transforming the unit of noise can result in the noise density at existing parameters (see 公式 31):

$$\text{Effective Resolution}_{SYS} = N - \log_2(\sigma_{HISTO\_SYS\_NOISE})$$

$$\text{For effective resolution}_{SYS} = N = 16$$

$$\Rightarrow \log_2(\sigma_{HISTO\_SYS\_NOISE}) \le 0$$

$$\Rightarrow \sigma_{HISTO\_SYS\_NOISE} \le 1LSB$$

$$\Rightarrow \sqrt{\left(\sigma_{HISTO\_AMP\_NOISE}\right)^2 + \left(\sigma_{HISTO\_ADC\_NOISE}\right)^2} \le 1LSB$$

$$\Rightarrow \sigma_{HISTO\_AMP\_NOISE} \le \sqrt{(1LSB)^2 - \left(\sigma_{HISTO\_ADC\_NOISE}\right)^2}$$

$$\Rightarrow V_{n\_AMP\_RMS} \times \frac{2^N}{V_{REF}} \le \sqrt{(1LSB)^2 - \left(\sigma_{HISTO\_ADC\_NOISE}\right)^2}$$

$$\Rightarrow V_{n\_AMP\_RMS} \le \sqrt{(1LSB)^2 - \left(\sigma_{HISTO\_ADC\_NOISE}\right)^2} \times \frac{V_{REF}}{2^N}$$

$$V_{n\_AMP\_DENSITY} \le \frac{\sqrt{(1LSB)^2 - \left(\sigma_{HISTO\_ADC\_NOISE}\right)^2} \times V_{REF}}{\sqrt{1.57 \times BW_{FLT}} \times 2^N} \quad (31)$$

where,

- N = ADC resolution
- $\sigma_{HISTO\_SYS\_NOISE}$ = standard deviation of the measured system noise in fractions of LSB
- $\sigma_{HISTO\_AMP\_NOISE}$ = standard deviation of the measured amplifier noise in fractions of LSB
- $\sigma_{HISTO\_ADC\_NOISE}$ = standard deviation of the measured ADC noise in fractions of LSB; transition noise in ADC datasheet
- BW_{FLT} = cutoff frequency of the filter
- $V_{n\_AMP\_RMS}$ = amplifier noise referred to the output
- $V_{n\_AMP\_DENSTY}$ = amplifier voltage noise density.

The next step is to derive the relationship between amplifier noise and the signal-to-noise ratio (SNR_{SYS}) of the system. The concept of system SNR is introduced in the previous 公式 3. 公式 32 shows the SNR equation with the maximum RMS signal of V_{REF} / ($2\sqrt{2}$) substituted. 公式 33 is algebraically rearranged to solve for the total noise ($V_{N\_TOT\_RMS}$). The relationship for total noise, including the amplifier and ADC noise, is substituted in 公式 34. 公式 35 solves for the amplifier noise. 公式 36 substitutes the ADC RMS noise as a function of the ADC SNR. Finally, 公式 37 converts the expression from RMS noise to noise density by dividing by the noise bandwidth. Using 公式 37 can determine the required noise spectral density for an amplifier given the system SNR requirement and the specified SNR of the ADC:

$$SNR_{SYS}(dB) = 20\log\left(\frac{\frac{V_{REF}}{2\sqrt{2}}}{V_{n\_TOT\_RMS}}\right) \tag{32}$$

$$V_{n\_TOT\_RMS} \le \frac{V_{REF}}{2\sqrt{2} \times 10^{\frac{SNR_{SYS}(dB)}{20}}} \tag{33}$$

$$\sqrt{V_{n\_AMP\_RMS}^2 + V_{n\_ADC\_RMS}^2} \le \frac{V_{REF}}{2\sqrt{2} \times 10^{\frac{SNR_{SYS}(dB)}{20}}} \tag{34}$$

$$V_{n\_AMP\_RMS} \le \sqrt{\left(\frac{V_{REF}}{2\sqrt{2} \times 10^{\frac{SNR_{SYS}(dB)}{20}}}\right)^2 - \left(V_{n\_ADC\_RMS}\right)^2} \tag{35}$$

$$V_{n\_AMP\_RMS} \le \sqrt{\left(\frac{V_{REF}}{2\sqrt{2} \times 10^{\frac{SNR_{SYS}(dB)}{20}}}\right)^2 - \left(\frac{V_{REF}}{2\sqrt{2} \times 10^{\frac{SNR_{ADC}(dB)}{20}}}\right)^2} \tag{36}$$

$$V_{n\_AMP\_DENSITY} \le \frac{\sqrt{\left(\frac{V_{REF}}{2\sqrt{2} \times 10^{\frac{SNR_{SYS}(dB)}{20}}}\right)^2 - \left(\frac{V_{REF}}{2\sqrt{2} \times 10^{\frac{SNR_{ADC}(dB)}{20}}}\right)^2}}{\sqrt{1.57 \times BW_{FLT}}} \tag{37}$$

where,

- V_{REF} = reference voltage
- $V_{n\_TOT\_RMS}$ = system total noise
- $V_{n\_AMP\_RMS}$ = input driver noise
- $V_{n\_ADC\_RMS}$ = ADC noise
- BW_{FLT} = cutoff frequency of filter
- $V_{n\_AMP\_DENSITY}$ = amplifier voltage noise density.

2.4.2.8 Low Power

Low power consumption is the key optimization parameter for this design. This parameter is essential for portable devices to save battery lifetime. Furthermore, reducing the power reduces heat generation, which may improve overall performance in some cases.

2.4.2.9 Input Bias Current

This system may be used with a multiplexer in certain cases. Choosing a low-bias current op amp is important if the multiplexer is connected before the input amplifier because the input bias current interacts with the multiplexer switch impedance, which generates errors. For further details on multiplexer design, see the *16-Bit 400-kSPS, Four-Channel MUX Data Acquisition System for High-Voltage Inputs Reference Design*[1].

2.5 Reference Voltage Design

The reference voltage provides the ADC with a standard voltage that can be used to compare the input signal and produce the corresponding output code. The bad accuracy of a reference highly degrades the system performance. Some ADCs have the reference voltage circuit integrated in the integrated circuit (IC), but an internal reference voltage circuit restricts the flexibility to design a higher performance reference voltage. External voltage reference circuits are used in a DAQ system if there is no internal reference in the ADC or if the accuracy of the internal reference is not sufficient to meet the performance goals of the system. These circuits provide low drift and very accurate voltages for ADC reference input. However, the output broadband noise of most references can be in the order of a few 100 μV_{RMS}, which degrades the noise and linearity performance of precision ADCs for which the typical noise is in the order of tens of μV_{RMS}. Hence, to optimize the ADC performance, the output of the voltage reference must be appropriately filtered and buffered as shown in 图 14.

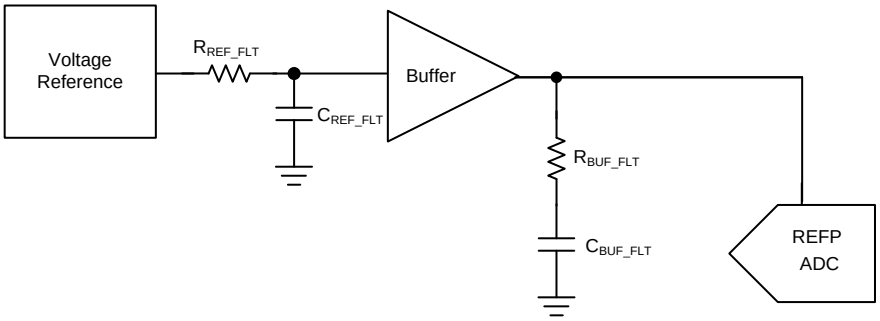


图 14. Block Diagram of Reference Driver

With new and increased integration, another option to drive the reference on the ADC is an integrated reference and buffer. This option replaces the entire reference driver circuit with one main component, eliminating the requirement of a buffer and most passive components and simplifying the design process. Even if an amplifier does meet the necessary specifications for the reference circuit such as wide bandwidth, low output impedance, low offset, and low drift, the power consumption should still be considered.

2.5.1 Reference Voltage and RC Filter

The reference noise can be categorized into peak-to-peak low-frequency flicker or 1/f noise (V_{1/f_REF_pp}) from 0.1 Hz to 10 Hz and higher frequency broadband noise, generally specified as a noise spectral density ($e_{n\_REF\_RMS}$) over a wide frequency range. The broadband output noise from the reference circuit can be band-limited by the 3-dB cutoff frequency (f_{REF_3dB}) of an RC filter at its output. So, the primary objective for the filter design is to keep the bandwidth low enough such that the integrated noise from the reference does not degrade the performance of the ADC. Hence, the total integrated noise from the reference ($V_{n\_REF\_RMS}$) must be kept at least three times less than the ADC noise to prevent any noise degradation in the system performance (see 公式 38).

$$V_{Noise\_REF\_RMS} \le \frac{1}{3} \times V_{Noise\_ADC\_RMS} \tag{38}$$

The value of $V_{n\_REF\_RMS}$ can be calculated by the RSS of the flicker noise and broadband noise density, as the calculation in 公式 39 shows.

$$V_{Noise\_REF\_RMS} = \sqrt{\left(\frac{V_{1/f\_REF\_PP}}{6.6}\right)^2 + e^2_{Noise\_REF\_RMS} \times \frac{\pi}{2} \times f_{REF\_3dB}} \tag{39}$$

Combining 公式 38 and 公式 39 results in the following 公式 40:

$$\sqrt{\left(\frac{V_{1/f\_REF\_PP}}{6.6}\right)^2 + e^2_{Noise\_REF\_RMS} \times \frac{\pi}{2} \times f_{REF\_3dB}} \le \frac{1}{3} \times \frac{V_{FSR}}{2\sqrt{2}} \times 10^{-\frac{SNR(dB)}{20}} \tag{40}$$

The variation in the broadband noise density of the voltage reference ranges from 100 nV/$\sqrt{Hz}$ to 1000 nV/$\sqrt{Hz}$ depending on the reference type and power consumption. In general, the reference noise is inversely proportional to its quiescent current (I_{Q_REF}). Broadband noise density is not always included in voltage reference datasheet; therefore, an approximation of the noise density for band-gap reference circuits is provided in 公式 41:

$$e_{Noise\_REF\_RMS} \approx \frac{1000\ nV}{\sqrt{Hz}} \times \frac{1}{\sqrt{2 \times I_{Q\_REF}(in\ \mu A)}} \tag{41}$$

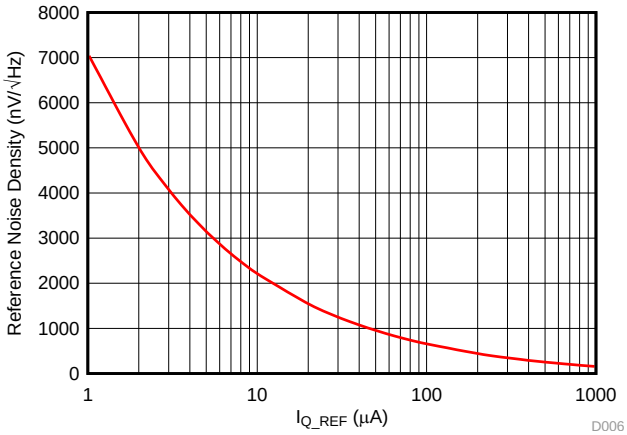


图 15. Characteristic Curve of Reference Noise versus Quiescent Current – Approximation of Noise Density for Band Gap References

By combining 公式 39, 公式 40, and 公式 41, the value of f_{REF_3dB} can be derived as shown in 公式 42:

$$f_{REF\_3dB} \le \frac{2 \times I_{Q\_REF}\,(\text{in } \mu A)}{\left(\frac{10000\ nV}{\sqrt{Hz}}\right)} \times \frac{2}{\pi} \times \left[\frac{1}{9} \times \frac{V_{FSR}^2}{8} \times 10^{-\frac{SNR(dB)}{10}} - \left(\frac{V_{1/f\_REF\_PP}}{6.6}\right)^2\right] \quad (42)$$

The value of the capacitor for the RC filter must be kept higher than 100 nF to keep its thermal noise lower than 0.2 μV_{RMS}. Using the selected value for C_{REF_FLT} and f_{REF_3dB}, the value of R_{REF_FLT} can be calculated using 公式 43.

$$R_{REF\_FLT} = \frac{1}{2\pi \times f_{REF\_3dB} \times C_{REF\_FLT}} \quad (43)$$

2.5.2 Reference Buffer and Capacitor (C_{BUF_FLT})

公式 44 calculates the difference in V_{REF} between conversions:

$$\Delta V_{REF} \leq \frac{V_{REF}}{2^N} \tag{44}$$

If the charge consumed during each conversion is Q_{REF}, then the calculation is as follows in 公式 45:

$$C_{BUF\_FLT} = \frac{Q_{REF}}{\Delta V_{REF}} \geq \frac{Q_{REF} \times 2^N}{V_{REF}} \tag{45}$$

The average value of Q_{REF} can be calculated from the maximum ADC conversion time (T_{CONV_MAX}) and the average value of reference input current (I_{REF}) specified in the ADC datasheets as follows in 公式 46:

$$Q_{REF} = I_{REF} \times T_{CONV\_MAX} \tag{46}$$

By combining 公式 45 and 公式 46, the minimum value of C_{BUF_FLT} can be obtained in the following 公式 47:

$$C_{BUF\_FLT} = \frac{Q_{REF}}{\Delta V_{REF}} \geq \frac{Q_{REF} \times 2^N}{V_{REF}} \tag{47}$$

The capacitor values derived from this equation are high enough to make the driving amplifier unstable, so TI recommends to use a series resistor (R_{BUF_FLT}) to isolate the amplifier output and make it stable. The value of R_{BUF_FLT} is dependent on the output impedance of the driving amplifier as well as on the signal frequency. Typical values of R_{BUF_FLT} range between 0.1 Ω to 2 Ω and the exact value can be found by using SPICE simulations. Note that higher values of R_{BUF_FLT} cause high voltage spikes at the reference pin, which affects the conversion accuracy.

After designing the appropriate passive filter for band-limiting the noise of the reference circuit, it is important to select an appropriate amplifier for using as a reference buffer. The key specifications to be considered when selecting an appropriate amplifier for reference buffer are addressed in the following subsections.

2.5.3 Output Impedance

The output impedance for a reference buffer must be kept as low as possible because the ADC draws current from the reference pin during conversion and the resultant drop in reference voltage is directly proportional to the output impedance of the driving buffer. Maintaining this low output impedance also helps to keep the amplifier stable while driving a large capacitive load (C_{BUF_FLT}).

2.5.4 Input Offset

The input offset error of the buffer amplifier must be as low as possible to ensure that the reference voltage driving the ADC is very accurate.

2.5.5 Offset Drift

The offset temperature drift of the reference buffer must be extremely low to ensure that the reference voltage for the ADC does not change significantly over the operating temperature range. For similar reasons, keeping a low long-term time drift for the buffer amplifier is also important.

3 Component Selection

3.1 Component Selection for ADC

The ADS8860 is an excellent choice to meet the system specification for a low-power, 16-bit, 1-MSPS, single-ended DAQ application. The device operates with a 2.5-V to 5-V external reference, offering a wide selection of signal ranges without additional input signal scaling. The device supports unipolar, single-ended analog inputs in the range of –0.1 V to V_{REF} + 0.1 V.

3.2 Component Selection for Input Driver

The input driver circuit must be able to settle within the ADC input specifications.

3.2.1 Charge Bucket Component Selection

The charge bucket is not part of the antialiasing filter, although it is part of the analog input driver circuit. The charge bucket must be able to charge the input capacitor inside the ADC.

3.2.1.1 Reducing Charge Kickback

In 节 2.4.1, the specified value of the input capacitor for the ADS8860 is 59 pF; therefore, use 公式 48 to calculate the value of capacitance:

$$C_{FLT} \geq 20 \times C_{SH}$$
$$\Rightarrow C_{FLT} \geq 1.18 \text{ nF} \quad (48)$$

At first, the selected standard value of capacitance is 1.2 nF, but the final value requires confirmation using a simulation to verify settling time and phase margin. The recommended type of capacitor is the C0G/NPO because of the low temperature coefficient and stable capacitance under varying voltages, frequency, and time.

3.2.1.2 Stability

In this design, the OPA320 is selected as the input driver. 图 16 and 图 17 show a simulation measuring the open-loop output impedance using TINA-TI. The impedance is relatively flat and 90 Ω in this case.

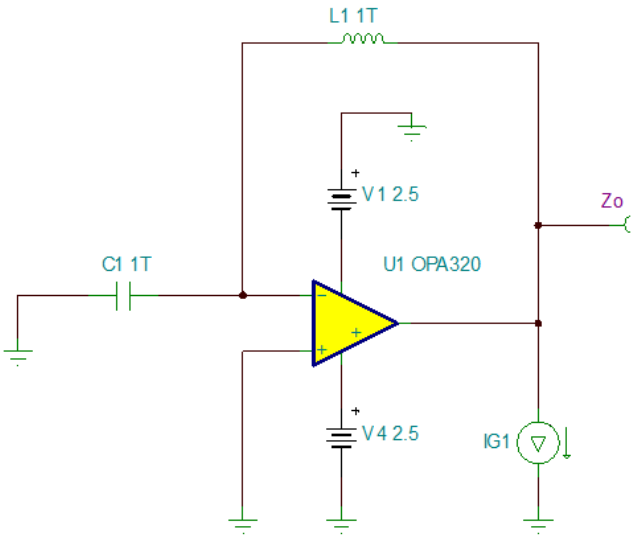


图 16. TINA-TI™ Schematic—Measuring Open-Loop Output Impedance of OPA320

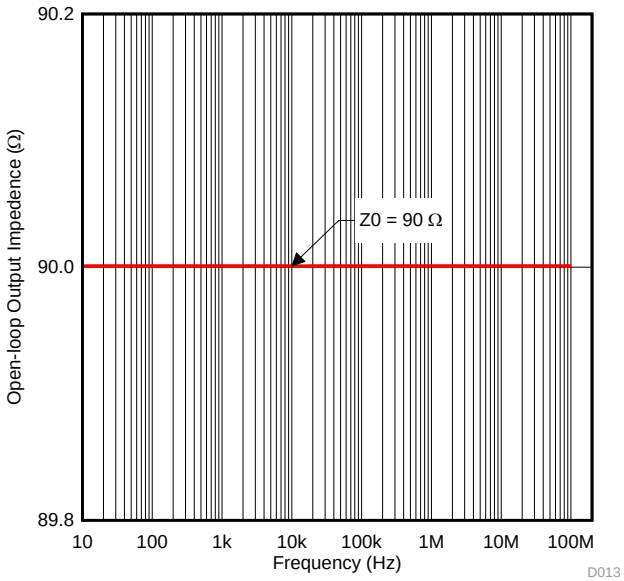


图 17. TINA-TI™ Simulation Result—Output Impedance of OPA320

Using 公式 49 and the open-loop output impedance from 图 17, the minimum value of filter resistance is calculated to be 10 Ω.

$$R_{FLT} \geq \frac{R_O}{9}$$
$$\Rightarrow R_{FLT} \geq 10 \quad (49)$$

At this point the filter capacitance and minimum value of the filter resistance have been determined. The settling time can then determine the maximum value of filter resistance.

3.2.1.3 Settling Time

The calculations in 节 2.4.1 explain the settling time. According to 公式 18, Where t_{ACQ} = 290 ns, ΔV = 201 mV, C_{FLT} = 1.2 nF and 1 LSB = 62.5 µV:

$$V_{REF} - V_{ADC\_IN}(t) \leq 1LSB$$

$$\Rightarrow R_{FLT} \times C_{FLT} \times \ln\left(\frac{\Delta V}{1LSB}\right) \leq t$$

$$\Rightarrow R_{FLT} \times C_{FLT} \leq 32.2\ ns$$

$$\Rightarrow R_{FLT} \leq 30\ \Omega \quad (50)$$

where,

- t_{ACQ} = 290 ns
- ΔV = 201 mV
- C_{FLT} = 1.2 nF
- 1 LSB = 62.5 µV.

A differential-mode RC filter is used to balance the output impedance looking through the ADS8860 device, as 图 18 shows. The differential-mode RC filter has the same cutoff frequency as the common-mode RC filter.

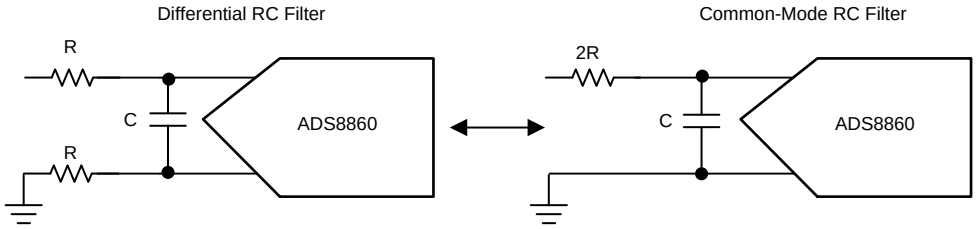


图 18. Design Configuration for Charge Bucket at ADC Input

3.2.1.4 *Final Selection of R_{FLT} and C_{FLT}—Check Stability and Settling Time Criteria*

In the TIPD173 design, 公式 49 and 公式 50 can be used to calculate the range of the capacitor and resistor. Based on the selected value of C_{FLT} and R_{FLT}, the settling time can be simulated using TINA-TI. At first, the value of the capacitor (C_{FLT}) follows the general guideline to select 1.2 nF as the charge bucket and determine the value of the resistor. However, the value of the RC time constant cannot settle the signal within 900 ns for the system specification because of low phase margin. Therefore, the value of the capacitor and resistor must be adjusted for short settling time and higher phase margin. After several steps, the final selected standard value of capacitance is 470 pF and the value of resistance is 68 Ω, which confirms the range for settling time (smaller than 900 ns) and stability. 表 2 shows the selected flow of C_{FLT} and R_{FLT}.

表 2. Selected Flow of R_{FLT} and C_{FLT} for Settling Time and Stability

STEP	CAPACITOR (C_{FLT})	RESISTOR (R_{FLT})	RANGE RESISTOR (R_{FLT})	SETTLING TIME	PHASE MARGIN
1	1.2 nF	$10 \le R_{FLT} \le 30$	10	1310 ns	28.7°
2	1.2 nF	$10 \le R_{FLT} \le 30$	30	1010 ns	55.2°
3	1 nF	$10 \le R_{FLT} \le 35$	35	993 ns	56.4°
4	820 pF	$10 \le R_{FLT} \le 42$	41.8	968 ns	57.7°
5	680 pF	$10 \le R_{FLT} \le 49$	49.3	947 ns	58.7°
6	560 pF	$10 \le R^{FLT} \le 59$	58.6	919 ns	59.5°
7	470 pF	$10 \le R_{FLT} \le 68$	68	852 ns	60°

3.2.2 Amplifier Selection

Some of the key specifications for the driving amplifier can be derived based on the values of R_{FLT} and C_{FLT}.

3.2.2.1 *Slew Rate*

The minimum slew rate of the driving amplifier for this application depends on the time allowed for the slewing of the amplifier output stage when a full-scale step is applied at the input. As 节 2.4.2 explains, the output stage of the amplifier slews during t_{QT} is 610 ns; therefore, the minimum required slew rate for the amplifier is calculated in 公式 51 as:

$$\text{Slew Rate} = \text{MAX}\left(\frac{\Delta V_{OUT}}{\Delta t}\right) = \frac{V_{REF}}{t_{QT}}$$

$$\Rightarrow \text{Slew Rate} > \frac{6.7\ \text{V}}{\mu\text{s}} \tag{51}$$

3.2.2.2 Bandwidth

This bandwidth must be much higher than the bandwidth of the ADC input circuitry to ensure that there is no attenuation of the input signal resulting from the bandwidth limitation of the amplifier (see 公式 52).

$$\text{Unity} - \text{Gain Bandwidth} \geq 4 \times \frac{1}{2\pi R_{FLT} C_{FLT}}$$
$$\Rightarrow \text{Unity} - \text{Gain Bandwidth} \geq 19.9\ \text{MHz} \quad (52)$$

3.2.2.3 Rail-to-rail Input and output Swing

This application uses an input signal with a full-scale voltage swing; therefore, an amplifier with support for rail-to-rail input and output (RRIO) swing is required.

3.2.2.4 Maximum Output Current Driver

The output current driver capability of the driving amplifier is calculated in 公式 53 using 公式 29:

$$I_{OUT} \geq \frac{C_{SH} \times V_{REF}}{C_{FLT} \times R_{FLT}}$$
$$\Rightarrow I_{OUT} \geq \frac{59 \times 10^{-12} \times 4.096}{0.47 \times 10^{-9} \times 68} = 7.56\ \text{mA} \quad (53)$$

3.2.2.5 Noise

The noise density of the amplifier can be calculated in 公式 54 by using 公式 31 and 公式 37.

For an effective resolution = 16-bit:

$$V_{n\_AMP\_DENSITY} \leq \frac{\sqrt{(1\text{LSB})^2 - (\sigma_{HISTO\_ADC\_NOISE})^2} \times V_{REF}}{\sqrt{1.57 \times BW_{FLT}} \times 2^N}$$
$$\Rightarrow V_{n\_AMP\_DENSITY} \leq 19\ \frac{\text{nV}}{\sqrt{\text{Hz}}} \quad (54)$$

where,

- $\sigma_{HISTO\_ADC\_NOISE}$ = transition noise = 0.5 LSB
- V_{REF} = 4.096 V
- BW_{FLT} = 4.97 MHz
- N = 16.

For an $SNRR_{SYS}$ > 90 dB:

$$V_{n\_AMP\_DENSITY} \leq \frac{\sqrt{\left(\frac{V_{REF}}{2\sqrt{2} \times 10^{\frac{SNR_{SYS}(dB)}{20}}}\right)^2 - \left(\frac{V_{REF}}{2\sqrt{2} \times 10^{\frac{SNR_{ADC}(dB)}{20}}}\right)^2}}{\sqrt{1.57 \times BW_{FLT}}}$$
$$\Rightarrow V_{n\_AMP\_DENSITY} \leq 11.6\ \frac{\text{nV}}{\sqrt{\text{Hz}}} \quad (55)$$

where,

- SNR_{SYS} = 90 dB
- SNR_{ADC} = 93 dB

- V_{REF} = 4.096 V
- BW_{FLT} = 4.97 MHz.

表 3. Calculated Specifications of Input Driving Amplifier versus OPA320 Specifications

SPECIFICATIONS	CALCULATED VALUES	OPA320
Slew rate (V/μs)	6.7	10
Unity gain bandwidth (MHz)	19.9	20
RIRO	Yes	Yes
Open-output impedance (Ω)	As low as possible	90
Maximum output current (mA)	7.56	20
Offset drift (μV/°c)	As low as possible	1.5 (typical)
Noise density (nV/√Hz)	11.6	7
Quiescent current (mA)	As low as possible	8.75 mW at VDD = 5 V (maximum)

3.3 Component Selection for Reference Driver

The reference driver must provide low offset, low drift, wide bandwidth and low output impedance.

3.3.1 Passive Component Selection

In the TIPD173 design, REF5040 is used to drive the ADS8860 and provides the 4-V reference voltage with 3-ppm/ºC low drift and 3-μV_{PP}/V low noise. The V_{OUT} pin requires a capacitor of 10 μF for line and load regulation. A series resistor of 0.2 Ω is used with the 10 μF for a smooth power up of the reference.

In 节 2.5.1, the noise from the reference should be bandwidth limited by designing a low-pass RC filter at the reference output. According to 公式 42, the maximum value of the 3-dB bandwidth for this filter can be calculated in 公式 56 as:

$$f_{REF\_3dB} \le \frac{2 \times I_{Q\_REF}(\text{in } \mu A)}{\left(\frac{10000\ nV}{\sqrt{Hz}}\right)} \times \frac{2}{\pi} \times \left[\frac{1}{9} \times \frac{V_{FSR}^2}{8} \times 10^{-\frac{SNR(dB)}{10}} - \left(\frac{V_{1/f\_REF\_PP}}{6.6}\right)^2\right]$$

$$\Rightarrow f_{REF\_3dB} \le 1.15\ kHz \quad (56)$$

The value of capacitor C_{REF_FLT} has been selected as 1 μF to keep the thermal noise of the capacitor at a low value. The minimum value of R_{REF_FLT} can be calculated in 公式 57 by using the previous 节 2.5.2:

$$R_{REF\_FLT} \ge \frac{1}{2\pi \times f_{REF\_3dB} \times 10^{-6}}$$

$$\Rightarrow R_{REF\_FLT} \ge \frac{1}{2\pi \times 1.15 \times 10^3 \times 10^{-6}} = 138\ \Omega \quad (57)$$

The value of R_{REF_FLT} has been selected as 1 kΩ for this design. The selected value for the resistor is much higher than the calculated minimum value to further reduce the bandwidth of the filter. The broadband noise contribution from the reference is negligible.

The next important passive element in this reference design is the capacitor C_{BUF_VLT}, which helps to regulate the voltage at the ADC reference pin under dynamic load conditions. According to the ADS8860 datasheet[2], the average current drawn into the reference pin (I_{REF}) is 300 μA and the T_{CONV_MAX} is equal to 710 ns for a maximum throughput of 1 MSPS. So according to 公式 47, the value of C_{BUF_FLT} can be calculated in 公式 58 as:

$$C_{BUF\_FLT} \geq \frac{300 \times 10^{-6} \times 710 \times 10^{-9} \times 2^{16}}{4.096} = 3.41\,\mu F \quad (58)$$

The value of C_{BUF_FLT} has been selected as 10 μF for this design.

3.3.2 Integrated Reference and Buffer

As previously mentioned, a new increased integration option to drive the reference on the ADC, an integrated reference, and buffer has been added. This option replaces the entire reference driver circuit with one main component, which avoids the long design process of choosing the correct amplifier for the best performance. Even when an amplifier does meet the necessary specifications for a design, such as wide bandwidth, low output impedance, low offset, and low drift, the power consumption must still be considered as well as the design time. The REF60xx family, a high-performance line of reference drivers offered by TI, has an integrated low-output impedance buffer. Each reference driver is trimmed during production to achieve a max drift of only 5 ppm/°C for both the reference and integrated buffer, combined. The device also consumes a low 820-μA quiescent current, while still being able to replenish a charge of 70 pC on a 47-μF capacitor in 1 μs. This integrated device decreases design time by eliminating the requirement of the entire reference driver circuit.

The REF6041 is specifically the ideal choice for this design, with an output of 4.096 V.

3.3.3 Amplifier Selection

The key amplifier specification to consider when designing a reference buffer for high-precision ADC are low offset, low drift, wide bandwidth, and low output impedance. In this design, the reference buffer is designed using the OPA333 and THS4281 in a composite double-feedback architecture. For details on designing the reference driver, see the *18-Bit Data Acquisition (DAQ) Block Optimized for 1-μs Full-Scale Step Response* reference design[3].

4 Simulation

The TINA-TI schematic in 图 19 shows the final system block diagram and selected component values as explained in previous sections.

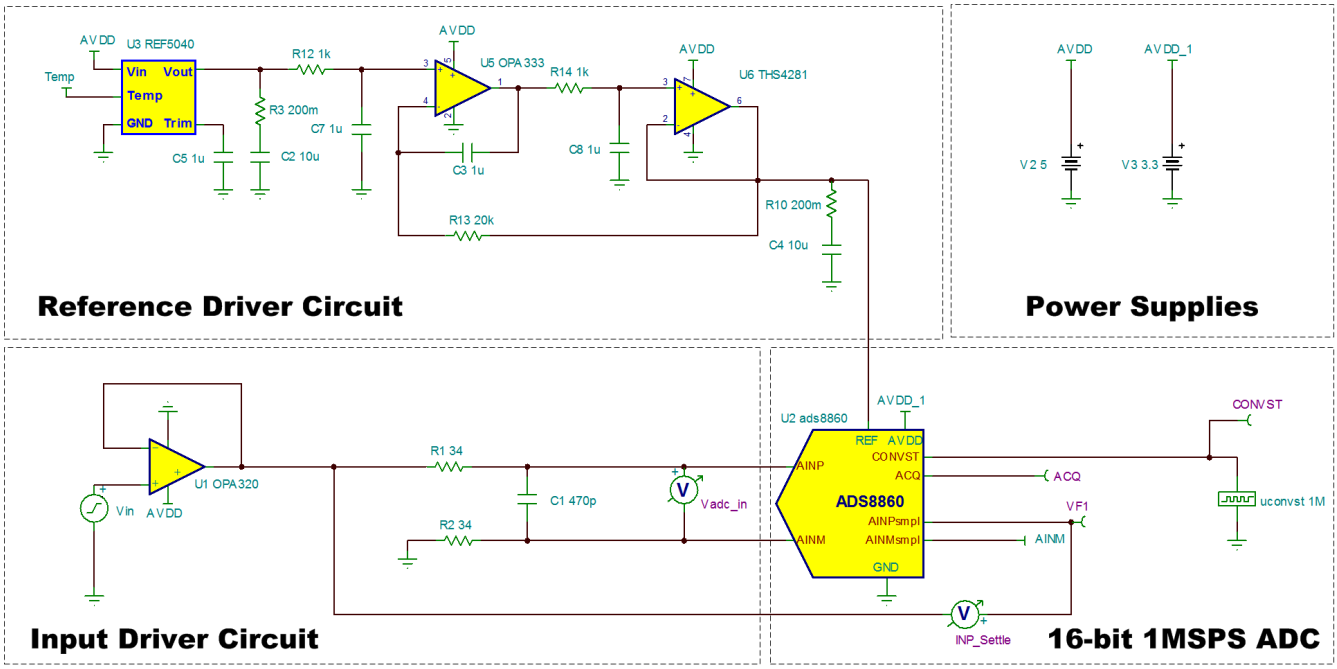


图 19. TINA-TI™ Schematic—Complete DAQ Block

The TINA-TI model in 图 19 is used to evaluate the capability of a 16-bit 1-MSPS DAQ system. The SPICE model can rapidly show the accurate system behavior to obtain the specified goal. This software also helps to reduce the design cost due to time saved by evaluating system performance before the PCB design. The details and results of the simulation are discussed in the following subsections.

4.1 Settling Time of Input Driver

The schematic shown in 图 19 models the behavior of a 16-bit settling time in a multiplexed application. In a multiplexed application, the worst case scenario is an input signal changing from a negative rail to a positive rail or vice versa. In 图 20 and 图 21, the model shows the transient response for these two cases and confirms that the settling time error converges to less than 1 LSB. INP_Settle shows the difference between the input driver output and sampled signal. Note that AINP_smpl represents the internal ADC sampled voltage across the sampling capacitor (C_{SH}). Thus, INP_Settle measures the error introduced during the sampling process. The inputs of the ADC show that the settling times within 1 LSB are 852 ns and 839 ns.

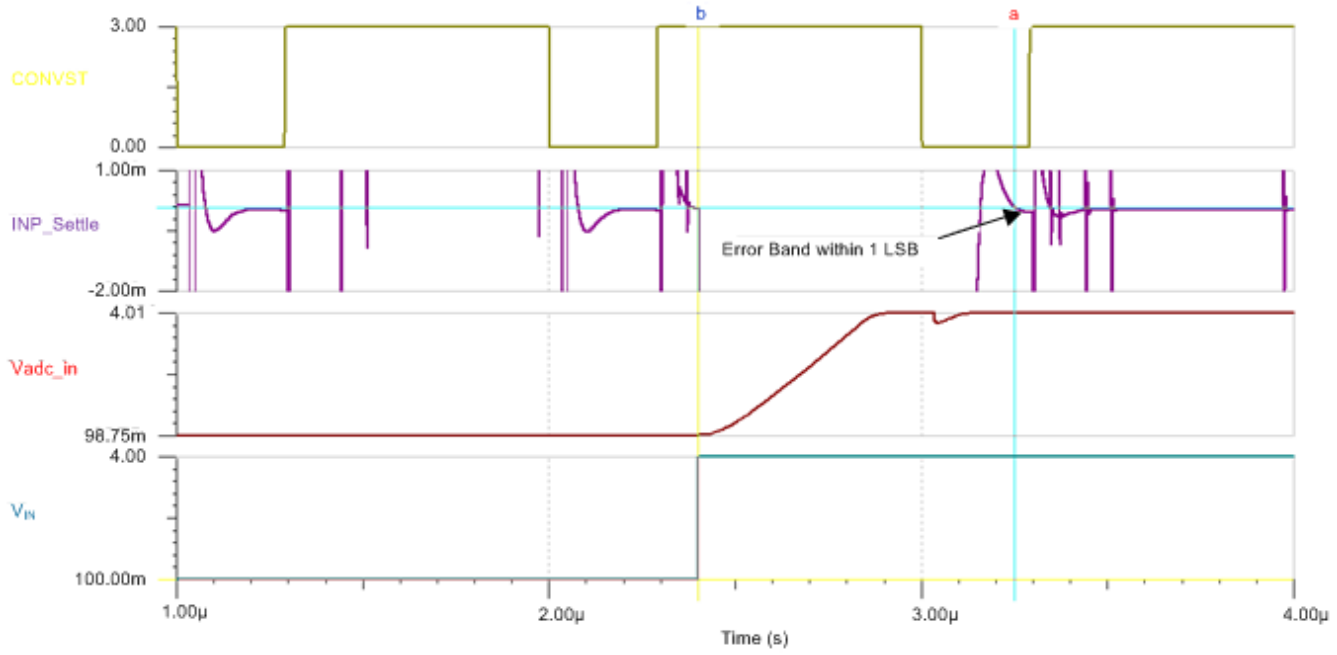


图 20. TINA-TI™ Simulation Result—ADC Input Settling Rising

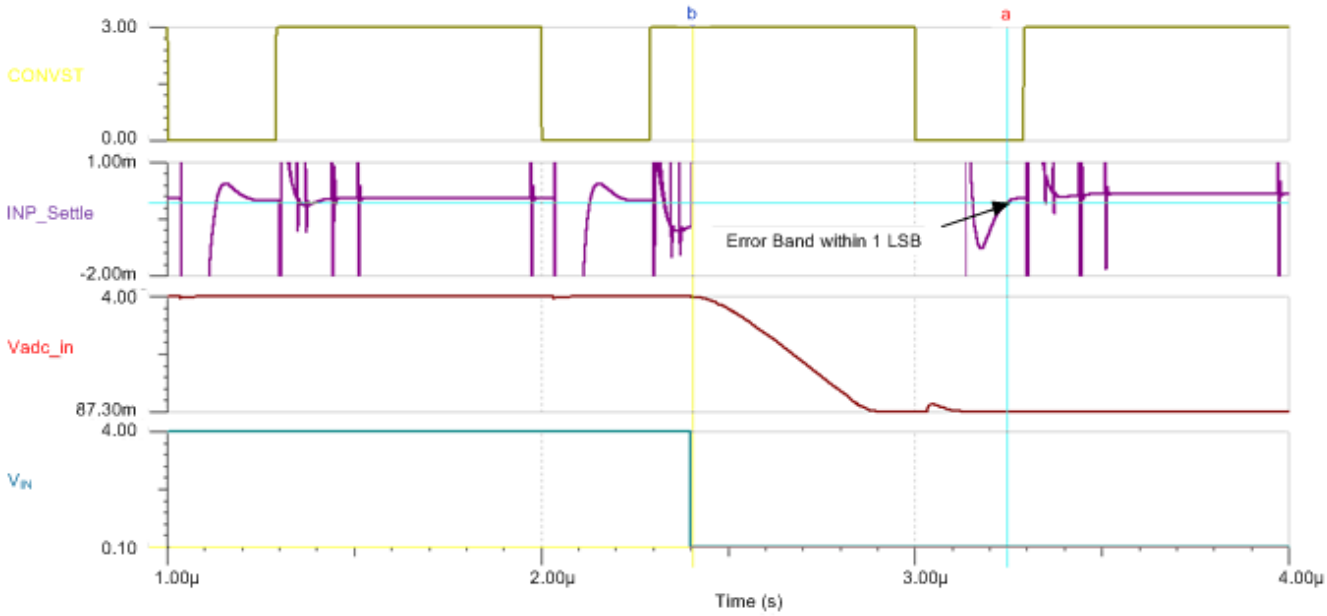


图 21. TINA-TI™ Simulation Result—ADC Input Settling Falling

4.2 Stability of Input Driver

The TINA-TI™ schematic in 图 22 simulates the stability of an input amplifier. In this design, the phase margin is the crucial parameter due to settling time (see further discussion in 节 2.2.1). A phase margin which is too small causes output ringing. For stability, the designer can increase the resistor to earn the phase margin as a viable solution; however, the RC time constant must be confirmed as converging within 1 LSB (see discussion in 节 2.4.1).

In this simulation, the amplifier behaves such as an open-loop configuration at a high frequency because the inductor has a very high impedance, which effectively makes it act as an open to the circuit. During DC operation, the circuit must bias at the normal operational region; otherwise, the simulated phase margin is incorrect. This circuit has a 60º phase margin at 8.94 MHz, as 图 23 shows.

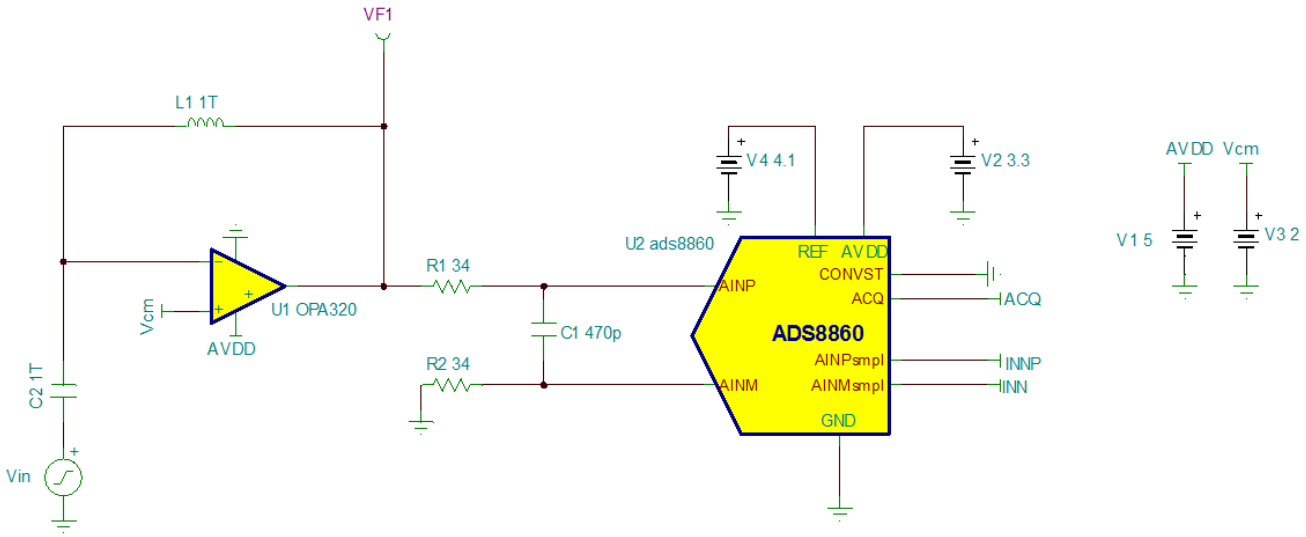


图 22. TINA-TI™ Schematic—Checking Input Amplifier Stability

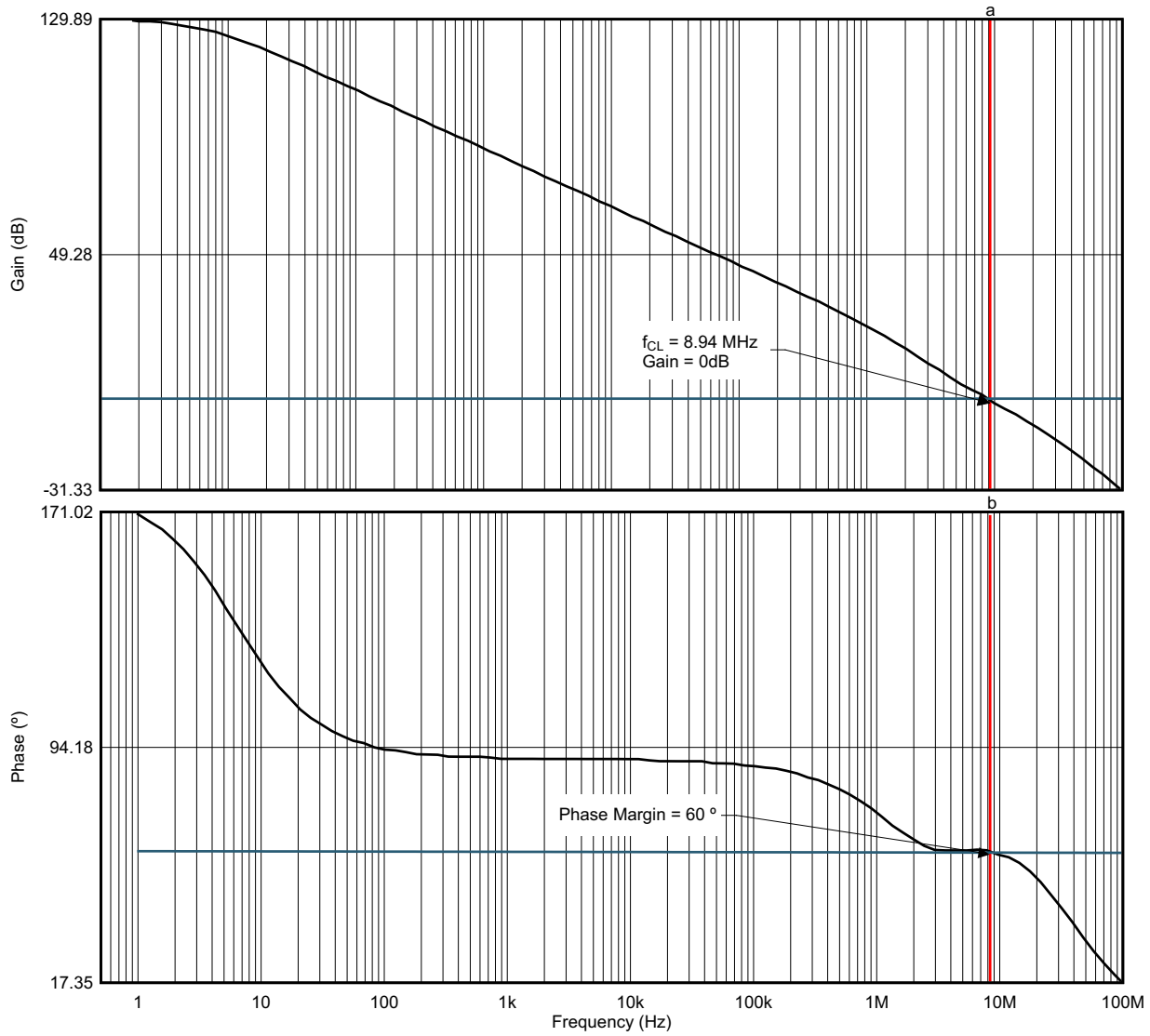


图 23. TINA-TI™ Simulation Result—Loop Gain Magnitude and Phase Plot for Input Driver Stability

4.3 Noise of Input Driver

The TINA-TI™ schematic that 图 24 shows is used for noise calculation of the input driver. The cutoff frequency of the RC filter is approximately 5 MHz, thus the total output noise starts to converge to 18.97 uV_{RMS} after 5 MHz (see 图 25).

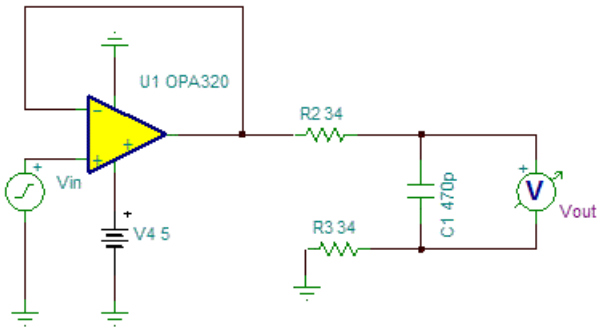


图 24. TINA-TI™ Schematic—Checking Input Driver Noise

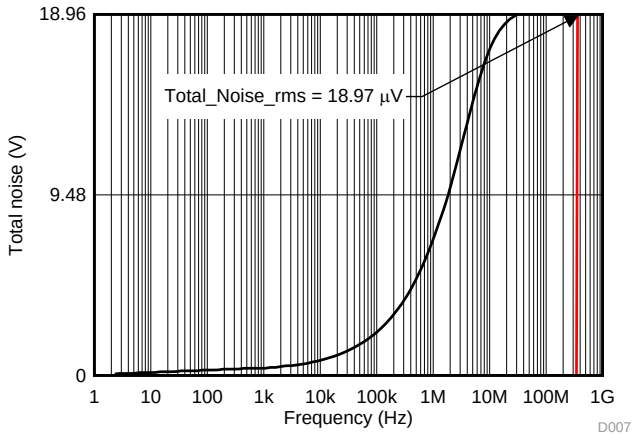


图 25. TINA-TI™ Simulation Result—Integrated Input Amplifier RMS Noise

5 Verification and Measured Performance

The measurement results for verification of this design are listed in this section.

5.1 Transient Settling

In this design, the worst-case scenario is that the multiplexer switches the channel; therefore, the input signal swings from the negative rail to the positive rail or vice versa. To make sure the signal is settling within 1 LSB, make sure that the measurement time is sufficient to confirm that any overshoot or ringing has been accounted for. As addressed in 2.3 节, the timing for settling is from the change of V_{IN} to the end of a sample. When V_{IN} has a longer settling time, the input driver settles closed to stable, as 图 26 and 图 27 show. Every point in these figures is based on the same settling time and takes the average of tens of thousands points to remove the noise. The step input also has a very-low drift output to guarantee the accuracy of test measurements.

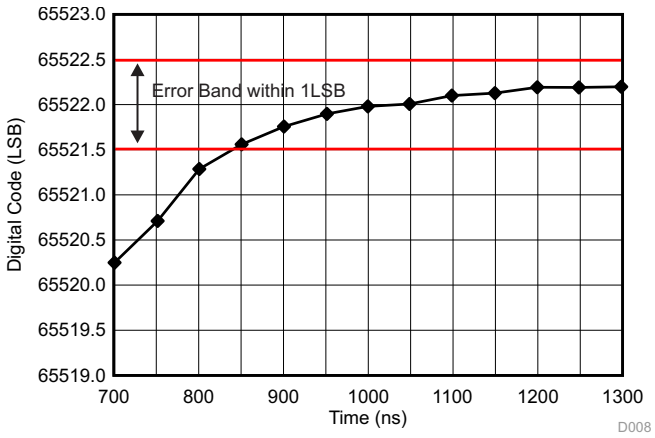


图 26. Measurement Data—Acquired Code in Different Settling Time for Rising Full-Scale Input

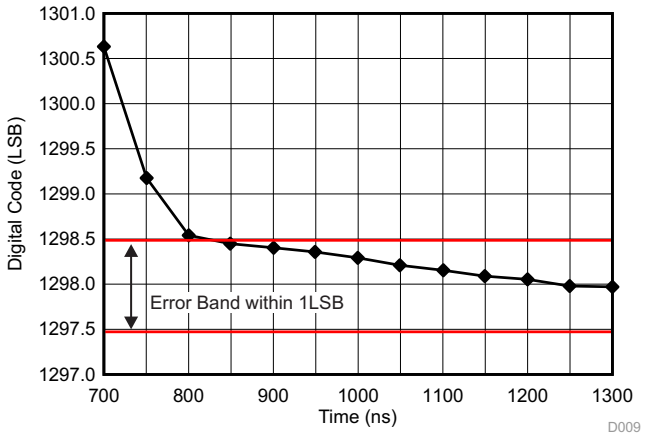


图 27. Measurement Data—Acquired Code in Different Settling Time for Falling Full-Scale Input

5.2 Static Performance

5.2.1 Effective Resolution

All ADC circuits suffer from some amount of inherent broadband noise contributed by the internal resistors, capacitors, and other circuitry, which is referred to the inputs of the ADC. The front-end driver circuit also contributes some noise to the system, which can also be referred to the ADC inputs. The cumulative noise, often known as the input-referred noise of the ADC, has a significant impact on the overall system performance. The most common way to characterize this noise is by using a constant DC voltage as the input signal and collecting a large number of ADC output codes. A histogram can then be plotted to show the distribution of output codes, which can be used to show the impact of noise on the overall system performance using TI's ADCPro™ software. In this design, the DC noise of the system is measured by inputting a mid-scale voltage, V_{IN} = ½ × V_{REF} = 2.048 V. 图 28 shows the resulting histogram of output codes that have a 16-bit effective resolution.

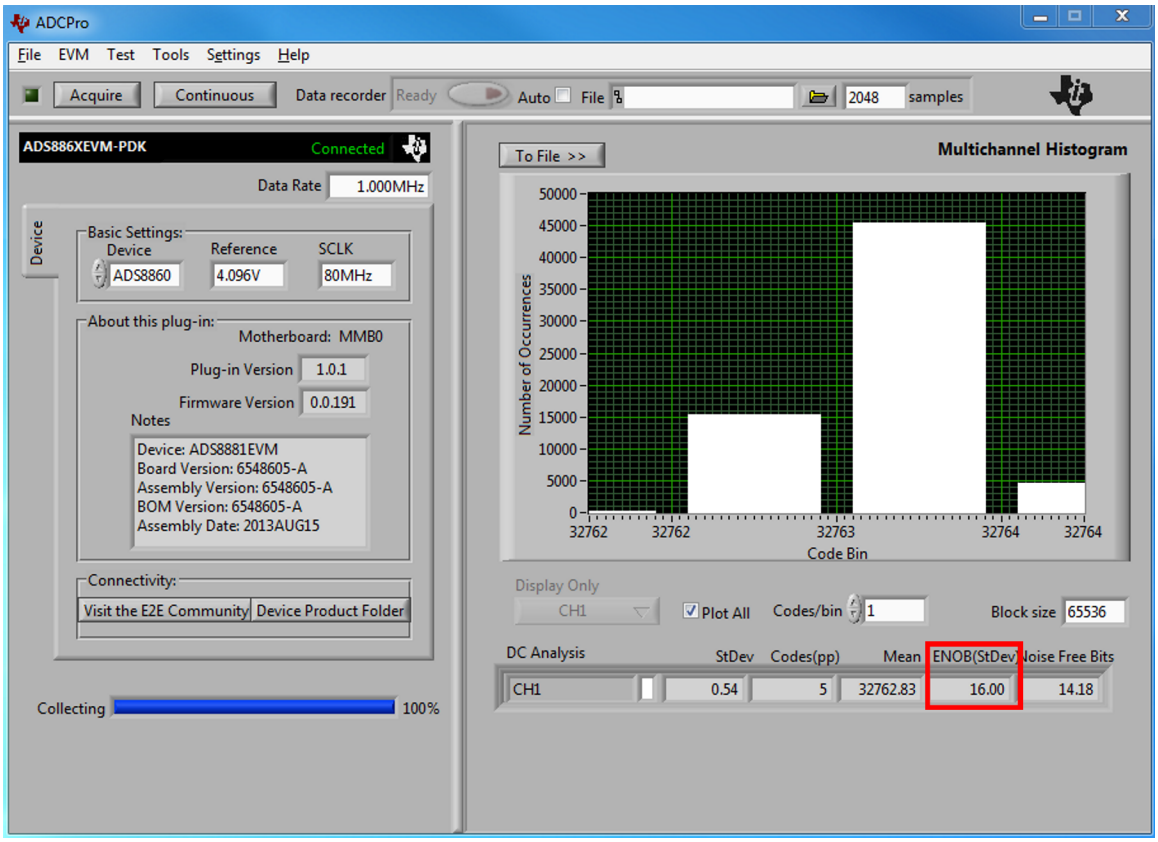


图 28. Measurement Data—Effective Resolution of DAQ Using ADCPro™

5.2.2 Linearity

The linearity of the system have been measured by sweeping the differential input voltage from 0.1 V to 4 V in 26 voltage steps and the integral non-linearity (INL) error is plotted after cancelling the offset and gain errors from the response. 图 29 shows the 26-point INL plot. The DAQ block provides an excellent linearity performance of ±0.5 LSB, as shown in the histogram. The amplifier used in the front end driver (OPA320) has a low output impedance, which results in extremely low distortion.

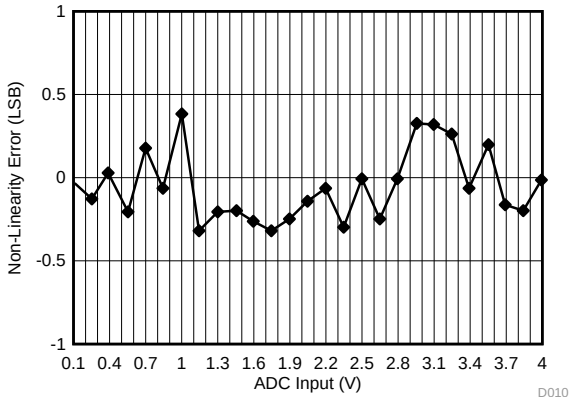


图 29. Measurement Data—ADC Linearity (26 Points)

5.3 Dynamic Performance

The measurements have been performed using a 10-kHz sinusoidal input signal. 图 30 shows the FFT of the DAQ. 表 4 shows the AC performance of the DAQ.

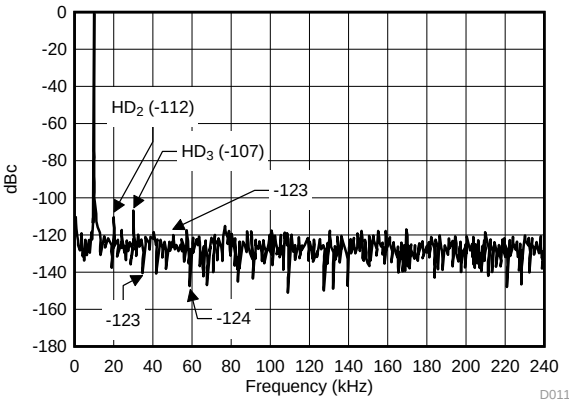


图 30. Measurement Data—FFT of DAQ Block

表 4. Measurement Data—Dynamic Performance

PARAMETERS	SPECIFICATIONS	MEASUREMENTS
Signal-to-noise ratio (SNR)	90 dB at V_{REF} = 4.096 V	90.5 dB
Total harmonic distortion (THD)	–104 dB at V_{REF} = 4.096 V	–105.4 dB
Signal-to-noise and distortion (SINAD)	89 dB at V_{REF} = 4.096 V	89.5 dB
Effective number of bits (ENOB)	14.5 bits	14.58 bits

6 Modifications

The comparison in 表 5 shows other RRIO, low-noise, low-drift, and wide-bandwidth precision amplifiers for input driver. To achieve very low power and a 1-MSPS settling time, the OPA320 is an excellent solution in this design. If the power consumption is not a primary design consideration, the OPA350, OPA353, and OPA365 can be used to achieve fast settling due to higher bandwidth and slew rate.

表 5. Alternative Amplifier for Modified System Requirements

OP AMP	RRIO	SETTLING TIME	SLEW RATE	BANDWIDTH	QUIESCENT CURRENT (MAX)
OPA350	Yes	480 ns	22 V/μs	38 MHz	7.5 mA
OPA353	Yes	480 ns	22 V/μs	44 MHz	8 mA
OPA365	Yes	440 ns	25 V/μs	50 MHz	5 mA

7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIPD173.

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIPD173.

7.3 PCB Layout Recommendations

The most important considerations in designing the PCB layout for this DAQ block are as follows:

- The length of traces from the reference buffer circuit (REF5040, THS4281, and OPA333) to the REFP input pin of the ADC should be kept as small as possible to minimize the trace inductance, which can lead to instability and potential issues with the accurate settling of the reference voltage.
- The input driver circuit, which comprises the OPA320 device, should be located as close as possible to the inputs of the ADC to minimize loop area, thus making the layout more robust against electromagnetic interference (EMI) and radio-frequency interference (RFI) rejection. Similarly, the resistors and capacitor of the charge bucket at the inputs of the ADC should be kept close together and close to the inputs of the ADC to minimize the loop area.
- The traces feeding the differential input voltage from the source up to the differential inputs of the ADC should be kept symmetrical without any sharp turns.

图 31 shows the complete PCB layout for this design.

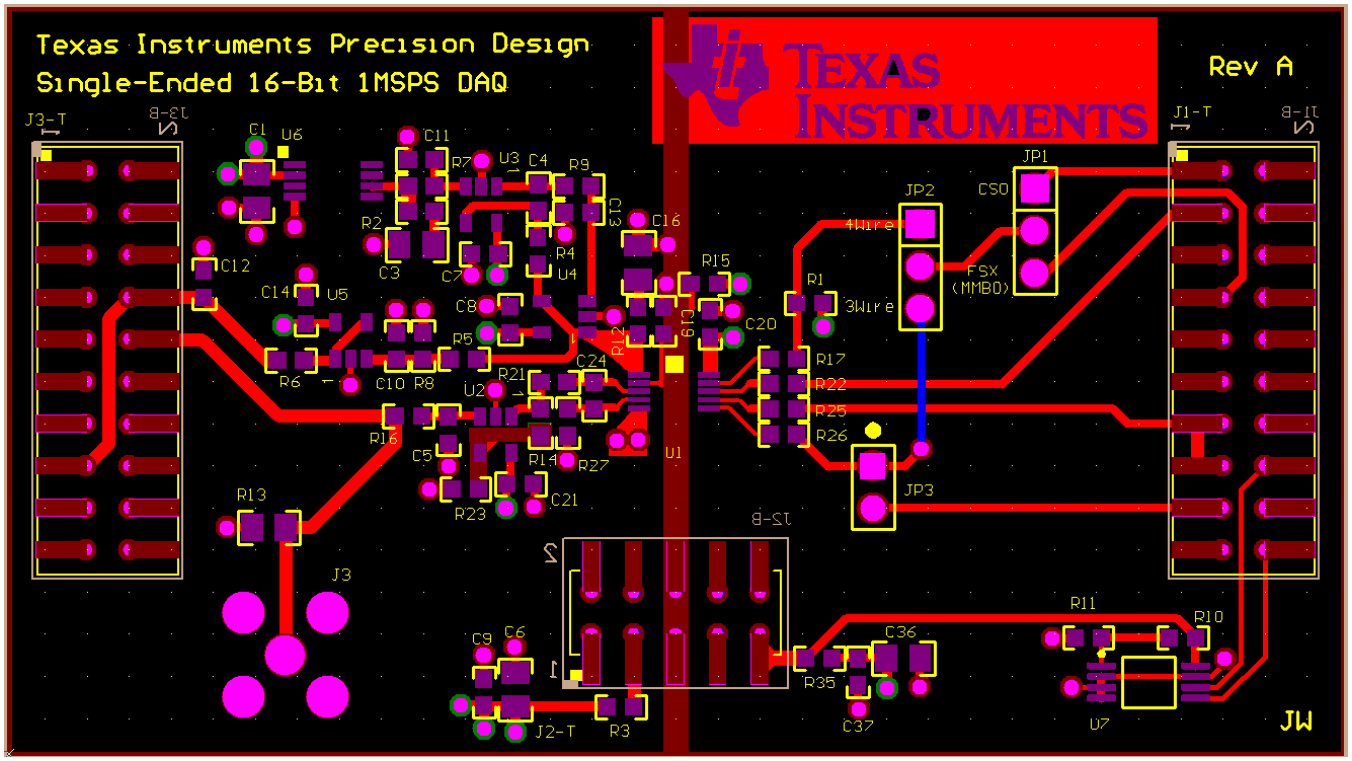


图 31. 16-Bit, 1-MSPS, Single-Ended DAQ Block PCB Layout

7.3.1 Layout Prints

To download the layer plots, see the design files at TIPD173.

7.4 Altium Project

To download the Altium project files, see the design files at TIPD173.

7.5 Gerber Files

To download the Gerber files, see the design files at TIPD173.

7.6 Assembly Drawings

To download the assembly drawings, see the design files at TIPD173.

8 Related Documentation

1. Texas Instruments, *16-Bit, 400-kSPS, Four-Channel MUX Data Acquisition System for High-Voltage Inputs Reference Design* , TIPD151 Reference Design (TIDU181)
2. Texas Instruments, *16-Bit, 1-MSPS, Serial Interface, microPower, Miniature, Single-Ended Input, SAR Analog-to-Digital Converter*, ADS8860 Datasheet (SBAS569)
3. Texas Instruments, *18-Bit Data Acquisition (DAQ) Block Optimized for 1-μs Full-Scale Step Response*, TIPD112 Reference Design (TIDU012)
4. Kay, Art; *Operational Amplifier Noise: Techniques and Tips for Analyzing and Reducing Noise*, Newnes 1st Edition, 2012
5. Texas Instruments; Green, T; *Selecting the right amplifier for precision CDAC SAR A/D*, TI Internal Presentation, Feb 2008
6. Texas Instruments; Kay, Art; Williams, I; *Slew rate*, TI Precision Workshop, Unpublished
7. Texas Instruments; Munikoti, Harsha; *A bone of contention: ENOB or effective resolution?*, TI E2E Community Forum - Precision Hub, June 2014 (http://e2e.ti.com/blogs_/b/precisionhub/archive/2014/06/13/a-bone-of-contention-enob-or-effective-resolution.aspx)

8.1 商标

9 About the Author

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修订历史记录 A

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (October 2014) to A Revision **Page**

- 已添加 new paragraph to *Reference Voltage Design* 22
- 已添加 *Integrated Reference and Buffer* subsection 33
- 已更改 schematics to updated versions available online through the *Schematics* subsection 44
- 已更改 schematics to updated versions available online through the *Bill of Materials* subsection 44

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