TI Designs：PMP20176
采用 TPS53647 且适用于 Intel® Stratix® 10 GX FPGA 的四相 140A 参考设计

说明

此参考设计侧重于提供适合为 Intel®Stratix®10 GX FPGA，并特别针对 1SG280-1IV 这一型号器件供电的紧凑型高性能多相解决方案。集成型 PMBus™方便轻松设置输出电压并遥测关键设计参数。此设计使得能够进行编程、配置、智能 VID 调整和电源控制，同时监控输入和输出电压、电流、功率和温度。TI 的 融合数字电源™设计人员用于对 FPGA 功率设计进行编程、监控、验证和特性描述。

资源

PMP20176	设计文件夹
TPS53647	产品文件夹
CSD95472Q5MC	产品文件夹
Fusion Digital Power 设计器	产品文件夹

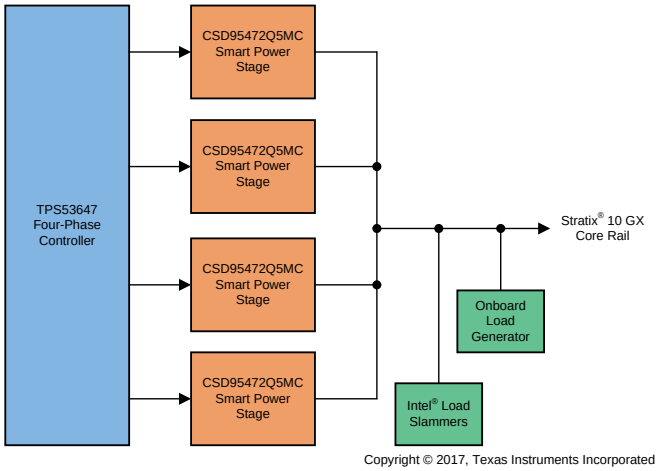
TI E2E™ Community — 咨询我们的 E2E 专家

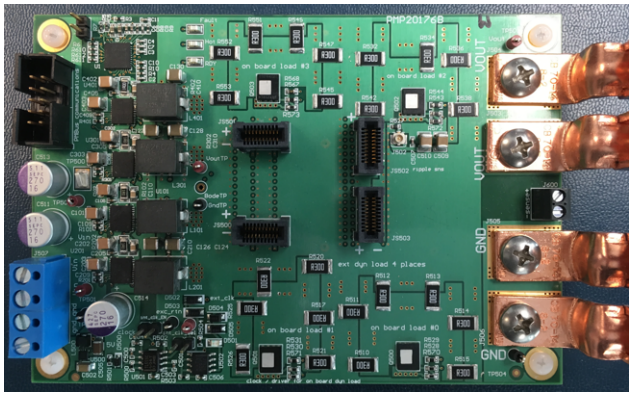
特性

- 全陶瓷输出电容器
- D-CAP+™调制器可实现出色的电流共享能力和瞬态响应
- 在 400kHz 条件下，峰值效率达 91.5%，V_{IN} = 12V，V_{OUT} = 0.9V，I_{OUT} = 60A
- 在无气流条件下具有优异的热性能
- 过压、过流和过热保护
- 兼容 PMBus，可实现输出电压设置和 V_{IN}、V_{OUT}、I_{OUT} 和温度遥测
- PMBus 和引脚捆绑编程选项

应用

- FPGA 内核电压轨电源
- 以太网交换机
- 防火墙和路由器
- 电信和基带单元
- 测试和测量





1 系统 说明

PMP20176 是一款高效率的大功率密度设计，采用四相降压控制器和 TI 专有智能功率级，该设计经优化适用于 Intel® Stratix® 10 GX FPGA 内核电压轨 应用。这些 FPGA 通常用于企业交换、电信基础设施、测试和测量以及云计算基础设施环境等这些高利用率应用，本设计可提供这些应用所需的高电流和快速瞬态响应。

400kHz 开关频率可维持 90.1% 的热设计电流效率，149kHz 高交叉频率可提供快速瞬态响应，且不存在稳定性问题。TPS53647 控制器使用 D-CAP+™ 多相调制器，可提供快速瞬态响应功能并能够精密调节输出电压。D-CAP+ 调制器在设计的四个相位之间实现可靠的电流平衡，在各种运行条件下都保持稳定，并对控制环路提供简单的 II 型补偿。此外，TPS53647 可兼容 TI 智能功率级（如本设计中使用的 CSD95472），后者可为高效率和集成式电流监控电路提供优化的驱动器 FET 解决方案。这些智能功率级的使用可节省布局面积，并消除了对外部电流感应组件的需求。

如果使用低功耗 Stratix 10 GX FPGA，或需要其他输出电容器组合，可在 WEBENCH®设计工具中修改设计。

1.1 主要系统规格

表 1. 主要系统规格

参数	规范
输入电源	12V ±10%
标称输出电压	0.9V
直流调节	<1.2%
直流纹波	最大 2%
交流纹波	±5%
最大输出电流	140A
热设计电流	100A
最大负载阶跃	500A/µs 时为 75A
相位数	四
开关频率	400kHz

2 System Overview

2.1 Block Diagram

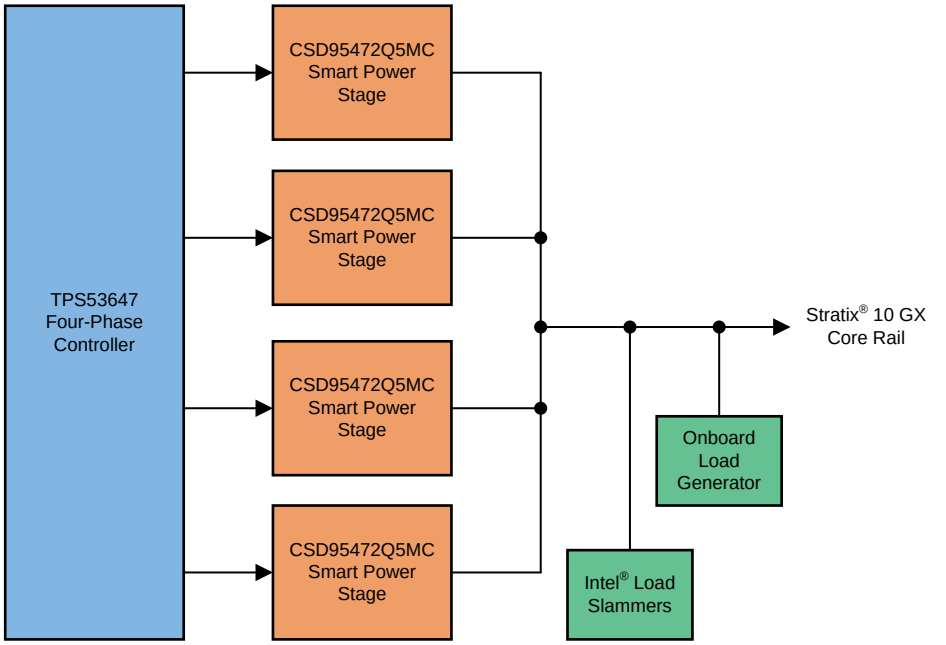


图 **1. PMP20176 Block Diagram**

2.2 Highlighted Products

2.2.1 TPS53647 – Four-Phase, D-CAP+™ Step-Down Buck Controller With NVM and PMBus™ Interface for ASIC Power and High-Current Point-of-Load

Features:

- 8-bit selectable boot voltage through pinstrap or non-volatile memory (NVM)
- One-, two-, three-, or four-phase operation
- 1.8-V or 3.3-V compatible PMBus™ system interface for fault monitoring and voltage, current, power, and temperature telemetry
- D-CAP+ modulator and eight independent levels of overshoot and undershoot reduction for excellent transient response
- Adjustable voltage positioning
- Dynamic phase shedding with programmable current threshold
- 6×6-mm, 40-pin, QFN PowerPAD™ integrated circuit package

2.2.2 CSD95472Q5MC – 60-A Synchronous Buck NexFET™ Smart Power Stage With DualCool™Package

Features:

- 60-A continuous current capability
- Low power loss of 2.3 W at 30 A
- High-frequency operation up to 1.25 MHz
- 3.3-V and 5-V pulse-width modulation (PWM) compatible
- Temperature-compensated bidirectional current sense
- Analog temperature output
- Integrated bootstrap diode and optimized deadtime
- 5-mm × 6-mm SON, low inductance, DualCool™ packaging

3 Getting Started Hardware and Software

3.1 Hardware

The hardware for the design is as follows:

- 12-V supply capable of 20 A
- 5-V supply capable of 1 A
- Function generator capable of pulses with < 1-µs rise times (optional)
- Oscilloscope with differential and passive probes
- Digital multimeter
- Three 25-A Intel Mini Load Slammers and associated control board (optional)

The function generator must be used if the onboard clock generator is not used to drive the onboard load transient generator. Intel mini load slammers can be used in place of the entire onboard load circuitry if desired.

3.2 Software

This design uses TI's Digital Fusion Power Designer software.

3.3 Test Setup

图 2 shows the PMP20176 test setup.

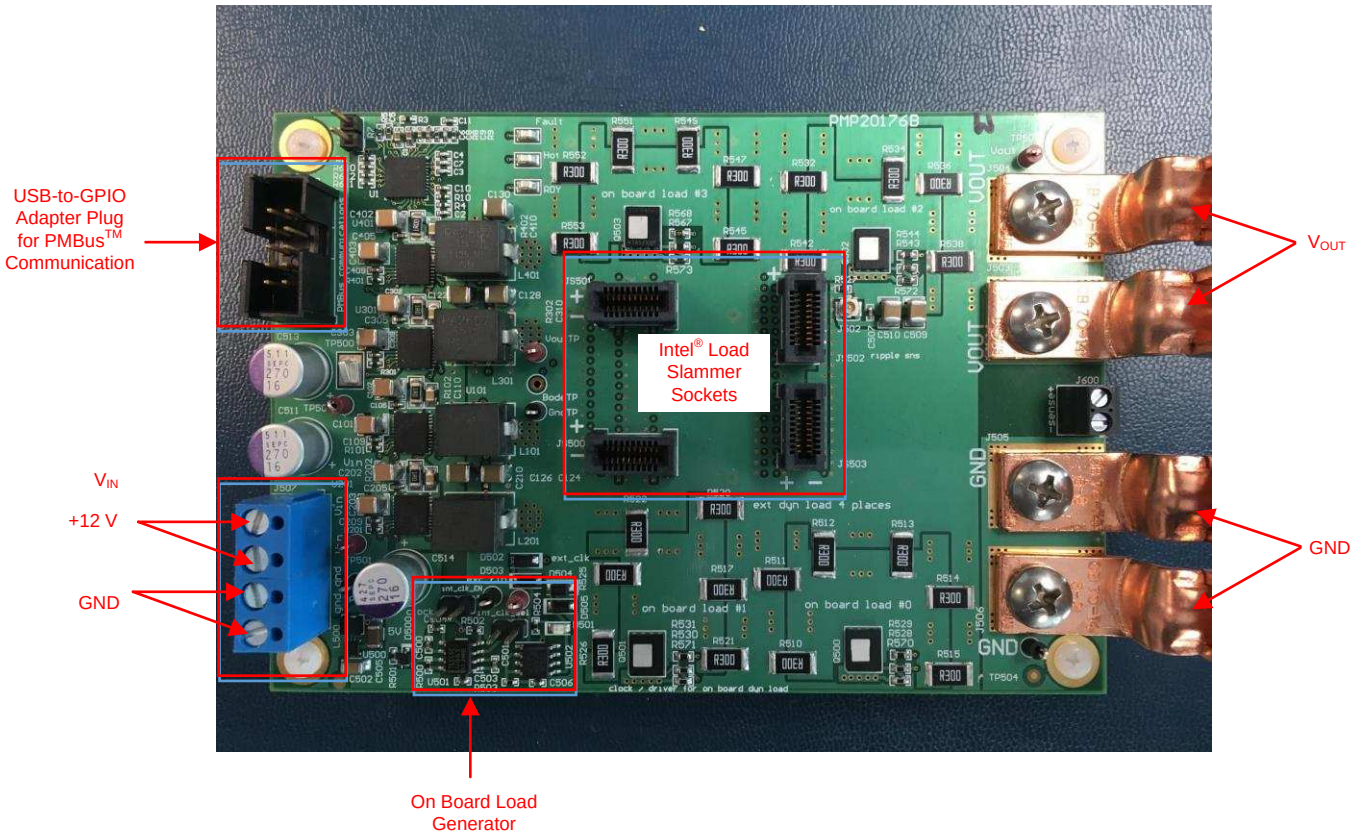


图 2. PMP20176 Test Setup

4 Test Results

4.1 Efficiency and Power Loss

Peak efficiencies of 91.9% (V_{IN} = 10.8 V), 91.5% (V_{IN} = 12 V), and 91.1% (V_{IN} = 13.2 V) have been measured for this design, as 图 3 shows. At a thermal design current (TDC) of 100 A, the efficiencies were 90.3%, 90.1%, and 89.9% for V_{IN} = 10.8 V, 12 V, and 13.2 V, respectively. When the load current is set to the maximum current of 140 A, the efficiency is 87.8% for V_{IN} = 10.8 V, 87.7% for V_{IN} = 12 V, and 87.6% for V_{IN} = 13.2 V. The curve in 图 3 and 图 4 includes the losses associated with the 5-V power stage VDD rail as well as the power losses associated with the inductors of each phase.

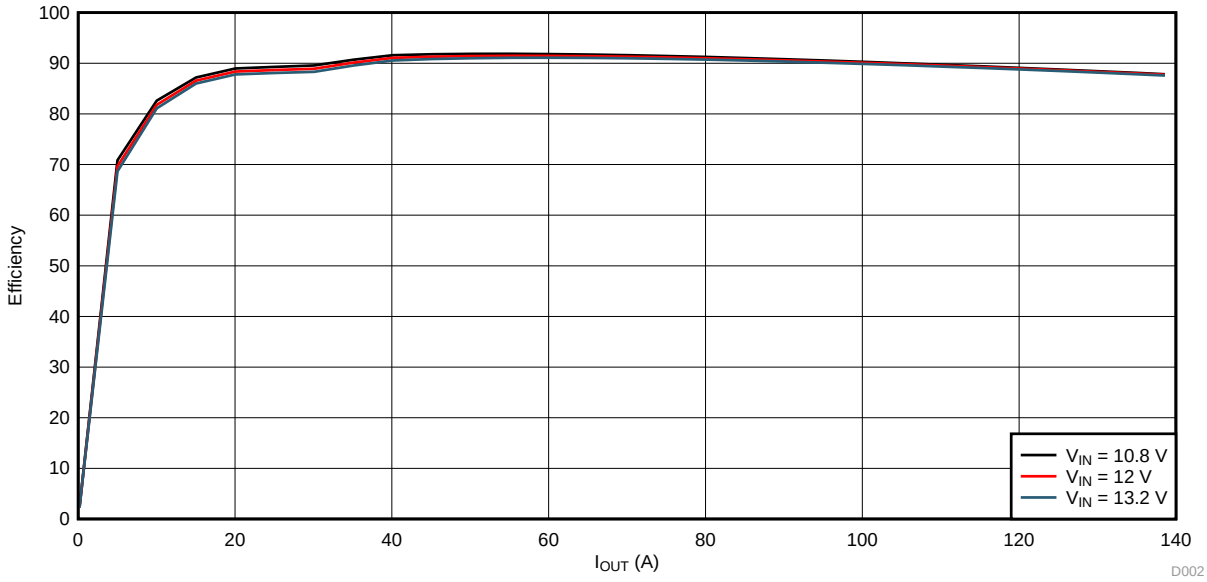


图 3. PMP20176 Efficiency Curves: V_{OUT} = 0.9 V, 400 kHz

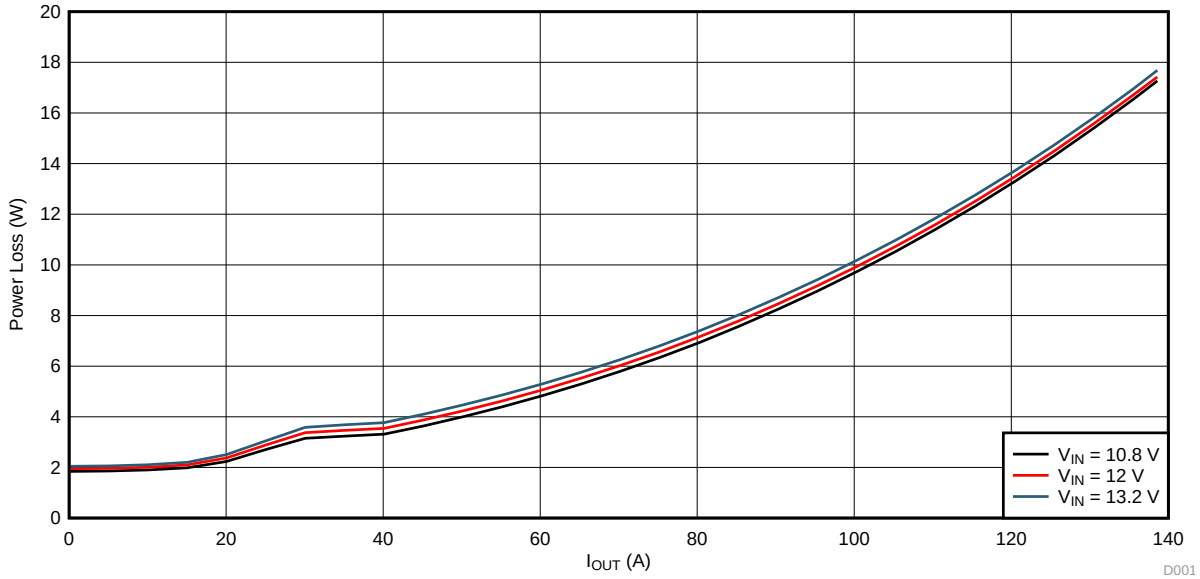


图 4. PMP20176 Power Loss Curves: V_{OUT} = 0.9 V, 400 kHz

4.2 Phase Ringing and Loop Stability

To ensure that the power MOSFETs inside the CSD95472 are not being damaged during normal operation, the phase nodes are probed at various output currents to ensure that any ringing is safely within the data sheet limits. No anomalies were observed during testing and 图 5 shows one such measurement with the load current set to 40 A. A peak voltage of 20.7 V with a duration of < 10 ns is measured, which places the ringing safely within the data sheet limits. 图 6 provides the results for measuring the switching frequency and shows it to be within the data sheet limits with no double pulsing or excessive jitter, which indicate that the system is stable.

To check the stability further, the control loop bode plot is obtained using a network analyzer with 49° of phase margin being measured at the 149-kHz unity gain frequency (see 图 7).

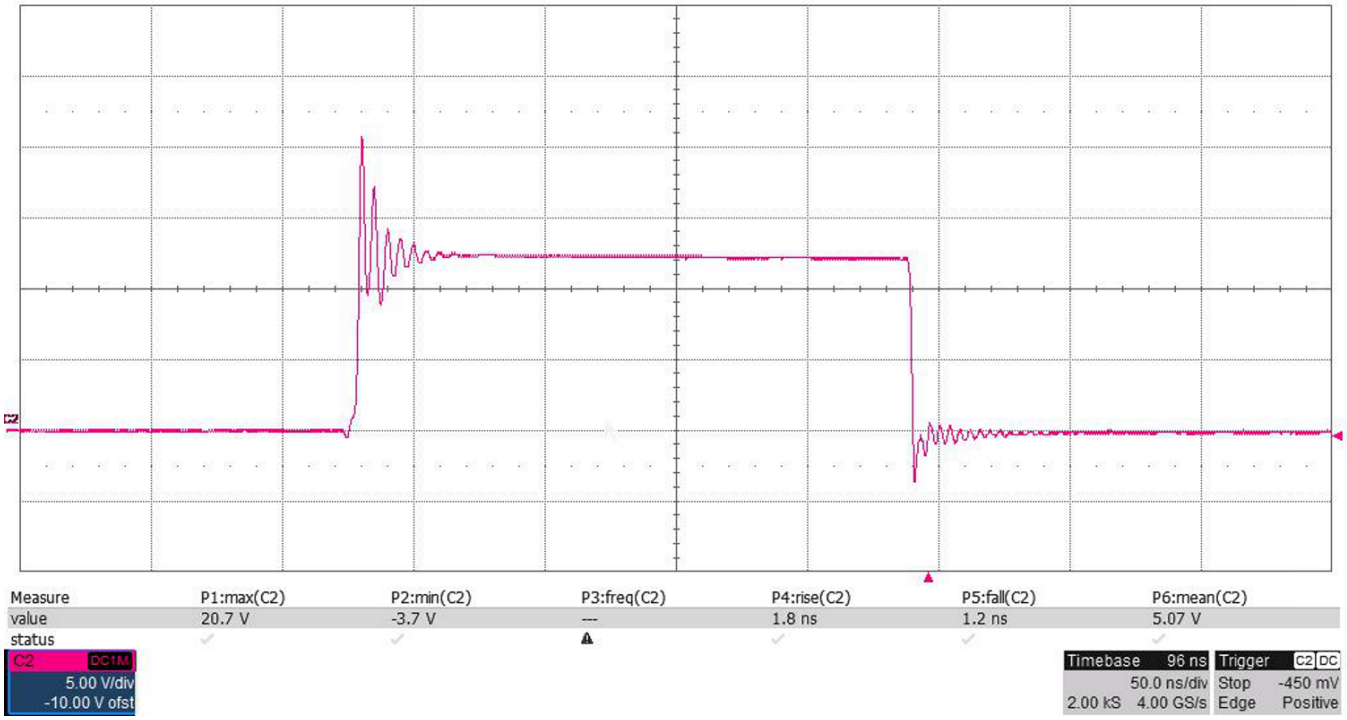


图 5. Phase Node Ringing With 40-A Load

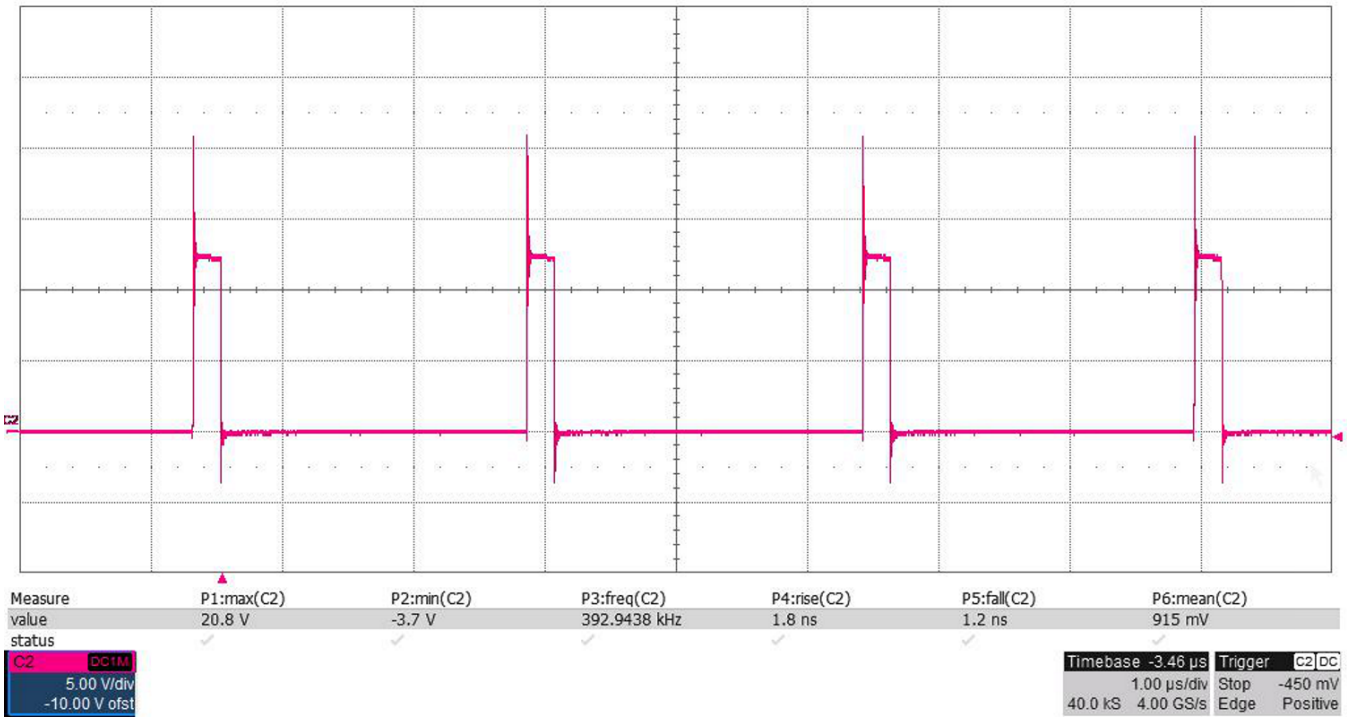


图 6. Phase Node Pulses

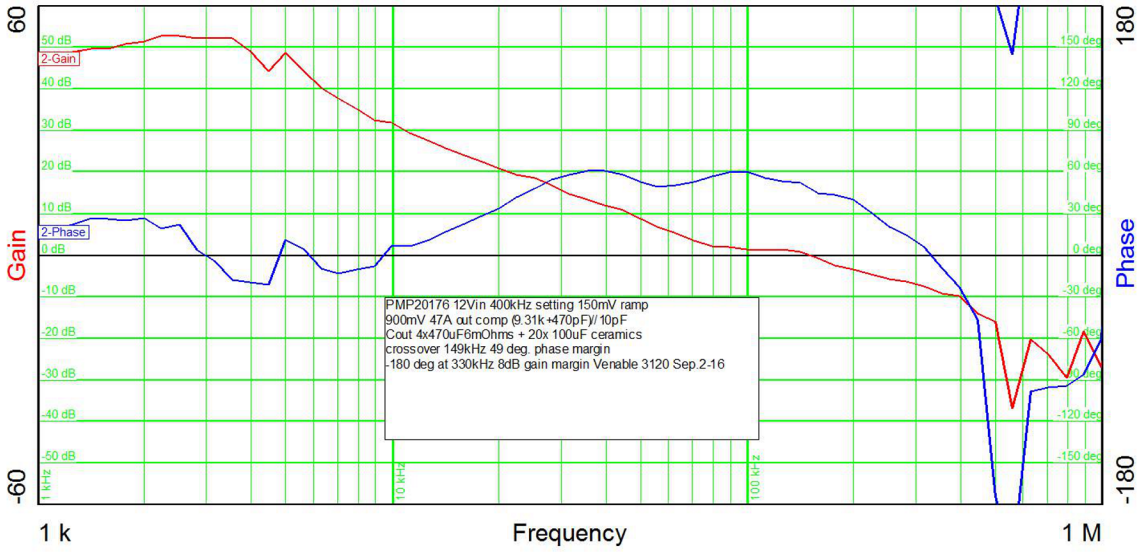


图 7. Bode Plot: 50-A Load, V_{IN} = 12 V

4.3 Thermal Performance

The design was placed in a 25°C environment under 100-A and 140-A loads at an output voltage of 0.9 V until it reached thermal equilibrium before taking measurements of the power stages and inductors using an infrared camera. Neither airflow or heatsinks are used at the TDC current to test a worst-case scenario. A setup more closely mimicking an end application was used when the 140-A current was applied.

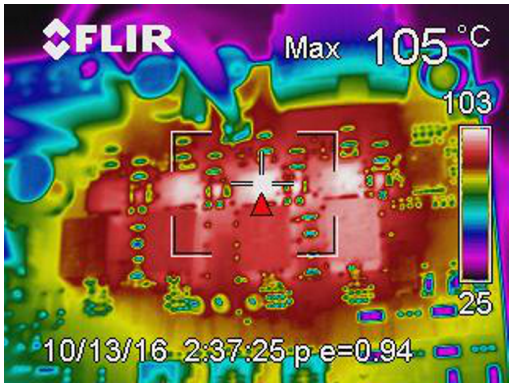


图 8. 100-A Load Thermal Performance, No Airflow

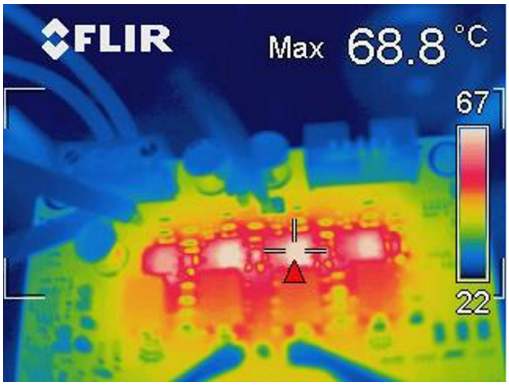


图 9. 140-A Load Thermal Performance, ≈350 LFM

4.4 Transient Response

A load step of 75 A was applied to the TPS53647 regulator under two test conditions. The first test condition is from 4 A to 79 A and the second test condition is from 65 A to the maximum load of 140 A. Under both conditions the load frequency was swept from 1 kHz to 1 MHz to check the stability under a wider range of operational corners. With no DC load line and an AC tolerance of ±5%, a peak-to-peak voltage swing of 90 mVpp is allowed at the nominal output voltage of 0.9 V. No stability issues were observed during testing and the output voltage remained within the regulation window.

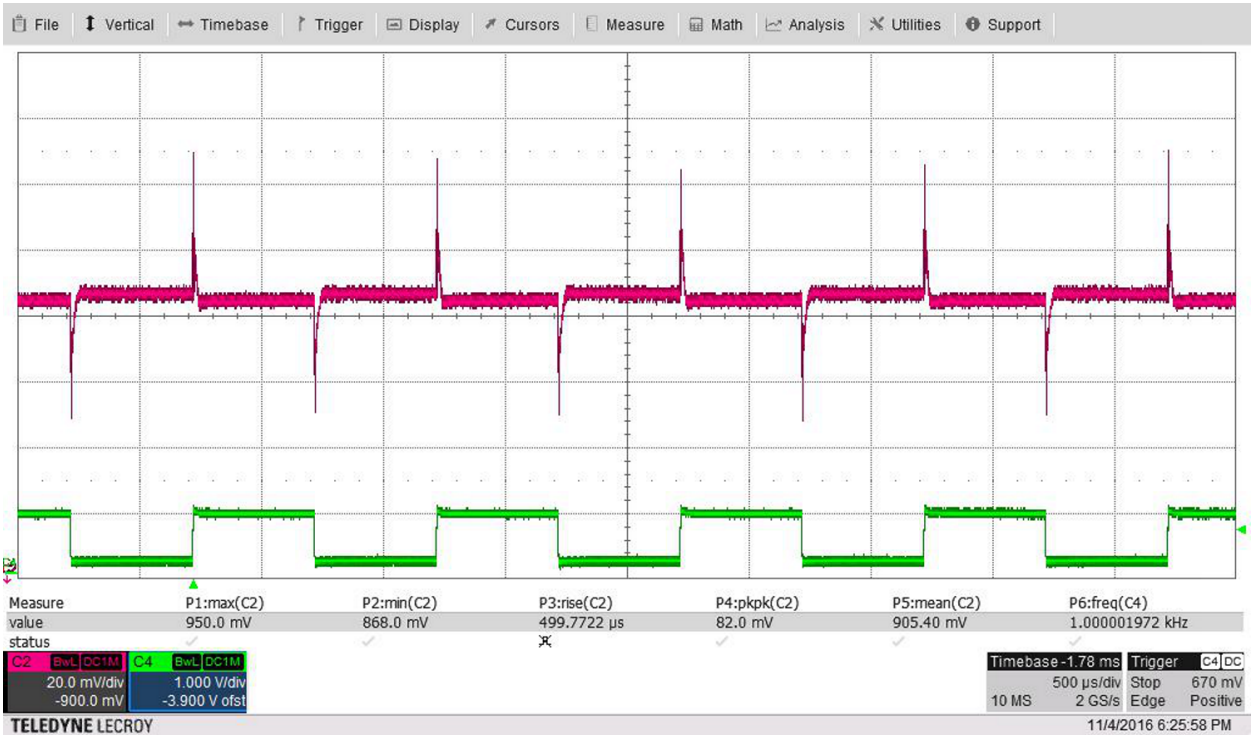


图 **10. 4-A to 79-A Transient, 1-kHz Load Frequency**

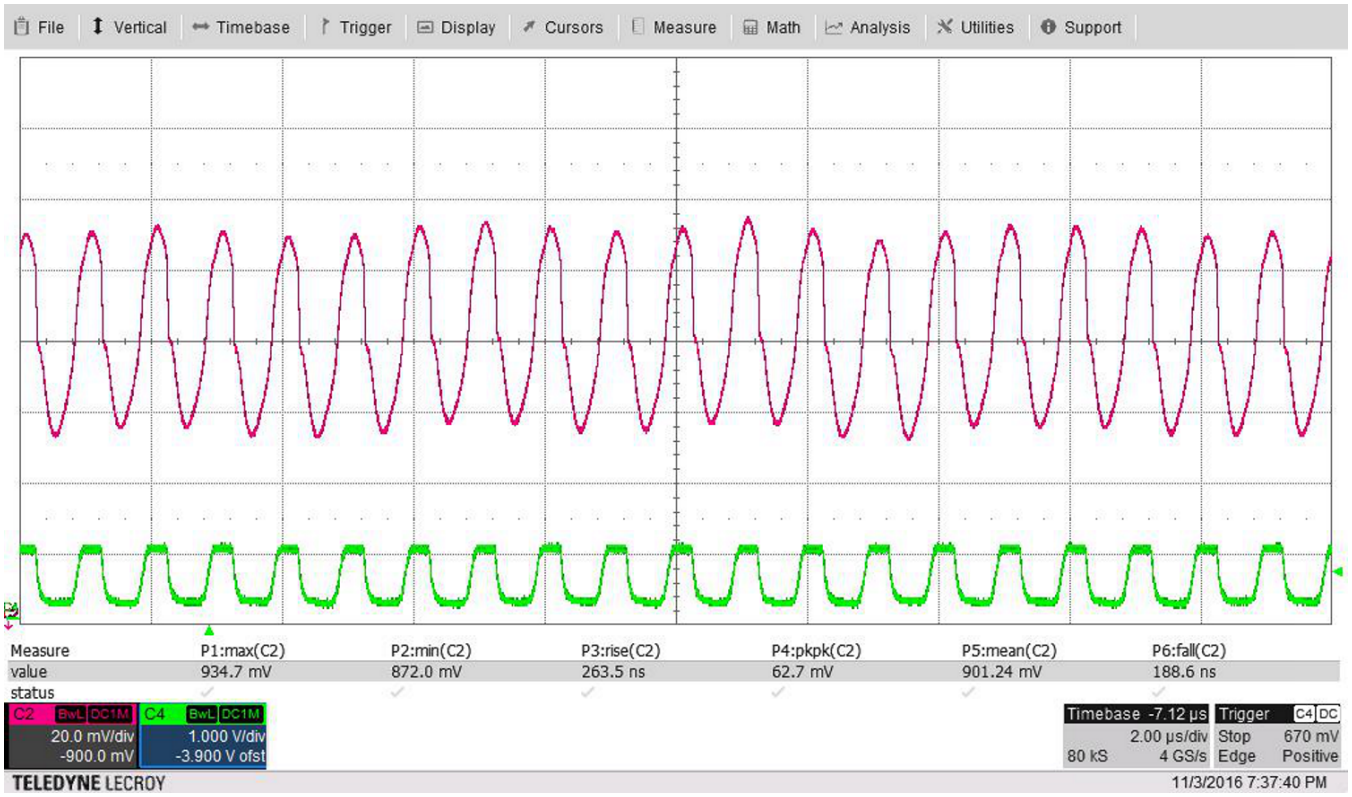


图 **11. 4-A to 79-A Transient, 1-MHz Load Frequency**

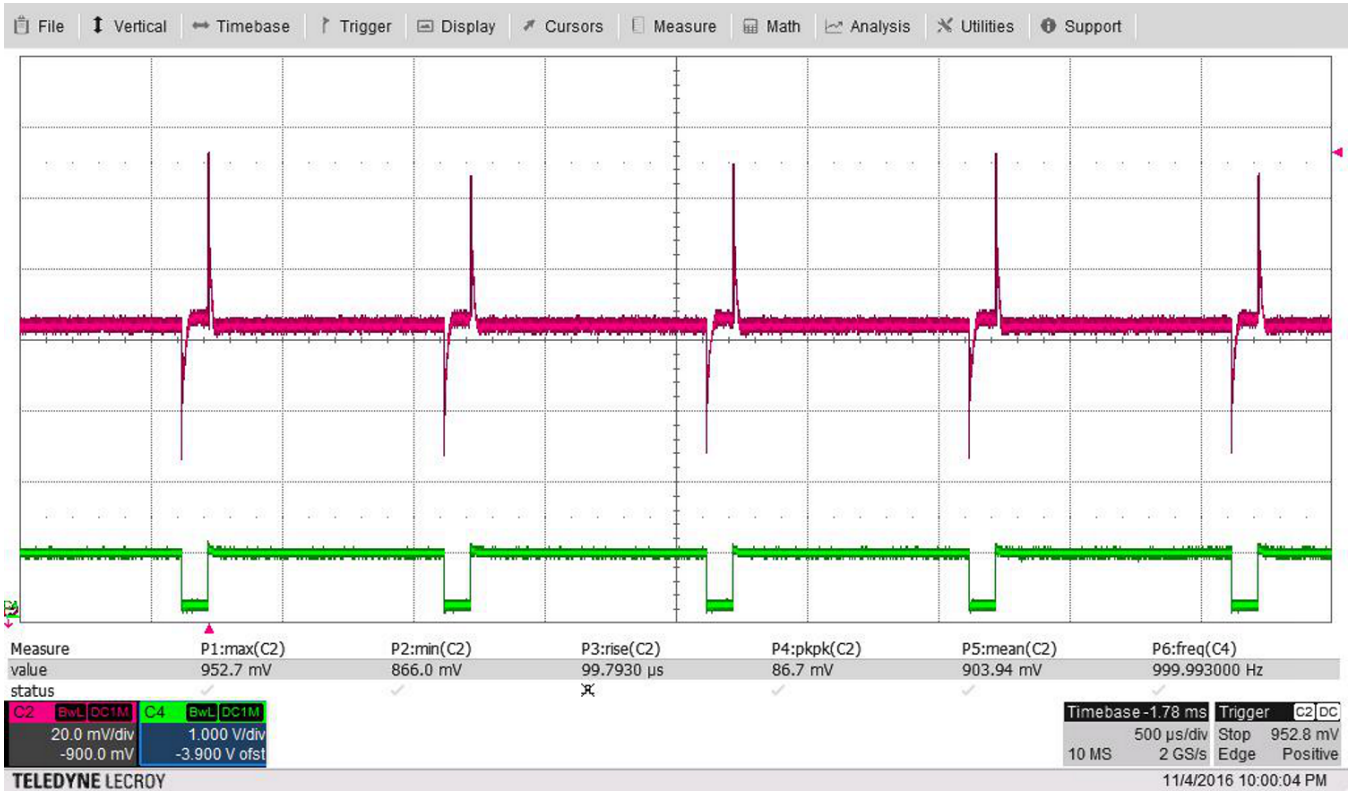


图 12. 65-A to 140-A Transient, 1-kHz Load Frequency

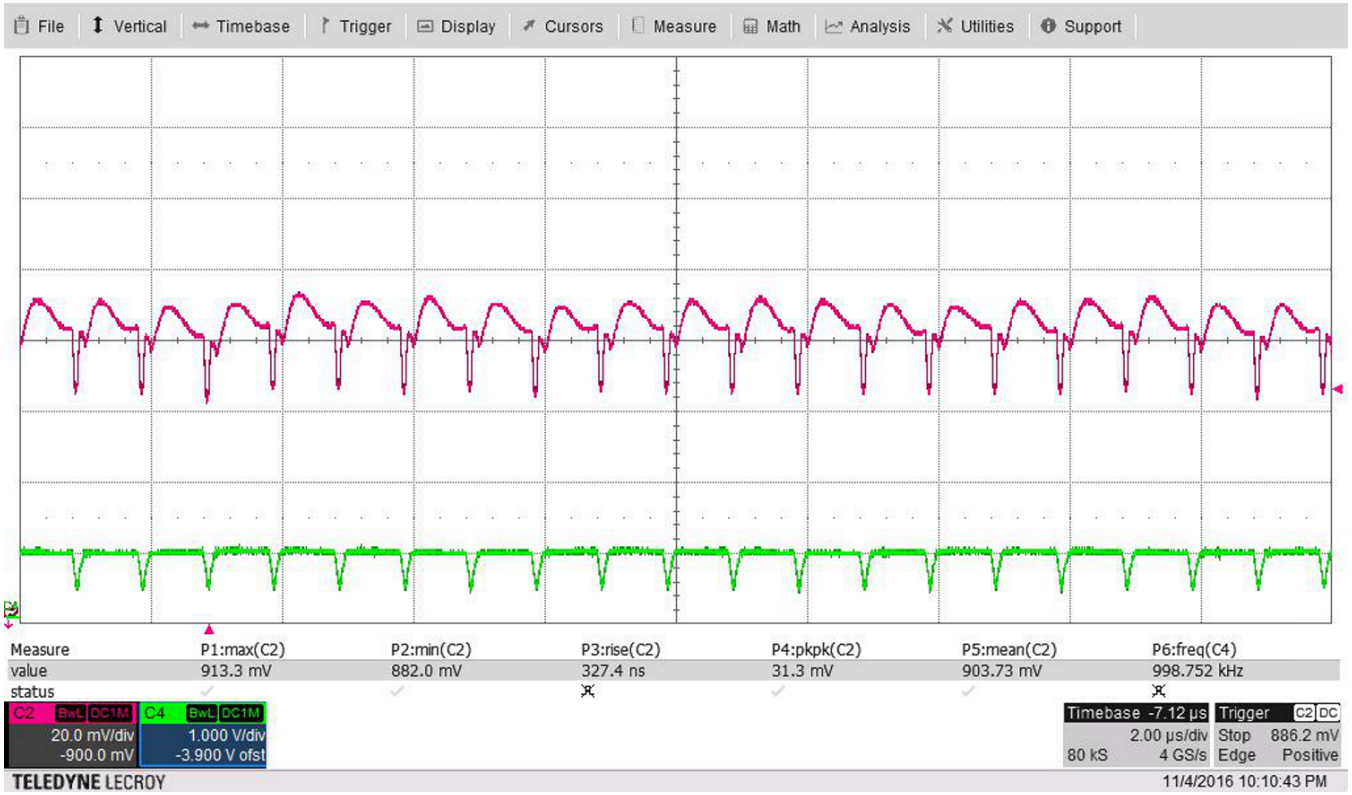


图 13. 65-A to 140-A Transient, 1-MHz Load Frequency

表 **2. Transient Response Validation Results**

LOAD STEP	TRANSIENT SPECIFICATION AT NOMINAL OUTPUT VOLTAGE	MEASURED RESULTS
4 A to 79 A, 1 kHz	90 mV_{PP}	82 mV_{PP}
4 A to 79 A, 1 MHz	90 mV_{PP}	62 mV_{PP}
65 A to 140 A, 1 kHz	90 mV_{PP}	86.7 mV_{PP}
65 A to 140 A, 1 MHz	90 mV_{PP}	31.3 mV_{PP}

4.5 Start-Up and Shutdown

Start-up and shutdown waveforms were taken at 4-A and 100-A loads while monitoring the enable, output voltage, and power good signals. For the high-current shutdown scenario, V_{OUT} is dragged below ground because the electronic load attached to the output of the regulator tries to maintain the 100-A load. Such behavior does not occur in real applications.

In the following scopeshots, C2 is the Enable signal, C3 is the V_{OUT} signal, and C4 is the PGOOD signal.

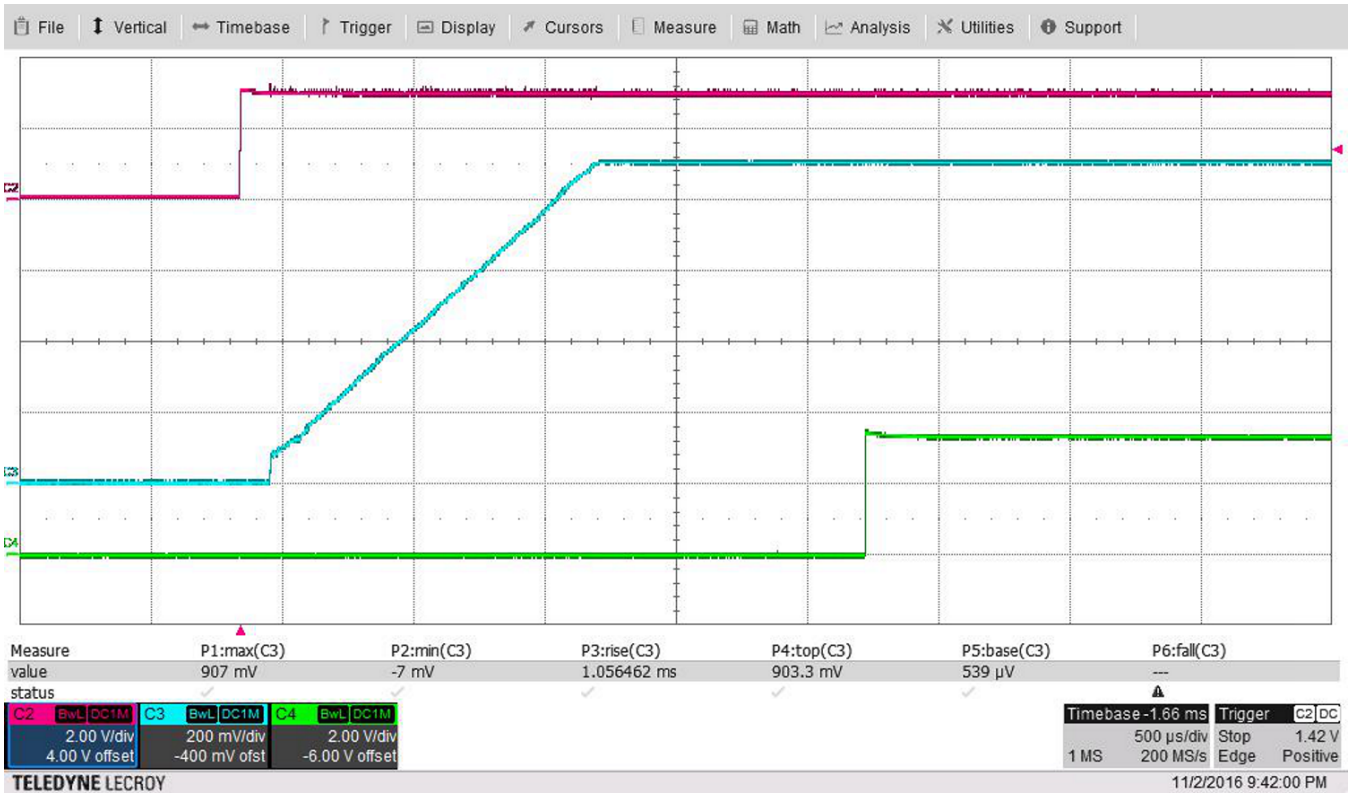


图 **14. 4-A Start-Up**

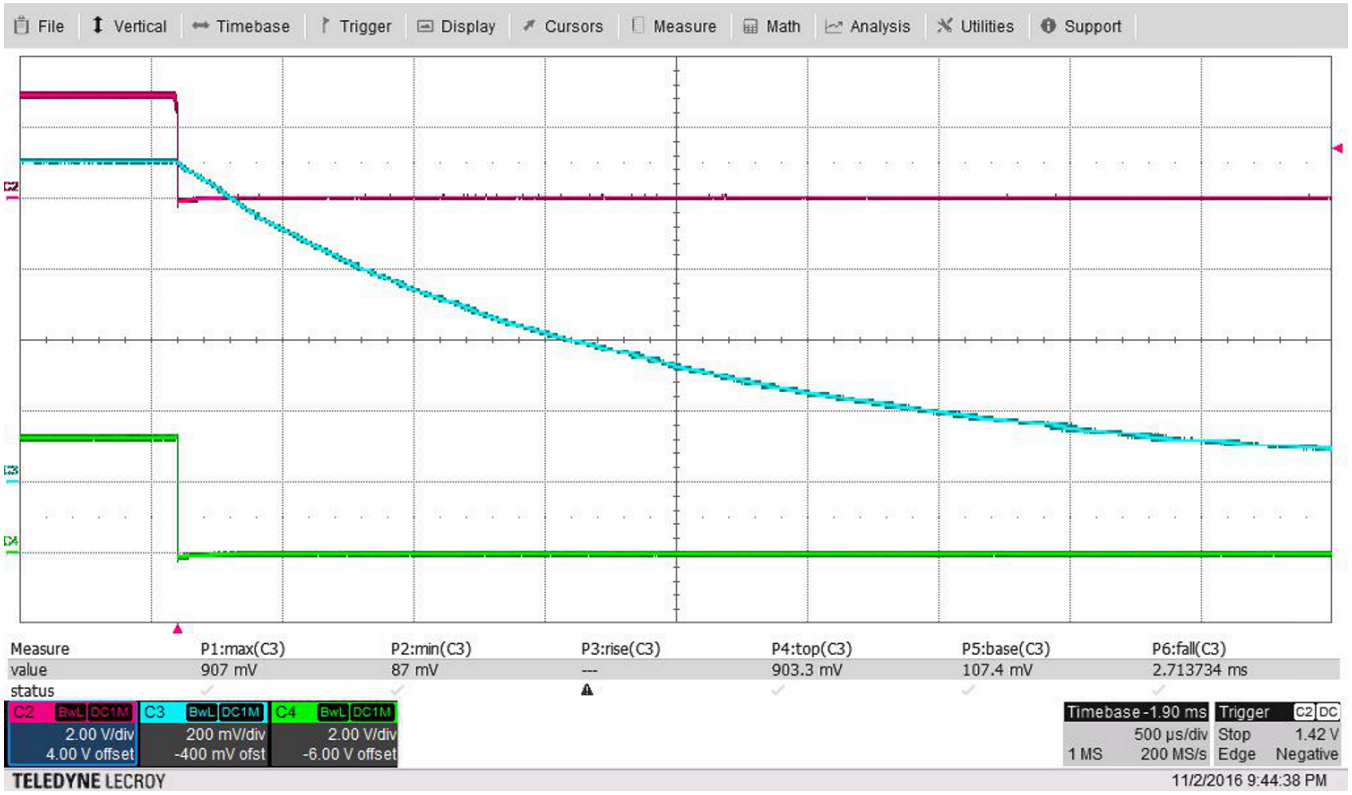


图 **15. 4-A Shutdown**

图 **16. 100-A Start-Up**

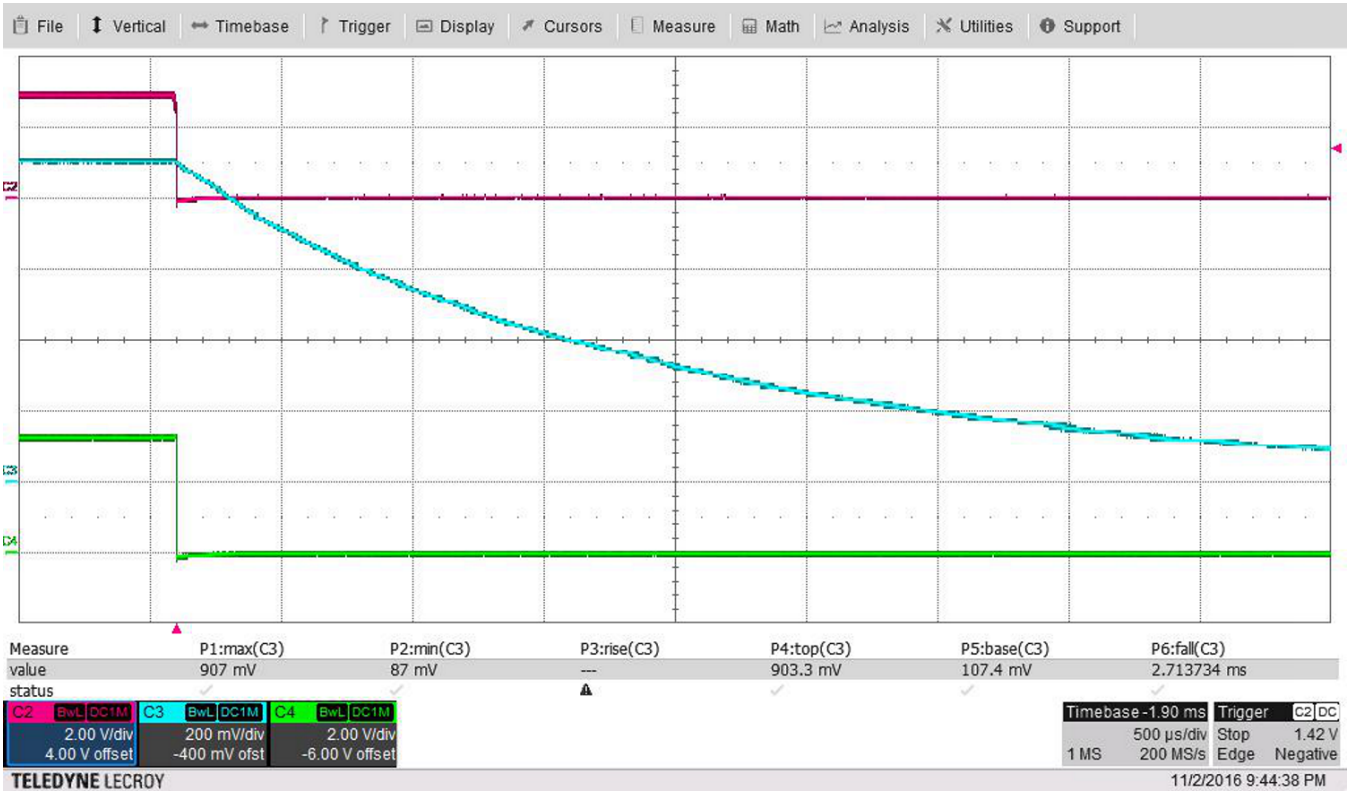


图 **17. 100-A Shutdown**

4.6 Protection Circuitry

The TPS53647 device also performed admirably when testing the on-chip protection mechanisms for this application. The overcurrent and overtemperature protection features work as intended when triggered and prevent the load and power stages from damage. Upon hitting the overcurrent limit, the controller enters hiccup mode and attempts to restart. 图 18 shows a single shutdown and 图 19 shows the hiccup mode. A successful power-up only occurred after removing the high current. After the overtemperature threshold was crossed, the output voltage decayed to 0 V (according to the load current) until the part had cooled off and a restart was triggered. In 图 20 and 图 21, a recovery time of 12 seconds was observed after the overtemperature fault occurred. For all testing, the PGOOD signal toggles low when the event occurs to signal a fault until V_{OUT} is brought back into regulation.

During overcurrent events, V_{OUT} is dragged below ground because the electronic load attached to the output of the regulator tries to maintain the load. Such behavior does not occur in real applications.

In the following scopeshots, C2 is the V_{OUT} signal and C4 is the PGOOD signal.

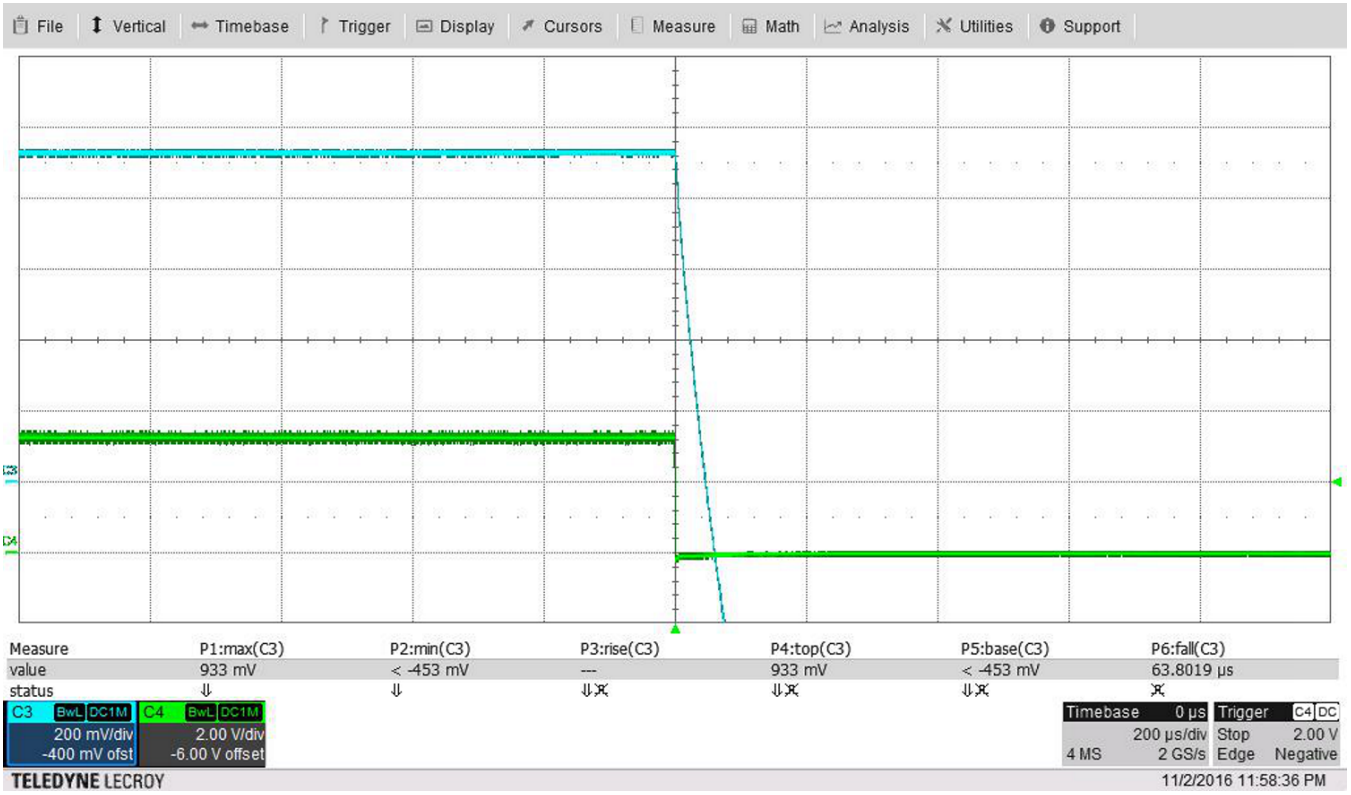


图 **18. Single Overcurrent Shutdown**

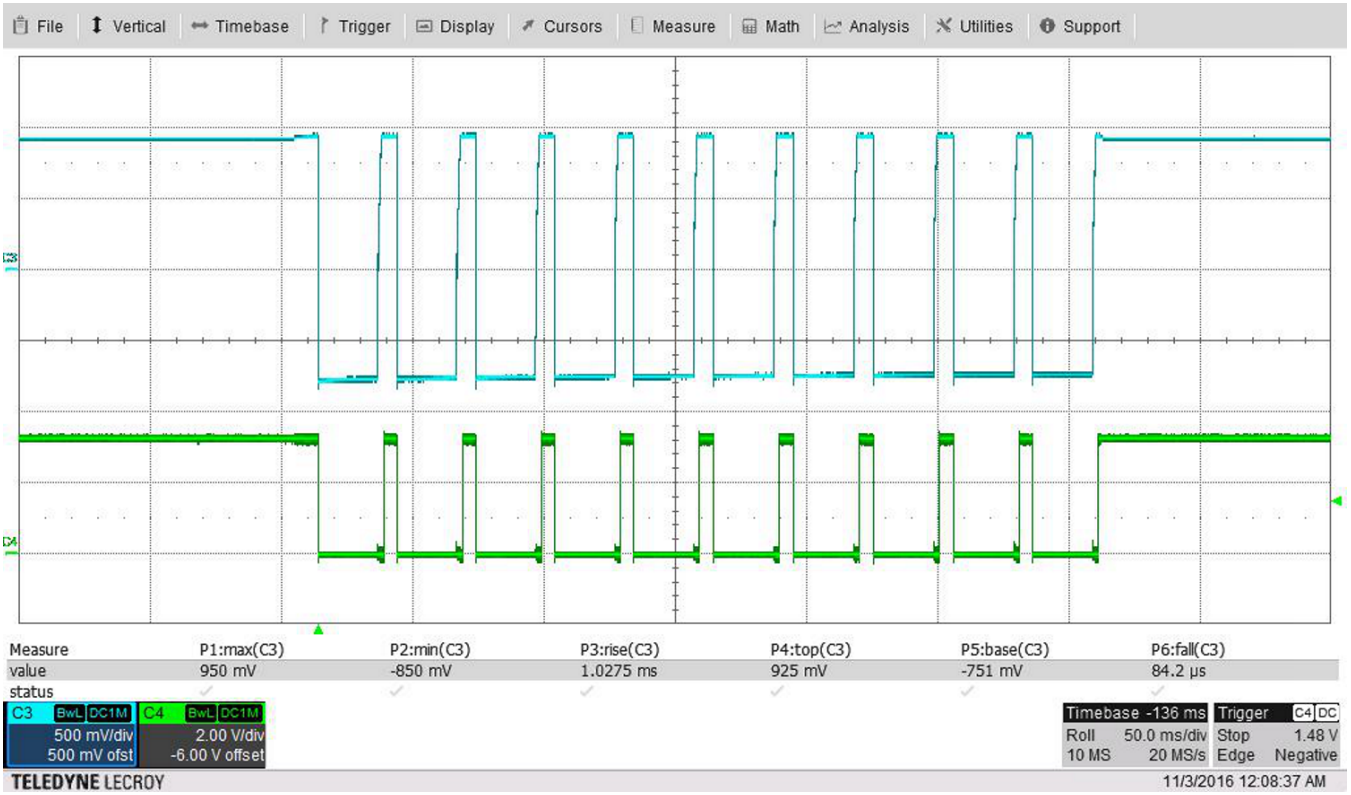


图 **19. Overcurrent Shutdown With Hiccup Mode**

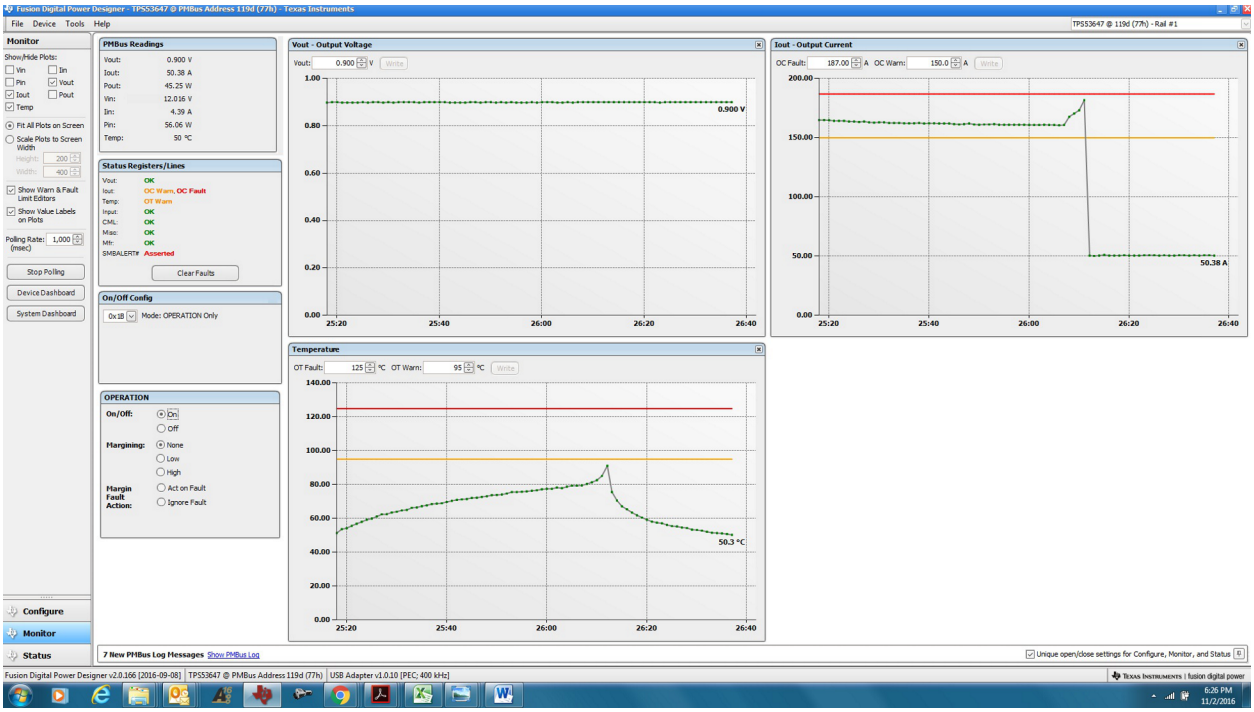


图 20. Single Overcurrent Shutdown as Seen in Fusion GUI

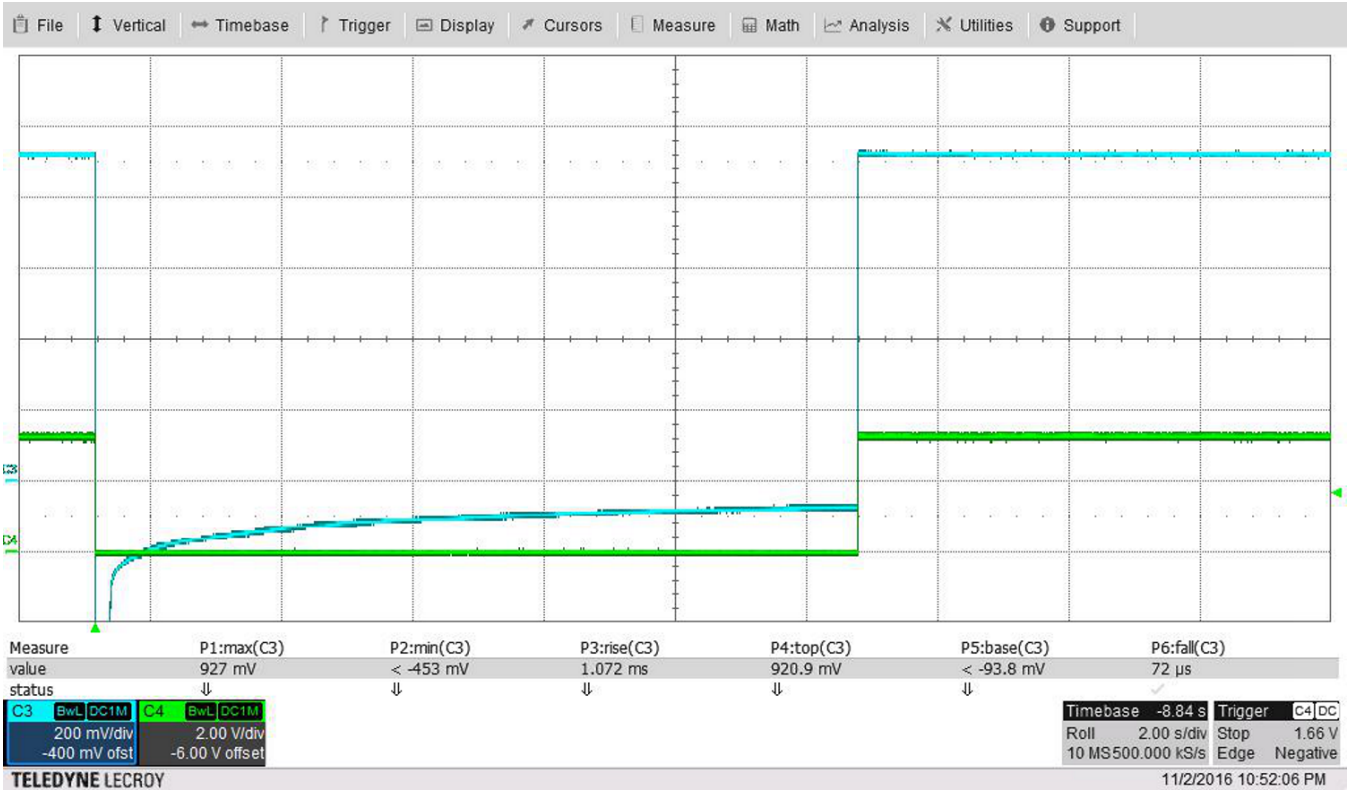


图 21. Overtemperature Shutdown With Recovery

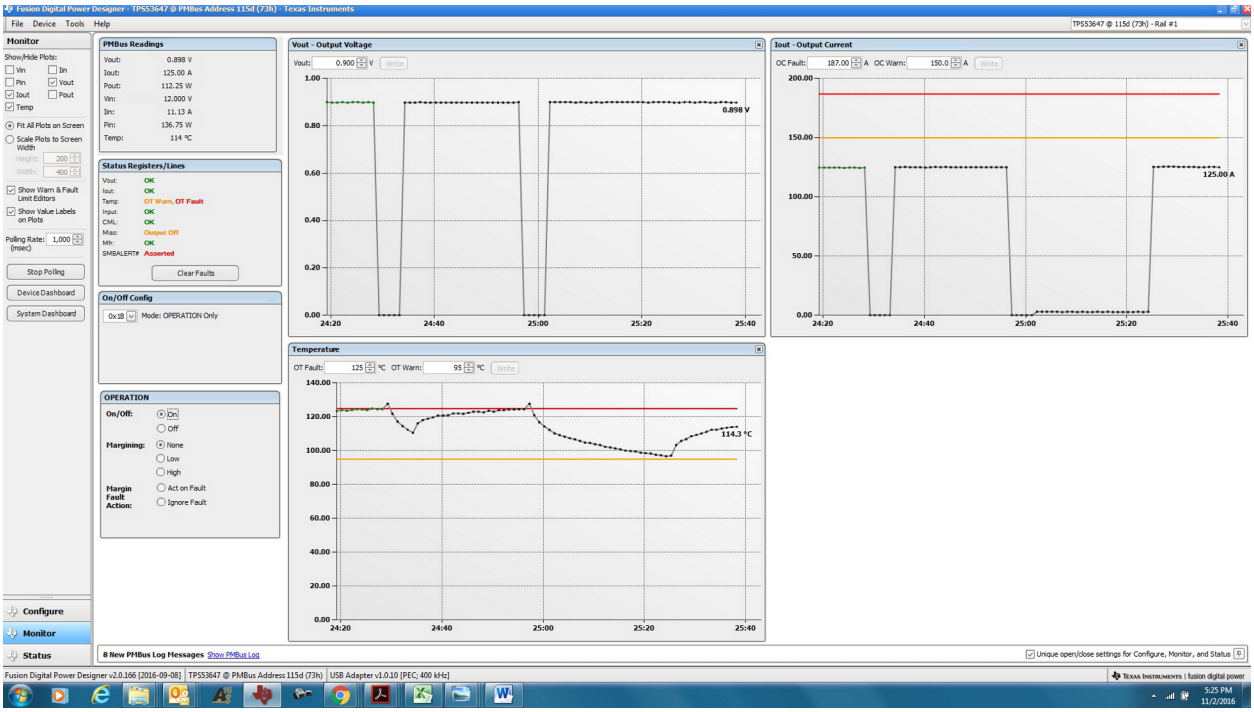


图 **22. Overtemperature Shutdown and Recovery as Seen in Fusion GUI**

5 VOUT_COMMAND Alignment Procedure Between FPGA and TPS53647

The TPS53647 supports Intel's VR12.0/12.5 VID (Voltage Identification) tables while Stratix 10 chips support the SmartVID 10-mV step VID table. With the FPGA default settings its VID codes don't match those of the TPS53647. For the testing in this report TI's software and USB-TO-GPIO cable were used so there was no conflict. In a real application however, the FPGA and TPS53647 must be configured properly in order to enable correct output voltage positioning between devices.

1. Ensure the TPS53647 is set up to use the Intel VR12.5 VID Table through either the correct pin-strap resistor or via NVM programming
   a. See Section 7.5 on page 31 of the controller datasheet for more information on programming the TPS53647
2. Using Intel's Quartus Prime Software, configure the FPGA to use the PMBus Direct Format
   a. Contact Intel support for the procedure if exact steps are needed
3. Set the proper Direct Coefficients (M, B, and R) to select the correct scaling and offset values such that the SmartVID block of the FPGA follows the VR12.5 VID Table
   a. M = 0x0064 (100d), B = 0xFFCF (-49d), R = 0x0000 (0d)
   b. Note VID Code 0 (0.00V) is not supported
   c. Refer to Table 1 on page 25 of the TPS53647 datasheet for the VR12.5 VID Table

6 Design Files

6.1 Schematics

To download the schematics, see the design files at PMP20176.

6.2 Bill of Materials

To download the bill of materials (BOM), see the design files at PMP20176.

6.3 PCB Layout Recommendations

Follow all the layout instructions as specified in the respective data sheet for each part when laying out a design using the TPS53647 controller and CSD95472 Smart Power Stage. Some other guidelines to consider include:

- Keep the layout for all four phases identical to ensure optimal current balancing and thermal performance between phases.
- Route noisy traces such as PWM and the PMBus lines on a separate layer than the sensitive analog sense lines such as VSP, VSN, COMP, IMON, and so forth.
- Use quality capacitors for both the input and output decoupling to obtain the maximum performance possible with respect to DC ripple and transient response. Capacitors must be voltage rated to at least 16 V on V_{IN} and 2.5 V on V_{OUT} with a dielectric rating of X5R or better.
- Ensure that the VOUT and GND nodes are routed on multiple layers of copper and connected with enough vias to handle the current requirements for the best thermal performance. Following this guideline allows for the maximum amount of heat to flow out of the power stages and inductors into the board.

6.3.1 Layout Prints

To download the layer plots, see the design files at PMP20176.

6.4 Gerber Files

To download the Gerber files, see the design files at PMP20176.

6.5 Assembly Drawings

To download the assembly drawings, see the design files at PMP20176.

7 Software Files

To download the Fusion Digital Power Designer software, see the following tool folder.

8 Related Documentation

1. Texas Instruments, *TPS53647 4-Phase, D-CAP+, Step-Down, Buck Controller with NVM and PMBus™ Interface for ASIC Power and High-Current Point-of-Load*, TPS53647 Data Sheet (SLUSC39)
2. Texas Instruments, *CSD95472Q5MC Synchronous Buck NexFET™ Smart Power Stage*, CSD95472Q5MC Data Sheet (SLPS599)
3. Intel, *Intel® Arria® 10 GX, GT, and SX Device Family Pin Connection Guidelines*, PCG-01017 (https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/dp/arria-10/pcg-01017.pdf)
4. Intel, *Power Reduction Features in Arria 10 Devices*, AN-711 (https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/an/an711.pdf)
5. Intel, *SmartVID Controller IP Core User Guide*, UG-SVID (https://www.altera.com/content/dam/alterawww/global/en_US/pdfs/literature/ug/ug_smartvid.pdf)
6. Intel, *25A Mini Slammer*, Product Page (https://designintools.intel.com/25A_Mini_Slammer_p/q6uj9a00ms25.htm)

8.1 商标

修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from A Revision (November 2017) to B Revision	Page
• 已添加 5 节	17

Changes from Original (August 2017) to A Revision	Page
• 更新了 Stratix® 10 FPGA 的型号，用 1SG280-1IV 代替 SG2800-I1V	1

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