

TI Designs: TIDA-01234

适用于汽车 LED 照明的 24W 升压和升压到电池参考设计



说明

此参考设计是一种 24W 高效 (94%) 低成本异步升压设计, 适用于基于 LM3481-Q1 的汽车 LED 应用。

资源

[TIDA-01234](#)

设计文件夹

[LM3481-Q1](#)

产品文件夹

[INA213-Q1](#)

产品文件夹



咨询我们的 E2E 专家

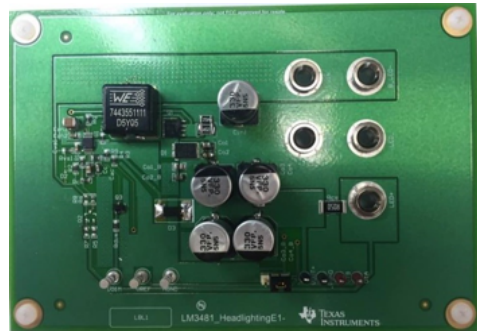
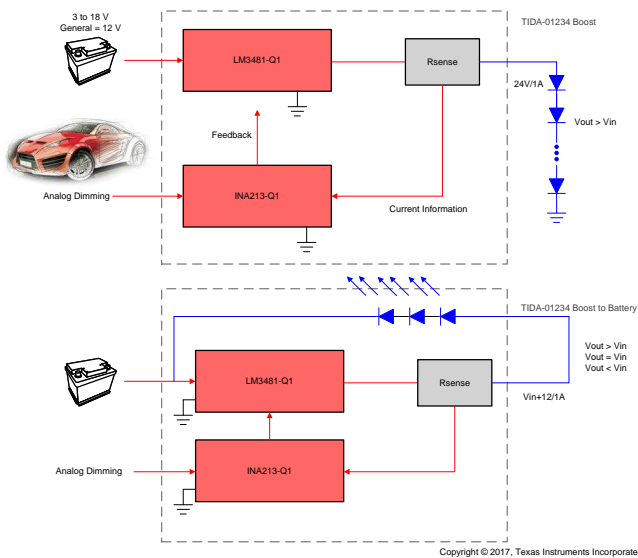
特性

- 24W 汽车 LED 驱动器解决方案
- 输入: 6V 至 18V, 输出: 24V@1A (升压) 和 $V_{IN} + 12V@1A$ (升压到电池)
- 对于升压, 12 V_{IN} 时的满载系统效率为 94%
- 对于升压到电池, 12 V_{IN} 时的满载系统效率为 88.9%
- 开关频率: 350kHz
- 0A 至 1A 全范围模拟调光
- 开路保护

应用

- 适用于汽车 LED 照明的 SMPS

TIDA-01234
24W Boost and Boost-to-Battery Reference Design for Automotive LED Lighting



该 TI 参考设计末尾的重要声明表述了授权使用、知识产权问题和其他重要的免责声明和信息。

1 System Description

This reference design is a 24-W, high-efficiency, low-cost, asynchronous boost design for automotive LED applications based on the LM3481-Q1. This design applies to automotive high brightness lighting such as headlights, tail lights, and interior LED lighting systems. The design also support analog LED brightness control and output open protection.

The design is divided into two major configurations:

1. Boost configuration:

- Wide input range from 6 to 18 V_{IN}
- Can drive multiple strings of six to seven LEDs at 1-A constant current
- High efficiency (94%), low cost

2. Boost-to-battery configuration:

- Wide input range from 6 to 18 V_{IN}
- Input voltage can either be higher, lower, or equal to required LED strings voltage
- High efficiency (89%), low cost

1.1 Key System Specifications

表 1. Key System Specifications

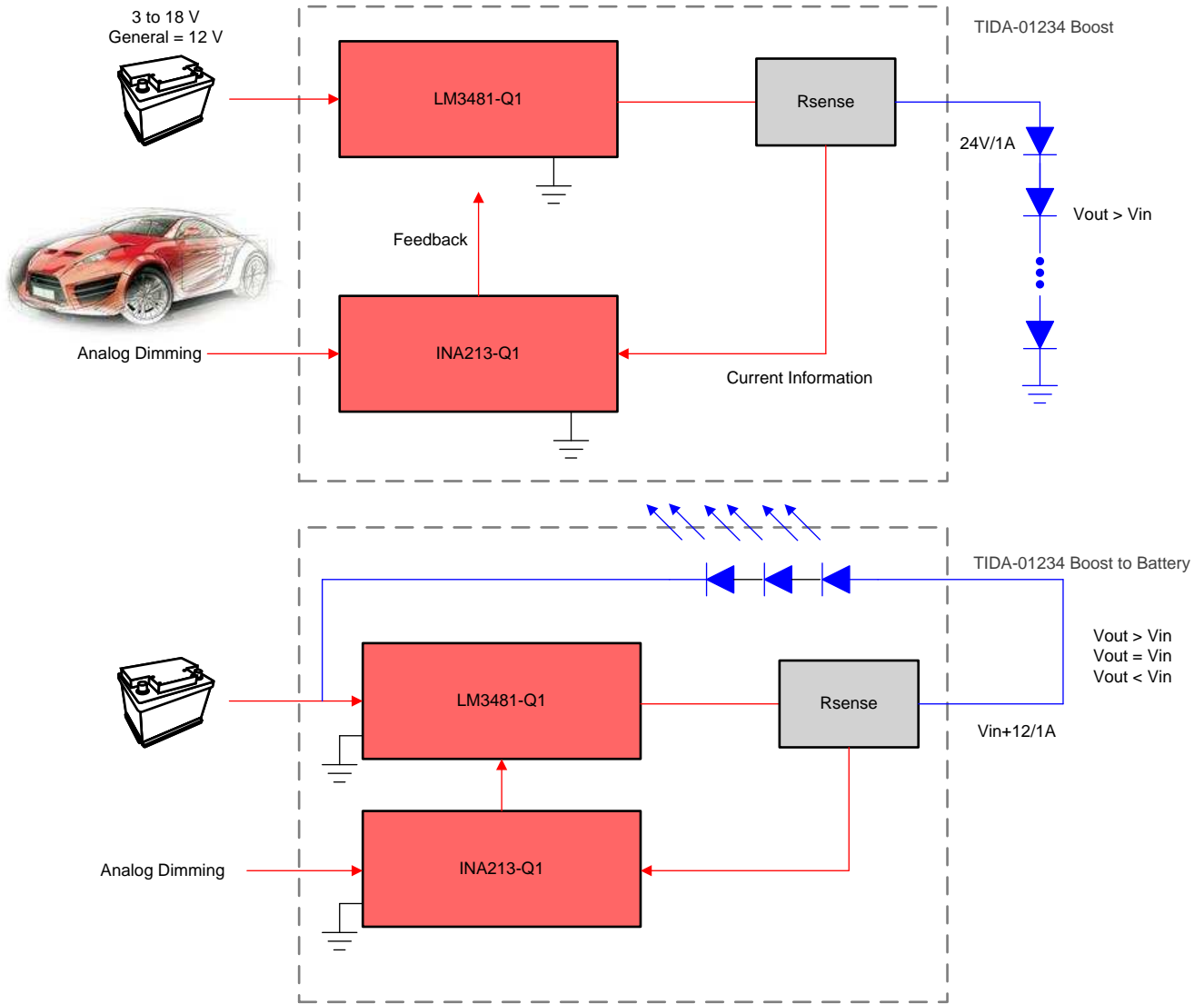
PARAMETER	SPECIFICATIONS
V_{IN} minimum	6-V DC
V_{IN} maximum	18-V DC
V_{OUT}	16 to 24 V (boost only), 8 to 12 V (boost-to-battery)
LED drive current (maximum)	1 A
Approximate switching frequency	350 kHz
LED dimming	0 to 1 A with no flickering

2 System Overview

2.1 Block Diagram

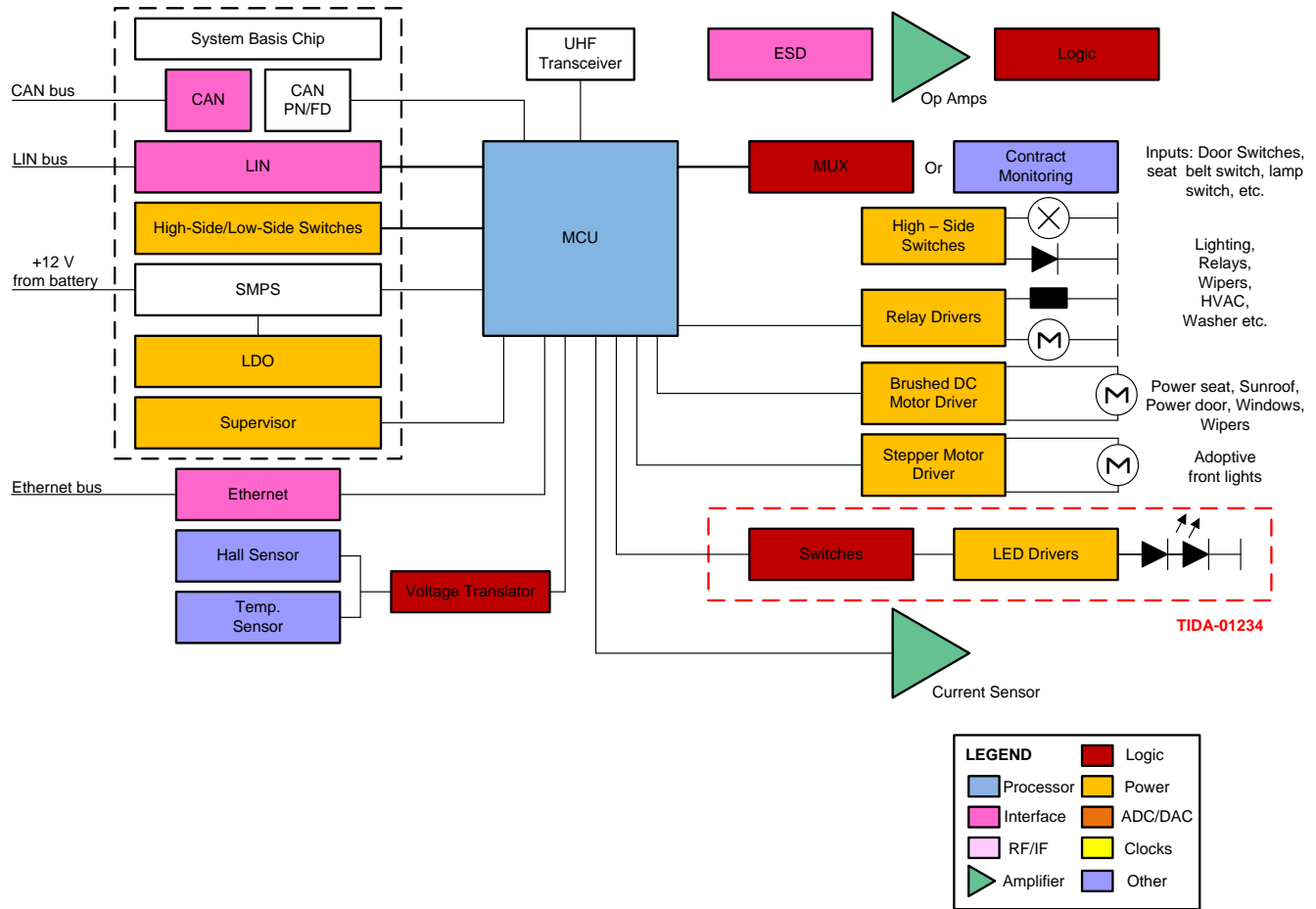
TIDA-01234

24W Boost and Boost-to-Battery Reference Design for Automotive LED Lighting



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图 1. TIDA-01234 Block Diagram



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图 2. Automotive LED Lighting Example Highlighting TIDA-01234

2.2 Highlighted Products

The following TI products are used in this reference design.

2.2.1 LM3481-Q1

- AEC-Q100 grade 1 qualified temperature: -40°C to 125°C operating junction temperature
- Wide supply voltage range: 2.97 to 48 V
- 100-kHz to 1-MHz adjustable and synchronizable clock frequency
- Pulse skipping at light loads
- Adjustable undervoltage lockout (UVLO) with hysteresis
- Internal soft-start

2.2.2 INA213-Q1

- AEC-Q100 grade 1 qualified temperature: -40°C to 125°C operating junction temperature
- Wide common-mode range: -0.3 to 26 V
- Offset voltage: $\pm 100\ \mu\text{V}$ (maximum; enables shunt drops of 10-mV full-scale)
- Accuracy:
 - $\pm 1\%$ gain error (maximum over temperature)
 - $0.5\text{-}\mu\text{V}/^{\circ}\text{C}$ offset drift (maximum)
 - $10\text{-ppm}/^{\circ}\text{C}$ gain drift (maximum)
- Quiescent current: 100 μA (maximum)
- SC70 package

2.3 System Design Theory

2.3.1 Boost Description

Generally, the output voltage can be programmed using a resistor divider and feedback pins. The output current depends on the load requirement. But for an LED application, constant current is necessary to keep a specific lightness. This design used current sensing to achieve constant current by the boost controller LM3481-Q1.

To keep constant current flowing through LED, there is a current sense resistor, R_{SHUNT} , at the output of the controller to sense how much current flows through it. This reference design uses a 50-m Ω current sense resistor to generate 50 mV of crossing voltage. This crossing voltage will be amplified by the INA213-Q1, which provides a gain = 50 V/V. Using an external voltage injected into the current sense amplifier reference at J1 allows for analog dimming of the LEDs at the output by changing the output current, as shown in 公式 1:

$$V_{FB} = \left[(I_{OUT} \times R_{SHUNT}) + V_{REF} \right] \times \frac{R3}{R3 + R4} \tag{1}$$

where:

- V_{FB} is 1.275 V
- R_{SHUNT} is 50 m Ω
- R3 equal to R4 are 10 k Ω

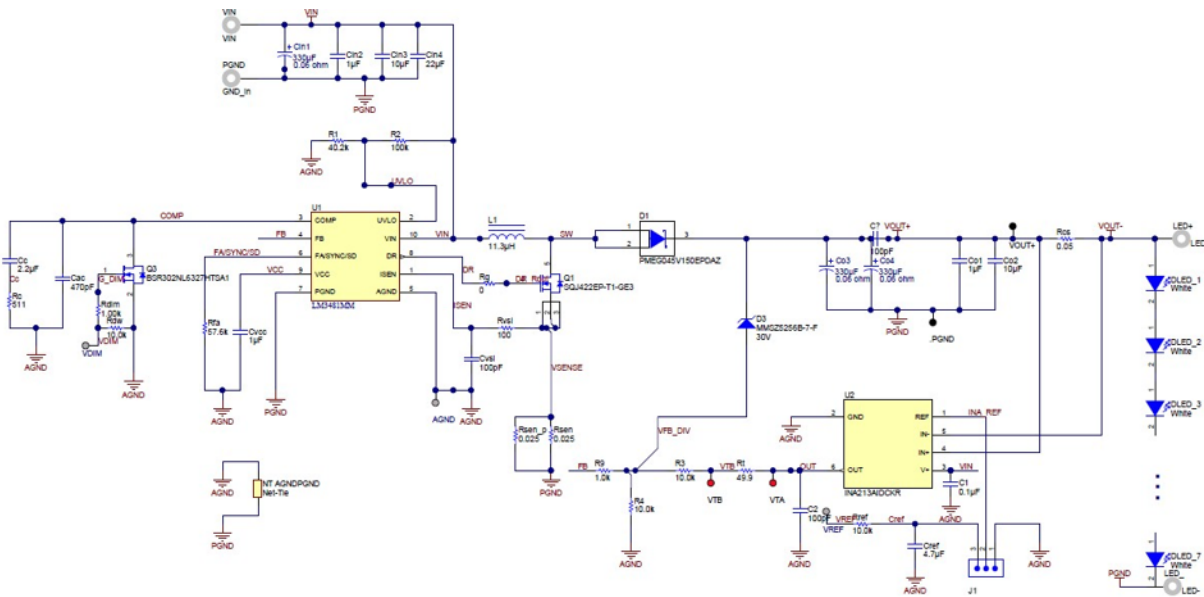


图 3. Boost Configuration and LM3481 Schematic

If the output LED burns out or is open at the output circuit, the output voltage will continuously rise. The TIDA-01234 design provides output open circuit protection. For the boost configuration, a Zener diode connected between V_{OUT} and V_{FB_DIV} , clamping the output voltage at the Zener voltage V_z plus the output voltage of the current sense amplifier.

2.3.2 Boost-to-Battery Description

In order to generate constant current with an output voltage closed to the input voltage, the designer must use a buck-boost or a SEPIC structure, which is complex and costly. By connecting the cathode of LED strings to the input instead of the GND, the TIDA-01234 can also be modified to boost-to-battery configuration. In this configuration, input voltage can either be higher, lower, or equal to the required LED strings voltage.

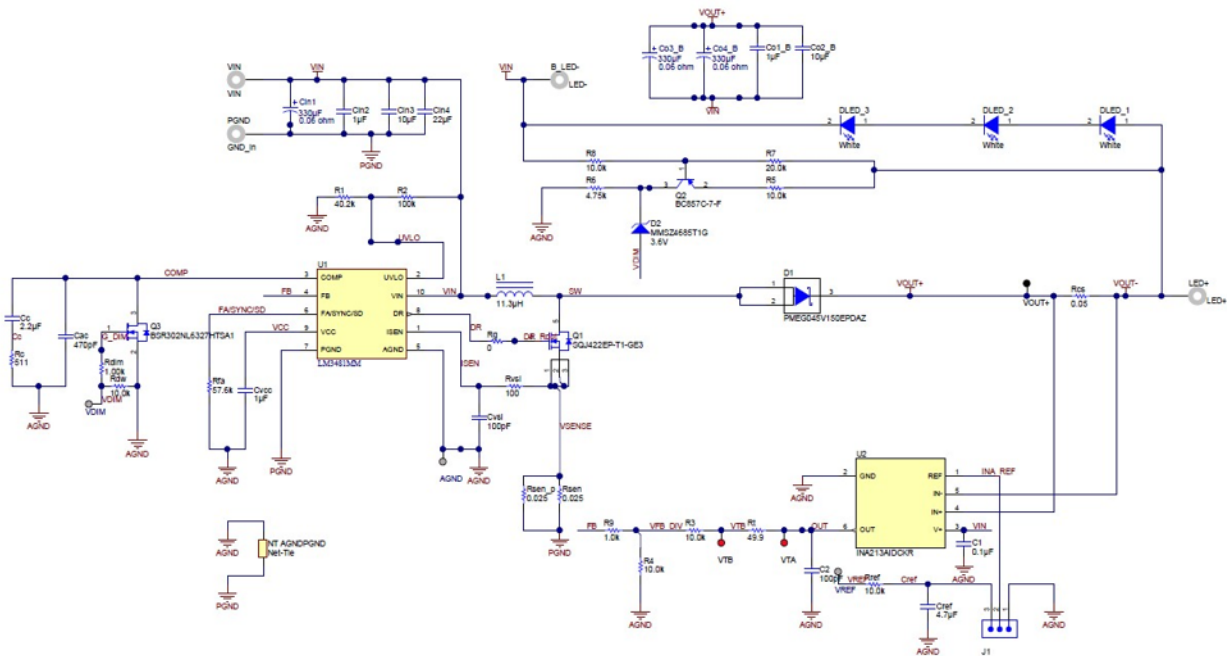


图 4. Boost-to-Battery Configuration and LM3481 Schematic

For boost-to-battery, the TIDA-01234 provides another solution for open circuit protection by using transistor Q2 combined with R5, R6, R7, R8, and D2 to detect differential voltage between output voltage and input voltage. When the differential voltage rises up to V_{OV} , where V_{OV} is overvoltage at the output, Zener diode D2 will turn on and pull the comp pin voltage down by Q3. As a result, the output voltage will stay low until the load is connected.

For design calculations and layout examples, see the devices' respective datasheets:

- LM3481-Q1 High-Efficiency Controller for Boost, SEPIC and Flyback DC-DC Converters (SNVS346)
- INA21x-Q1 Automotive-Grade, Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors (SBOS475)

3 Testing and Results

3.1 Boost Configuration Test Results

3.1.1 Thermal Data

The infrared thermal image shown in 图 5 was taken at a steady state with 12 V_{IN} and full load of a 1-A load current (current sense comparator reference set to 0 V) for boost configuration.

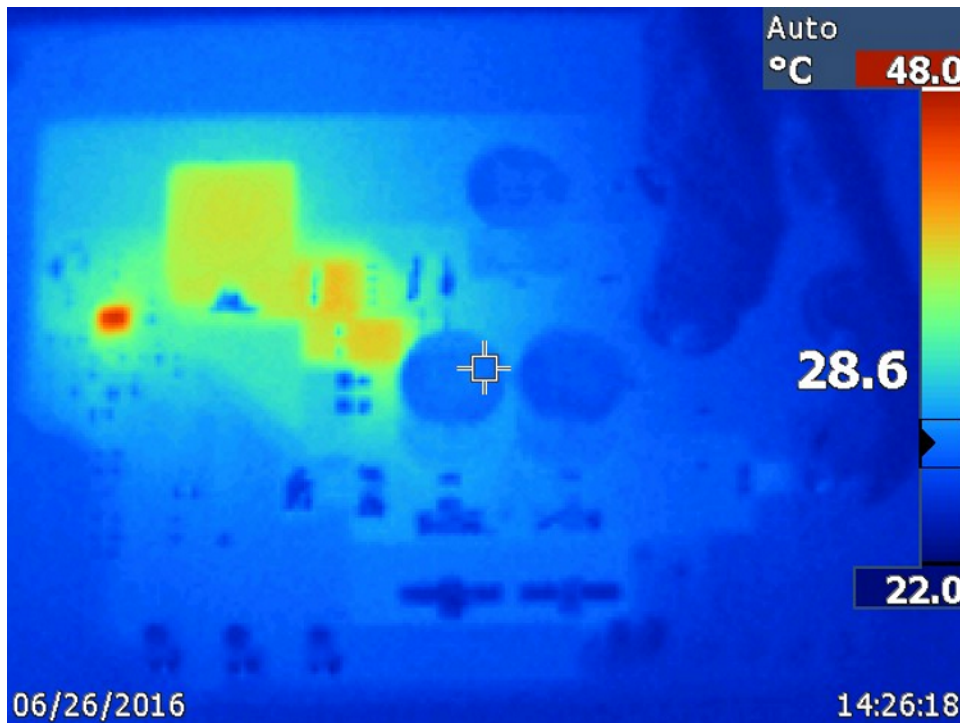


图 5. Thermal Image of Boost Configuration

3.1.2 Efficiency Data

3.1.2.1 Efficiency Chart

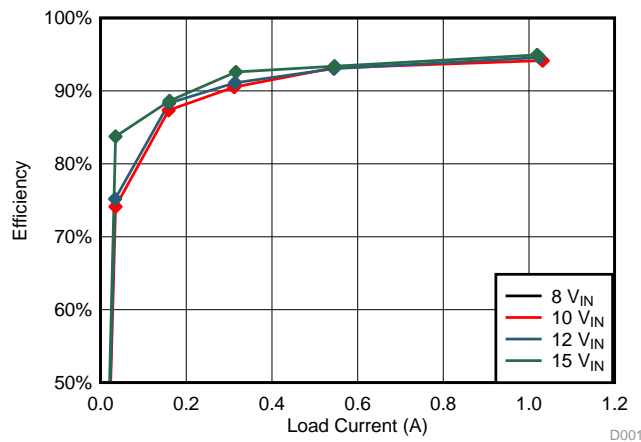


图 6. Boost Efficiency versus Load Current at Various Input Voltages

3.1.2.2 Efficiency Data

表 2. Boost Efficiency Table at 6 V_{IN}

REF (V)	V _{IN} (V)	I _{IN} (A)	V _{OUT} (V)	I _{OUT} (A)	EFF (%)
0	6.004	4.278	23.67	1.009	92.98394
1.0	6.006	2.082	22.20	0.524	93.02897
1.8	6.002	0.835	20.67	0.218	89.91135
2.2	6.000	0.291	19.56	0.075	84.02062
2.5	6.000	0.002	11.63	0	0

表 3. Boost Efficiency Table at 10 V_{IN}

REF (V)	V _{IN} (V)	I _{IN} (A)	V _{OUT} (V)	I _{OUT} (A)	EFF (%)
0	10.005	2.564	24.11	1.010	94.92563
1.0	10.006	1.251	22.17	0.525	92.98378
1.8	10.005	0.500	20.71	0.219	90.66447
2.2	10.008	0.181	19.59	0.076	82.19060
2.5	10.000	0.002	12.53	0	0

表 4. Boost Efficiency Table at 12 V_{IN}

REF (V)	V _{IN} (V)	I _{IN} (A)	V _{OUT} (V)	I _{OUT} (A)	EFF (%)
0	12.006	2.140	24.02	1.010	94.42397
1.0	12.009	1.043	22.18	0.526	93.14427
1.8	12.002	0.423	20.74	0.219	89.46618
2.2	12.000	0.153	19.62	0.076	81.21569
2.5	12.000	0.002	11.96	0	0

表 5. Boost Efficiency Table at 15 V_{IN}

REF (V)	V _{IN} (V)	I _{IN} (A)	V _{OUT} (V)	I _{OUT} (A)	EFF (%)
0	15.01	1.687	23.77	1.010	94.81014
1.0	15.005	0.833	22.19	0.526	93.38176
1.8	15.000	0.339	20.76	0.220	89.81711
2.2	15.004	0.114	19.64	0.076	87.26562
2.5	15.000	0.002	14.96	0	0

3.1.3 Boost Configuration Waveforms

3.1.3.1 Switching and Output Current

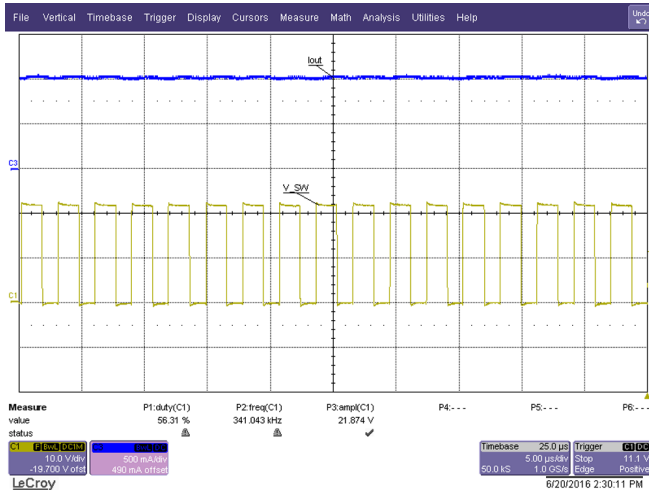


图 7. 12-V_{IN} 和 0-V 参考 on 电流检测比较器提供最大输出电流

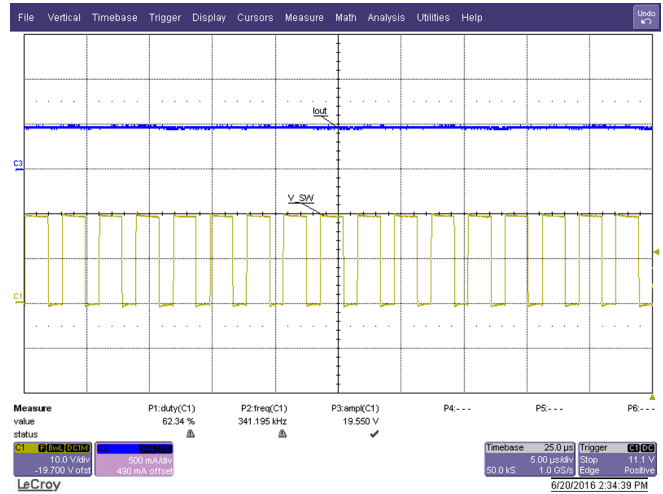


图 8. 12 V_{IN} 和 1.2-V 参考 on 电流检测比较器提供最大输出电流

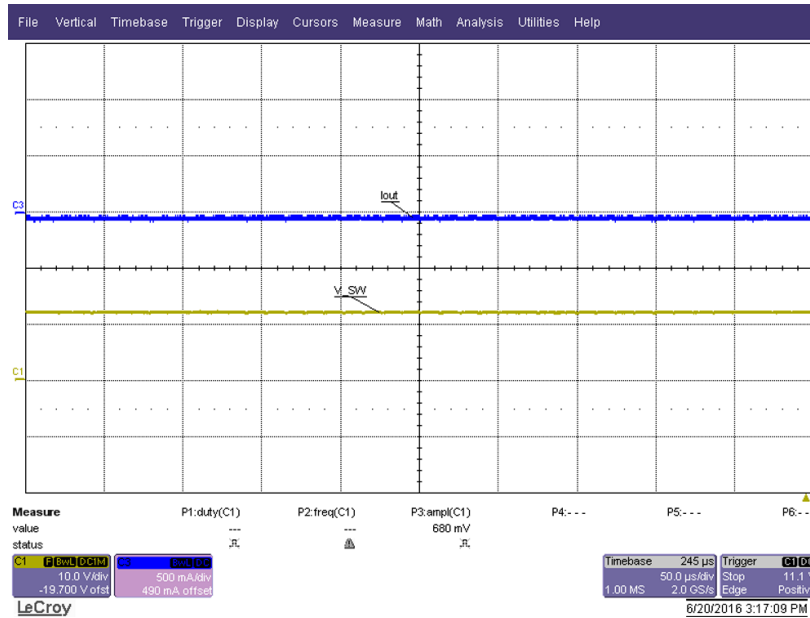


图 9. 12 V_{IN} 和 2.5-V 参考 on 电流检测比较器提供最大输出电流

注: Ch1 (yellow trace): Switch node voltage, Ch2 (pink trace): Output current

3.1.3.2 System Startup Waveforms

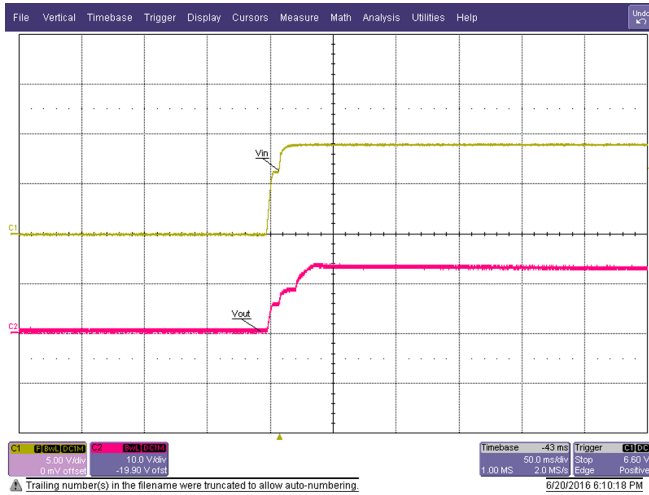


图 10. Startup Into No Load (Current Sense Comparator Reference Voltage Set to 2.5 V) at 9 V_{IN}

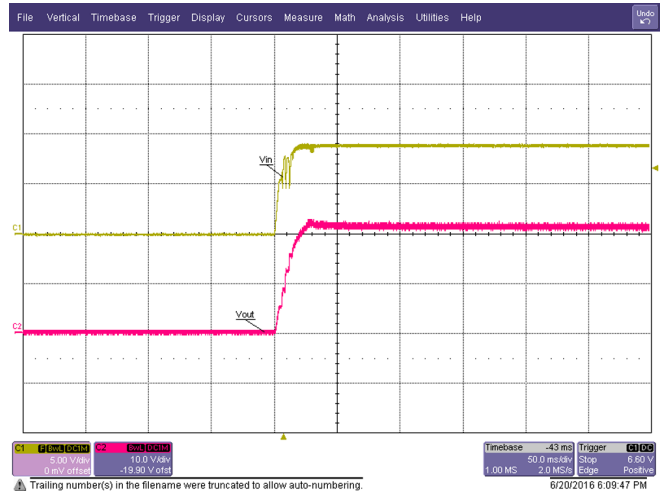


图 11. Startup Into No Load (Current Sense Comparator Reference Voltage Set to 0 V) at 9 V_{IN}

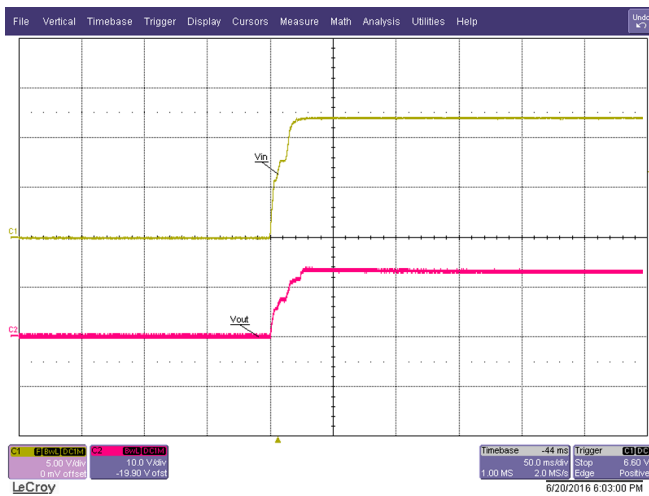


图 12. Startup Into No Load (Current Sense Comparator Reference Voltage Set to 2.5 V) at 12 V_{IN}

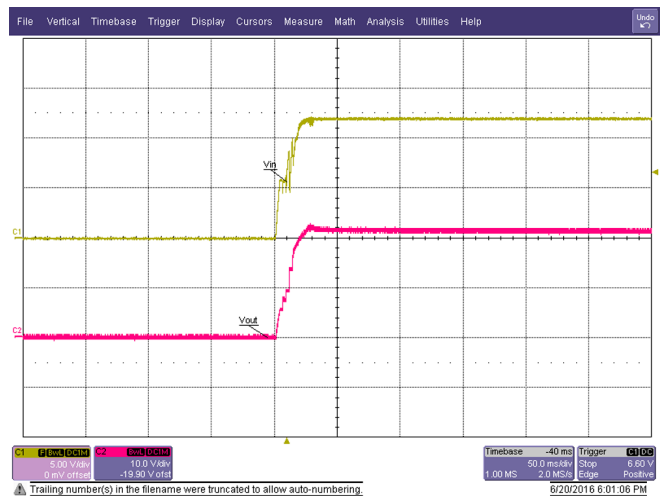


图 13. Startup Into No Load (Current Sense Comparator Reference Voltage Set to 0 V) at 12 V_{IN}

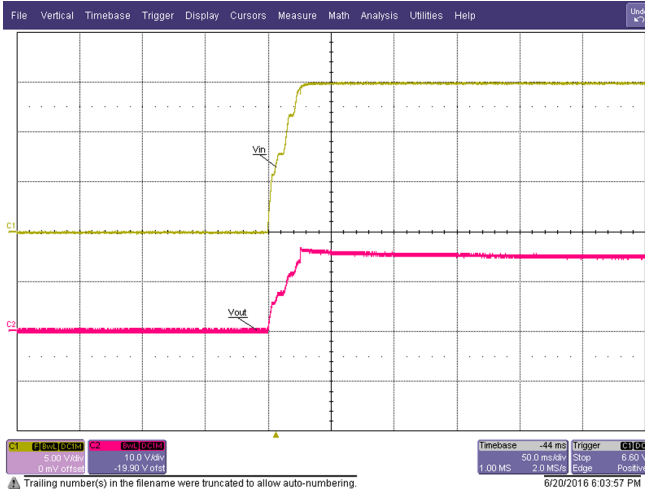


图 14. Startup Into No Load (Current Sense Comparator Reference Voltage Set to 2.5 V) at 15 V_{IN}

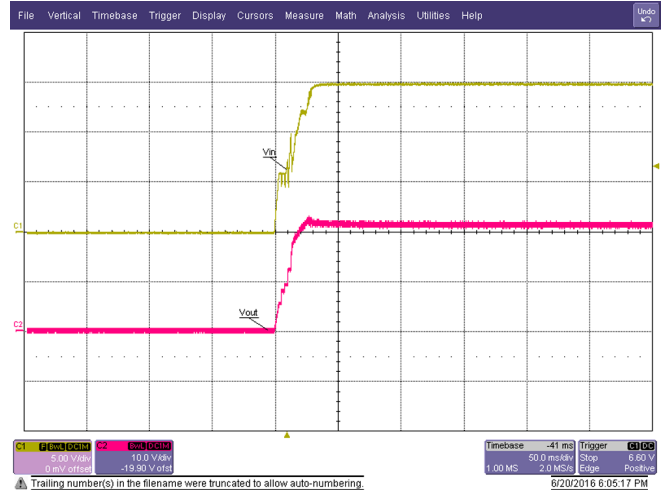


图 15. Startup Into No Load (Current Sense Comparator Reference Voltage Set to 0 V) at 15 V_{IN}

注: Ch1 (yellow trace): V_{IN}, Ch2 (pink trace): V_{OUT}

3.1.4 Analog Dimming

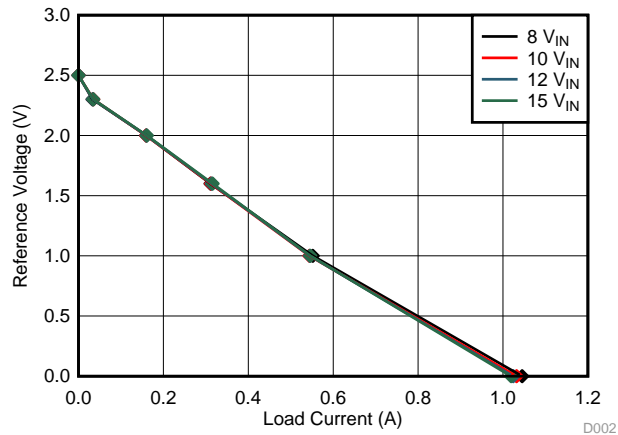


图 16. Reference Voltage for Current Sense Comparator versus Load Current

注: 图 16 shows the current regulation for the boost configuration.

3.1.5 Loop Response

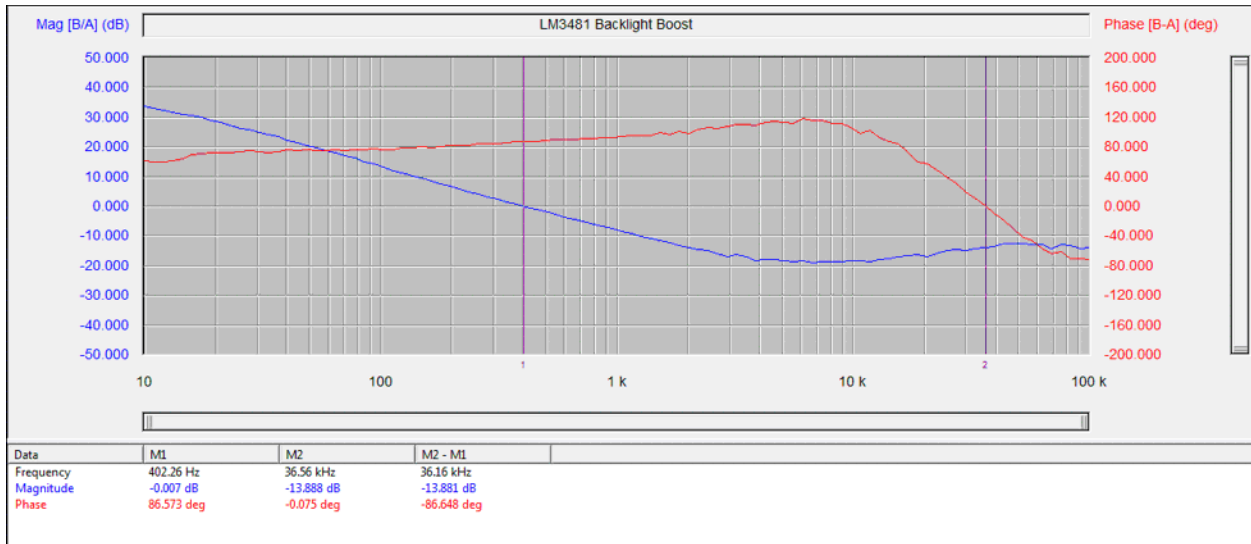


图 17. 6- V_{IN} Loop Response Showing a Stable System With Gain Margin: 13.8 dB and Phase Margin: 86.5°

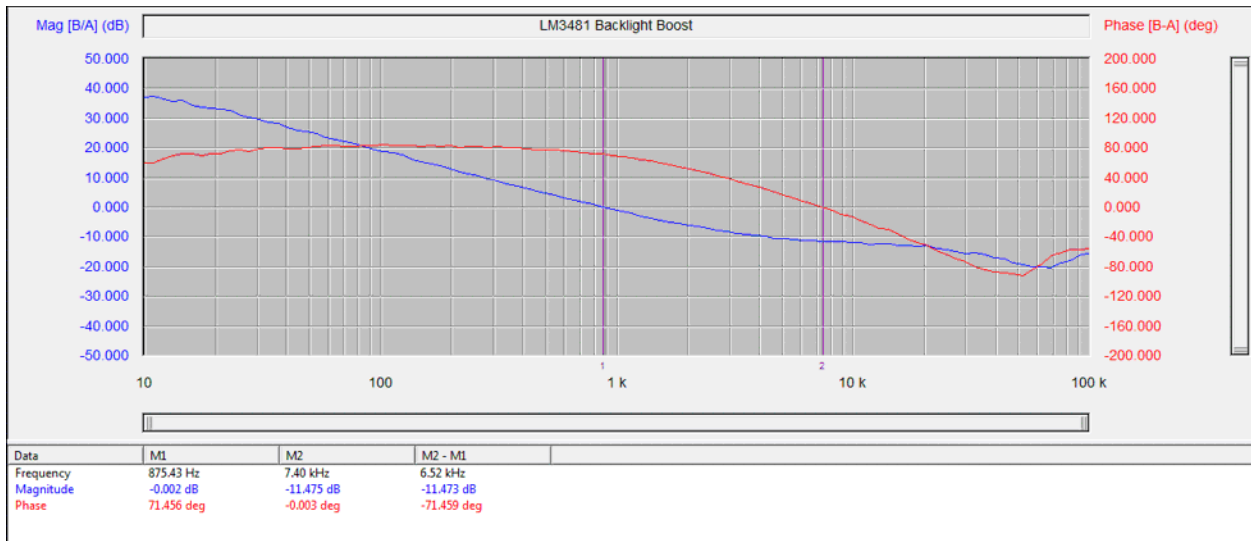


图 18. 12- V_{IN} Loop Response Showing a Stable System With Gain Margin: 11.4 dB and Phase Margin: 71.4°

3.2 Boost-to-Battery Configuration Test Results

3.2.1 Thermal Data

The infrared thermal image shown in 图 19 was taken at steady state with 12 V_{IN} and full load of a 1-A load current (current sense comparator reference set to 0 V) for boost-to-battery configuration.

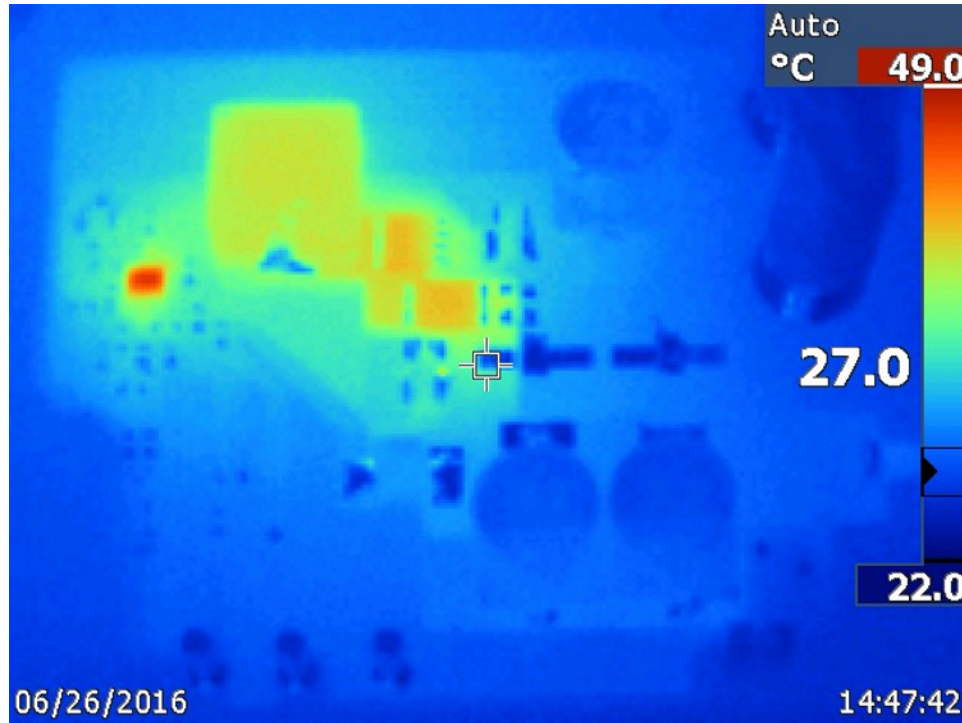


图 19. Thermal Image of Boost-to-Battery

3.2.2 Efficiency Data

3.2.2.1 Efficiency Chart

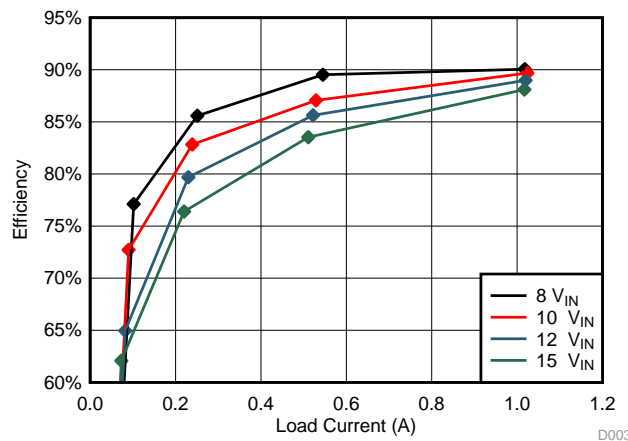


图 20. Boost-to-Battery Efficiency versus Load Current at Various Input Voltages

3.2.2.2 Efficiency Data

表 6. Boost-to Battery Efficiency Table at 6 V_{IN}

REF (V)	V _{IN} (V)	I _{IN} (A)	V _{OUT} (V)	I _{OUT} (A)	EFF (%)
0	6.000	1.918	10.18	1.018	90.05249
1.0	6.000	0.970	9.56	0.545	89.52234
1.8	6.006	0.438	8.97	0.251	85.58679
2.2	6.002	0.188	8.53	0.102	77.10728
2.5	6.000	0.002	0	0	0

表 7. Boost-to Battery Efficiency Table at 10 V_{IN}

REF (V)	V _{IN} (V)	I _{IN} (A)	V _{OUT} (V)	I _{OUT} (A)	EFF (%)
0	10.002	1.161	10.17	1.024	89.68129
1.0	10.004	0.577	9.50	0.529	87.06223
1.8	10.009	0.258	8.95	0.239	82.83436
2.2	10.008	0.105	8.49	0.090	72.71326
2.5	10.000	0.002	0	0	0

表 8. Boost-to Battery Efficiency Table at 12 V_{IN}

REF (V)	V _{IN} (V)	I _{IN} (A)	V _{OUT} (V)	I _{OUT} (A)	EFF (%)
0	12.006	0.970	10.16	1.020	88.98643
1.0	12.002	0.482	9.49	0.522	85.63199
1.8	12.002	0.215	8.94	0.230	79.68439
2.2	12.000	0.089	8.46	0.082	64.95506
2.5	12.000	0.002	0	0	0

表 9. Boost-to Battery Efficiency Table at 15 V_{IN}

REF (V)	V _{IN} (V)	I _{IN} (A)	V _{OUT} (V)	I _{OUT} (A)	EFF (%)
0	15.002	0.781	10.15	1.017	88.10221
1.0	15.001	0.387	9.49	0.511	83.53259
1.8	15.006	0.171	8.91	0.220	76.39050
2.2	15.003	0.066	8.42	0.073	62.07445
2.5	15.000	0.002	0	0	0

3.2.3 Boost-to-Battery Configuration Waveforms

3.2.3.1 Switching and Output Current

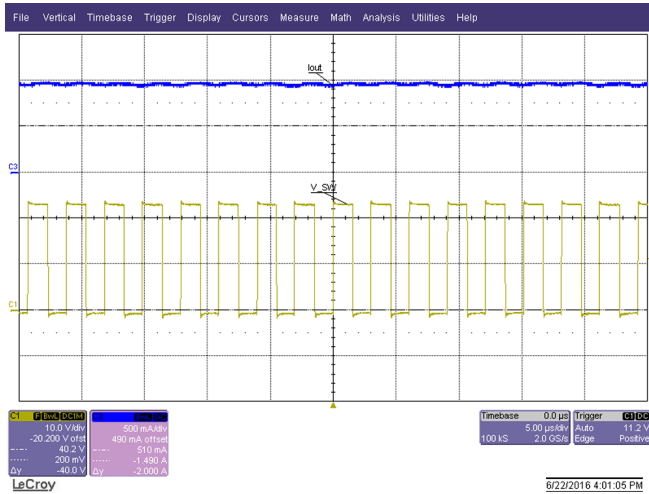


图 21. 12-V_{IN} 和 0-V 参考 on 电流检测比较器提供最大输出电流

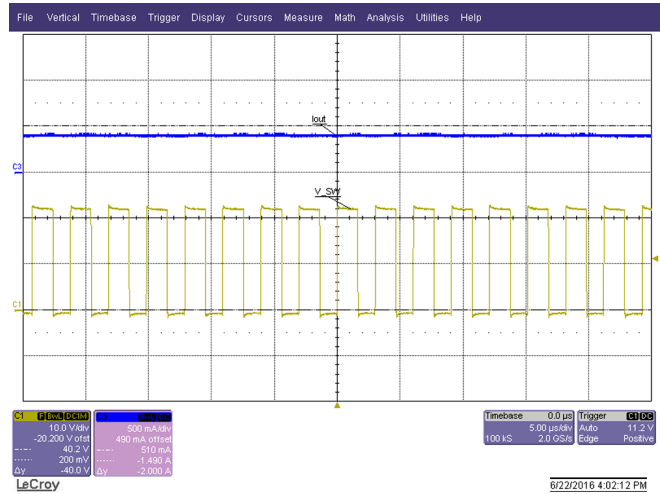


图 22. 12-V_{IN} 和 0-V 参考 on 电流检测比较器提供最大输出电流

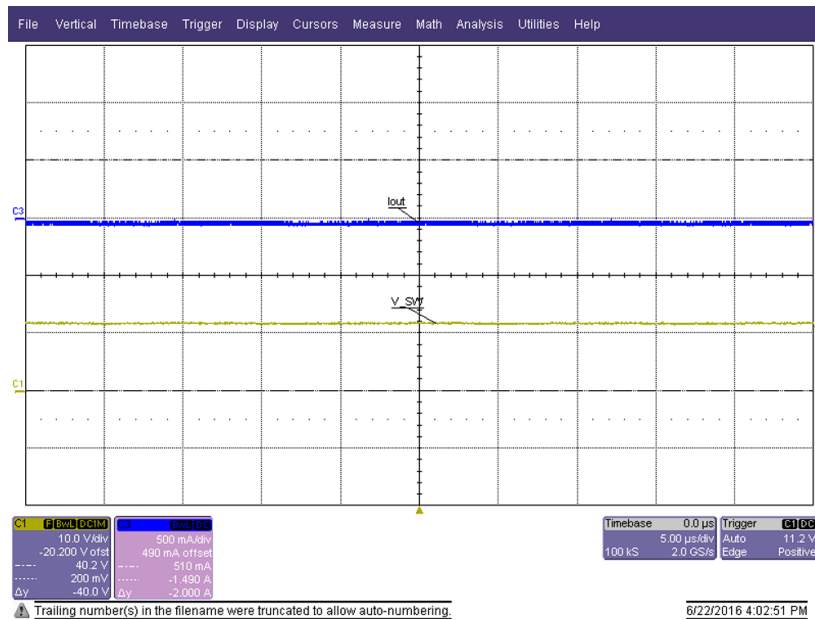


图 23. 12-V_{IN} 和 2.5-V 参考 on 电流检测比较器提供最大输出电流

注: Ch1 (yellow trace): Switch node voltage, Ch2 (pink trace): Output current

3.2.3.2 System Startup Waveforms

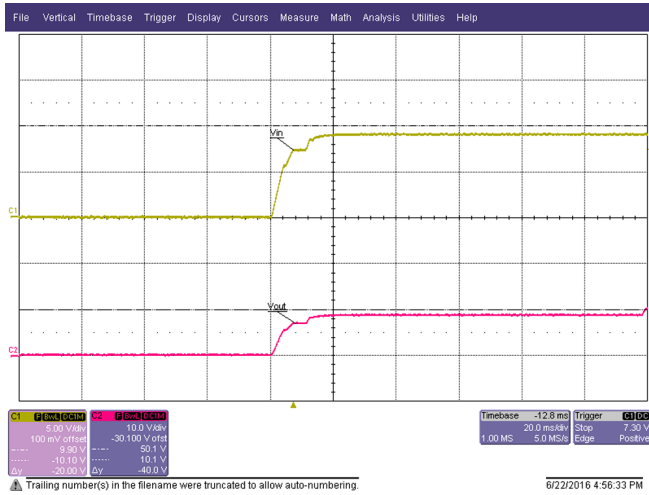


图 24. Startup Into No Load (Current Sense Comparator Reference Voltage Set to 2.5 V) at 9 V_{IN}

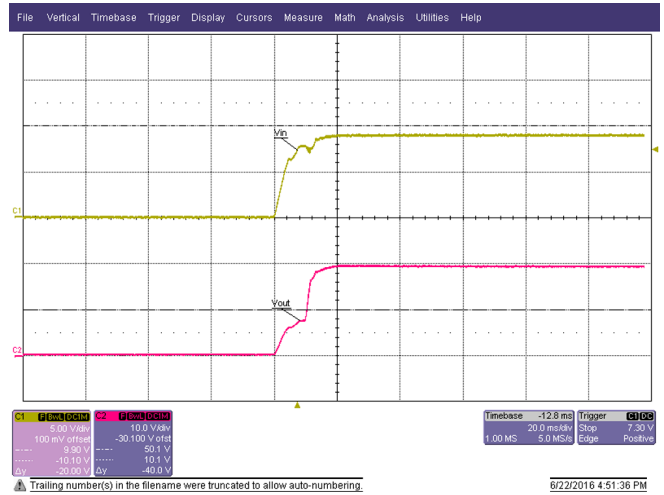


图 25. Startup Into No Load (Current Sense Comparator Reference Voltage Set to 0 V) at 9 V_{IN}

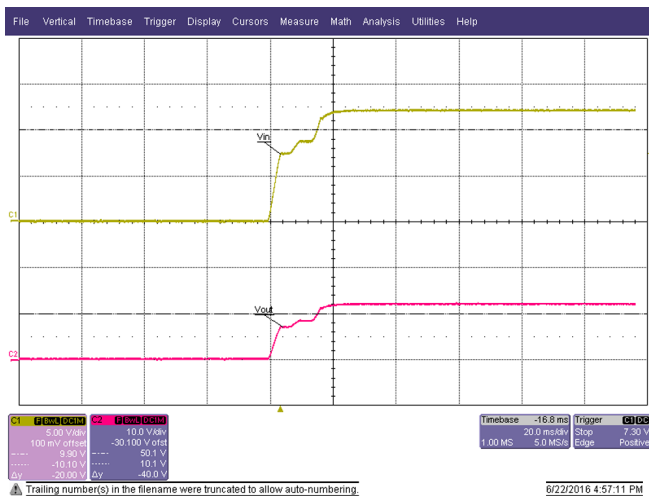


图 26. Startup Into No Load (Current Sense Comparator Reference Voltage Set to 2.5 V) at 12 V_{IN}

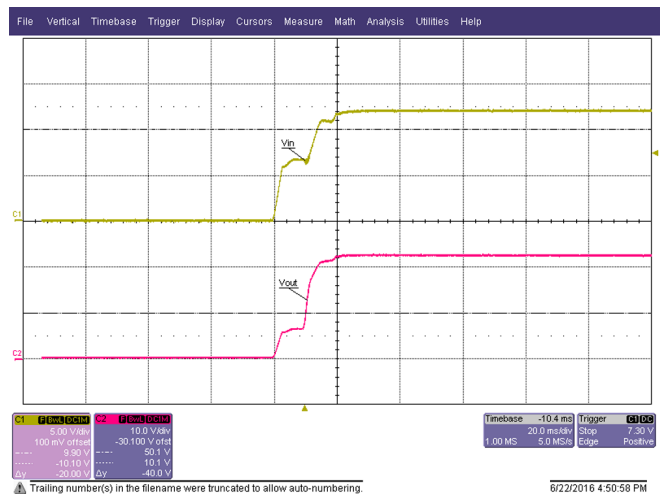


图 27. Startup Into No Load (Current Sense Comparator Reference Voltage Set to 0 V) at 12 V_{IN}

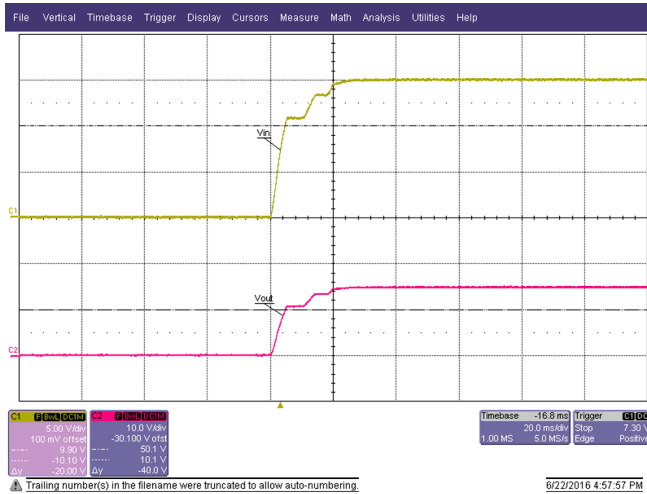


图 28. Startup Into No Load (Current Sense Comparator Reference Voltage Set to 2.5 V) at 15 V_{IN}

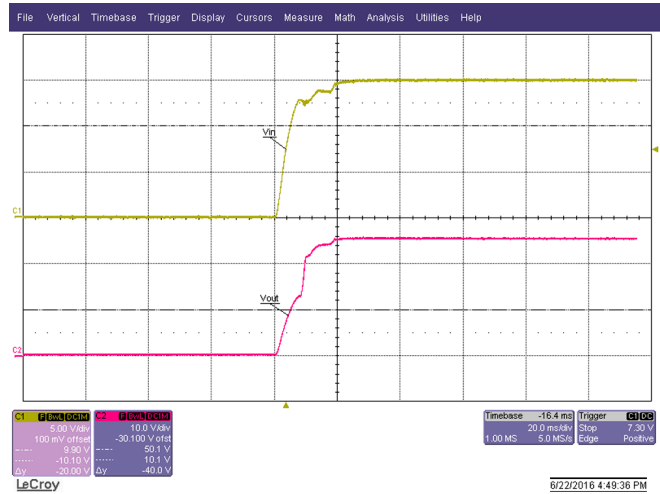


图 29. Startup Into No Load (Current Sense Comparator Reference Voltage Set to 0 V) at 15 V_{IN}

注: Ch1 (yellow trace): V_{IN}, Ch2 (pink trace): V_{OUT}

3.2.4 Analog Dimming

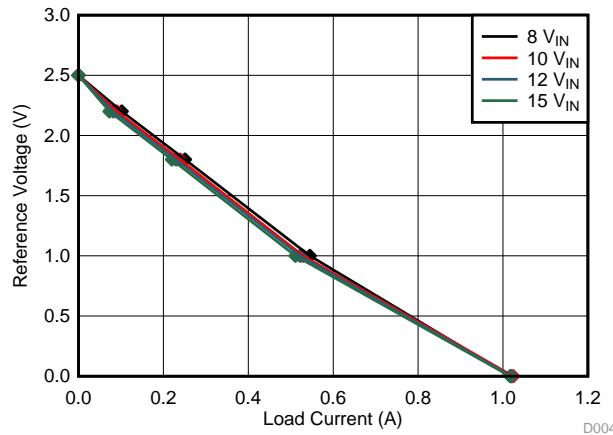


图 30. Reference Voltage for Current Sense Comparator versus Load Current

注: 图 30 shows the current regulation for the boost configuration.

3.2.5 Open Circuit Protection

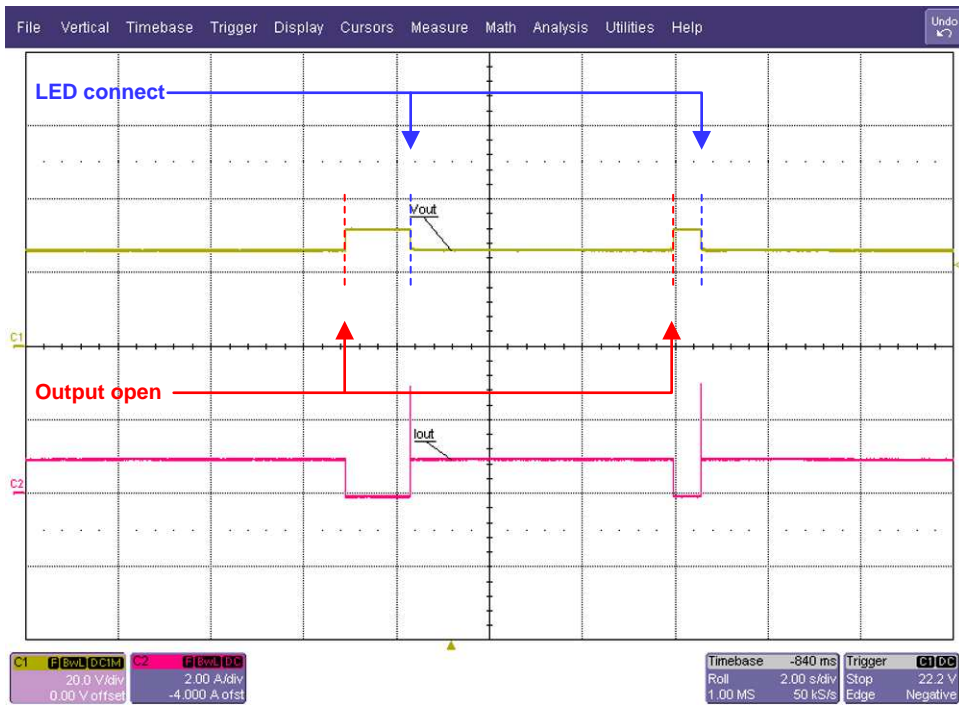


图 31. Boost-to-Battery Open Circuit Protection

3.2.6 Loop Response

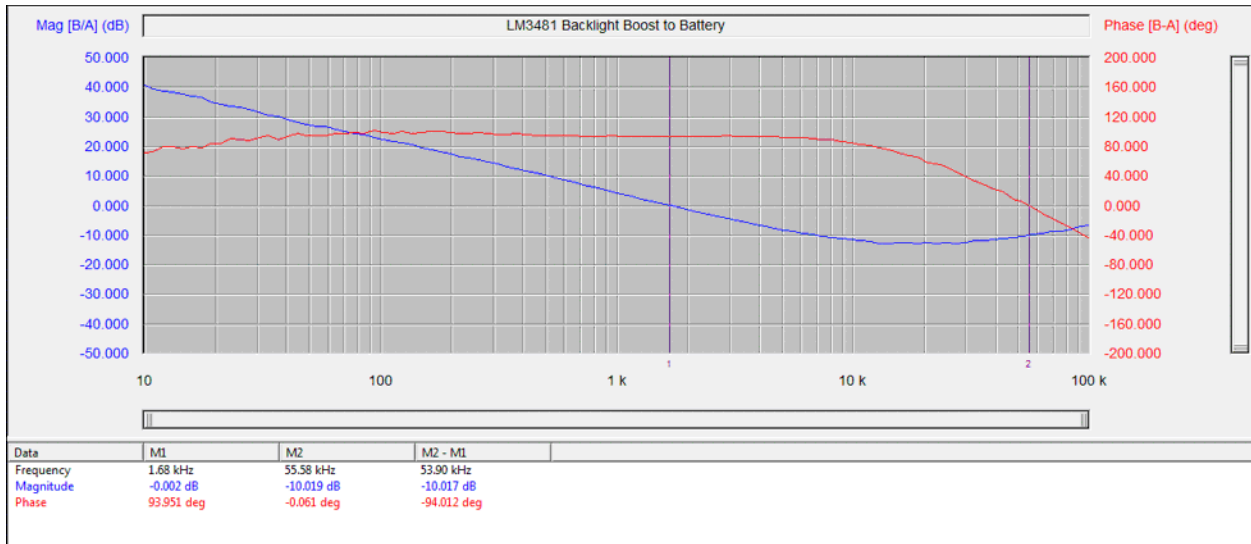


图 32. 6-V_{IN} Loop Response Showing a Stable System With Gain Margin: 10.0 dB and Phase Margin: 93.95°

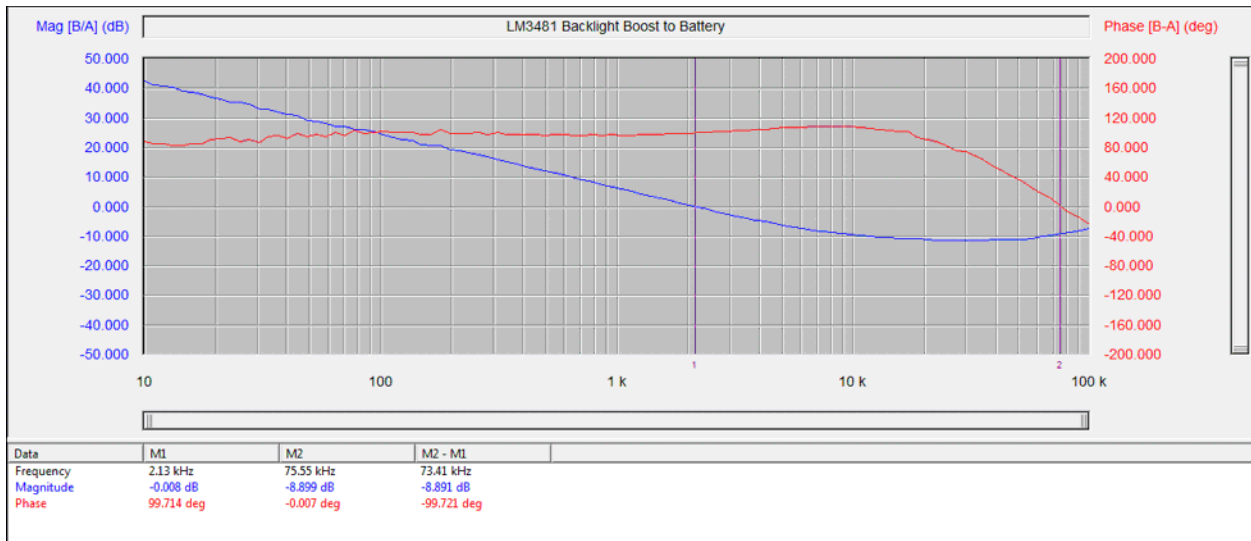


图 33. 12-V_{IN} Loop Response Showing a Stable System With Gain Margin: 8.9 dB and Phase Margin: 99.7°

4 Design Files

4.1 Schematics

To download the schematics, see the design files at [TIDA-01234](#).

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-01234](#).

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at [TIDA-01234](#).

4.4 Altium Project

To download the Altium project files, see the design files at [TIDA-01234](#).

4.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-01234](#).

4.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-01234](#).

5 Software Files

To download the software files, see the design files at [TIDA-01234](#).

6 Related Documentation

This reference design did not use any related documentation.

6.1 商标

All trademarks are the property of their respective owners.

7 About the Author

SHAQUILLE CHEN is a field application engineer at Texas Instruments where he is responsible for major account in Taiwan. Shaquille earned his master of technology (M.Tech) from the National Taiwan University of Science and Technology in Taipei.

修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (August 2016) to A Revision	Page
• 已更改 在预览草案的基础上进行更改以适应当前设计指南模板	1

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