TI Designs：TIDA-01416
适用于 NXP™ i.MX7 系列应用处理器的小巧高效且灵活易用型电源参考设计

说明

该小巧高效且灵活易用型电源参考设计展示了一款适用于 NXP™i.MX7 处理器的完整电源解决方案。这个简单的解决方案仅使用五个直流/直流转换器和一个序列发生器集成电路 (IC) 为 i.MX7 供电，是一款具有高成本效益的设计。该参考设计支持多种工业 应用 以及需要小型、高效、灵活电源解决方案的任何应用。

资源

TIDA-01416	设计文件夹
TLV62080、TLV62084A	产品文件夹
TLV62085	产品文件夹
LM3880	产品文件夹

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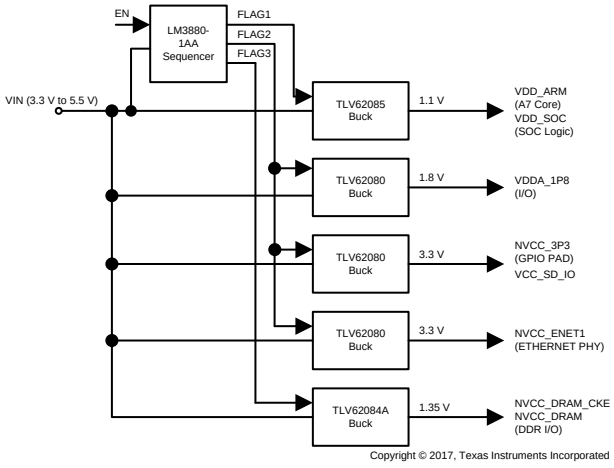
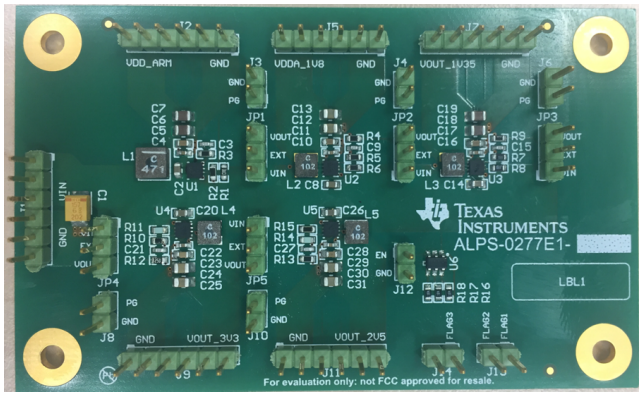
特性

- 3.3V 至 5.5V 输入电压范围
- DCS-Control™可实现快速瞬态响应的拓扑
- 高效率和低静态电流
- 可实现轻负载效率的省电模式
- TLV6208x 系列方案可实现低成本解决方案

应用

- 设备
- 测试和测量
- 电子销售终端
- 物联网





该 TI 参考设计末尾的重要声明表述了授权使用、知识产权问题和其他重要的免责声明和信息。

1 System Description

The i.MX7 series application processor from NXP is a highly-integrated, multi-market applications processor designed to enable various applications. This TIDA-01416 reference design provides a scalable power solution for several i.MX7 processor versions supporting space-constrained and cost-sensitive systems. The power architecture follows the source material in *i.MX 7Dual Family of Applications Processors Datasheet*. A 1.1-V rail is required for the core and system on chip (SoC), a 1.8-V rail for the input/output (I/O) pads, a 3.3-V rail for I/O and SD card pads, a 3.3-V rail for Ethernet controller, and a 1.35-V rail for DDR3 I/O pad supply.

This reference design achieves high efficiency by using efficient, integrated DC/DC converters and no low dropout (LDO) linear regulators. High efficiency results in a low self-temperature rise and higher reliability.

1.1 Key System Specifications

表 **1. Key System Specifications**

PARAMETER		SPECIFICATIONS	DETAILS
Input voltage range		3.3 V to 5.5 V	—
OUTPUTS PROVIDED			
VDD_ARM, VDD_SOC	Voltage setpoint	1.1 V	节 3.1.1
	Ripple	< 20 mV	
	Transient response	< 5%	
	Load regulation	< 0.4 %	
	Line regulation	< 0.4%	
VDDA_1P8	Voltage setpoint	1.8 V	节 3.1.2
	Ripple	< 25 mV	
	Transient response	< 5%	
	Load regulation	< 0.4 %	
	Line regulation	< 0.4 %	
NVCC_3P3, NVCC_ENET1	Voltage setpoint	3.3 V	节 3.1.3
	Ripple	< 20 mV	
	Transient response	< 5 %	
	Load regulation	< 0.4 %	
	Line regulation	< 0.4 %, V_{IN} > 3.3 V	
NVCC_DRAM	Voltage setpoint	1.35 V	节 3.1.4
	Ripple	< 20 mV	
	Transient response	< 5%	
	Load regulation	< 0.4 %	
	Line regulation	< 0.4%, V_{IN} > 3.3 V	
Efficiency (each regulator at half of its rated load)		—	节 3.1.1, 节 3.1.2, 节 3.1.3, 节 3.1.4
Efficiency (each regulator at its full rated load)		—	节 3.1.1, 节 3.1.2, 节 3.1.3, 节 3.1.4
Sequencing order (power up)		1. VDD_ARM and VDD_SOC; 2. VDDA_1P8, NVCC_3P3, NVCC_SD_IO, and NVCC_ENET1; 3. NVCC_DRAM_CKE	节 3.1.5
Sequencing order (power down)		1. NVCC_DRAM_CKE; 2. VDDA_1P8, NVCC_3P3, and NVCC_SD_IO; 3. VDD_ARM and VDD_SOC	

2 System Overview

2.1 Block Diagram

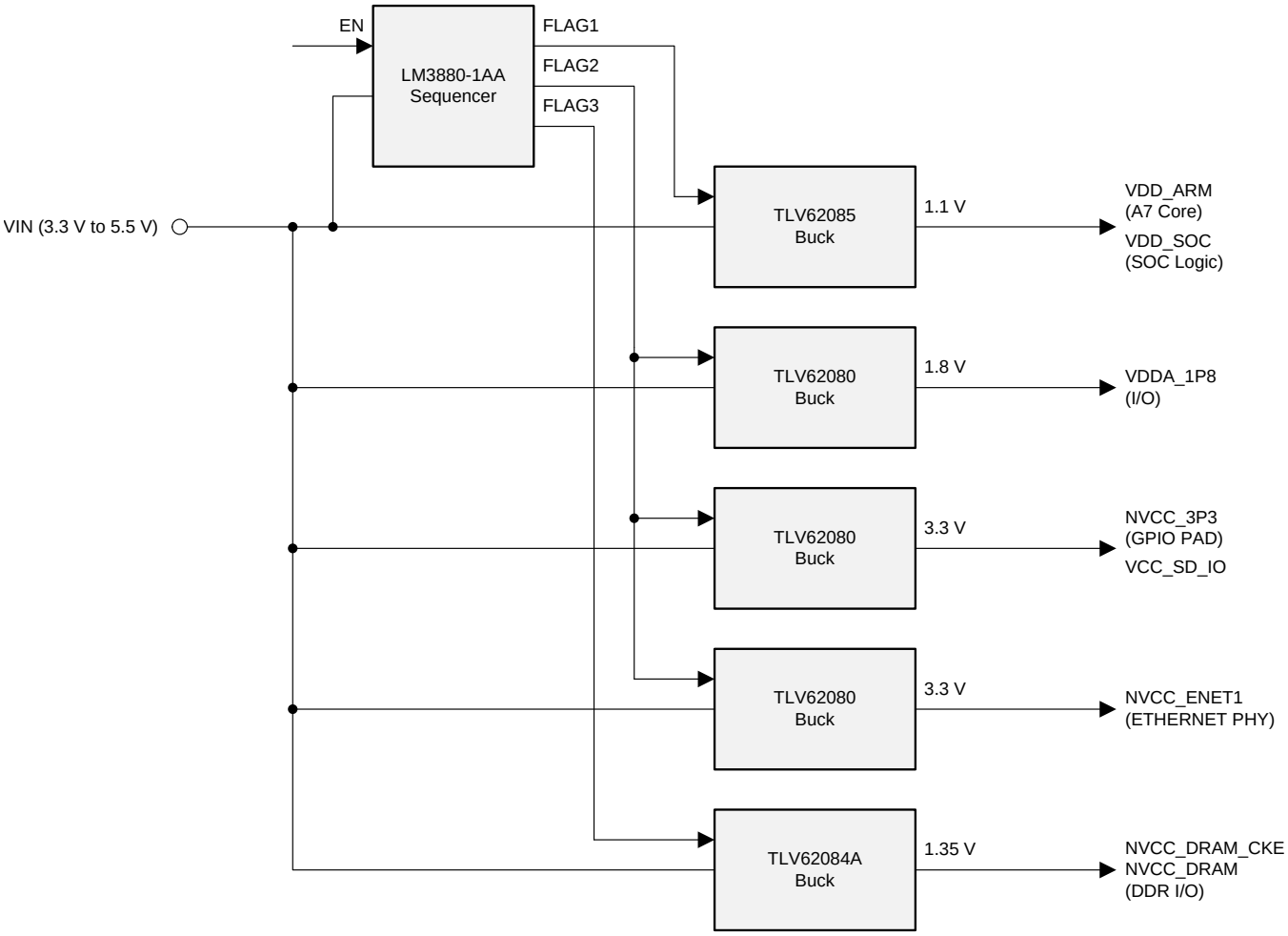


图 **1. Block Diagram**

2.2 Highlighted Products

2.2.1 TLV62085

The TLV62085 is a 3-A, high-frequency, synchronous step-down converter optimized for small solution size and high efficiency. At medium to heavy loads, the converter operates in pulse-width modulation (PWM) mode and automatically enters power save mode operation at light load to maintain high efficiency over the entire load current range. Its DCS-Control™ topology (**D**irect **C**ontrol with **S**eamless transition into power save mode) enables a very-fast transient response to regulate the output voltage during heavy load changes, while its high switching frequency enables the use of a small inductor and output capacitor.

2.2.2 TLV62080, TLV62084A

The TLV6208x family of devices are small buck converters with few external components that enable cost-effective solutions. The 1.2-A (TLV62080) and 2-A (TLV62084A) synchronous step-down converters provide high-efficiency over a wide output current range. At medium to heavy loads, the TLV6208x converters operate in PWM mode and automatically enter power save mode operation at light-load currents to maintain high efficiency over the entire load current range. With DCS-Control architecture, excellent load transient performance and output voltage regulation accuracy are achieved.

2.2.3 LM3880

The LM3880 Simple Power Supply Sequencer offers the easiest method to control power-up sequencing and power-down sequencing of multiple independent voltage rails. The LM3880 contains a precision enable pin and three open-drain output flags. When the LM3880 is enabled, the three output flags sequentially release, after individual time delays, thus permitting the connected power supplies to start up. The output flags follow a reverse sequence during power down when the enable pin is pulled down.

2.3 System Design Theory

The application processor power requirements are a function of the specific functionality used in a given application. In most cases, the current drawn by each rail is not known precisely during the design phase. Only gross estimates are available when the power supply is designed. For this reason, this reference design uses DC/DC converters that are high enough power to support the majority of i.MX7 applications, while still supplying a small solution size and high efficiency. Use 2-A converters to provide the 1.8-V and 3.3-V I/O rails and a 3-A converter for the common 1.1-V core and SoC rail. The output voltages of the converter are adjustable with external resistor feedback dividers.

The i.MX7 application processor only requires a simple sequencing of the power rails. VDD_SOC must be stable before NVDCC_DRAM and NVDCC_DRAM_CKE start to ramp. For down sequencing, first NVCC_DRAM and NVDCC_DRAM_CKE must be powered down before VDD_SOC is disabled. Though no specific sequencing is required for the other rails, this reference design also applies a controlled sequencing of the other rails to reduce the inrush current drawn from the input source, as well as to provide a controlled system start-up. The LM3880-1AA Simple Sequencer starts VDD_SOC and VDD_ARM first; then VDD_1P8, NVCC_3P3 VCCA, and NVCC_ENET1 second; and then finally, the 1.35-V converter (NVCC_DRAM_CKE and NVCC_DRAM rail). This reference design uses the 1AA version of LM3880, which provides a sequencing power-up order of FLAG1, FLAG2, and FLAG3 with a delay time (t_{DELAY}) of 10 ms. Power-up sequencing starts when the enable pin of the LM3880 device is pulled high and power-down sequencing starts when the enable pin is pulled low (see 图 2). An external enable signal must be applied at jumper J12, such as from a microcontroller (MCU) or signal generator.

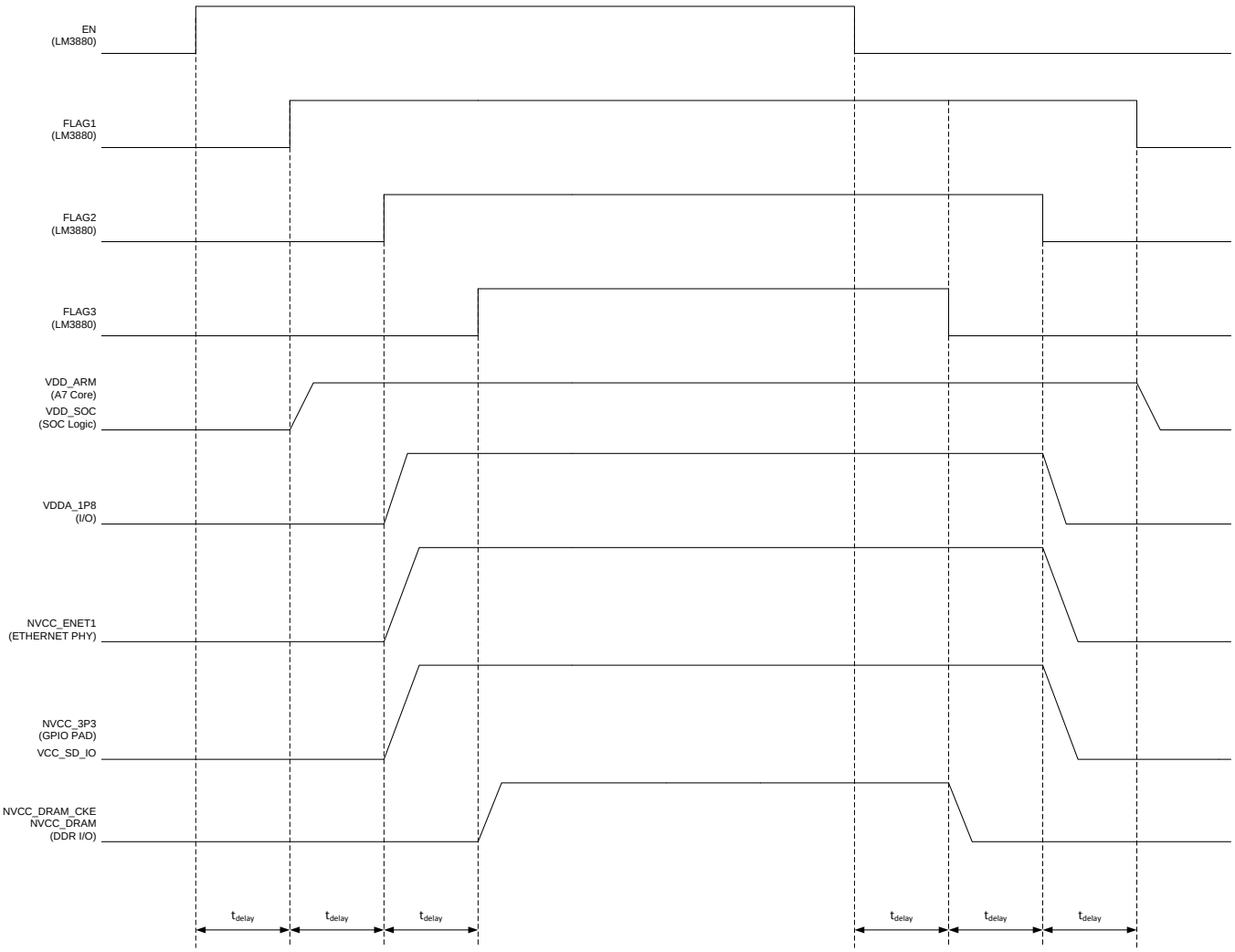


图 2. Power Sequencing

3 Hardware, Software, Testing Requirements and Test Results

To test this reference design, apply an input voltage (typically 3.6 V) to the J1 input connector. Apply an enable signal to jumper J12 with a signal generator to initiate the power-up sequencing of the output rails. For the high level, apply at least 1.4 V (maximum level is V_{IN}); for the low level, apply less than 1.0 V.

3.1 Testing and Results

This section includes the relevant test results to power the i.MX7 application processor. Unless otherwise noted, all testing was conducted with 3.6 V_{IN} and at room temperature.

3.1.1 VDD_ARM, VDD_SOC

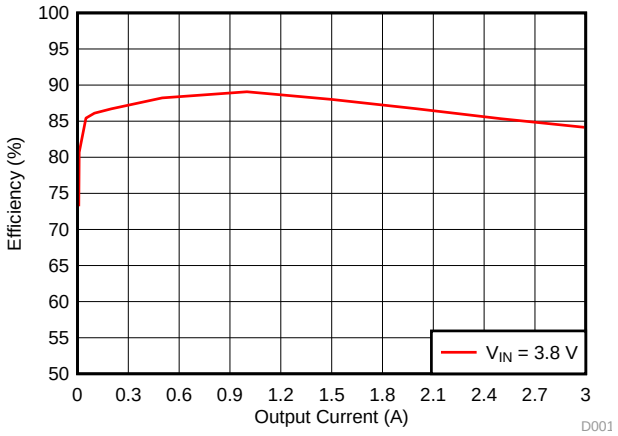


图 **3. VDD_ARM, VDD_SOC Efficiency (3.8 V_{IN})**

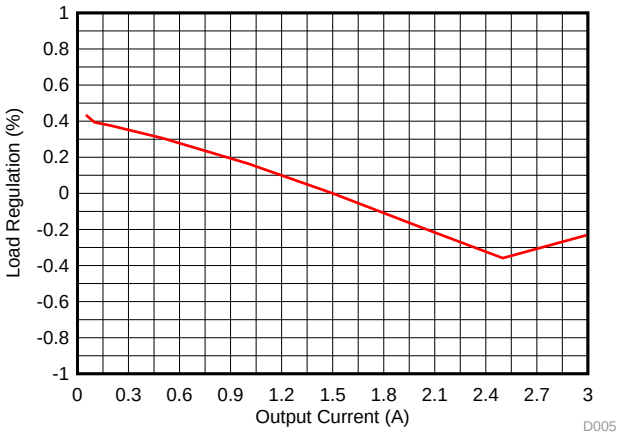


图 **4. VDD_ARM, VDD_SOC Load Regulation (3.8 V_{IN})**

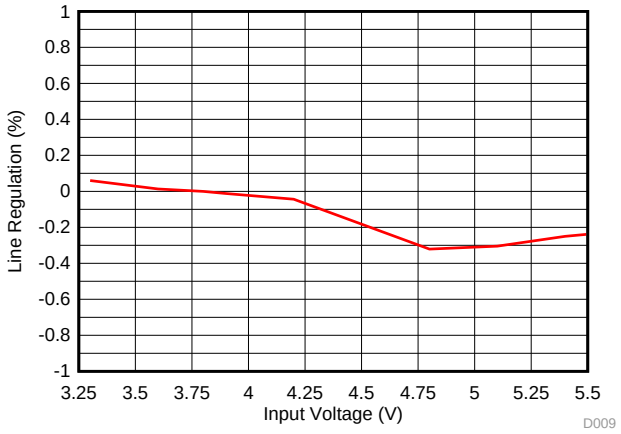


图 **5. VDD_ARM, VDD_SOC Line Regulation (3-A Load)**

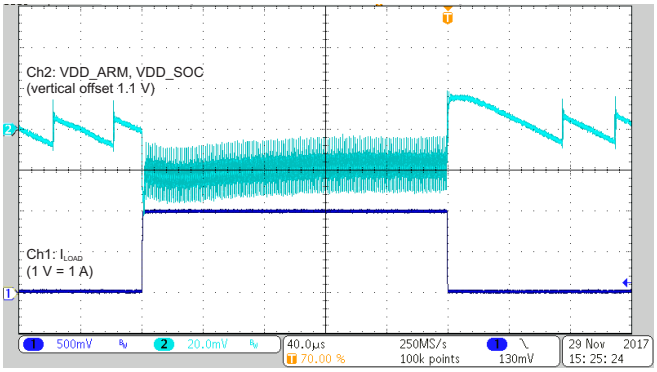


图 6. VDD_ARM, VDD_SOC Transient Response
(V_{IN} = 3.8 V, 10-mA to 2-A Load Step)

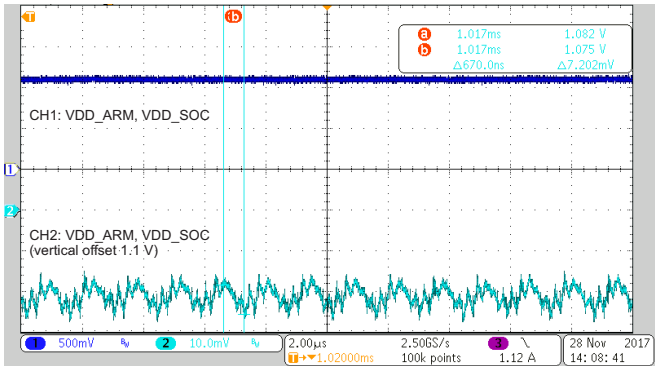


图 7. VDD_ARM, VDD_SOC Ripple
(V_{IN} = 3.8 V, 3-A Load)

3.1.2 VDDA_1P8

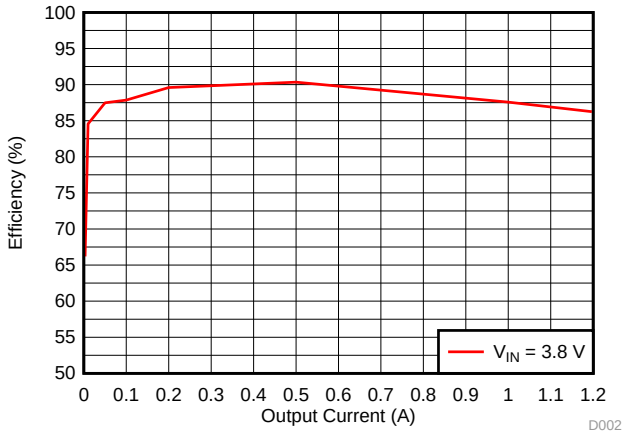


图 8. VDDA_1P8 Efficiency (3.8 V_{IN})

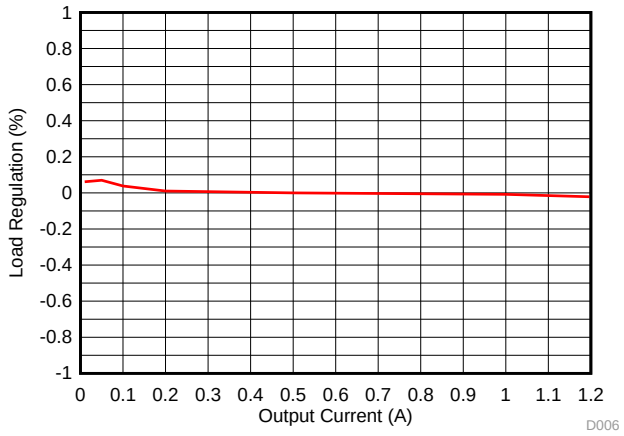


图 9. VDDA_1P8 Load Regulation (3.8 V_{IN})

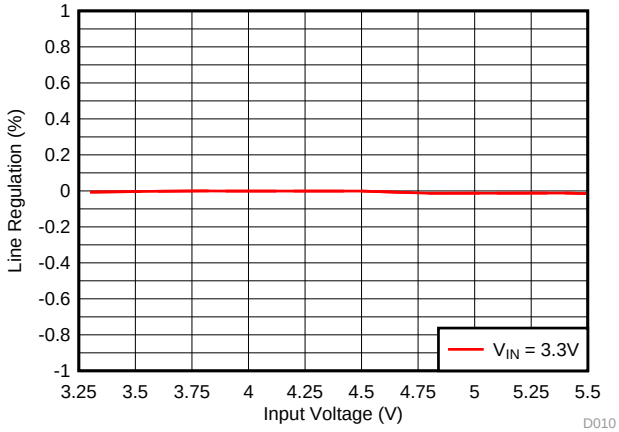


图 10. VDDA_1P8 Line Regulation (1.2-A Load)

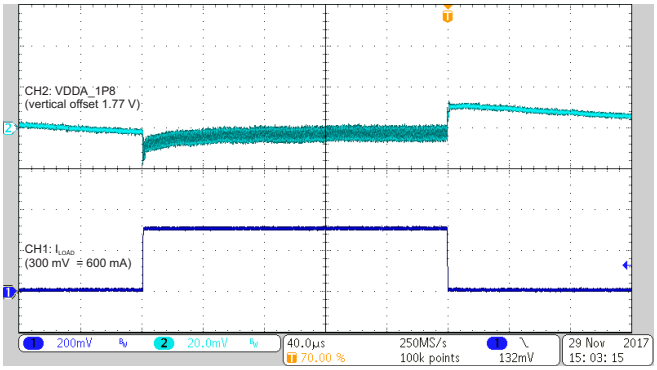


图 11. VDDA_1P8 Transient Response (V_{IN} = 3.8 V, 1-mA to 600-mA Load Step)

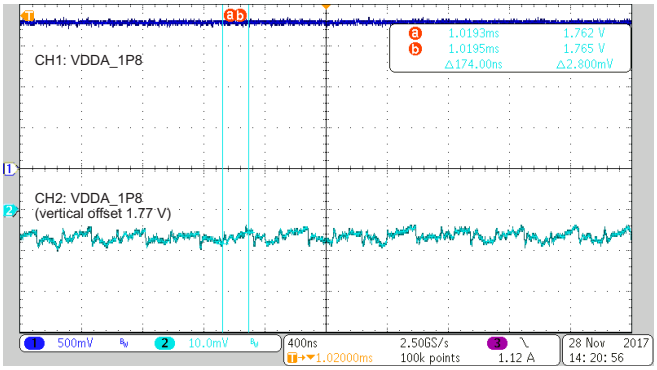


图 12. VDDA_1P8 Ripple (V_{IN} = 3.8 V, 1.2-A Load)

3.1.3 NVCC_3P3

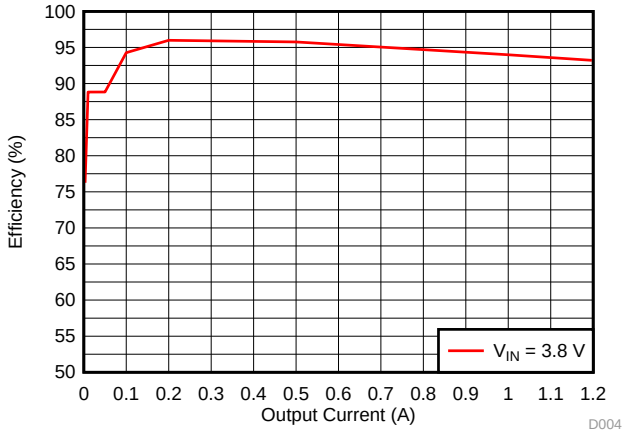


图 13. NVCC_3P3 Efficiency (V_{IN} = 3.8 V)

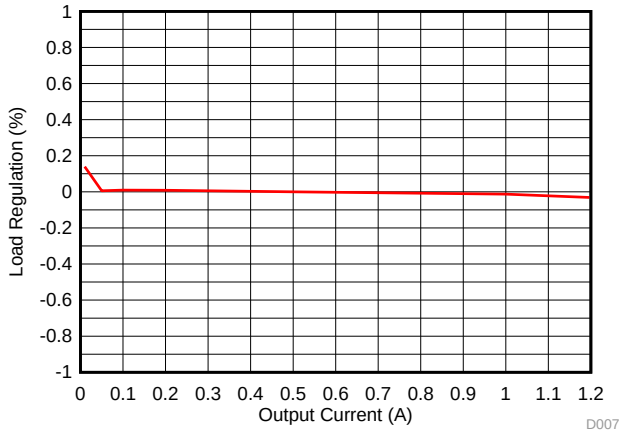


图 14. NVCC_3P3 Load Regulation (V_{IN} = 3.8 V)

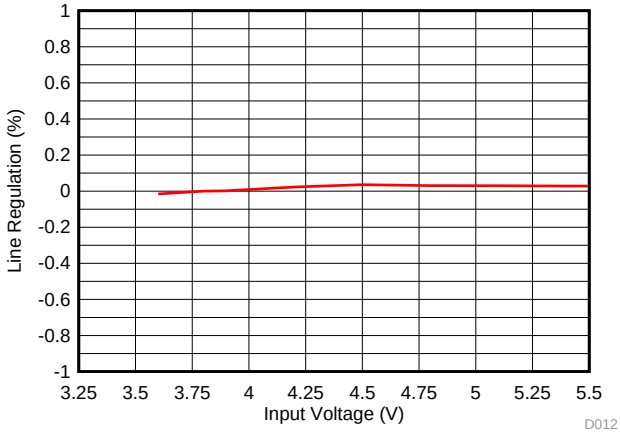


图 15. NVCC_3P3 Line Regulation (1.2-A Load)

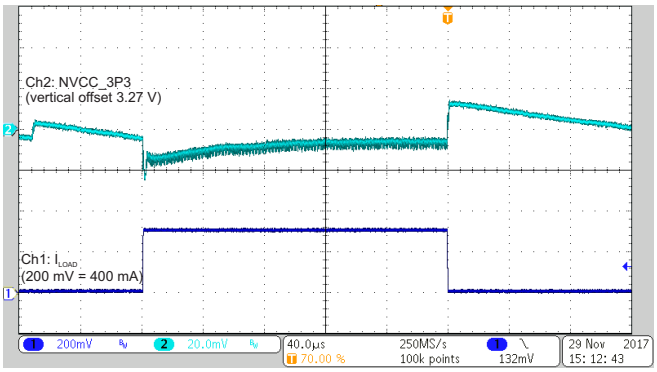


图 16. NVCC_3P3 Transient Response (V_{IN} = 3.8 V, 1-mA to 600-mA Load Step)

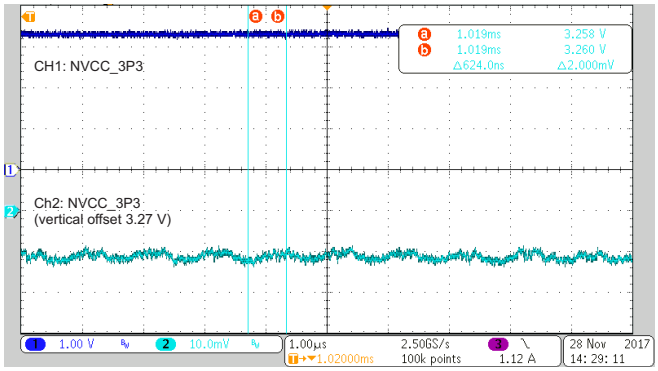


图 17. NVCC_3P3 Ripple (V_{IN} = 3.8 V, 1.2-A Load)

3.1.4 NVCC_DRAM

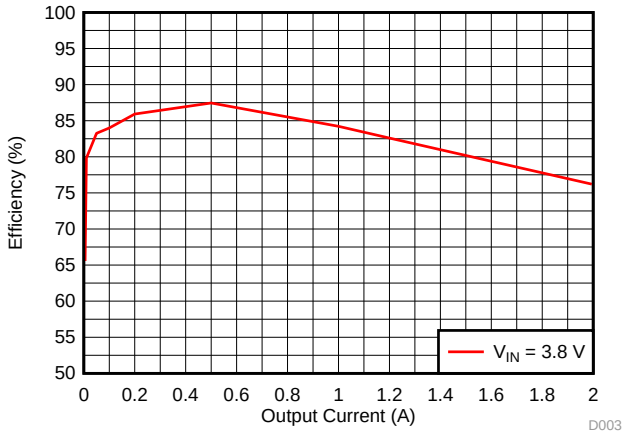


图 18. NVCC_DRAM Efficiency (V_{IN} = 3.8 V)

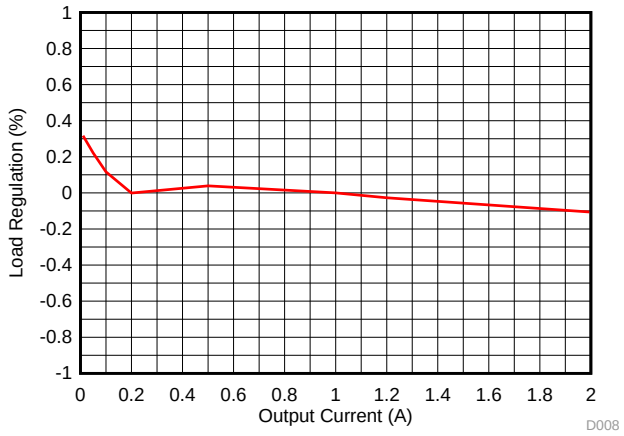


图 19. NVCC_DRAM Load Regulation (V_{IN} = 3.8 V)

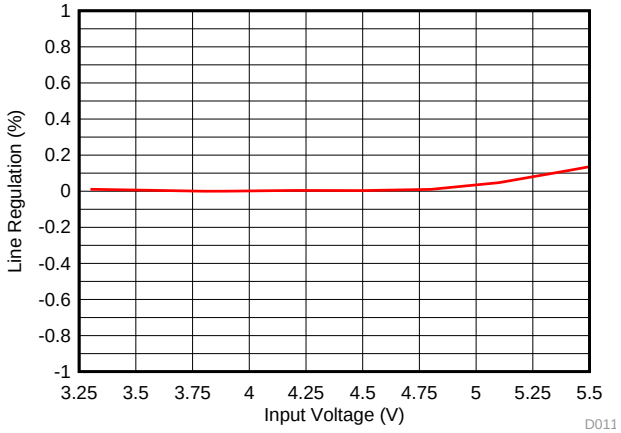


图 20. NVCC_DRAM Line Regulation (2-A Load)

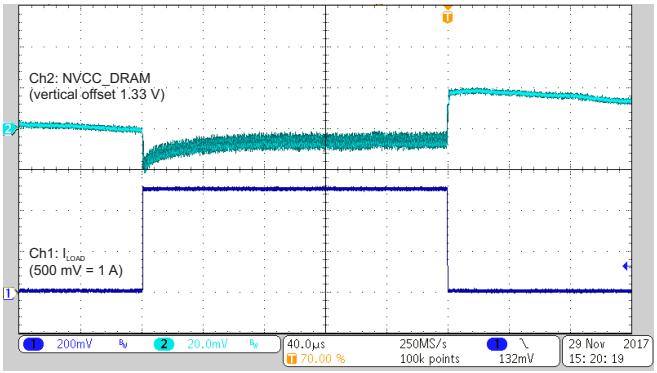


图 21. NVCC_DRAM Transient Response (V_{IN} = 3.8 V, 1-mA to 1-A Load Step)

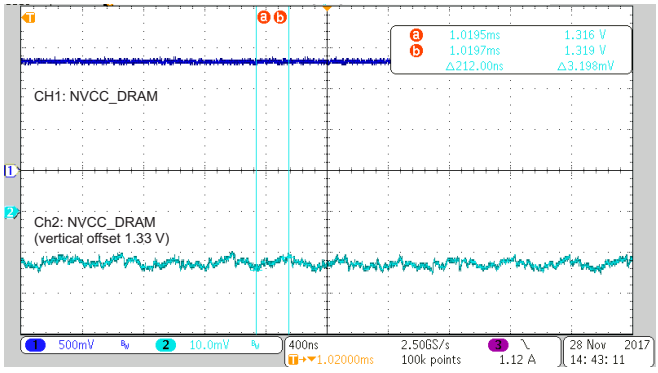


图 22. NVCC_DRAM Ripple (V_{IN} = 3.8 V, 2-A Load)

3.1.5 System Power Up and Power Down

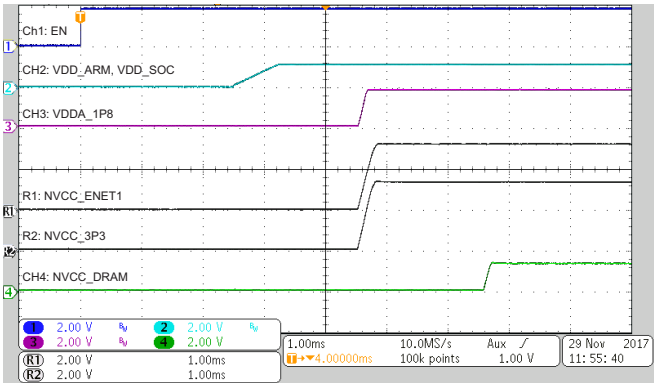


图 23. Power Up (V_{IN} = 3.8 V, No Load)

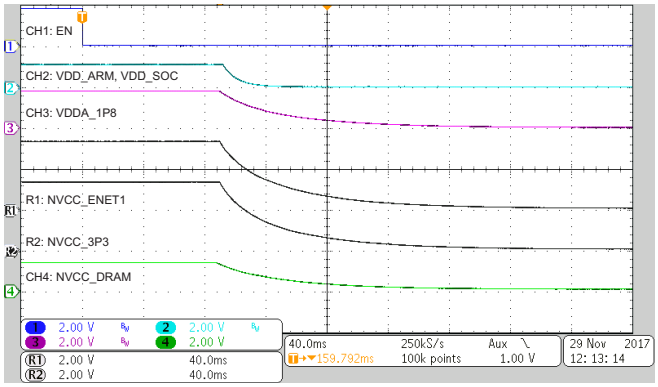


图 24. Power Down (V_{IN} = 3.8 V, No Load)

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01416.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01416.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01416.

4.4 Gerber Files

To download the Gerber files, see the design files at TIDA-01416.

4.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01416.

5 Related Documentation

1. NXP, *i.MX 7Dual Family of Applications Processors Datasheet*
2. Texas Instruments, *High Efficiency 3-A Step-Down Converterin 2-mm×2-mm VSON Package*
3. Texas Instruments, *1.2-A and 2-A High-Efficiency Step-Down Converter in 2-mm×2-mm WSON Package*
4. Texas Instruments, *Simple Power Sequencer*
5. Texas Instruments, *High-efficiency, low-ripple DCS-Control™ offers seamless PWM/power-save transitions*

5.1 商标

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