TI Designs：TIDA-01432

可充电且具有增强的数据路径性能的汽车无源媒体集线器参考设计

说明

此汽车参考设计展示了适用于需要数据传输的媒体端口的独特方法。此设计能够通过 15W USB Type-C™端口支持 USB 2.0。通过利用包含符合 AEC-Q100 标准且经过 CISPR-25 5 类测试的模拟集成电路 (IC) 在内的完整参考设计，客户可加快其媒体端口系统的速度。此参考设计通过灵活的无源解决方案，最大程度地简化了研发工作。该解决方案使系统能与音响主机进行角色交换，并能使用 1x2 英寸小型解决方案为 USB Type-C 和传统器件充电。

资源

TIDA-01432	设计文件夹
TPS254900-Q1	产品文件夹
LM74610-Q1	产品文件夹
TUSB319-Q1	产品文件夹
TUSB213-Q1	产品文件夹
LMS3635-Q1	产品文件夹
SN74HCT1G04-Q1	产品文件夹

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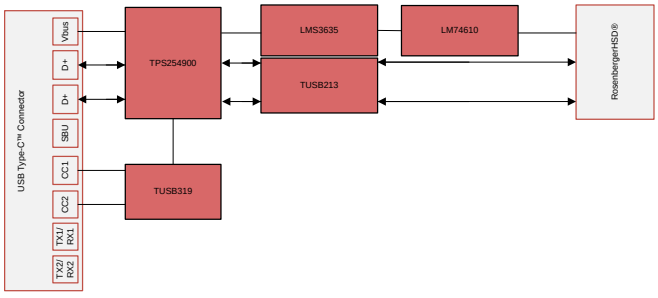
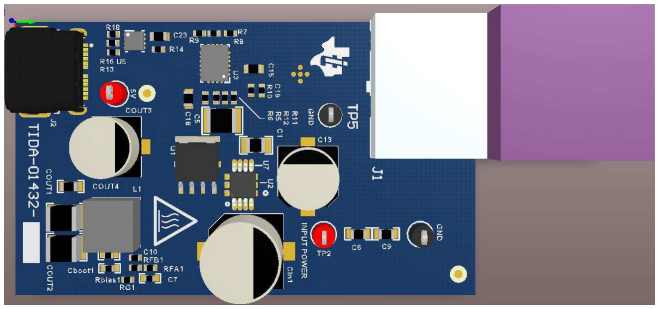
特性

- LM74610-Q1 智能二极管模拟理想的二极管整流器，并在反极性情况下为下游器件提供保护
- TUSB319-Q1 和 TPS254900-Q1 分别为 CC1/CC2 和 D+/D- 线路提供协商，从而为 Type-C 或传统下游器件充电
- 基于典型媒体接口板尺寸（1 x 2 英寸）的小型解决方案尺寸
- 针对高达 40V 输入瞬态电压的电池短路保护和负载突降保护
- 汽车级 LMS3635-Q1 可通过独特的 Hotrod ™封装来优化电源，并减少寄生效应，以便缓解 EMI 而又不干扰调幅或调频频带频率
- TUSB213-Q1 提供优化的高速性能，以便通过 USB-IF 电气合规性测试，并满足高达 3 米的 USB-IF 近端和远端眼图测试
- 与领先的 On-The-Go (OTG) 系统兼容

应用

- 汽车音响主机（支持远程显示）
- 汽车中端和高端音响主机
- 远程媒体中心





该 TI 参考设计末尾的重要声明表述了授权使用、知识产权问题和其他重要的免责声明和信息。

1 System Description

This end equipment is designed to connect to a head unit through a 1- to 3-m cable and allow users to plug in host-flip-capable devices (also known as on-the-go) to the external USB Type-C™ port. Designing an active media hub can be costly and time consuming. With a digital control that is typically located in the head unit, this passive solution provides improved signal performance within a remote media hub. This reference design helps to minimize design efforts by providing a simple passive solution which is capable of role swapping with the head unit.

1.1 Key System Specifications

表 **1. Key System Specifications**

PARAMETER	COMMENTS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	5.5	12	36	V
F_{SW}	Switching frequency	360	400	440	kHz
$R_{DS(ON)}$	ON resistance of power switch	—	45	69	mΩ
V_{DC-DC}	DC-DC system output	4.75	5.0	5.25	V
I_{OUT}	VBUS	0.5	1.5	3.0	A
D+/D–	High speed	—	480	—	Mbps

2 System Overview

2.1 Block Diagram

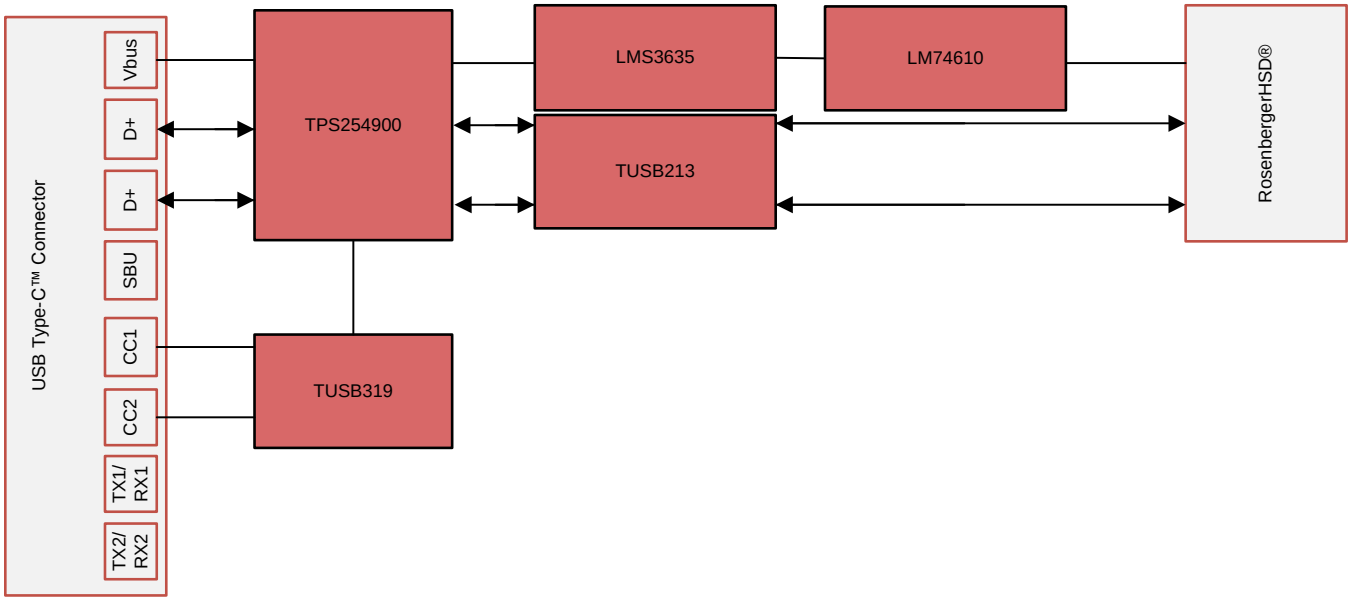


图 **1. TIDA-01432 Block Diagram**

2.2 Highlighted Products

2.2.1 TUSB213-Q1: USB 2.0 High-Speed Signal Conditioner

The TUSB213 is a USB high-speed (HS) signal conditioner designed to compensate for intersymbol interference (ISI) signal loss in a transmission channel. TUSB213 has a patent-pending design which is agnostic to USB low-speed (LS) and USB full-speed (FS) signals and does not alter their signal characteristics, while HS signals are compensated. In addition, the design is compatible with USB on-the-go (OTG) and battery charging (BC) specifications.

Programmable signal gain through an external resistor permits fine-tuning device performance to optimize signals, which helps to pass USB HS electrical compliance tests at the connector.

图 2 shows the TUSB213-Q1 functional block diagram and 图 3 shows the TUSB213 simplified circuit.

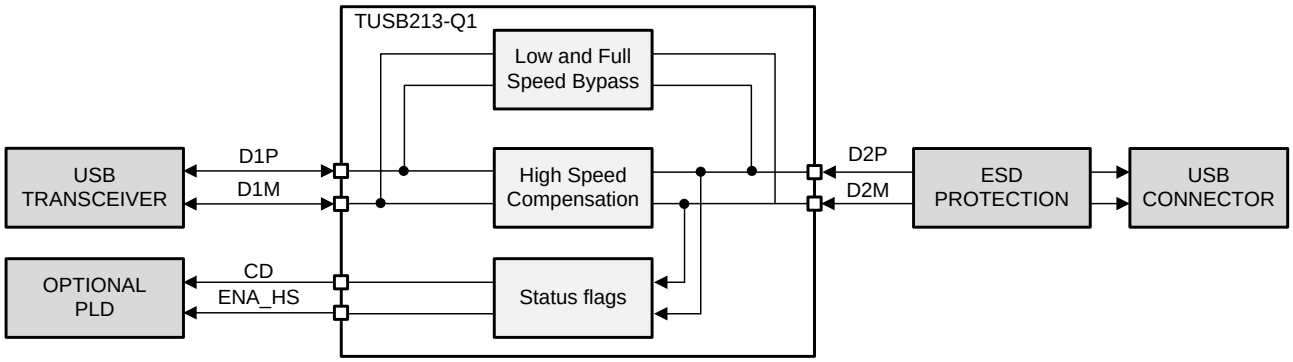


图 2. TUSB213-Q1 Functional Block Diagram

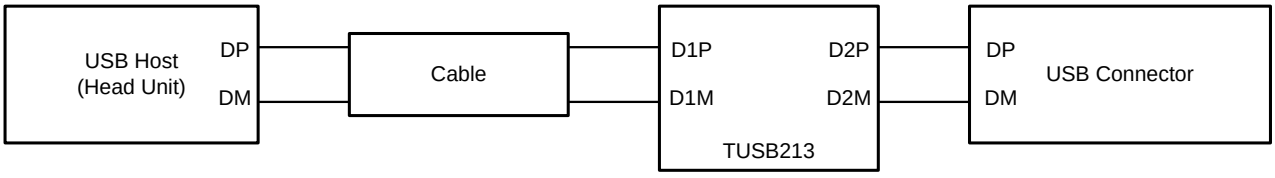


图 3. TUSB213 Simplified Circuit

2.2.2 TUSB319-Q1: Automotive USB Type-C™ DFP Port Controller

The USB Type-C ecosystem operates around a small form factor (SFF) connector and cable that is flippable and reversible. A scheme is required to determine the connector orientation because of the nature of the connector. Additional schemes are required to determine when a USB port is attached and the acting role of the USB port (downstream-facing port (DFP) and upstream-facing port (UFP)), as well as to communicate Type-C current capabilities. These schemes are implemented over the CC pins according to the USB Type-C specifications. The TUSB319-Q1 device provides configuration channel (CC) logic for determining USB port attach and detach, cable orientation, and Type-C current mode for DFP applications (see 图 4 and 图 5).

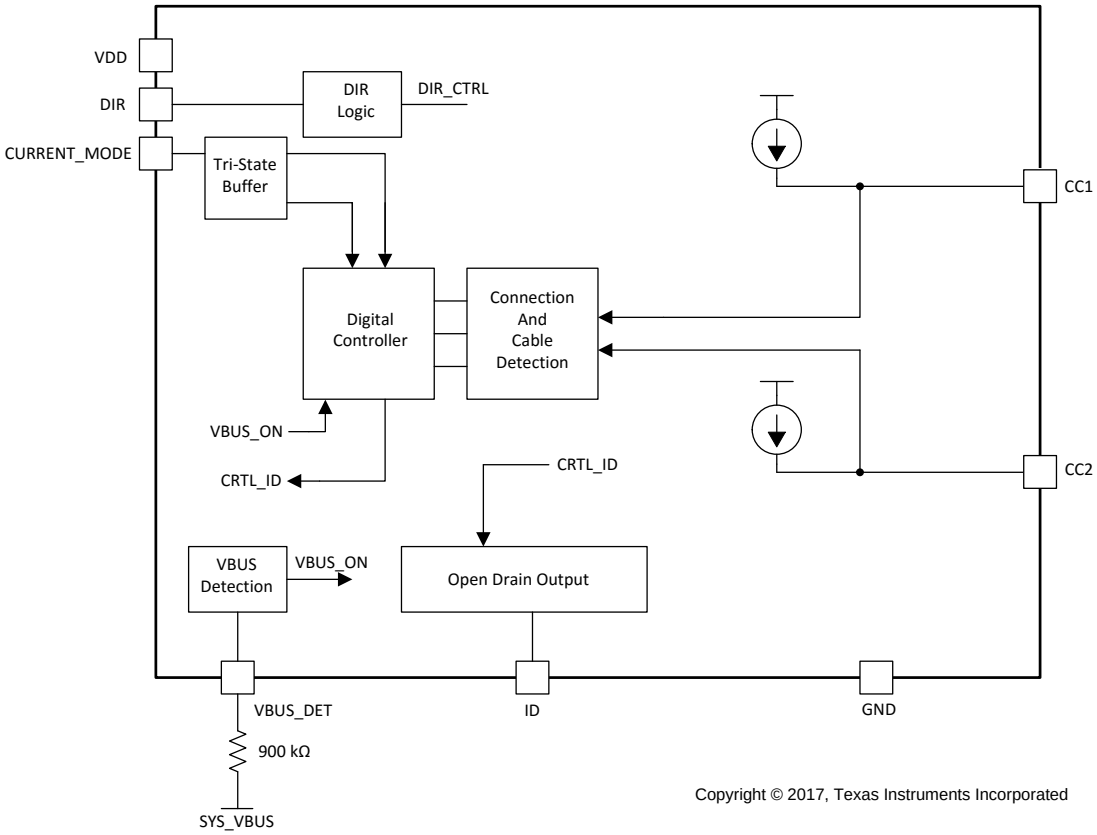


图 4. TUSB319-Q1 Functional Block Diagram

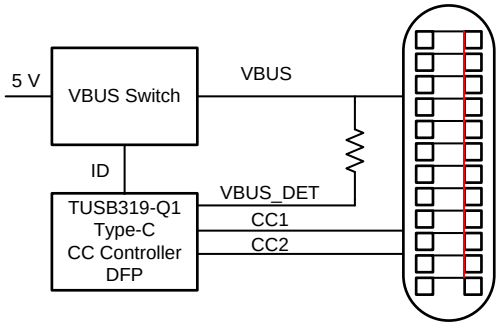


图 5. TUSB319-Q1 Simplified Circuit

2.2.3 LMS3635-Q1: 3.5-A, 36-V Synchronous, 400-kHz, Step-Down Converter

The LMS3635-Q1 are wide-input voltage range, low quiescent current, high-performance regulators with internal compensation (see 图 6 and 图 7). This device is designed to minimize end-product cost and size while operating in demanding automotive and high-performance industrial environments. The normal operating frequency is 400 kHz, which allows the use of small passive components. This device has a low, unloaded current consumption which eliminates the requirement for an external back-up low-dropout regulator (LDO). The LMS3635-Q1 low-shutdown current and high maximum-operating voltage also allows the elimination of an external load switch. An advanced reset output is provided to further reduce system cost, which can often eliminate the use of an external reset device.

The LMS3635-Q1 is designed with flip-chip or HotRod™ technology, which greatly reduces the parasitic inductance of the pins. In addition, the layout of the device allows for reduction in the radiated noise generated by the switching action through partial cancellation of the current-generated magnetic field. As a result, the switch-node waveform exhibits less overshoot and ringing.

The LMS3635-Q1 is AEC-Q1 qualified in addition to having electrical characteristics ensured up to a maximum junction temperature of 150°C. The LMS3635-Q1 is available in an SON package with wettable-flanks, which allows easy inspection of the soldering without requiring x-ray checks.

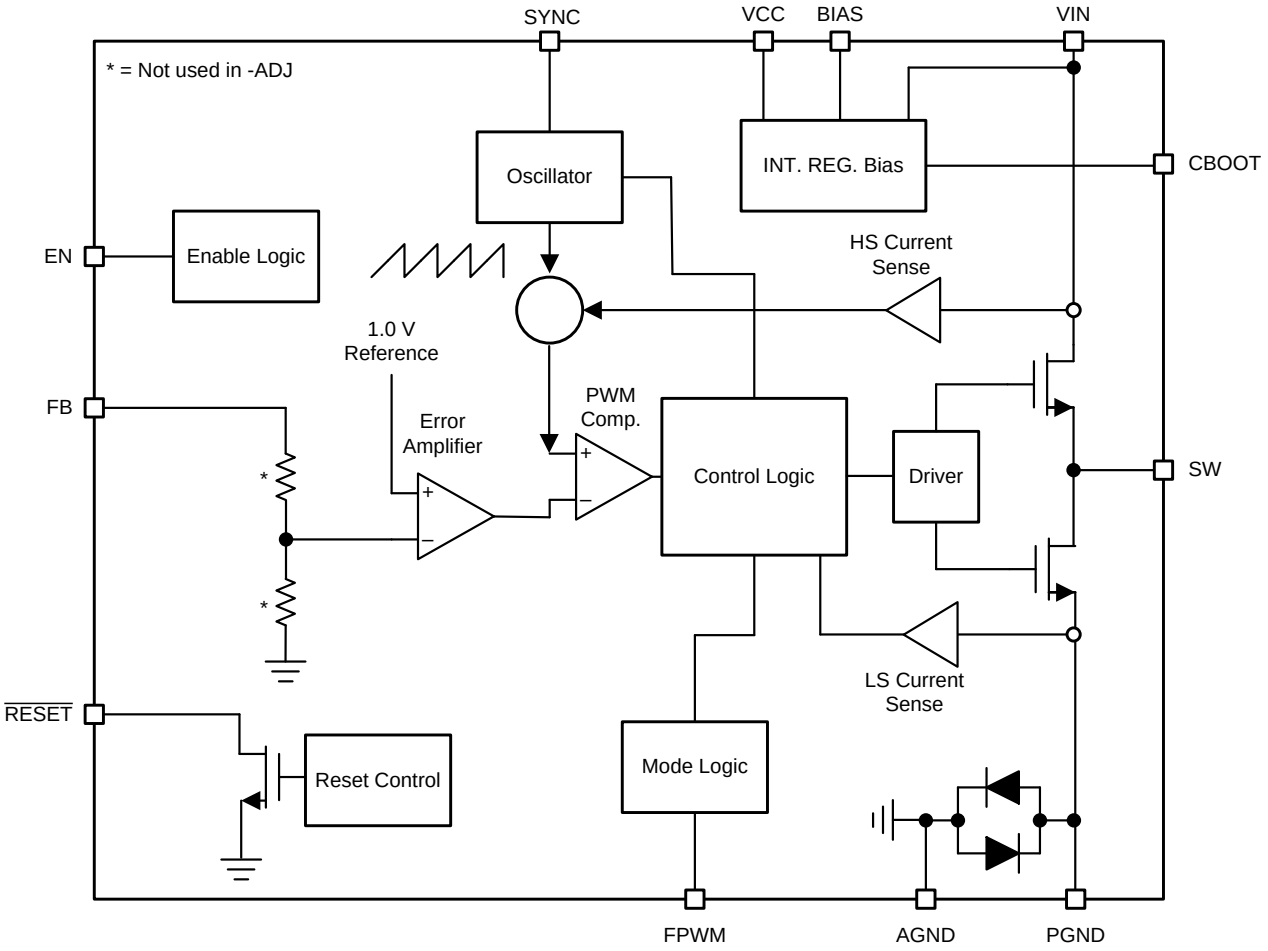


图 6. LMS3635-Q1 Functional Block Diagram

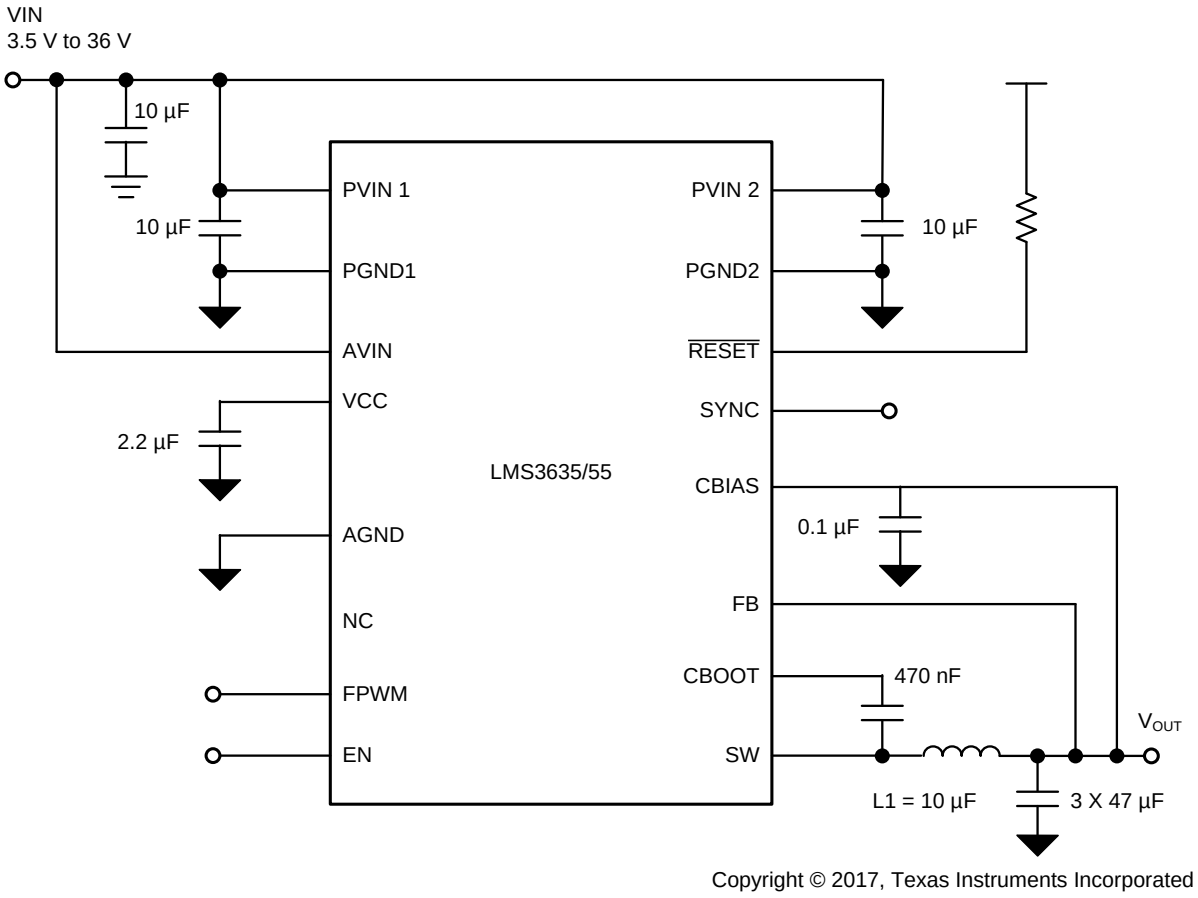


图 **7. LMS3635-Q1 Simplified Circuit**

2.2.4 LM74610-Q1: Zero I_Q Reverse-Polarity-Protection Smart Diode

Most systems in automotive or industrial applications require fast-response reverse polarity protection at the input stage. Schottky diodes or P-Channel field-effect transistors (PFET) are typically used in most power systems to protect the load in the case of negative polarity. The main disadvantage of using diodes is voltage drop during forward conduction, which reduces the available voltage and increases the associated power losses. PFET solutions are inefficient for handling high load current at a low input voltage.

The LM74610-Q1 is a zero I_Q controller that is combined with an external N-channel MOSFET to replace a diode or PFET reverse polarity solution in power systems (see 图 8 and 图 9). The voltage across the MOSFET source and drain is constantly monitored by the LM74610-Q1 ANODE and CATHODE pins. An internal charge pump is used to provide the GATE drive for the external MOSFET. This stored energy is used to drive the gate of MOSFET. The voltage drop depends on the RDS_{ON} of a particular MOSFET in use, which is significantly smaller than a PFET. The LM74610-Q1 has no ground reference, which makes it identical to a diode.

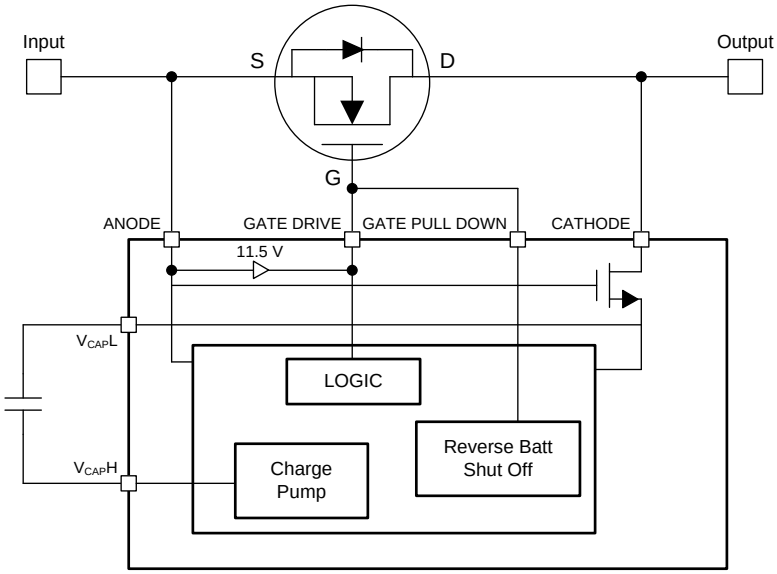


图 8. LM74610-Q1 Functional Block Diagram

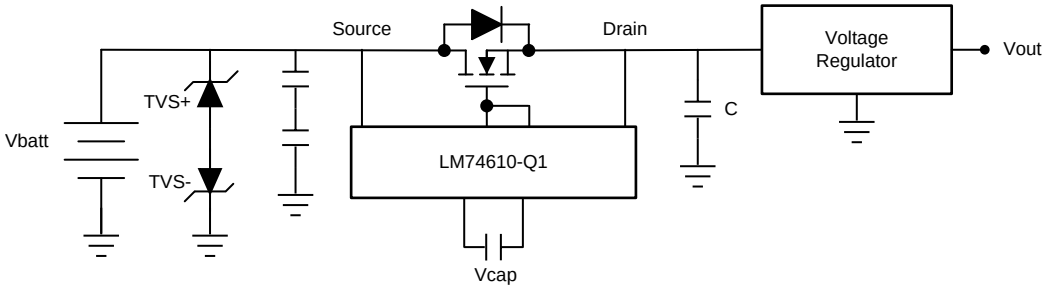


图 9. LM74610-Q1 Simplified Circuit

2.2.5 TPS254900-Q1: Automotive Charging Port Controller and Power Switch With Short-to-Battery Protection

The TPS254900-Q1 device is a USB charging controller and power switch which integrates D+ and D– short-to-battery protection, cable compensation, current monitor (IMON), and International Electrotechnical Commission (IEC) certified electrostatic discharge (ESD) protection suitable for automotive USB charging and USB port-protection applications (see 图 10 and 图 11).

The integrated power distribution switch uses N-channel MOSFETs suitable for applications that encounter short circuits or heavy capacitive loads. The device allows the user to adjust the current-limit thresholds using external resistors. The device enters constant-current mode when the load exceeds the current-limit threshold.

The TPS254900-Q1 device provides VBUS, D+, and D– short-to-battery protection. These features protect the upstream voltage regulator, automotive processor, and hub when these pins are exposed to fault conditions.

The device also integrates charging downstream port (CDP) mode, defined in the BC1.2 specification, to enable up to 1.5-A fast charging of most portable devices during data communication.

The TPS254900-Q1 device integrates a cable compensation (CS) feature to compensate for long-cable voltage drop. This feature keeps the remote USB port-output voltage constant to enhance the user experience under high-current charging conditions.

The TPS254900-Q1 device provides a current-monitor function (IMON) by connecting a resistor from the IMON pin to GND to provide a positive voltage linearly with load current. This function can be used for system power or dynamic power management.

Additionally, the device provides ESD protection up to ±8 kV (contact discharge) and ±15 kV (air discharge) per IEC 61000-4-2 on DP_IN and DM_IN.

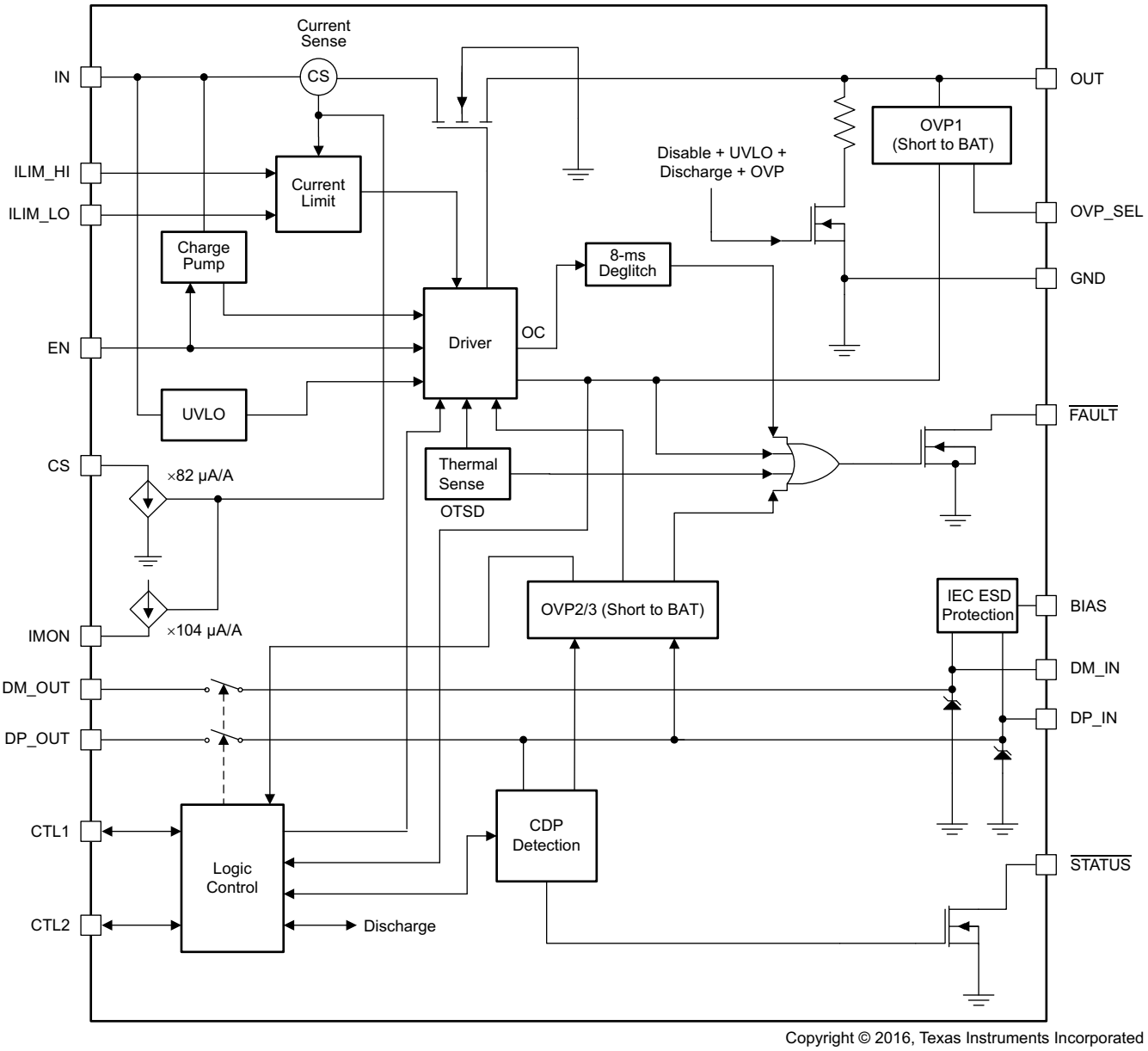


图 10. TPS254900-Q1 Functional Block Diagram

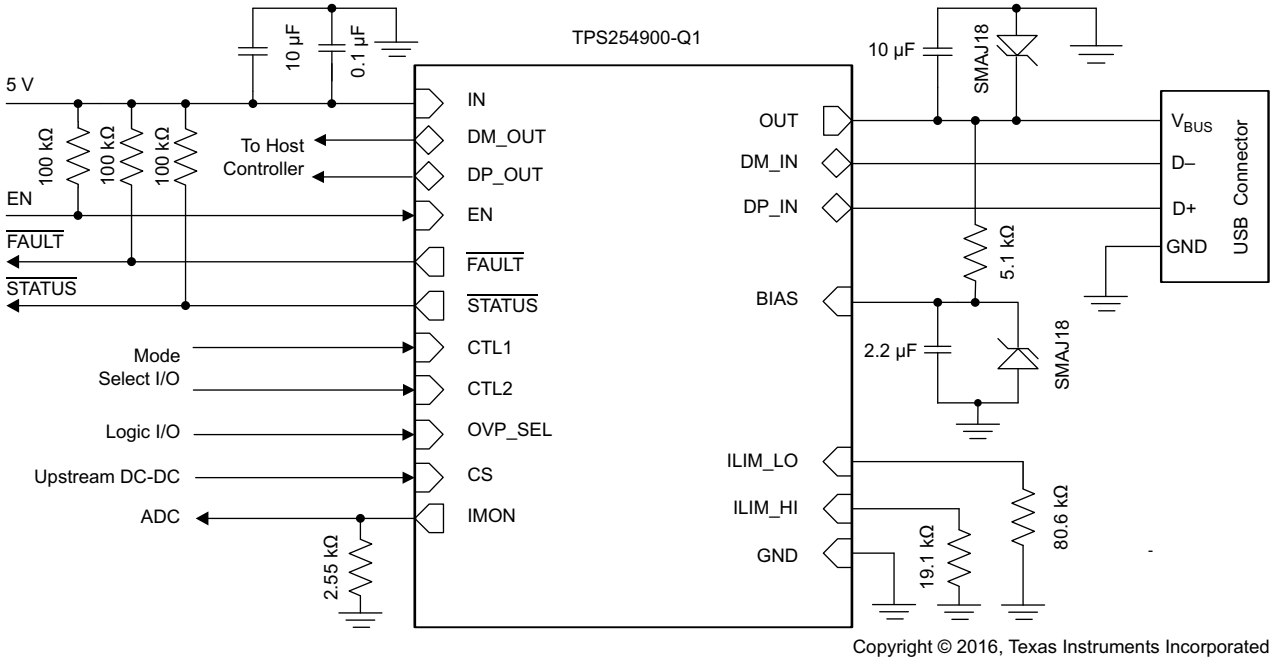


图 **11. TPS254900-Q1 Simplified Circuit**

2.3 System Design Theory

This reference design has been created to support USB Type-C DFP charging and CDP legacy charging in addition to USB 2.0 data. As the previous 图 1 shows, the TIDA-01432 is a media interface subsystem that can be connected as a remote media hub to a head unit. This design focuses on the signal integrity of the USB 2.0 data lines and is capable of OTG functionality while simultaneously supplying a charge to the port.

The specific goal of this design is to meet automotive standards and use parts that are already released (or planned to be released) as automotive Q-100 grade qualified. Meeting the pertinent protection standards as required by automotive original equipment manufacturers (OEMs) is important when designing a subsystem for automotive infotainment. The parts in this design have been selected to support typical protection requirements such as reverse battery protection, current limiting, short-to-battery protections, as well as ESD protections. Additionally, power supplies typically require a spread spectrum to mitigate electromagnetic interference (EMI) and switching frequency outside of the AM and FM band while supporting wide input off-battery operation. Take careful action during the circuit board layout to improve thermal dissipation and EMI to ultimately pass CISPR-25 class 5 and the USB Implementers Forum (USB-IF) specifications for near-end and far-end tests up to 3 m.

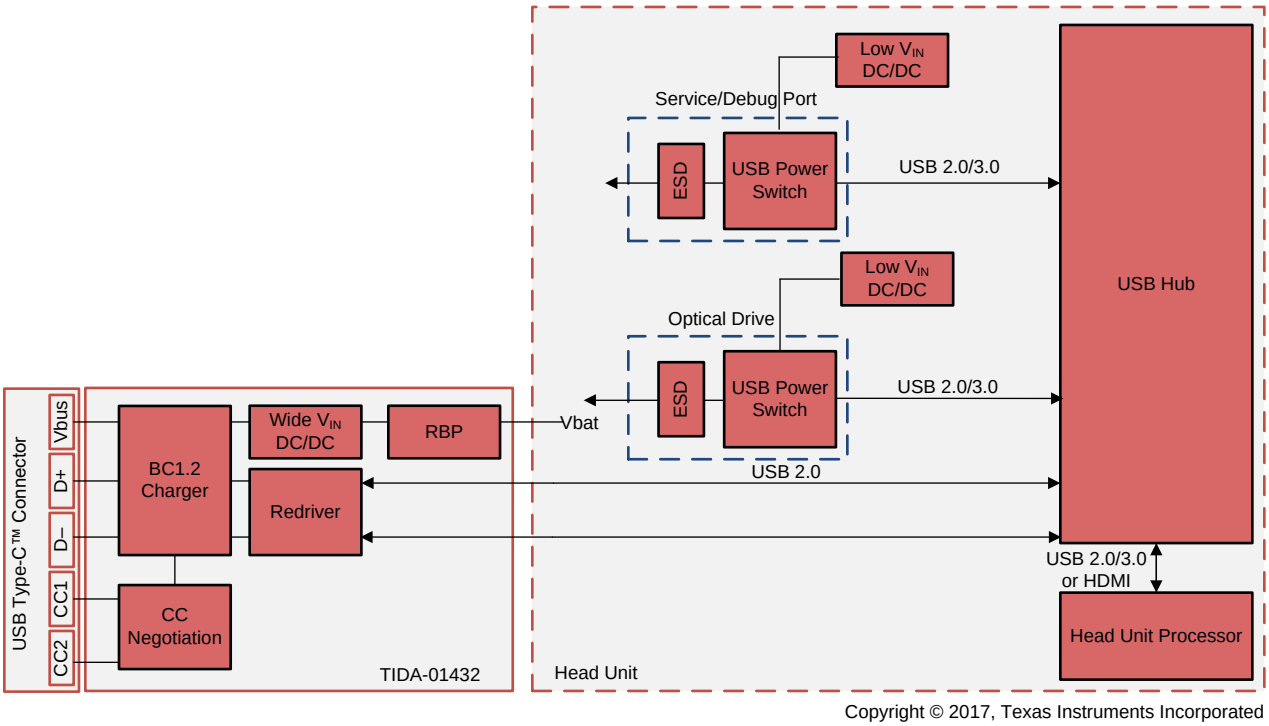


图 12. TIDA-01432 System Integration Concept

2.3.1 Charging Design Overview

USB Type-C connectors offer many benefits including reversible orientation, high-speed data rates, and high-power capabilities. For this particular design, the port is 15-W capable and supports high-speed USB 2.0 data. The USB Type-C controller transmits its 3-A current capability over the CC1/CC2 lines and the power switch of the BC1.2 controller instantiates charging for the UFP device for each case where a Type-C to Type-C connector is connected. For situations that use a Type-C to legacy connector (Type-A, micro Type-B, and so forth), the current capability is not received through CC1/CC2 lines but rather through the

data lines (D+/D–). By using the BC1.2 controller, the system can negotiate all the electrical signatures on D+/D–, which are provided to support CDP protocols. The use of this controller allows host and client devices to acknowledge the protocol handshake and draw additional current beyond the 500-mA or 900-mA maximum defined by USB 2.0 and USB 3.0, respectively. For more information about the theory behind this configuration, see *TPS25810 Charging Port Over USB Type-C™* (SLVA768).

2.3.2 Data Design Overview

As previously mentioned, the ability to flip the USB Type-C connector makes the design user friendly; however, this implementation still requires careful design consideration. The Type-C connector supports speeds up to 12 Gbps per lane, even though this design only uses USB 2.0 (480 Mbps). The signal integrity remains a priority during this design and care must be taken when routing the D+/D– signals. See 6.3 节 for more layout details.

2.3.3 Reverse Battery Protection

Reverse battery protection is a requirement for every electronic subsystem in a vehicle recognized by OEM standards as well as load dump protection standards ISO 16750-2. The LM74610 is used to control the negative-channel field-effect transistor (NFET) to protect the load in a negative polarity condition. This device is used to emulate an ideal diode by using an NFET in series with the battery supply. This configuration has the advantage of a highly effective and efficient substitute for reverse battery protection to the traditional rectifier. The LM74610 device has no power pin and no ground reference and thus requires zero I_Q and reducing standby current drawn from the battery. Additionally, the voltage drop across the FET is so inconsequential that it allows the wide V_{IN} buck regulator to operate at even lower battery input voltages. This property is an advantage for scenarios such as cold crank when the battery voltage temporarily drops to as low as 3.5 V. A traditional diode solution usually has a 700-mV voltage drop, so the buck converter would not be able to maintain the 5-V_{OUT} system voltage. With the smart diode solution, the buck still receives close to 5 V during this condition and can continue to operate.

图 13 shows a schematic of the reverse battery protection (LM74610).

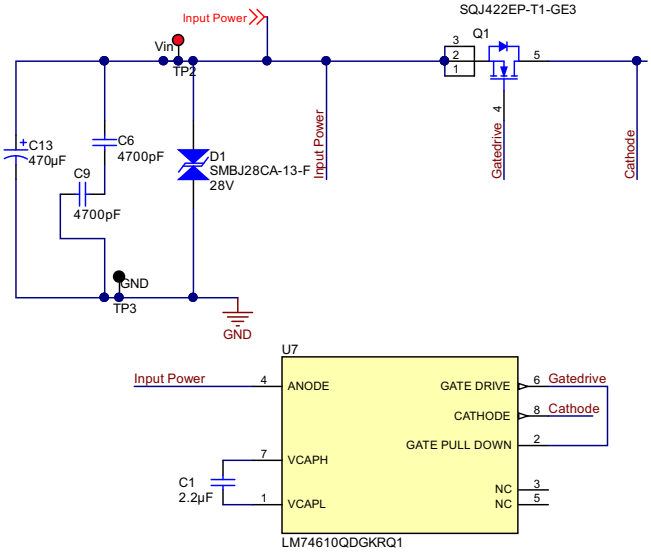


图 13. LM74610 Smart Diode Reverse Battery Protection

2.3.3.1 MOSFET

The LM74610-Q1 product folder has tools to help run simulations using the WEBENCH® circuit design and selection simulation services. *LM74610-Q1 Zero IQ Reverse Polarity Protection Smart Diode Controller* (SNOSCZ1) also outlines the MOSFET selection for the LM74610-Q1. The following are important characteristics to design around:

- Continuous drain current (I_D)
- Maximum drain-to-source voltage ($V_{DS(MAX)}$)
- Gate-to-source threshold voltage ($V_{GS(TH)}$)
- Drain-to-source on resistance ($RDS_{(ON)}$)

The rate for I_D must exceed the load current, which is 3 A ($I_D > I_{LOAD}$) in this system, and the body diode maximum current $I_S \geq I_D$. The gate-to-source threshold voltage must also be $V_{GS(TH)} \leq 3$ V. The NFET outlined in 表 2 has been selected for this application.

表 **2. TVS Diode Parameters**

PARAMETER	COMMENTS	MIN	TYP	MAX	UNIT
D1 SMBJ28A					
VRWM	Reverse standoff voltage	—	28.0	—	V
VC	Clamping voltage	—	—	45.4	V
VBR	Breakdown voltage	31.1	—	35.8	V
D2 SMBJ14A					
VRWM	Reverse standoff voltage	—	14.0	—	V
VC	Clamping voltage	—	—	23.2	V
VBR	Breakdown voltage	15.6	—	17.9	V

The diode breakdown voltages must be chosen such that transients are clamped at the voltages that protect the MOSFET and the remainder of the system. In the previous 图 13, the positive clamping diode D1 clamps above the double battery (jump-start) and clamped load dump voltages, but lower than the maximum operating voltage of the downstream devices. In this case, the positive clamping diode starts to clamp around 28 V, but has a maximum clamp voltage just below 40 V (ideally, somewhere around 36 V), which is why D1 was chosen for its maximum clamping voltage.

The reverse clamping diode D2 should clamp all negative voltages greater than the battery voltage so that it does not short out during a reverse-battery condition. Because the battery voltage is likely to be 14 V, D2 is selected to block all negative voltages greater than this voltage.

The particular package used is SMBJ, which supports 600-W peak power levels, in regards to the power levels for transient-voltage-suppression (TVS) diodes. This package is sufficient for ISO 7637-2 pulses and suppressed load dump case (ISO-16750-2 pulse B). Unsuppressed load dumps (ISO-16750-2 pulse A) may require higher-power TVS diodes such as SMCJ or SMDJ. For more information about designing the TVS diodes for this application, see *LM74610-Q1 Zero IQ Reverse Polarity Protection Smart Diode Controller* (SNOSCZ1) .

2.3.3.2 LC Filter and Output Capacitors

After the LM74610 setup, an LC filter is used for two main functions:

1. Prevent EMI
2. Prevent high-frequency voltage on the power line from passing through to the power supply of the regulator

For EMI filter designs, determining the attenuation and appropriate cutoff frequency is important to properly calculate the capacitor and inductor values. For further clarification, see *AN-2162 Simple Success With Conducted EMI From DC-DC Converters* (SNVA489).

The regulator is switching at 400 kHz; therefore, TI recommends to set the cutoff frequency to be approximately 1/10 f_{SW}. The cutoff frequency is set as follows in 公式 1:

$$f_C = 400\ \text{kHz} = \frac{1}{\left(2\pi\sqrt{L_C}\right)} \quad (1)$$

Common values are chosen for C3 and LF1 (10 µF and 8.2 nH, respectively). 图 14 shows the resulting filter.

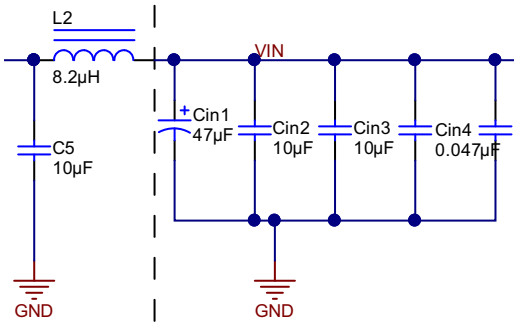


图 14. Input LC Filter

2.3.4 Power Supply

The LMS3635 is selected for its optimization for automotive applications. The LM53635 meets many of the requirements for automotive applications, such as:

- Wide V_{IN} operation with transient tolerance up to 42 V
- Wettable flanks
- Spread spectrum
- Switching frequency outside AM band (400 kHz)
- Low EMI and switch noise
- External frequency synchronization
- AEC-Q100 automotive qualified

The following 图 15 and 节 2.3.4.1 outline the design parameters used in the LMS3635-Q1 DC-DC.

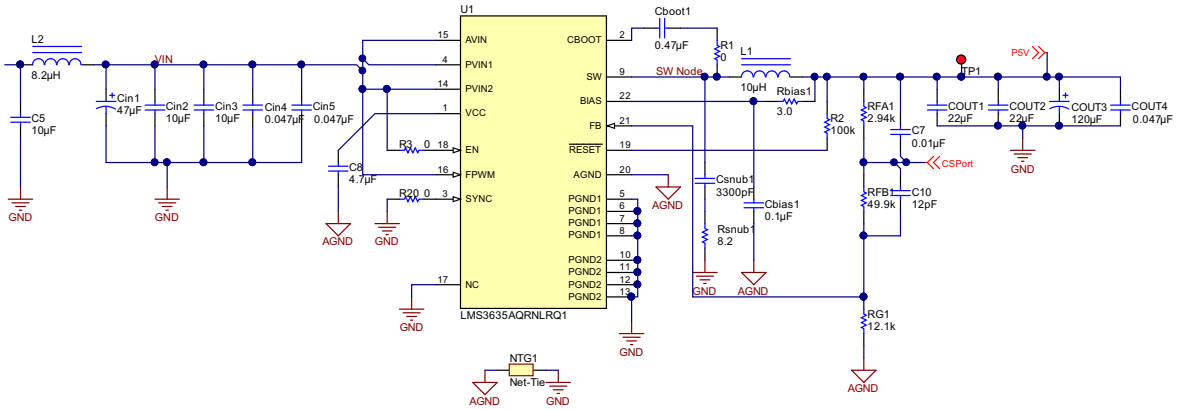


图 15. LMS3635-Q1 Wide V_{IN} DC-DC Converter Schematic

2.3.4.1 Input Capacitor

Ceramic capacitors are typically used at the input of a power supply because they provide a low-impedance source to the regulator in addition to supplying ripple current and isolating switching noise from other circuits. Because the input of the regulator can detect voltages up to 40 V, the rating of the capacitors must accommodate these voltages (see 表 3). Consequently, a bulk capacitor of 47 µF is used to meet the necessary input capacitance for ripple current and switching noise isolation. In addition, small high-frequency bypass capacitors connected directly between the VIN and PGND pins are used to reduce noise spikes and help to reduce conducted EMI. Additional high-frequency capacitors can be used to help manage conducted EMI or voltage spike issues that may be encountered.

表 **3. Input Capacitor Selection**

NOMINAL CAPACITANCE	VOLTAGE RATING	ESR	PART NUMBER
47 uF	63 V	650 mΩ	667-EEE-FK1J470P
Two 10 uF	50 V	1 mΩ	GRM32ER71H106KA2L
Two 0.047 uF	50 V	1 mΩ	GRM188R71H473KA61D

The input capacitors must be able to handle both the RMS current $I_{RMS(CIN)}$ and the dissipated power $P_{D(CIN)}$. The input capacitors are picked for bulk capacitance $I_{RMS(CIN)}$ and $P_{D(CIN)}$. TI recommends to use X5R, X7R, or a comparable material to maintain proper tolerances over voltage and temperature. The device requires a minimum of 22 µF on PVIN1 and 10 µF on PVIN2.

2.3.4.2 DC-DC Inductor Selection

LM53625/35-Q1, 2.5-A or 3.5-A, 36-V Synchronous, 2.1-MHz, Step-Down DC-DC Converter (SNVSAA7) provides recommendations for selecting the DC-DC inductor. The optimal inductance for the LMS3635-Q1 device at a 5-V output is 10 µH (see 表 4). An inductor with a saturation current of 4.9 A is chosen to balance size and performance.

表 **4. Inductor Selection**

NOMINAL INDUCTANCE	SATURATION CURRENT	DCR	PART NUMBER
10 uH	4.9 A	50 mΩ	XAL5050-103MEB

2.3.4.3 Output Capacitor Selection

The LMS3635-Q1 is optimized to work with low equivalent-series-resistance (ESR) ceramic capacitors such as X5R or X7R ceramic capacitors. The impedance of the capacitor can be dominated by capacitive, resistive, or inductive elements within the capacitor, depending on the frequency of the ripple current. Ceramic capacitors, however, have very low ESR, stay capacitive up to high frequencies, and the inductive component can usually be neglected. Ultimately, the capacitor helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and low enough ESR to perform these functions. A good practice is to target output peak-to-peak ripple voltage (VOUT_Ripple_PP) to be within ±5%; however, adding more output capacitance is a task for improving transient performance. Limiting the maximum value of total output capacitance between 600 µF and 800 µF is still important because a higher capacitance can disrupt the start-up of a regulator or the loop stability. 表 5 shows the values for the output capacitors.

表 5. Output Capacitor Selection

NOMINAL CAPACITANCE	VOLTAGE RATING	ESR	PART NUMBER
One 120 µF	10 V	25 mΩ	APXE100ARA121MF6
Two 22 µF	25 V	2 mΩ	GRM32ER61E226KE15
One 0.047 µF	25 V	1 mΩ	GCM188R71E473KA7D

2.3.4.4 Output Voltage and Cable Compensation

For the fixed-output voltage versions, the FB input is connected directly to the output voltage node, preferably near the top of the output capacitor. If the feedback point is located farther away from the output capacitors (that is, remote sensing), then a small 100-nF capacitor may be required at the sensing point.

The regulator selected for this design uses the adjustable version due to the requirement for cable compensation. When a load draws current through a long or thin wire, an I_R drop occurs that reduces the voltage delivered to the load. In the vehicle from the voltage regulator 5-V output to the VPD_IN (input voltage of portable device), the total resistance of the power switch RDS_{ON} and cable resistance causes an I_R drop at the portable device input. So the charging current of most portable devices is less than their expected maximum charging current. The TPS254900-Q1 device detects the load currents and sets a proportional sink current that can be used with the LMS3635-Q1 device. The gain G_{CS} of the sink current proportional to the load current is 75 µA/A.

The following calculations in 公式 2 and 公式 3 are used to design the feedback network on the LMS3635-Q1:

$$RG1 = V_{REF} \times \frac{RFB1}{Ouput\ Voltage - V_{REF}} \quad (2)$$

where,

- V_{REF} = 1 V.

$$RFA1 = \frac{(RDS_{ON} + RDS_{WIRE})}{G_{CS}} \quad (3)$$

where,

- RDS_{WIRE} is typically 80 mΩ/m to 120 mΩ/m and up to 3-m long,
- G_{CS} = 75 µA/A,
- RDS_{ON} is the ON resistance of the TPS254900-Q1.

For this design, assume that RDS_{WIRE} is 150 mΩ. RFB1 is chosen as 49.9 kΩ; therefore, RG1 = 12.5 kΩ (standard value 12.1 kΩ) and RFA1 = 2.4 kΩ (standard value 2.94 kΩ).

2.3.5 USB BC1.2 Controller

The TPS254900-Q1 was chosen for its optimization in automotive applications. The TPS254900-Q1 meets many of the requirements required for typical automotive applications such as:

- Support for VBUS D+, and D– short-to-battery protection
- Cable compensation

The operation of charging over the USB Type-C port circuit depends on the TPS254900 device to provide the electrical signatures on D+/D– to support USB BC1.2 CDP-compliant charging. 图 16 shows the schematic.

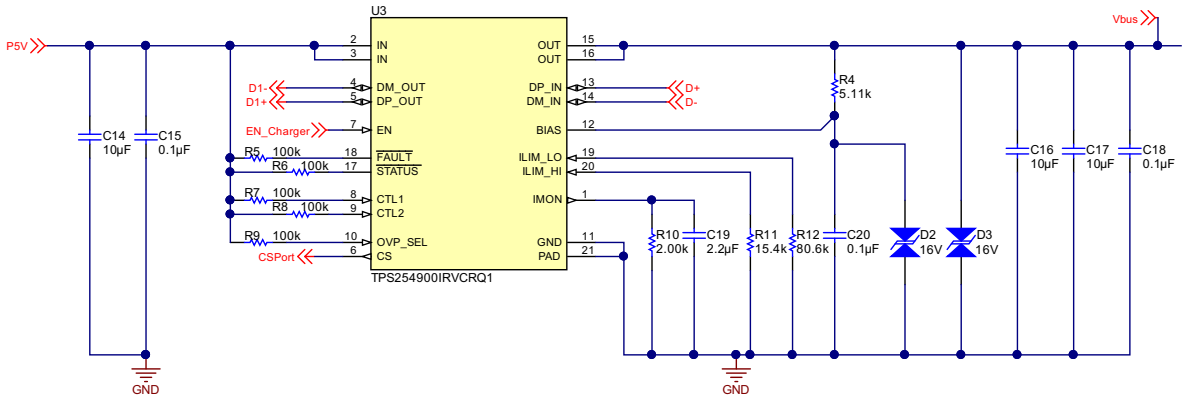


图 **16. TPS254900-Q1 Legacy USB BC1.2 Controller**

The internal switch of the TPS254900-Q1 is connected to the 5-V power source and the output powers VBUS. After connecting a device to the USB Type-C port, the enumeration occurs to either provide CDP or SDP charging.

A CDP port is a USB port that follows USB BC1.2 requirements and supplies a minimum of 1.5 A per port. CDP ports provide power and meet USB2.0 requirements for device enumeration. USB2.0 communication is supported and the host controller must be active to allow charging. What separates a CDP from an SDP is the host-charge handshaking logic that identifies this port as a CDP. A CDP is identifiable by a compliant BC1.2 client device and allows for additional current draw by the client device.

As shown in the previous 图 16, CTL1 and CTL2 are connected through R7 and R8 for the configuration of SDP, SDP1, or CDP mode. See the following 表 6 for the configurations.

表 **6. Control Pin Configurations**

CTL1	CTL2	MODE	FAULT REPORT	NOTES
0	0	Client	OFF	Power switch is disabled, only the analog switch is on
0	1	SDP	ON	Standard SDP
1	0	SDP1	ON	No OUT discharge between CDP and SDP1 for port power management (PPM)
1	1	CDP	ON	No OUT discharge when changing between 10 or 11

2.3.6 USB Type-C™ CC Negotiator

The TUSB319-Q1 has been chosen because it supports USB Type-C along with legacy USB BC1.2 charging. The TUSB319-Q1 supports:

- USB Type-C compliant DFP control
- Up to 3-A current advertisement on CC lines
- V_{BUS} detection for ease-of-use with legacy charging and USB power switch

图 17 shows a schematic of the TUSB319 USB Type-C port controller.

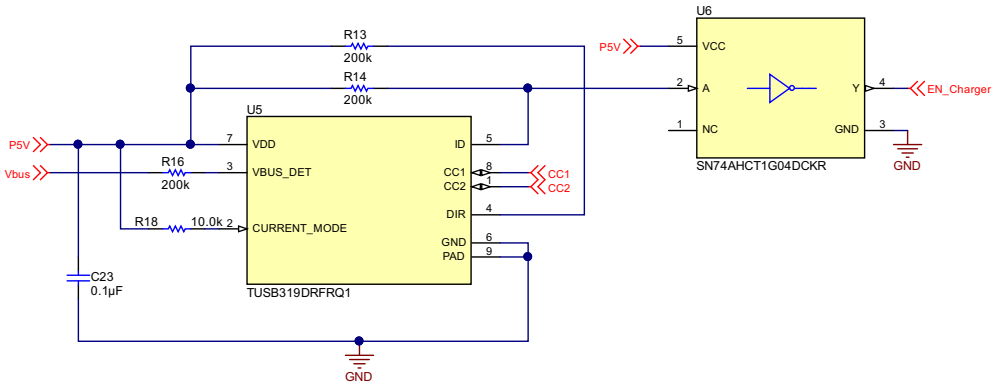


图 17. USB Type-C™ Port Controller

Three settings are available for advertising the current on the CC lines that can be determined by setting the CURRENT_MODE pin to low, medium, or high (advertising 500 mA/900 mA, 1.5 A, or 3 A, respectively). This design is set to 3 A using a 10-kΩ resistor pulled high. Use a 500-kΩ resistor to set the CURRENT_MODE to 1.5 A. Tie the pin to GND or leave it disconnected for 500 mA/900 mA, which is USB2.0 versus USB3.0.

VBUS detection uses a connection through a large resistor to detect whether or not VBUS < 800 mV. Use a large resistor to protect against voltages that the TUSB319 device is not capable of withstanding. When VBUS_DET falls below the VBUS threshold, the ID pin asserts low.

The ID pin establishes active mode, which communicates to the system that the USB port has been attached. This pin activates the TPS254900-Q1 device after detecting that a USB Type-C plug has been connected. An inverter is required because the ID pin is active low and the enable pin of the TPS25490-Q1 is active high.

The DIR pin advertises the plug orientation and asserts high if the plug is in position 2 (pins B1 through B12) or low if the plug inserted is in position 1 (pins A1 through A12).

2.3.7 Data Signal Redriver

Signal quality is the main driving factor for this design. Use of the TUSB213 redriver is sufficient because it is designed to compensate for signal loss without altering signal characteristics. Additionally, the TUSB213 is also designed to be compatible with USB OTG specifications.

图 18 shows a schematic of the TUSB213 USB2.0 redriver.

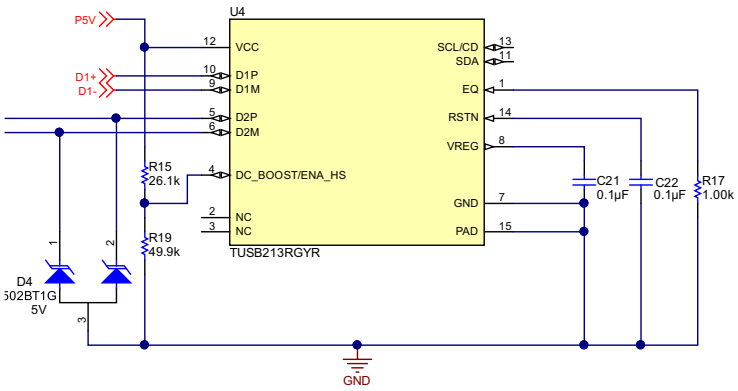


图 **18. TUSB213 Redriver**

Configure the TUSB213 device in multiple ways for the ideal signal enhancement. The two main features include the equalizer, or EQ (see 表 7), and DC boost (see 表 8).

表 **7. Equalizer Settings**

PARAMETER	EQ0	EQ1	EQ2	EQ3
Resistor value	160 Ω	1.7 kΩ	3.8 kΩ	6 kΩ

表 **8. DC Boost Settings**

PARAMETER	V (MINIMUM)	V (MAXIMUM)
Low	0 V	0.4 V
Mid	1.6 V	—
High	2.4 V	3.6 V

The DC_Boost feature is not 5-V tolerant, so a voltage divider is required when pulling the boost high.

If the source is 5 V, the ratio of R2 / (R2 + R1) for low = 0.02, mid = 0.32, and high = 0.62. A 49.9-kΩ resistor is used for R19; the high-boost R15 = 26.1-kΩ, the mid-boost R15 = 107-kΩ, and the low-boost R15 was disconnected with R19 grounded. Only by asserting the RSTN pin can both DC Boost and EQ be disabled; they cannot be disabled independently.

A 0.1 uF is required to stabilize the internal LDO and for a clean power reset (respectively) for both the VREG and RST pins.

Another function of this device is the I^2C mode for device configuration, status readback, and test purposes. Pin-strapping is used in this reference design in the place of I^2C mode.

TVS diodes are also placed on the D+ and D– lines for protection and voltage limiting.

3 Getting Started

The hardware setup is a straightforward process:

1. Connect J1 pins 1 and 3 to a host. This reference design uses a RosebergerHSD® for the data connection to a host.

   A host is required to be able to charge legacy devices in CDP mode; otherwise, these legacy devices revert to SDP mode and only draw 500 mA or 900 mA depending on the USB2.0 or USB3.0 connection. Note that devices, such as an Apple® iPhone®, do not charge unless they are in CDP mode because of minimum current draw requirements. A Type-C-to-Type-C connection does not require a connection to a USB host.
2. Connect the preferred power supply. The input voltage can be 5.5 V to 36 V and must be capable of up to 3.0 A. Connect J1 pins P1 and P2 to the approximate 12 V and ground, respectively.
3. Connect the UFP, which can be done using one of the two following options:
   a. USB Type-C to USB Type-C connector
   b. USB Type-C connector to the legacy USB cable (USB Type-A or Type-B)

图 19 shows a photo of the typical TIDA-01432 hardware setup.

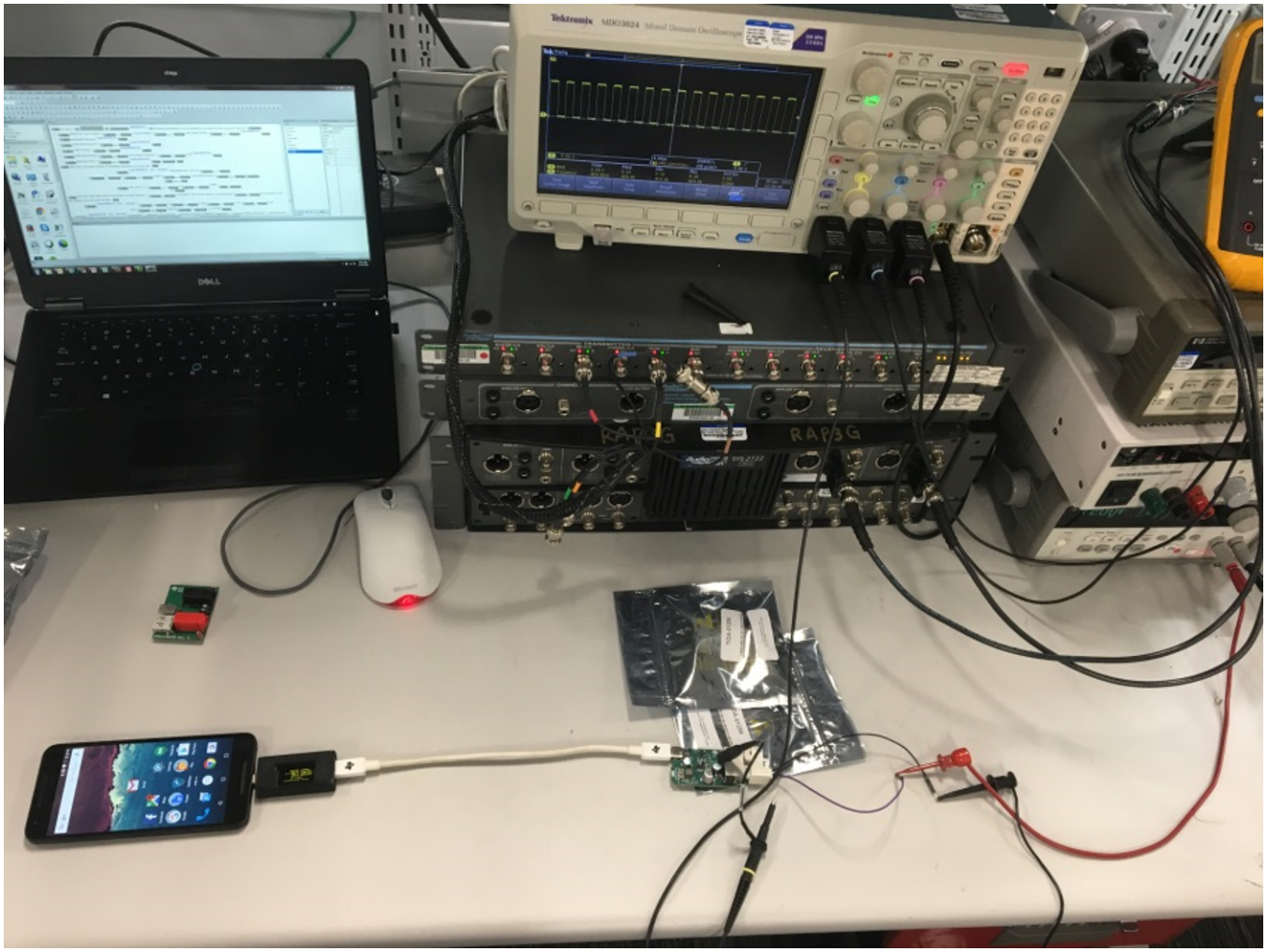


图 19. Typical TIDA-01432 Hardware Setup

4 Layout Recommendations

The TIDA-01432 PCB is a four-layer board:

- The top layer is composed of signals, power, and components.
- The second layer is a GND plane.
- The third layer is a power layer and signal layer.
- The bottom layer is composed of signals, power, and components.

This reference design diligently follows the recommendations specified in the respective data sheets for most of the components, aside from a few slight deviations to optimize for EMI and size constraints. The top and bottom layers are fully filled with copper (ideally) for thermal performance. The second layer is a ground layer to prevent high-speed traces from coupling. The third layer is used to route 5-V input power rails. For a layout guide, see the recommendations for individual components in the following subsections and their respective data sheets.

4.1 Reverse Battery Protection

For the reverse battery protection (see 图 20), the input capacitors are placed on the front of the board while the diode D1 is placed on the bottom of the board to save space. Take care to keep these components close to the input connectors of the board. The input to the LM74610 device passes through the TVS diodes to pin 4 and the anode of Q1. To make routing easier, Q1 is placed below the LM74610 device so that the gate drive and gate pulldown of Q1 and VCAPH/VCAPL can be routed directly underneath the part. The output at the cathode of Q1 goes directly to the LC filter. For additional EMI protection, a common-mode choke can be used with the pi filter to reduce high-frequency EMI.

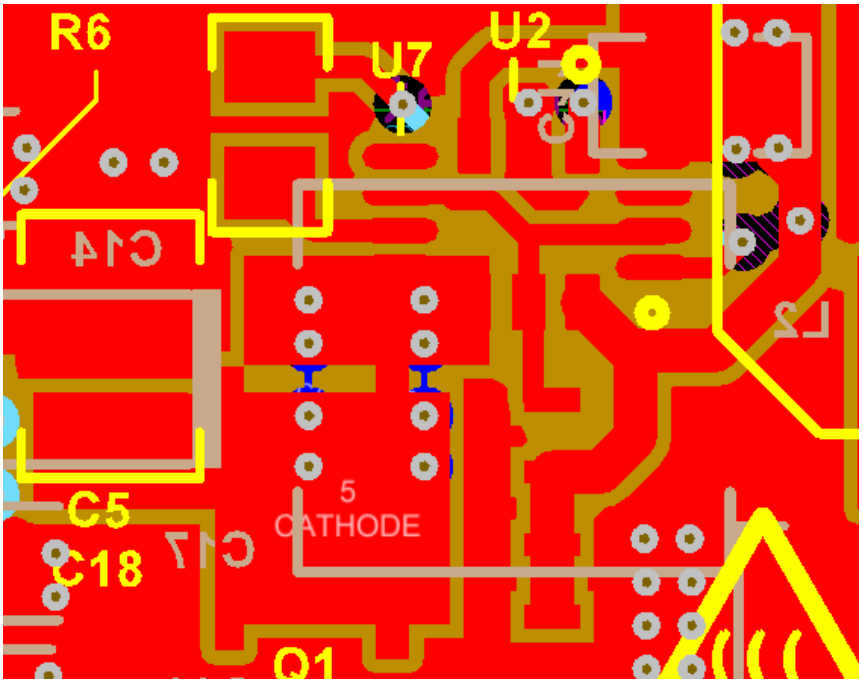
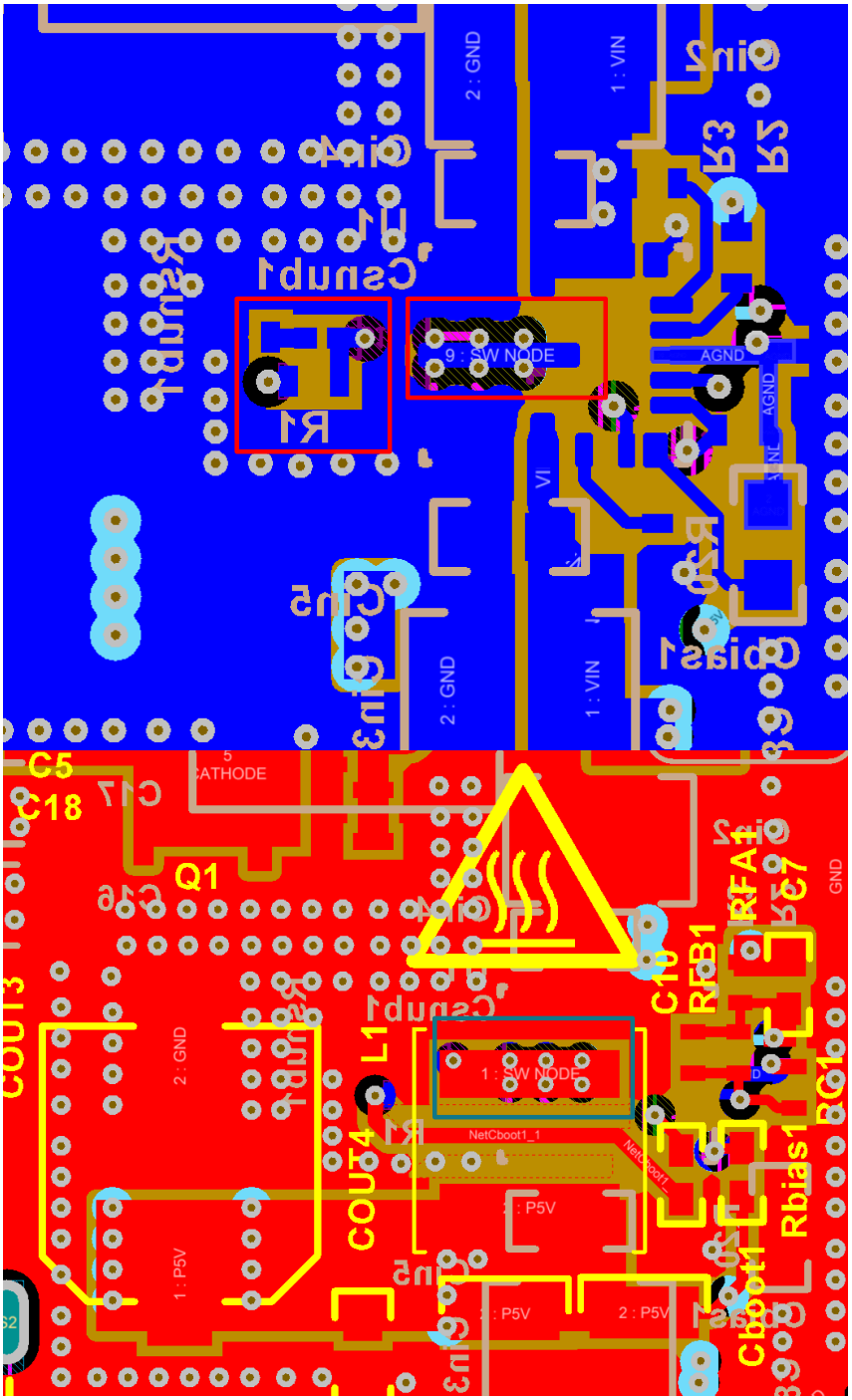


图 **20. Reverse Battery Protection Layout**

4.2 Power Supply

Although this component is optimal for EMI performance, carefully consider using the LM53635 device to reduce EMI. See the data sheet for the LM53635-Q1 *LM53625/35-Q1, 2.5-A or 3.5-A, 36-V Synchronous, 2.1-MHz, Step-Down DC-DC Converter* (SNVSAA7) to follow the direct recommendations for this particular part. The following instructions highlight a few deviations from the data sheet recommendation that pertain specifically to this TI Design.



Note: The switch node is connected on the top and bottom of the board to minimize EMI and couple the thermals between the IC and inductor. A snubber and tuning resistor are also added.

图 **21. LMS3635-Q1 Layout**

4.2.1 General Power Layout Recommendations

Consider the following recommendations for the general power layout:

1. The solid copper plane below the input capacitors ensures a solid connection between the GNDs on both sides of the regulator. Ultimately, the placement of this copper plane is to reduce parasitic loop inductance and thus minimize switch node ringing, reduce EMI, and help with power dissipation.
2. Flood the GND surrounding the switch node to isolate the switch node from coupling into surrounding pins.
3. Place vias on the inside of the input and output capacitors to help lower parasitics.

WARNING

The TIDA-01432 may become hot during operation due to dissipation of heat. Avoid contact with the inductor and ICs. Follow all applicable safety procedures applicable to the operating space.

4.2.2 Layout Recommendations for Specific Discreet Power Components

Consider the following layout recommendations for the specific discreet power components:

1. Input capacitors: The parasitic input inductance is halved because the IC has symmetric inputs. Maximize this performance by placing two matching input capacitors as close to the input pins as possible. The larger input capacitors are also placed close to the board edge, which helps to physically shield the power IC from additional EMI.
2. Inductor: An important rule when designing any power supply is to keep the switch node as small as possible and away from any feedback resistors that may be susceptible to the switching. This design uses a unique technique which consists of placing the inductor on the opposite side of the board directly underneath the IC. This technique allows:
    1. The board size to remain small
    2. The switch node to remain compact
    3. The thermals to couple from the IC to the inductor

    Additionally, the CBOOT is placed close to the inductor on the top side of the board with a 3-Ω to 10-Ω resistor placed in series with the CBOOT to tune the rise time of the switching and reduce EMI.
3. Output capacitors: Place capacitors on both sides of the board and as close to the inductor as possible to save space.
4. Add a snubber network on the bottom side of the board from the switch node to the ground to help minimize switch ringing.

4.3 Legacy Charge Controller

See the data sheet to follow the direct recommendations for the TPS254900-Q1 device. The following instructions highlight a few deviations made from the data sheet recommendation that pertain specifically to this TI Design. Many of the surrounding components are simply configuration passives; making close, compact placements between these components and the TPS254900-Q1 device is crucial.

图 22 shows a layout image of the legacy charge controller.

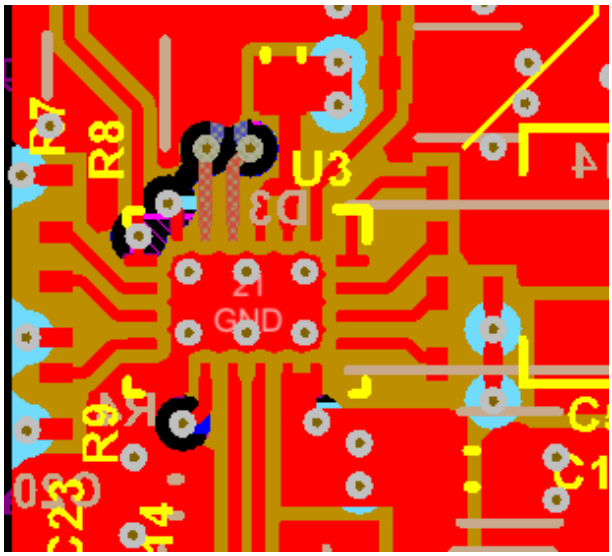


图 **22. Legacy Charge Controller Layout**

4.4 USB Type-C™ Controller

See the data sheet for the TUSB319-Q1 *TUSB319-Q1 USB Type-C DFP Port Controller* (SLLSEV4) to follow the direct recommendations. The TUSB319-Q1 is placed close to the USB Type-C connector to maintain signal integrity for the CC control lines.

图 23 shows a layout image of the USB Type-C controller.

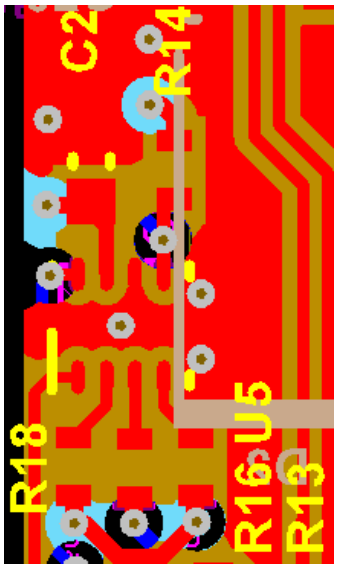


图 **23. USB Type-C™ Controller Layout**

4.5 USB Redriver and Signal Routing

One of the most important considerations for the layout of this component are the D+, D–, D1+, and D1– signals. The USB-IF standards for USB2.0, the Universal Serial Bus 2.0 specification, and data require that these lines must be 90-Ω differential pairs. Additionally, trace length matching is a concern so adding trace length is beneficial to maintaining signal integrity. Use a free online impedance calculator from Mantaro Product Development Services to calculate the differential micro-strip impedance, trace width, separation, and so forth. The signals for the D+/D– signal pair are differentially routed on the top layer to the TPS254900-Q1. From this location, the D1+/D1– pair are routed on the bottom layer to the TUSB213-Q1. From the TUSB213-Q1 location, the length is matched and routed differentially to the RosenbergerHSD connector. Pins 3 and 1 are D2+ and D2–, respectively, and must be connected to a head unit or other host in this configuration, accordingly.

图 24 shows a layout image of the USB redriver and signal routing.

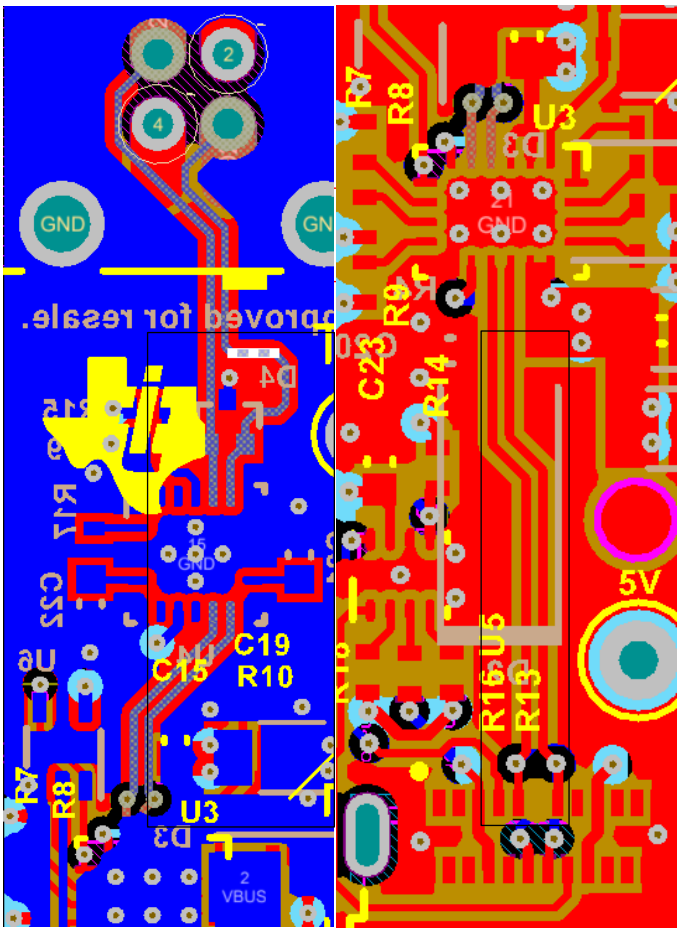


图 **24. USB Redriver and Signal Routing Layout**

5 Testing and Results

The following tests were conducted on the TIDA-01432 board to show the performance characteristics. 图 25 shows a photo of the typical test measurement setup.

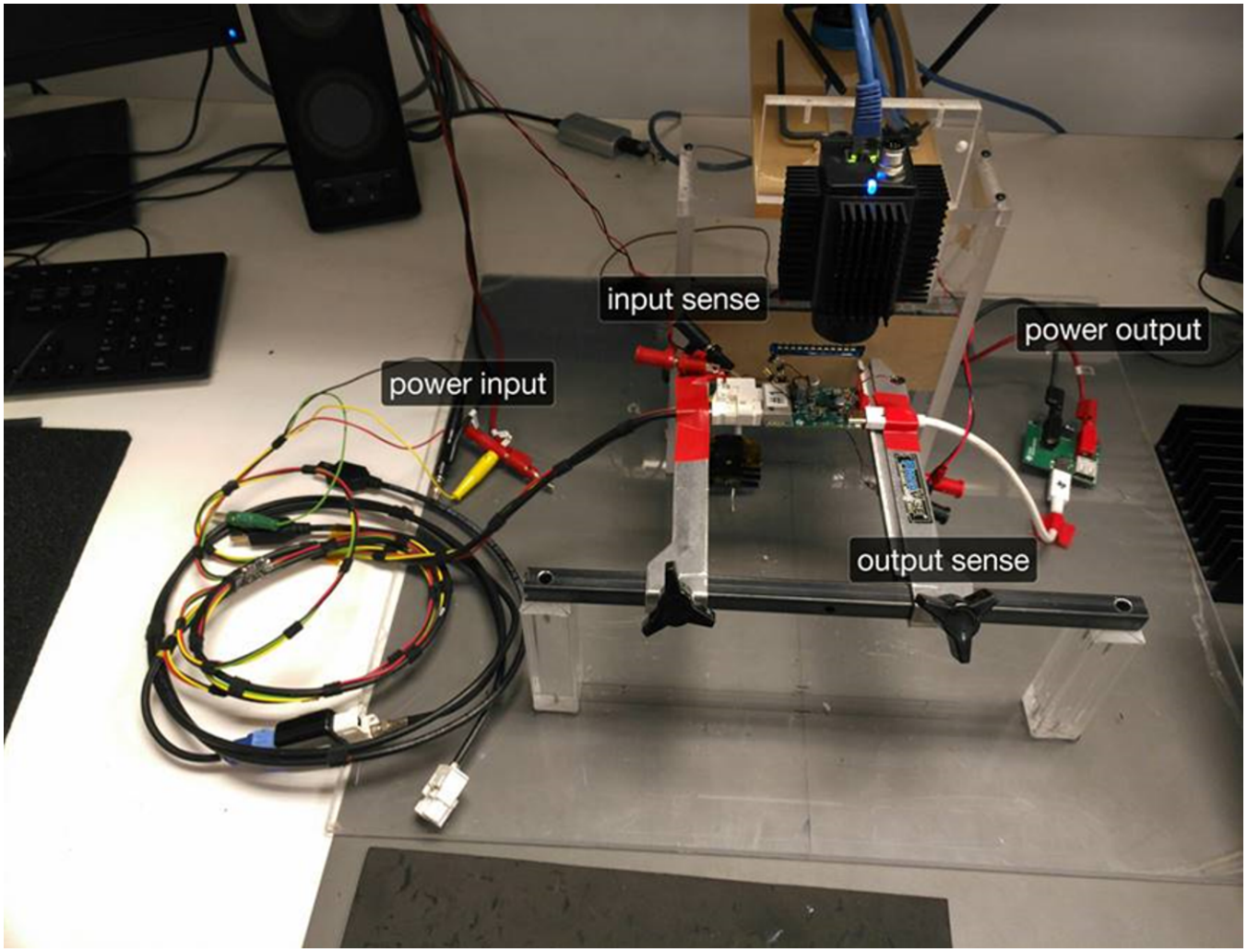


图 **25. TIDA-01432—Typical Test Measurement Setup**

5.1 Power Supply

The following subsections outline the tests conducted on the power supply to analyze the performance of the LMS3635-Q1.

5.1.1 Start-Up

As the following 图 26 and 图 27 show, the start-up was measured at C13 for V_{IN} (green), the USB 5 V at C16 (yellow), and the LMS3635 at COUT3 (blue). These measurements were taken with a resistive load for I_{OUT} = 0 A and I_{OUT} = 3 A.

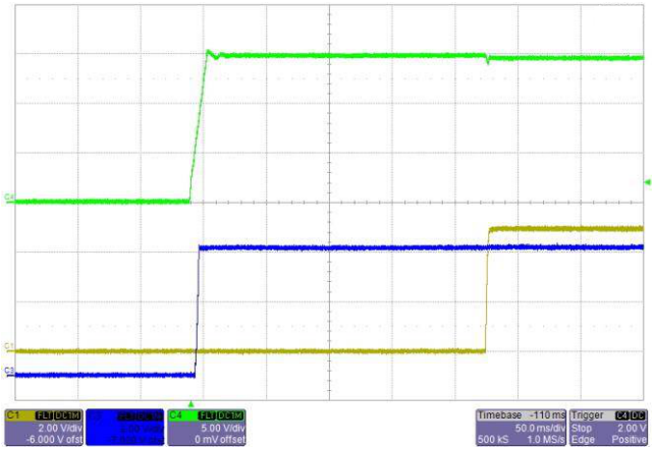


图 26. V_{IN} = 14.5 V (Green), LMS3635 5 V_{OUT} (Blue), USB 5 V (Yellow)—Start-Up = 15 ms at I_{OUT} = 0 A

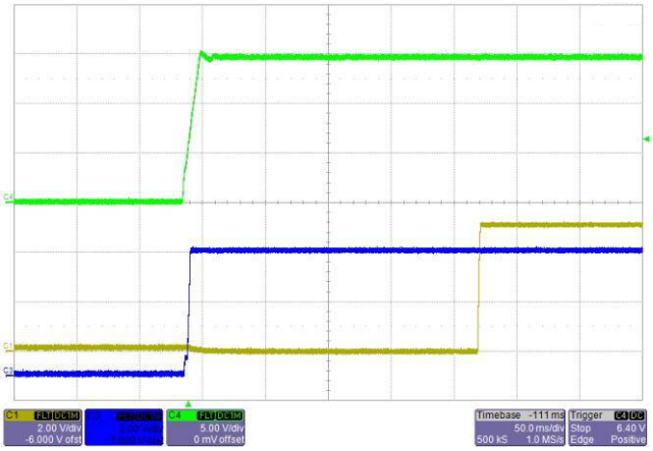


图 27. V_{IN} = 14.5 V (Green), LMS3635 5 V_{OUT} (Blue), USB 5 V (Yellow)—Start-Up = 10 ms at I_{OUT} = 3 A

5.1.2 Shutdown

As the following 图 28 and 图 29 show, the shutdown was measured at C13 for V_{IN} (green), the USB 5 V at C16 (yellow), and the LMS3635 at COUT3 (blue). Measurements were taken with a resistive load for I_{OUT} = 0 A and I_{OUT} = 3 A.

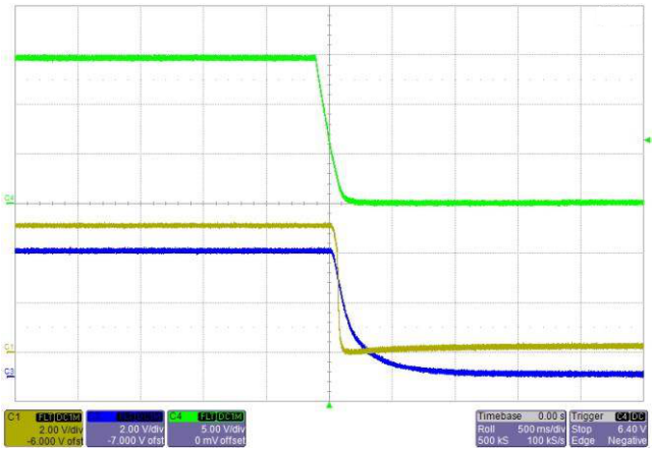


图 28. V_{IN} = 14.5 V (Green), LMS3635 5 V_{OUT} (Blue), USB 5 V (Yellow)—Shutdown = 150 ms at I_{OUT} = 0 A

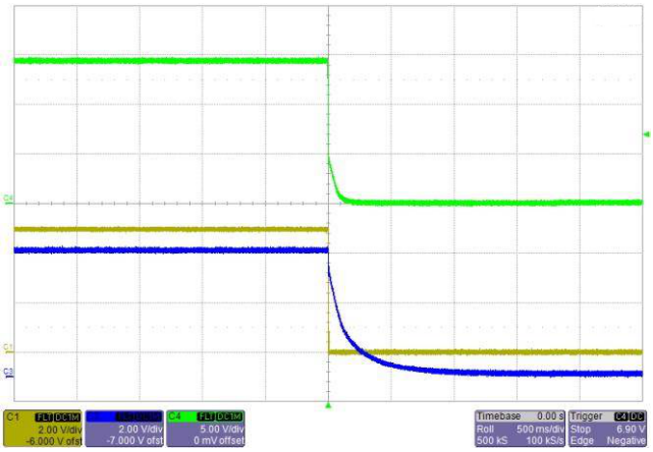


图 29. V_{IN} = 14.5 V (Green), LMS3635 5 V_{OUT} (Blue), USB 5 V (Yellow)—Shutdown = 50 ms at I_{OUT} = 3 A

5.1.3 Switch Node

As the following 图 30 and 图 31 show, the switch node was measured between R1 and GND. The regulator is set to a 400-kHz switching frequency and is confirmed in the test measurements. The switching frequency is clean with no ringing.

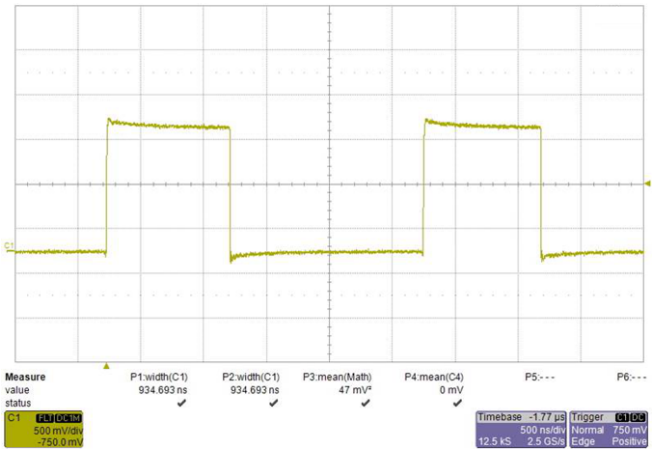


图 30. V_{IN} = 14.5 V, f_{SW} = 400 kHz (≈2500-ns Period)—No Load

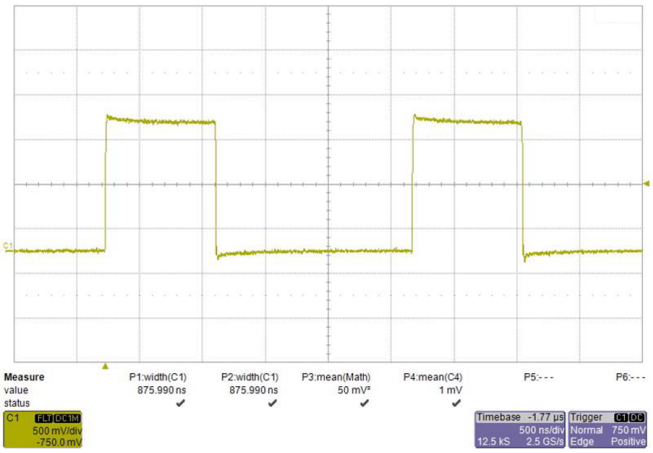


图 31. V_{IN} = 14.5 V, f_{SW} = 400 kHz (≈2500-ns Period)—3-A Load

5.1.4 Spread Spectrum

The following measurement in 图 32 was taken to show the spread spectrum feature of the LMS3635-Q1. The measurement point is between R1 and GND. The measurement triggers the signal on the rising edge in normal mode.

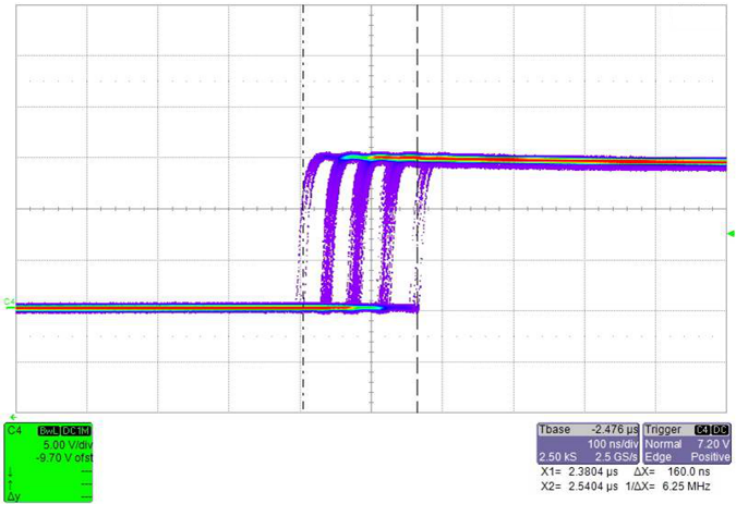


图 32. Spread Spectrum is ±3% of Switching Frequency

5.1.5 Transient Response

A probe was used with a short ground connection to avoid additional noise and increase measurement accuracy. The following 图 33 shows the load current versus the output voltage measurement (AC coupled).

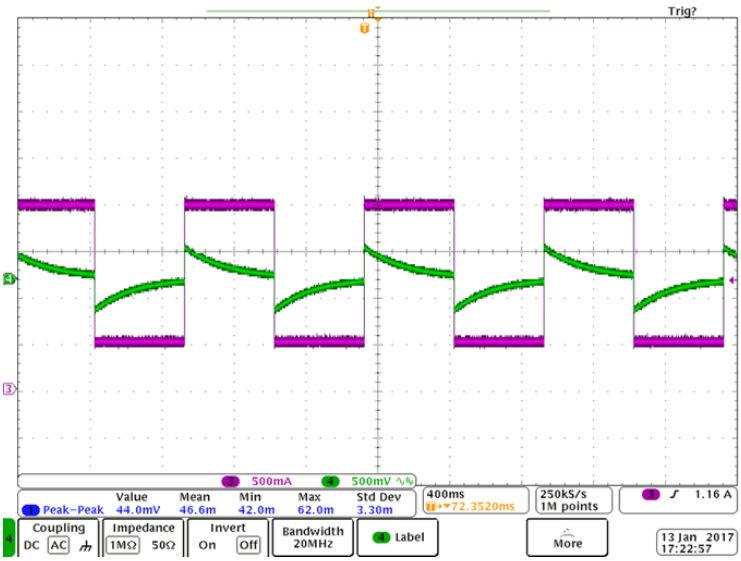


图 33. V_{IN} = 13.5 V, Load Step = 0.5 A to 2 A (Switching), Load Transient = 250 mV at LMS3635 V_{OUT} (COUT3)

5.1.6 Load Regulation

The purpose of measuring load regulation is to identify how the output voltage of the buck regulator responds to increases in load current. This design, however, uses cable compensation to overcome long cable lengths that affect the voltage on VBUS. Therefore, the load regulation measurement is affected by the cable compensation feature. The following 图 34 and 图 35 show the differences between load regulation of the board when cable compensation is enabled and disabled.

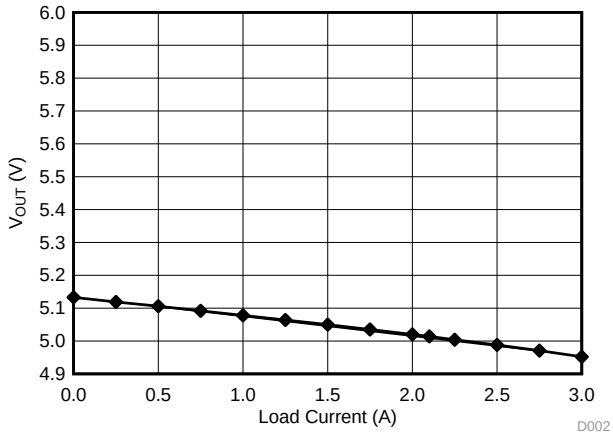


图 34. V_{IN} = 14.5 Measured at C13, USB V_{OUT} Measured at C16, Cable Compensation Disabled

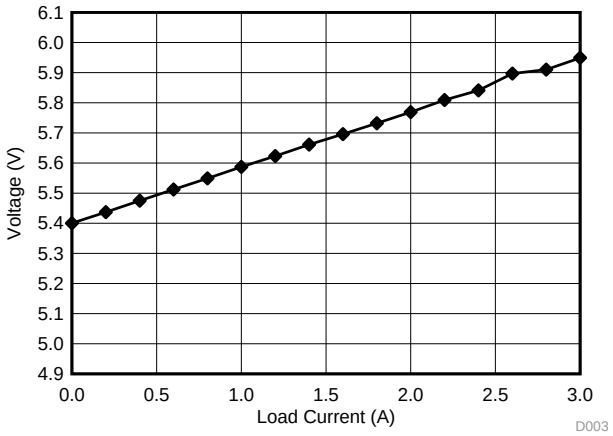


图 35. V_{IN} = 14.5 Measured at C13, USB V_{OUT} Measured at C16, Cable Compensation Enabled

5.1.7 Line Regulation

Line regulation shows the correlation of output voltage to input voltage. 图 36 shows both the output of the LMS3635-Q1 (measured at COUT3) and the TIDA-01432 (measured at C16). When 4.8 V < V_{IN} < 6 V, both output voltages begin to drop with the V_{IN}. For 3.5 V < V_{IN} < 4.8 V, then the USB output of the TIDA-01432 begins to shut down.

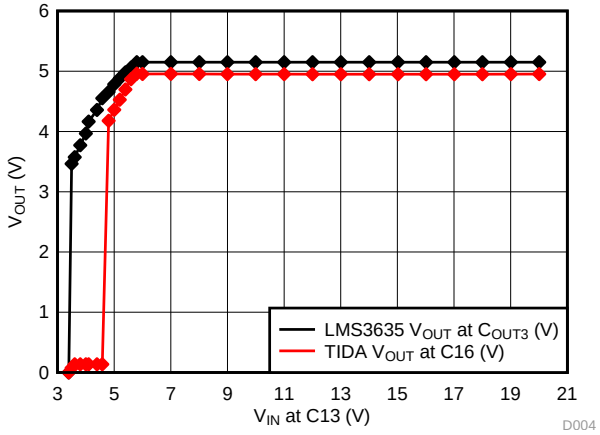


图 36. V_{IN} = 0 V to 20 V Measured at C13, 1.7-Ω Load

5.1.8 Input Voltage Ripple

The input voltage ripple was measured with a probe using a short ground connection across C13 (see 图 37 and 图 38). The input ripple is low (< 20 V_{PP}) due to placement of an LC filter at the input to mitigate EMI.

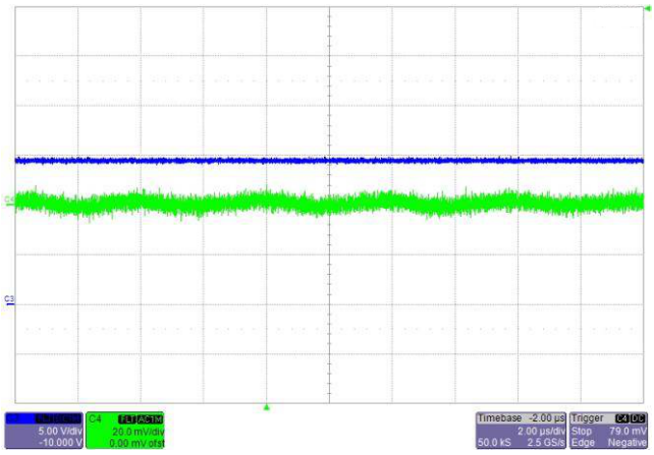


图 37. V_{IN} = 14.5 V Measured at C13 With No Load

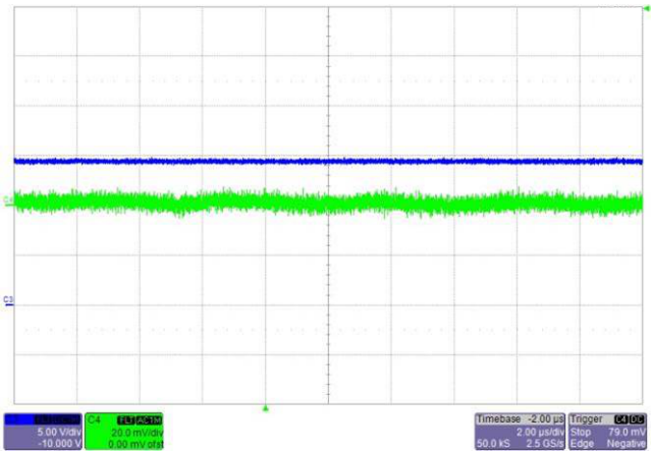


图 38. V_{IN} = 14.5 V Measured at C13 With 3-A Load

5.1.9 Output Voltage Ripple

The output voltage ripple was measured with a probe using a short ground connection across COUT3 (see 图 39 and 图 40). The output ripple was measured to be < 20 mV_{PP}, which is within the ±5% recommended for power regulators.

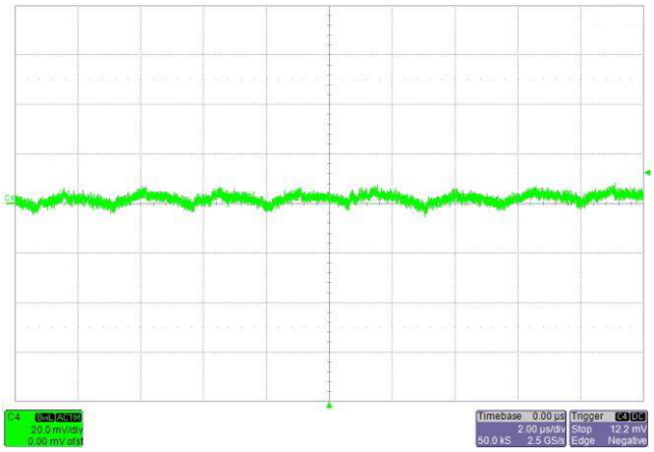


图 39. V_{IN} = 14.5-V Output Ripple Measured at COUT3 With No Load

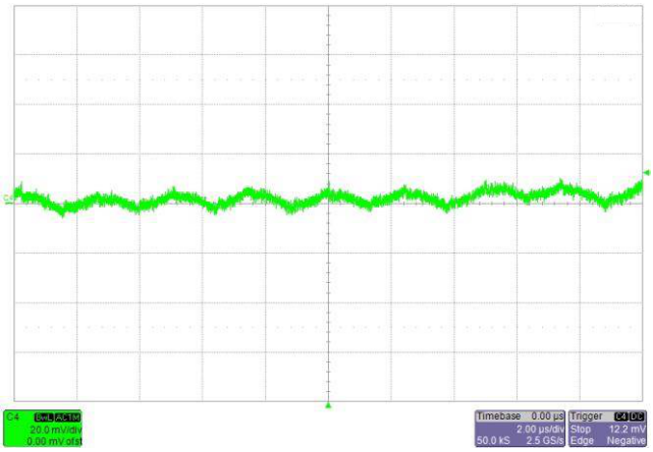


图 40. V_{IN} = 14.5-V Output Ripple Measured at COUT3 With 3-A Load

5.1.10 Efficiency

The following 图 41 and 图 42 show the overall efficiency of the design and the efficiency of the LMS3635-Q1 device. The overall efficiency should be lower than the LMS3635-Q1 because of the added USB power switch. The efficiency for the overall board performance is approximately 90% while the LMS3635-Q1 efficiency is greater than 90%, which is as expected.

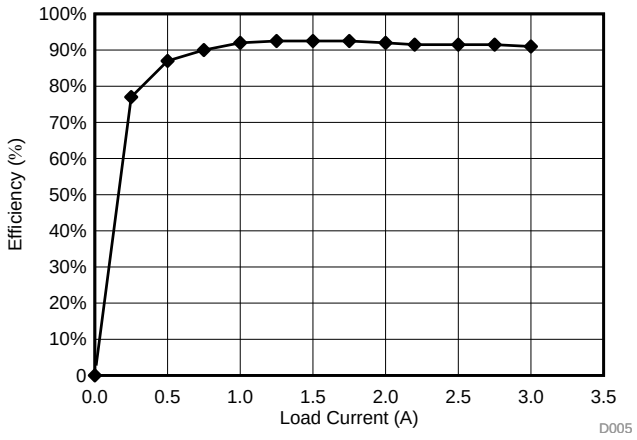


图 41. V_{IN} = 14.5 V Measured at C13 With TIDA-01432 Efficiency—Measured at COUT3

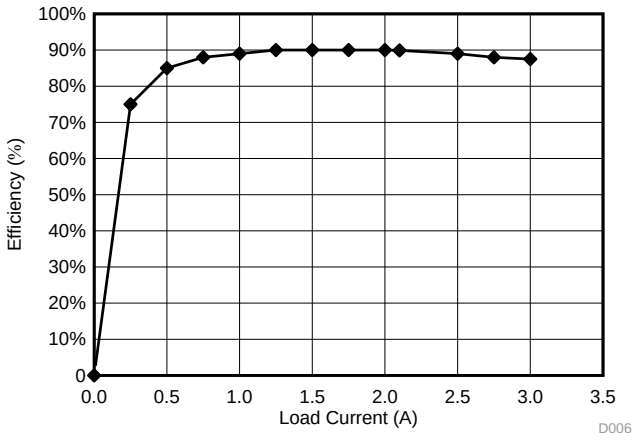


图 42. V_{IN} = 14.5 V Measured at C16 and LMS3635-Q1—Measured at COUT3

5.1.11 Thermal Performance

A good thermal performance is crucial because of the small surface area and placement sites of typical USB ports in automotive applications. The following 图 43 and 图 44 show the thermal measurements of this design. A FLIR AX5 thermal camera was used and the system was soaked at full load (3 A) at an ambient temperature of 25ºC for 20 min. The thermal images show both sides of the board, from which the user can observe that the temperature from the LMS3635-Q1 (77.4ºC) and output inductor (78.2ºC) are coupled very closely after 20 min.

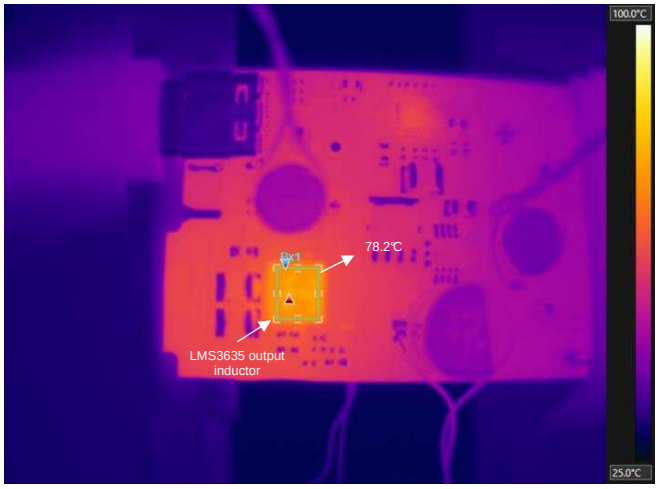


图 43. LMS3635-Q1 Output Inductor at 78.2ºC: V_{IN} = 14.5 V, I_{LOAD} = 3 A, Soak Time = 20 min, Ambient Temperature 25ºC

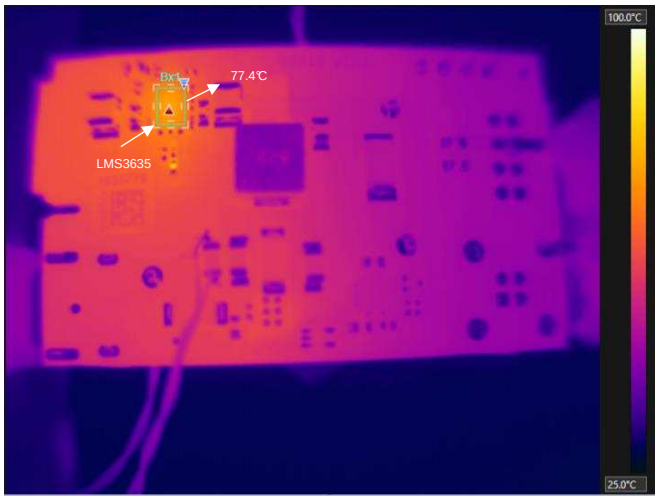


图 44. LMS3635-Q1 IC at 77.4ºC: V_{IN} = 14.5 V, I_{LOAD} = 3 A, Soak Time = 20 min, Ambient Temperature 25ºC

5.2 USB Data

The USB-IF Compliance Program provides product test requirements that designers must be able to meet before permitting the use of the USB-IF logo. See the compliance testing requirements at http://www.usb.org/developers/compliance/ and be sure to look for the instructions specified under SuperSpeed, High-Speed, and Low and Full-Speed. The following subsection outlines the tests performed for USB 2.0 standards.

5.2.1 USB Signal Integrity Measurements

The testing for the near-end signal integrity measurements use a laptop running an xHCI HSETT program. The following screenshots in 图 45 and 图 46 show the setup steps for designating the computer as a host, sending the test packets through the cable to the design, and recording the eye diagram on the oscilloscope.

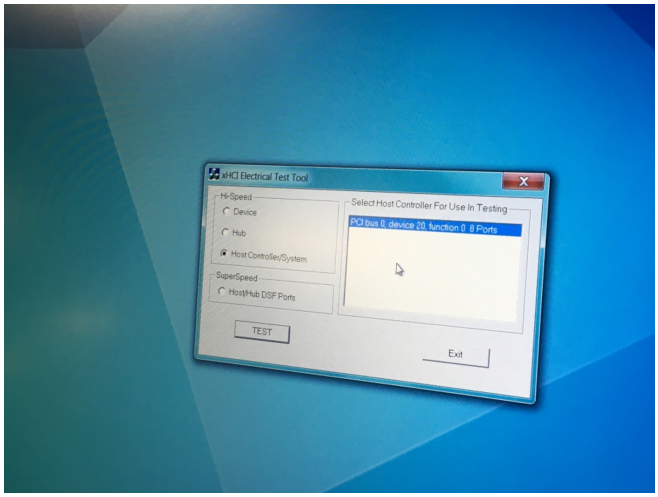


图 **45. xHCI HSETT Program Setup**

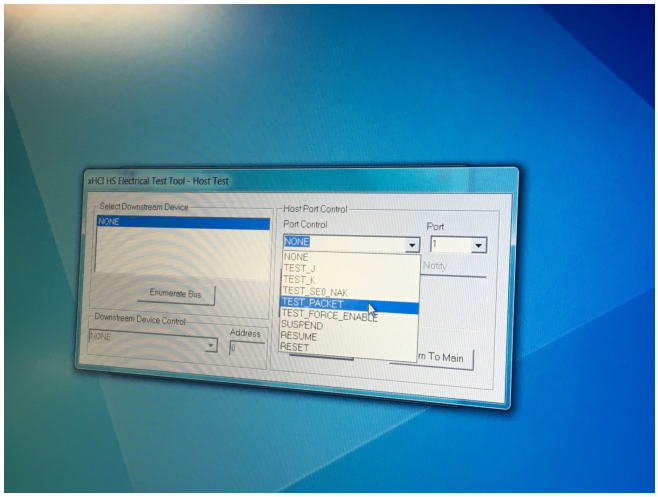


图 **46. Port Control Selection**

5.2.1.1 Near-End Procedure

The computer USB Host is connected in three different configurations: the USB Type-A to Rosenberger cable (measured at 1.9 m), an additional 1-m cable, and then an additional, approximate 2-m cable that is added to the original 1.9-m cable. The lengths range from approximately 1.9 m to 4 m. The signals that pass through these cables are measured at the output of the TIDA-01432 board using SMA-to-SMA connectors on a certified USB-IF test fixture. A USB Type-C to USB Type-A connector is used between the TIDA-01432 and USB-IF test fixture because the output of the TIDA-01432 is a USB Type-C connector. The following block diagram in 图 47 and the photo in 图 48 show the full test setup.

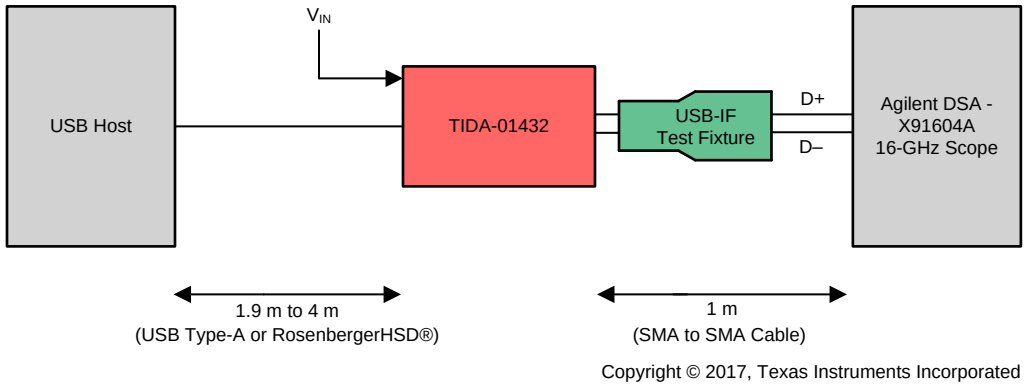


图 **47. Block Diagram of Near-End Test Setup**

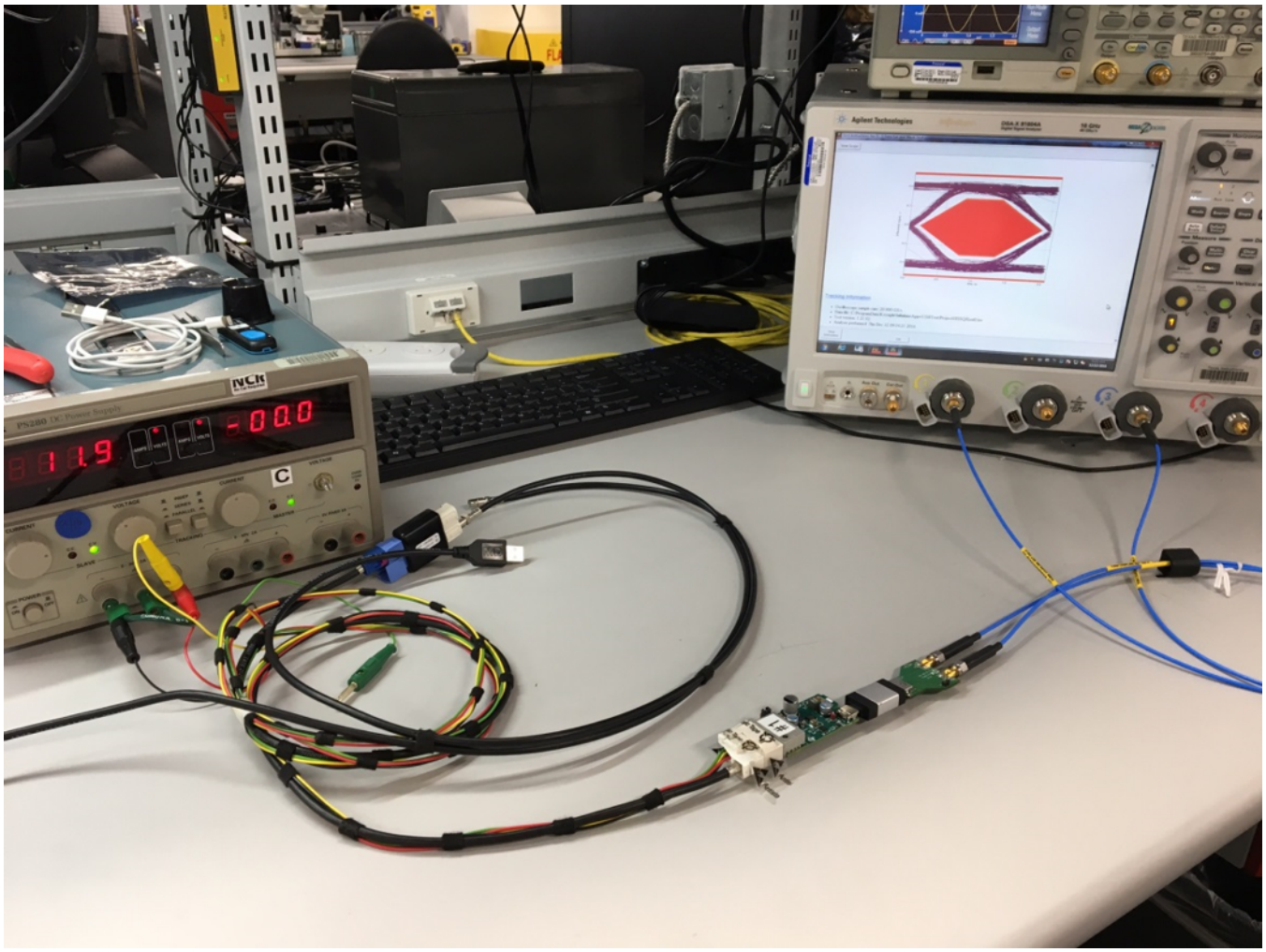


图 **48. Near-End Test Setup Photo**

5.2.1.2 Near-End Results

As previously mentioned, this reference design uses three different cable lengths which includes the various cables used in addition to the provided USB Type-A to Rosenberger cable. The following 表 9 lists the results of the USB IF near-end compliance in addition to the corresponding eye diagrams for a 2.9-m cable (see 图 49 and 图 50). The user may receive satisfactory eye diagram results for cable lengths longer than 3 m if using a single USB Type-A to Rosenberger cable and a decent quality junction connector

表 **9. Near-End Eye Diagram results**

STATUS	CABLE LENGTH	
	1.9 m	2.9 m
Redriver disabled	Pass	Fail (3129 dp)
Redriver enabled	Pass	Pass

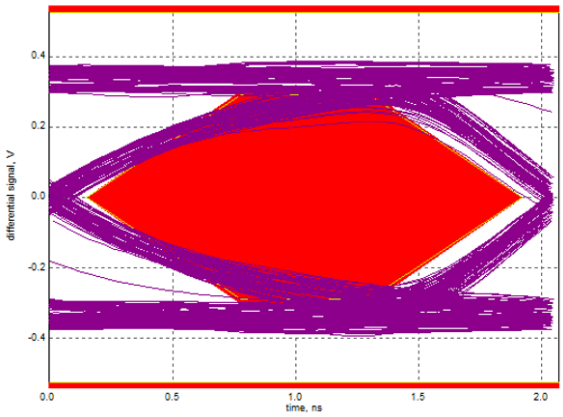


图 **49. Near-End USB-IF Test With TUSB213-Q1 Disabled**

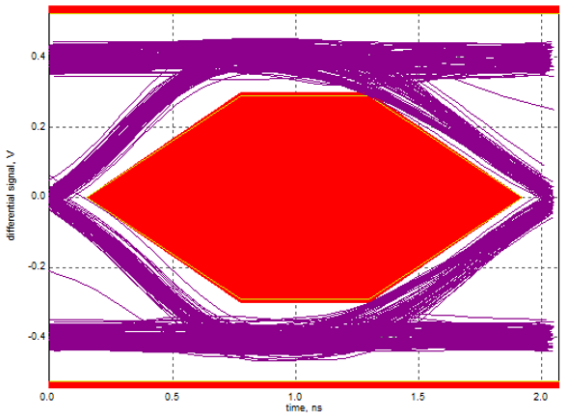


图 **50. Near-End USB-IF Test With TUSB213-Q1 Enabled**

5.2.1.3 Far-End Procedure

The computer USB host is connected to the USB-IF test fixture, which allows the USB host to use the attached device to send test packets back through the TIDA-01432 for measurement by the scope. The total amount of cable is 3.9 m. During testing, only one set of cables was used due to the lack of proper junction connectors to convert between cables. The block diagram in 图 51 and the photo in 图 52 show the test setup.

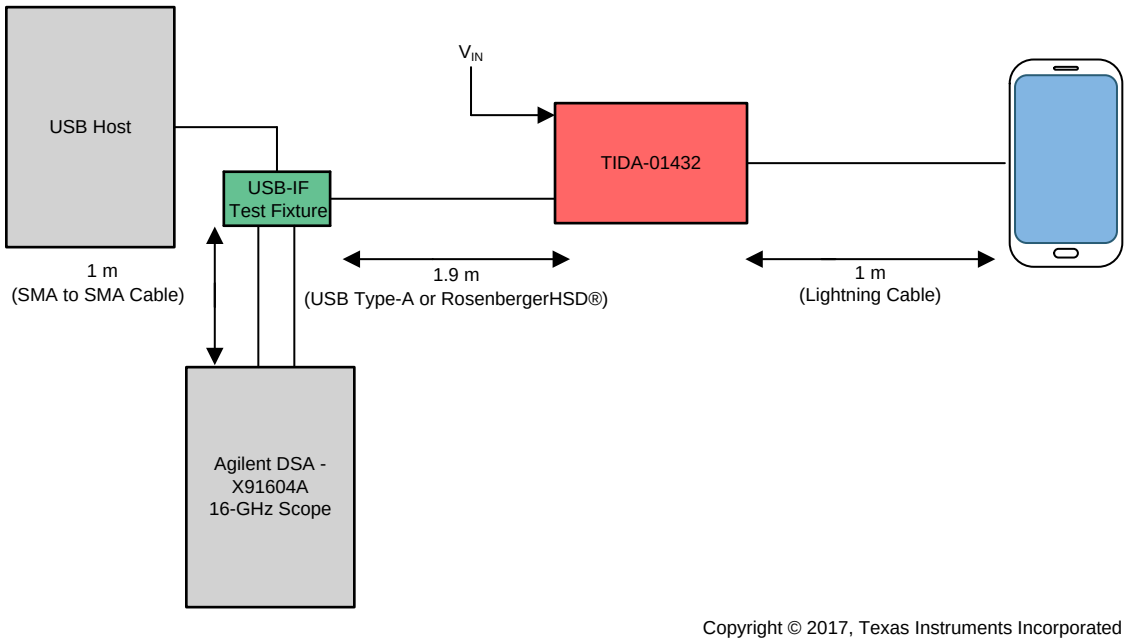


图 51. Block Diagram of Far-End Test Setup

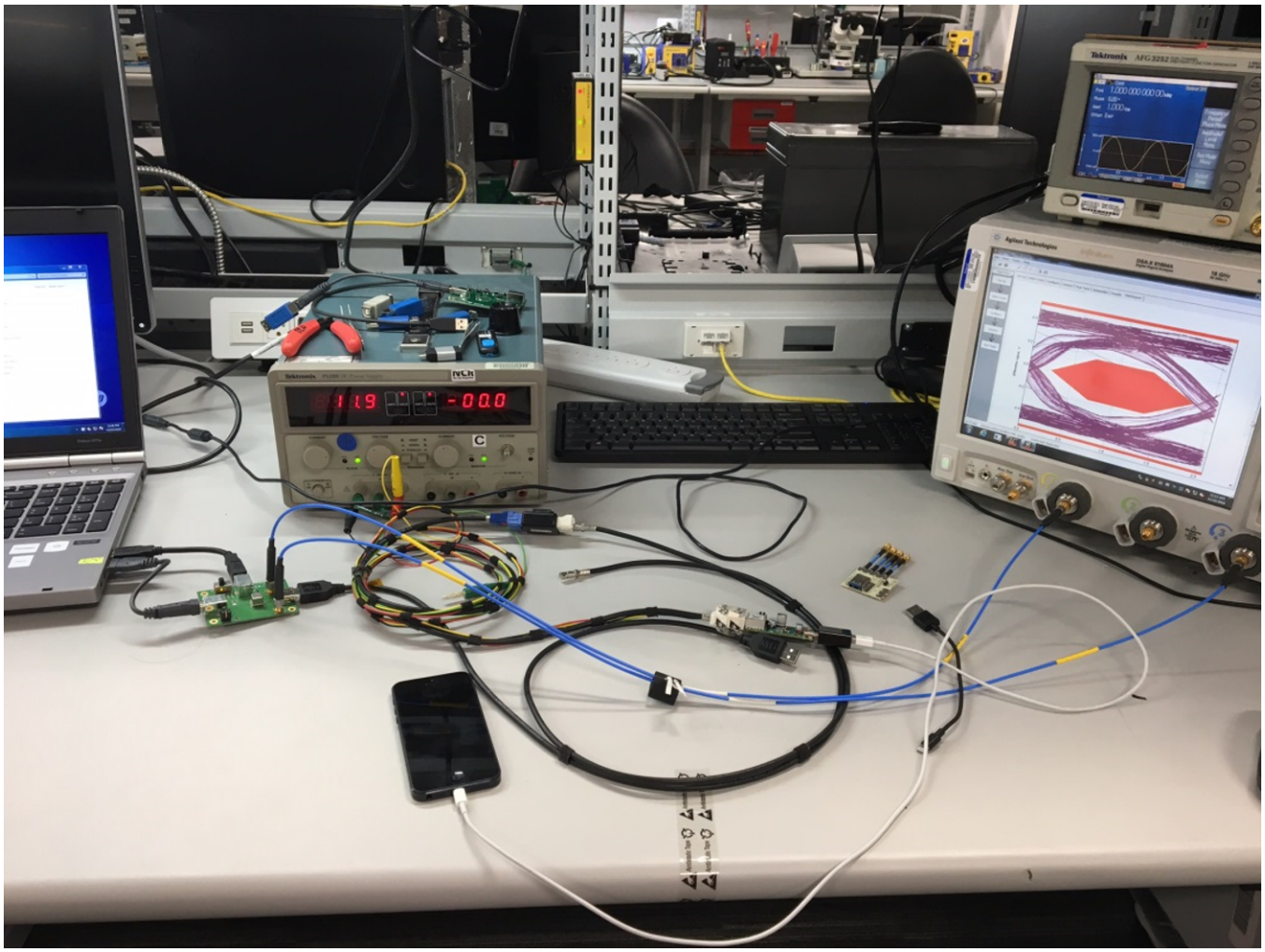


图 **52. Far-End Test Setup Photo**

5.2.1.4 Far-End Results

表 10 lists the results of the USB IF far-end compliance. These results are for the USB IF far-end compliance in addition to the corresponding eye diagram. All tests were performed using a standard 1-m lightning cable.

表 **10. Far-End Eye Diagram Results**

FAR END RESULTS	
Redriver disabled	Fail, 60 dp
Redriver enabled	Pass

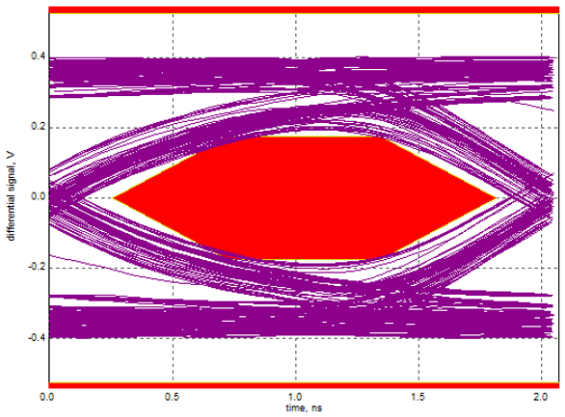


图 53. Far-End USB-IF Test With TUSB213-Q1 Disabled

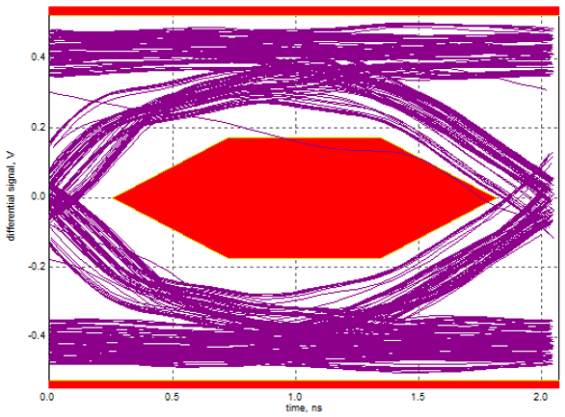


图 54. Far-End USB-IF Test With TUSB213-Q1 Enabled

5.3 CISPR 25 Class 5

This reference design has been built and tested with the goal to pass CISPR 25 class 5 standards, which is the strictest of the CISPR classification standards. This CISPR EMI testing was performed in an in-house lab following similar guidelines as the international standard "to protect on-board receivers from disturbances produced by conducted and radiate emissions arising in a vehicle" (CISPR). This reference design is tested in these settings and under these rigid guidelines to ensure that the board does not interfere with other equipment in the vehicle. As outlined in the standard, this test is performed to confirm that radiated disturbances do not disrupt the broadcast and mobile service or band. (1)

For this test, a 14.5-V power supply was used in conjunction with short cables to run the test using optimized performance. A 1.7-Ω resistive load was additionally used to emulate a similar load that USB devices draw. For further details about requirements and test setup in a third-party facility, see *CISPR 25 Class 5 USB Type-C ™ Port With USB3.0 Data Support Reference Design* (TIDUC55).

图 55 shows a photo of the CISPR 25 class 5 testing for the TIDA-01432 design.

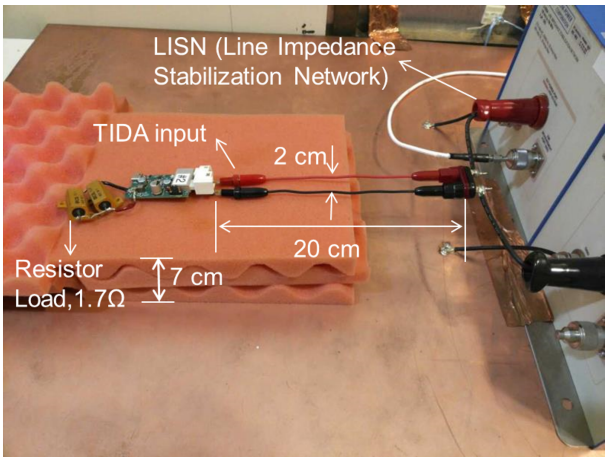


图 55. TIDA-01432 CISPR 25 Class 5 Testing

(1) CISPR 25 Ed. 3.0 b: 2008, *Corrigendum 1 - Vehicles, boats and internal combustion engines - Radio disturbance characteristics - Limits and methods of measurement for the protection of on-board receivers*

A standard procedure in EMI testing is to take a base measurement of the background noise. The following 图 56 and 图 57 show the EMI performance of the overall testing lab at low frequency and high frequency for conducted emissions testing.

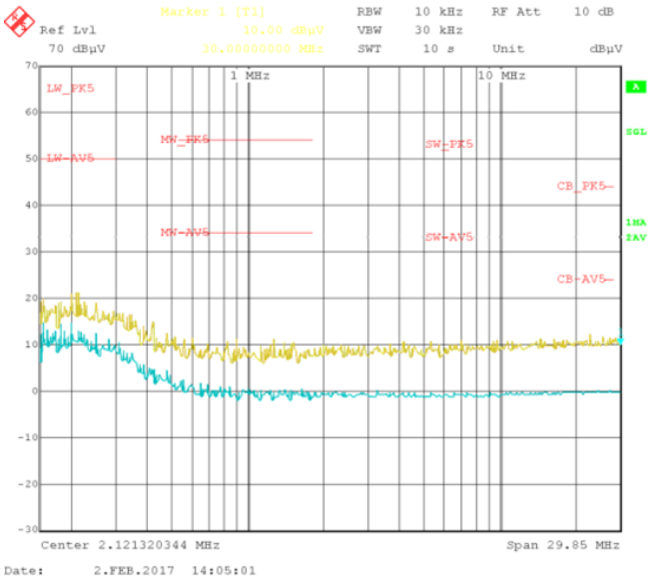


图 56. Low-Frequency Testing (100 kHz to 30 MHz) of Conducted EMI Performance

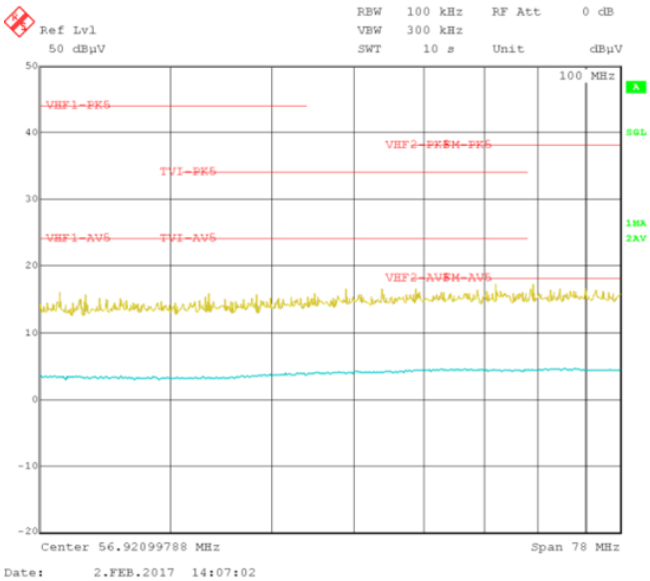


图 57. High-Frequency Testing (30 MHz to 100 MHz) of Conducted EMI Performance

Both low-frequency- and high-frequency noise floors were low enough to test the design. The system was then turned on and the line impedance stabilization networks were able to analyze the EMI. As the following 图 58 and 图 59 show, the 400-kHz switching frequency and its subsequent peaks are all below the AM band threshold for the low-frequency plot as well as the high-frequency plot.

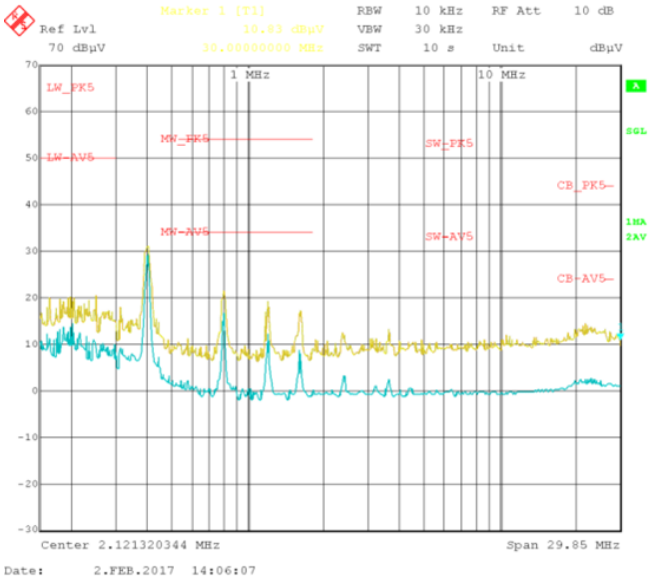


图 58. Low-Frequency Testing (100 kHz to 30 MHz) of Conducted EMI Performance

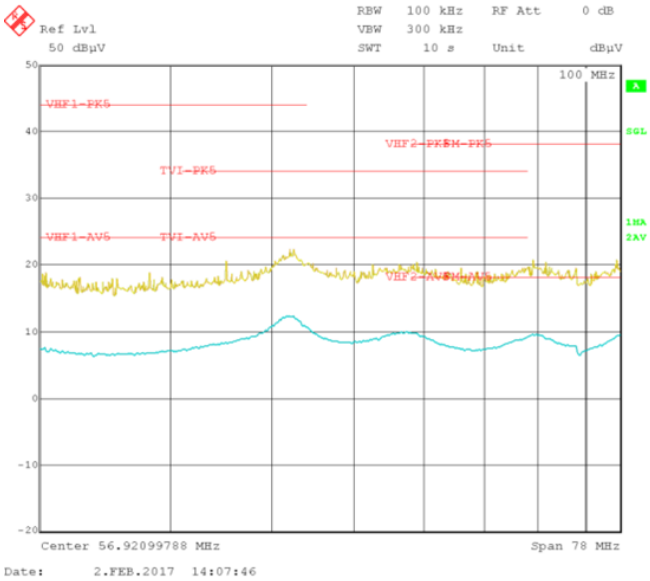


图 59. High-Frequency Testing (30 MHz to 100 MHz) of Conducted EMI Performance

6 Design Files

6.1 Schematics

To download the schematics, see the design files at TIDA-01432.

6.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01432.

6.3 PCB Layout Recommendations

6.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01432.

6.4 Altium Project

To download the Altium project files, see the design files at TIDA-01432.

6.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01432.

6.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01432.

7 Software Files

To download the software files, see the design files at TIDA-01432.

8 Related Documentation

1. Texas Instruments, *TPS25810 Charging Port Over USB Type-C™*, TPS25810 Application Report (SLVA768)
2. Texas Instruments, *LM74610-Q1 Zero IQ Reverse Polarity Protection Smart Diode Controller*, LM74610-Q1 Data Sheet (SNOSCZ1)
3. Texas Instruments, *AN-2162 Simple Success With Conducted EMI From DC-DC Converters*, AN-2162 Application Report (SNVA489)
4. Texas Instruments, *LM53625/35-Q1, 2.5-A or 3.5-A, 36-V Synchronous, 2.1-MHz, Step-Down DC-DC Converter*, LM53625/35-Q1 Data Sheet (SNVSAA7)
5. Texas Instruments, *TUSB319-Q1 USB Type-C DFP Port Controller*, TUSB319-Q1 Data Sheet (SLLSEV4)
6. Texas Instruments, *CISPR 25 Class 5 USB Type-C™ Port With USB3.0 Data Support Reference Design*, TIDA-00987 Reference Design (TIDUC55)

8.1 商标

9 Terminology

CC— Configuration channel

CDP— Charging downstream port

DFP— Downstream-facing port

EMI— Electromagnetic interference

ESD— Electrostatic discharge

ESR— Equivalent series resistance

IC— Integrated circuit

IEC— International Electrotechnical Commission

ISI— Intersymbol interference

LDO— Low-dropout regulator

NFET— Negative-channel field-effect transistor

OEM— Original equipment manufacturer

OTG— On-the-go

PFET— P-Channel field-effect transistors

SFF— Small form factor

TVS— Transient voltage suppression (diode)

UFP— Upstream-facing port

10 About the Author

HOPE BOVENZI is a systems engineer at Texas Instruments. Hope earned her bachelor of science in electrical engineering from the University of California at Davis in 2012. As a member of the Automotive Systems Engineering team at Texas Instruments, she is responsible for developing reference design solutions for the Automotive Infotainment and Cluster segment focusing on Media Interface and Telematics systems and has a background in power design.

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