TI Designs：TIDA-01567
适用于扩展坞的 USB Type-C™ 端口的电压裕量调节电源参考设计

说明

此参考设计可轻松实现与支持电压裕量调节功能的 USB Type-C™电源的系统集成。TPS62136 降压转换器可高效地将电源从常用 9V、12V 或 15V 适配器转换为 USB Type-C 端口，直接接受微控制器 (MCU) 的数字信号，从而将输出电压从 USB 标准 5V 电压改为更高的可编程电压。此输出电压压摆率符合 USB Type-C 规范。特别适用于使用扩展坞对智能手机电池进行快速充电的 应用， 在 USB Type-C 电缆上传输的电流高达 4A 时，更高的电压可提供更大功率。

资源

TIDA-01567	设计文件夹
TPS62136	产品文件夹

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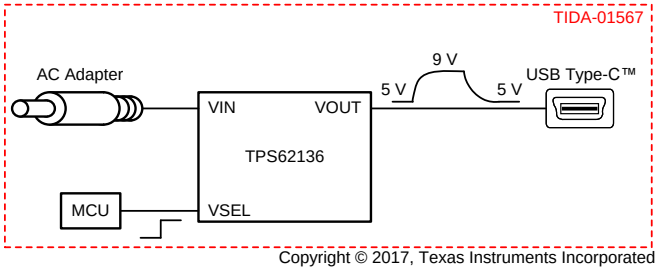
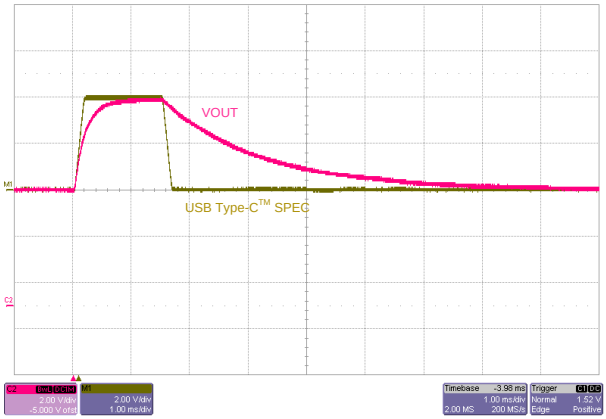
特性

- 借助压摆率控制可轻松调节的 V_{OUT}
- 采用单个数字输入引脚的 V_{OUT} 裕量调节
- 4A 输出电流
- 效率大于 90%（峰值 99%）
- 9V 至 17V 输入电压范围

应用

- 扩展坞
- 智能手机快速充电
- USB Type-C 端口





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1 System Description

The USB Type-C™ specification allows the USB host to adjust the voltage on the USB cable to meet the instantaneous application demands. A common application for USB Type-C ports, especially in docking stations, is fast-charging batteries in smartphones and other portable devices. In fast-charging, the USB voltage is increased to deliver more power to the battery while maintaining the same current in the USB cable. This design uses the TPS62136 step-down converter, which operates from common 9-, 12-, and 15-V adaptors and outputs up to 4 A of current.

This reference design switches between the common 5- and 9-V output voltages with a single digital input pin of the TPS62136 step-down converter. This voltage is fully adjustable from 0.8 V to 12 V to meet specific application requirements, which result from voltage drops across cables, USB protection switches, connectors, PCB traces, and so on. The system MCU drives the VSEL (voltage select) pin of the TPS62136 device to change the output voltage between the two levels.

This design uses simple circuitry to intentionally slow down the output voltage slew rate to meet the USB Type-C specification of slower than 30 mV/µsec. This output voltage margining is smooth and controlled.

1.1 Key System Specifications

表 **1. Key System Specifications**

PARAMETER	SPECIFICATIONS
Input voltage range (V_{IN})	9 V to 17 V
Output voltage (VSEL = Low)	5 V
Output voltage (VSEL = High)	9 V
Output voltage range (adjustable by R1, R2, R3, and Radd)	0.8 V to 12 V
Output current	4 A
Output voltage slew rate	< 30 mV/µsec

2 System Overview

2.1 Block Diagram

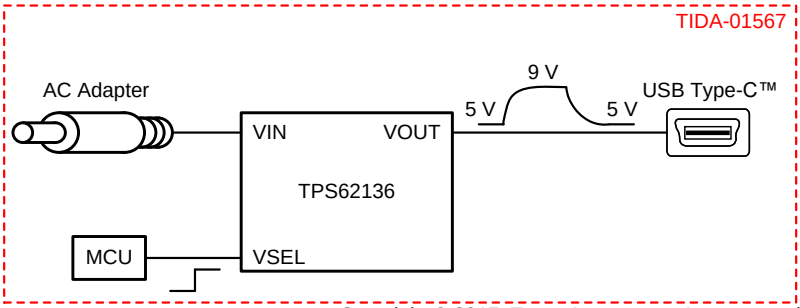

图 **1. TIDA-01567 Block Diagram**

2.2 Schematic Reference

图 2 shows a schematic of the TIDA-01567 reference design.

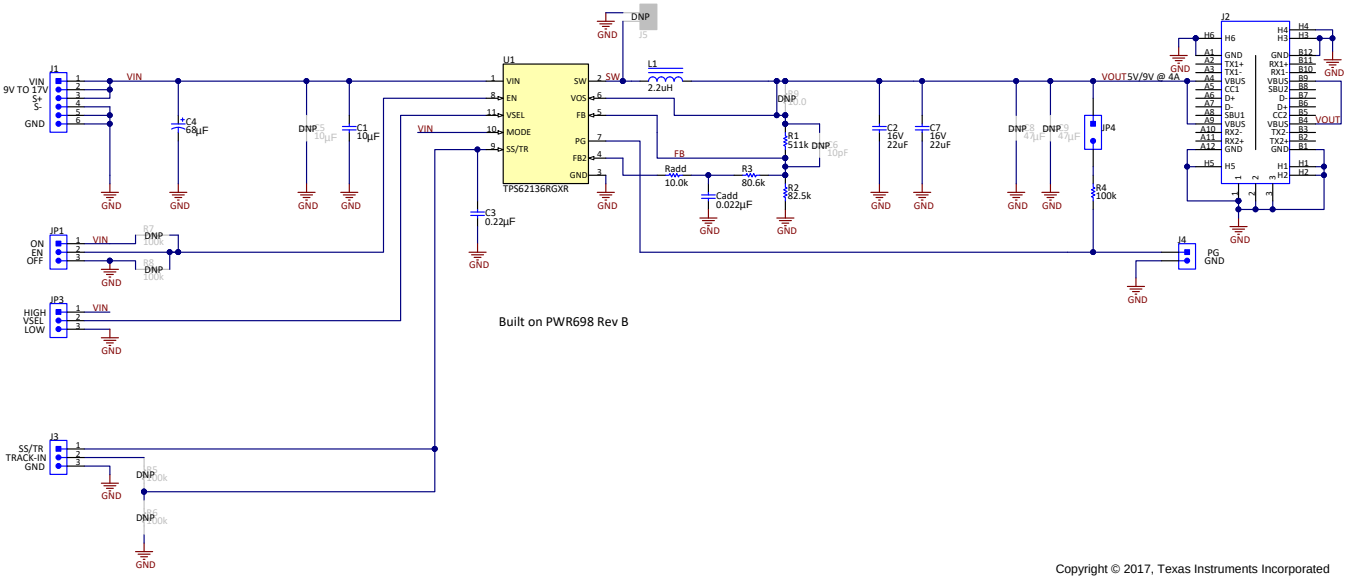

图 **2. TIDA-01567 Schematic**

2.3 Design Considerations

2.3.1 Output Voltage Slew Rate Control

The TPS62136 regulates the voltage at its feedback (FB) pin to 0.7 V. Typically, two resistors (R1 and R2) set the output voltage based on their gain from the FB pin to the output voltage. For a voltage-margining power supply, a third resistor (R3) connects the FB pin to GND through the FB2 pin of the integrated circuit (IC). FB2 is an output pin and is either floating or connected to GND based on the state of the VSEL input pin.

Changing VSEL immediately changes the state of FB2, which immediately changes the operating point of the TPS62136 device. Due to the very-fast transient response of the TPS62136, the output voltage quickly moves to the new operating point. This output voltage slew rate is way faster than what the USB Type-C specification allows; therefore, implement an RC filter, Radd and Cadd, to slow down this output voltage transition.

Choose empirical values for Radd and Cadd to sufficiently slow down the output voltage slew rate. As a starting point, choose Radd and Cadd values whose product (time constant) is in the range of the desired slew time. After choosing values and verifying that the slew rate is slow enough, be sure to measure the final circuit for sufficient control-loop stability and transient response. Set the lower output voltage level as described in the device data sheet and as calculated in 公式 1, by the choice of R1 and R2. Also set the higher output voltage level as described in the device data sheet and as calculated in 公式 2, by the choice of R1, R2, and R3. The same equations can be used, if the sum of R3 and Radd in the design is used in place of R3 in the data sheet equation.

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \tag{1}$$

$$R3 = \frac{V_{O1} \times R1 \times R2^2}{(V_{O2} - V_{O1}) \times \left(R1 \times R2 + R2^2\right)} \text{ for } V_{O2} > V_{O1} \tag{2}$$

Operate the TPS62136 device in forced pulse-width modulation (PWM) mode to control the output voltage slew rate from the higher voltage back down to the lower voltage. In forced PWM mode, the TPS62136 actively sinks the output voltage by moving energy from the output to the input to bring the output voltage back down. Alternatively, if using power save mode, the TPS62136 device does not sink the output voltage. Instead, the output voltage remains at the higher voltage, even after being configured to return to the lower voltage, and only decreases due to outside effects such as the external load and leakage currents.

2.3.2 Soft-Start Time

The selection of capacitor C3 controls the soft-start time. Choosing a larger C3 value increases the soft-start time to be much longer than the time constant formed by R3 and Cadd. Because Cadd must be charged to the 0.7-V FB pin voltage during start-up, the output voltage may overshoot its 5-V target if the soft-start time is not sufficiently long.

2.4 Highlighted Products

2.4.1 TPS62136

The TPS62136 is an efficient, small, and easy-to-use synchronous step-down converter that converts input voltages up to 17 V down to output voltages from 0.8 to 12 V at up to 4 A of current. Its VSEL pin allows easy adjustment of the output voltage by a single digital input, which typically comes from the system MCU. Hiccup overcurrent protection and output discharge enable safe system integration.

3 Hardware and Test Results

3.1 Hardware

The TIDA-01567 design is built on the TPS62136EVM-698 with the minimal changes as indicated in the TIDA-01567 *Schematics* and *Bill of Materials*. On the TPS62136EVM-698 device, change the inductor, output capacitors, FB resistors, soft-start capacitor, and add Radd and Cadd. Then, set the shunt on JP1 to enable the device, the shunt on JP2 to operate in PWM mode, and remove the shunt on JP3. Drive JP3 with a function generator to achieve voltage margining.

3.2 Test Results

3.2.1 Voltage Margining Slew Rate

图 3 and 图 4 show the voltage margining slew rate at both no load and full load, respectively. Each meets the USB Type-C specification.

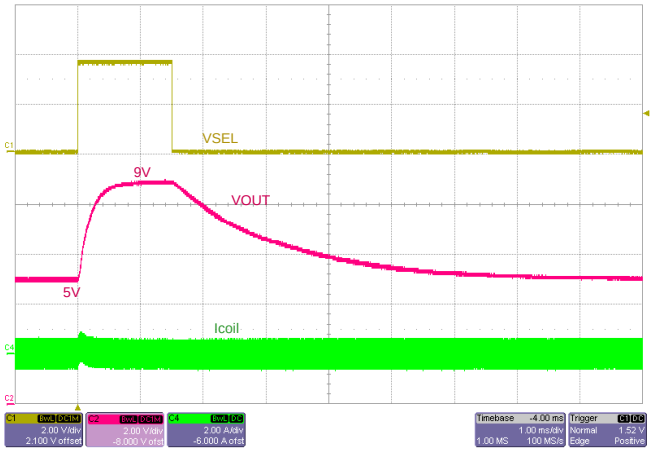

图 3. Voltage Margining Slew Rate (Load = 0 A)

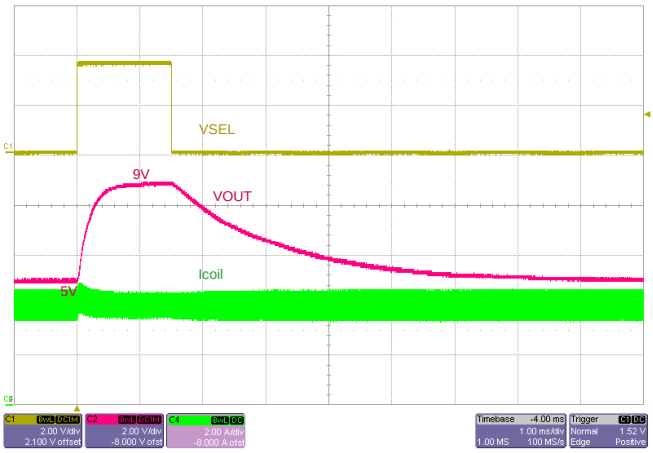

图 4. Voltage Margining Slew Rate (Load = 4 A)

3.2.2 Efficiency

图 5 and 图 6 show the efficiency at various input voltages.

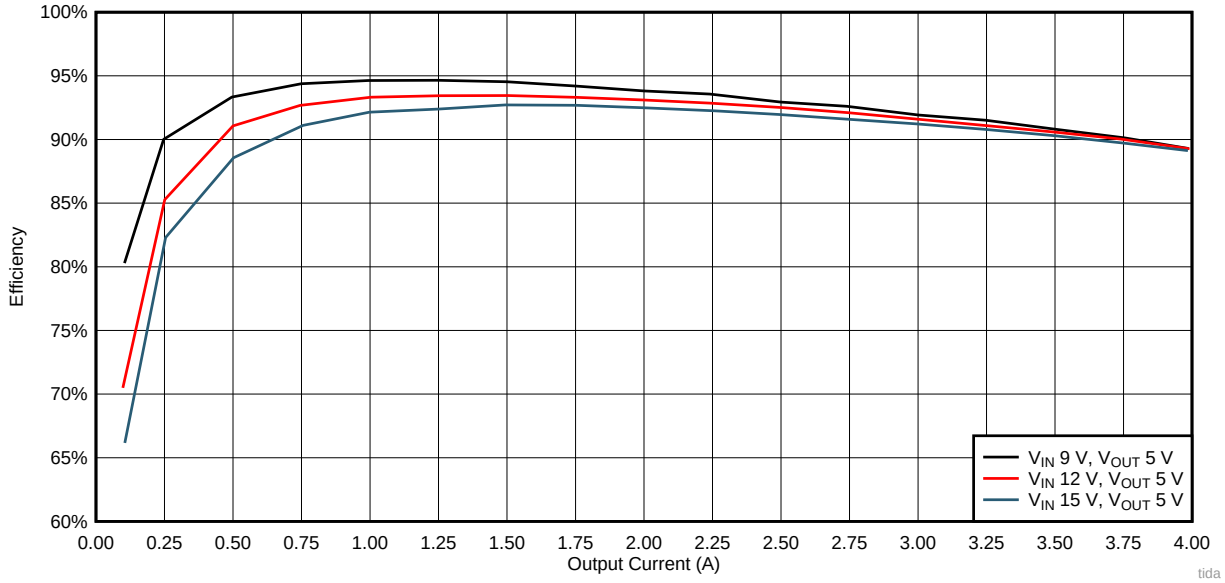

图 5. Efficiency (V_{OUT} = 5 V)

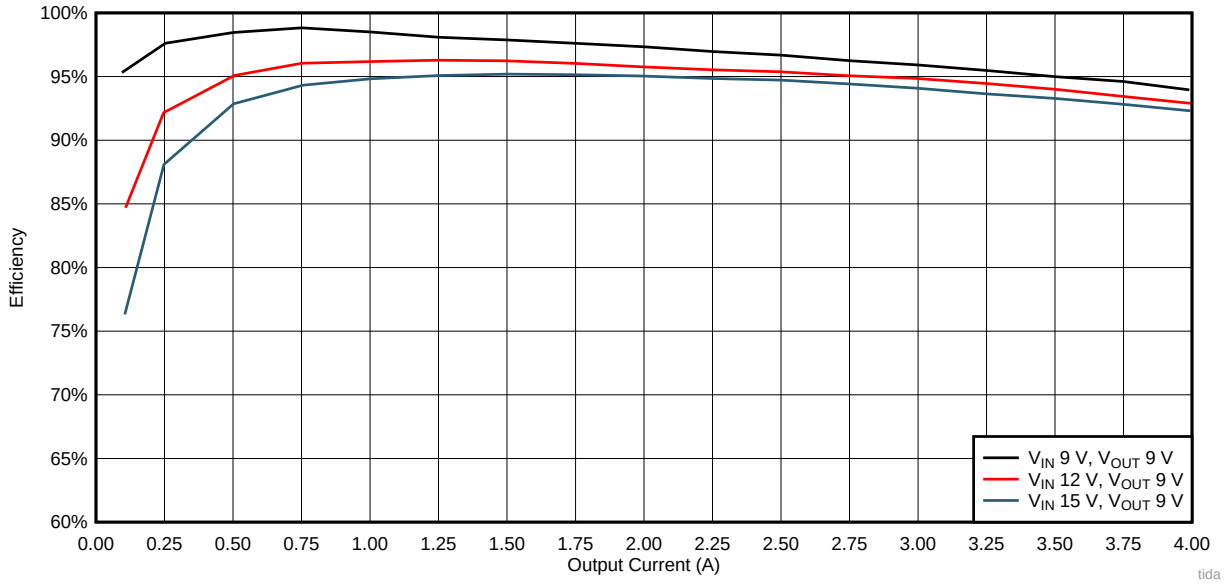

图 6. Efficiency (V_{OUT} = 9 V)

3.2.3 Load Transient Response

图 7 and 图 8 show the load transient response. The lack of ringing in the output voltage indicates sufficient stability.

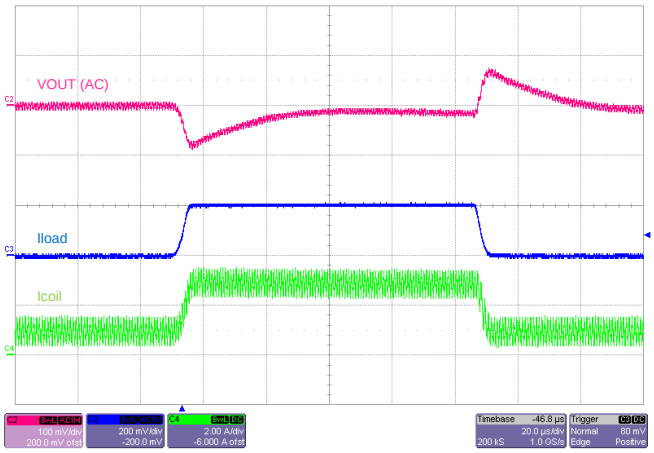

图 7. Load Transient Response
(V_{OUT} = 5 V, 1-A to 3-A Load Step)

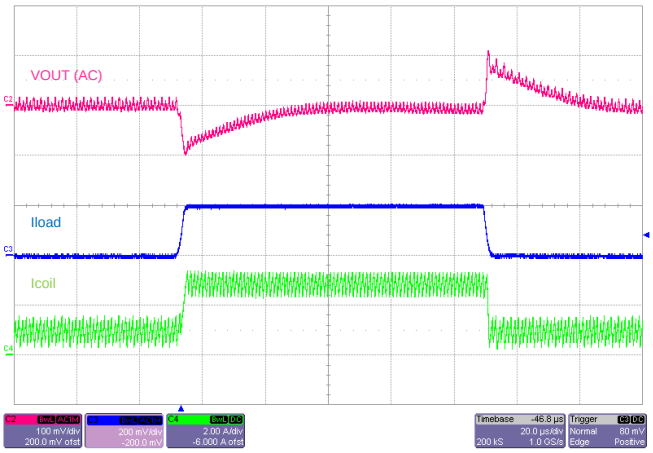

图 8. Load Transient Response
(V_{OUT} = 9 V, 1-A to 3-A Load Step)

3.2.4 Output and Input Voltage Ripple

图 9 through 图 12 show the output and input voltage ripple.

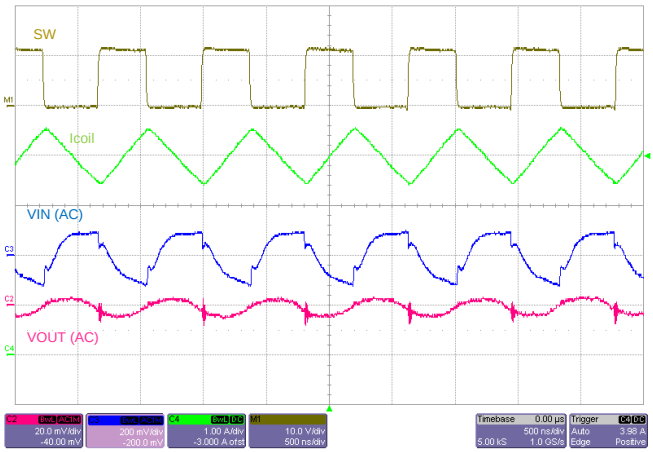

图 9. Output and Input Voltage Ripple
(V_{OUT} = 5 V, Load = 4 A)

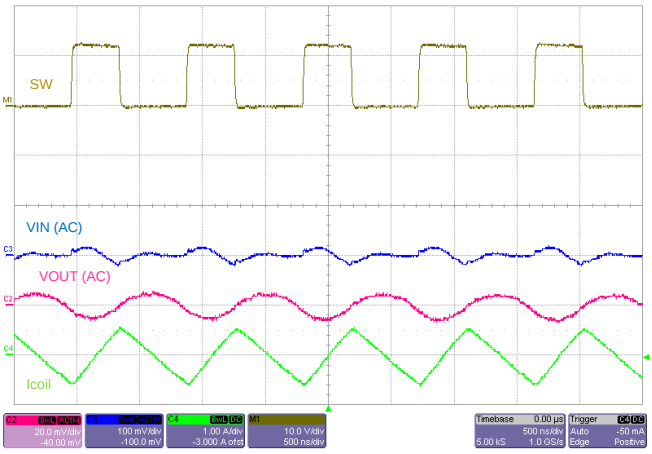

图 10. Output and Input Voltage Ripple
(V_{OUT} = 5 V, Load = 0 A)

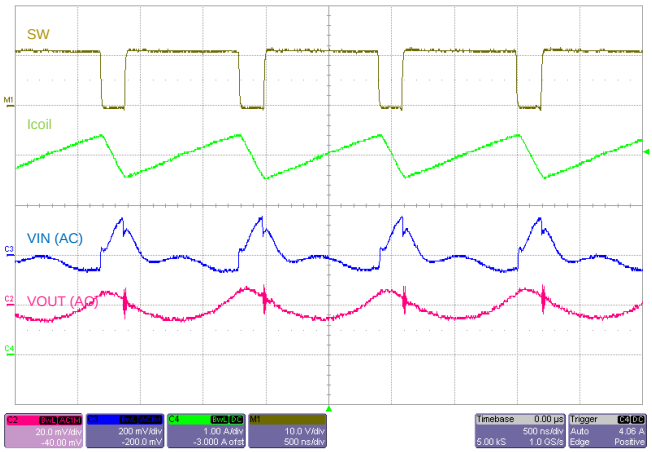

图 11. Output and Input Voltage Ripple (V_{OUT} = 9 V, Load = 4 A)

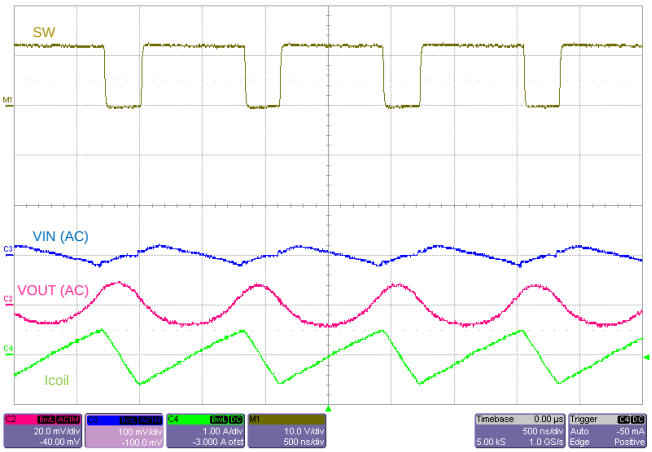

图 12. Output and Input Voltage Ripple (V_{OUT} = 9 V, Load = 0 A)

3.2.5 Start-Up and Shutdown

图 13 and 图 14 show the start-up and shutdown behavior.

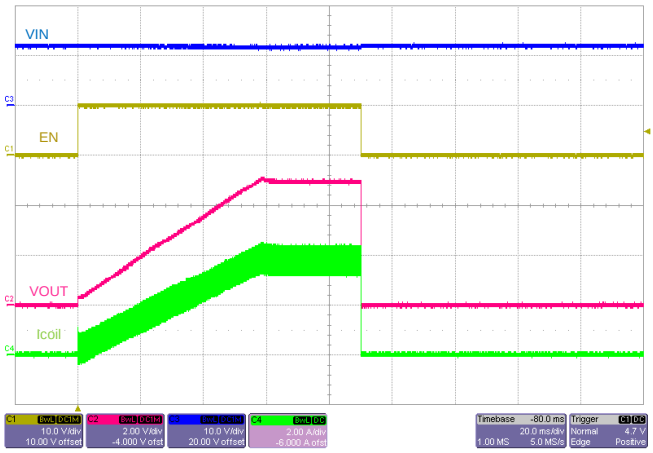

图 13. Start-Up and Shutdown (V_{OUT} = 5 V, Load = 4 A)

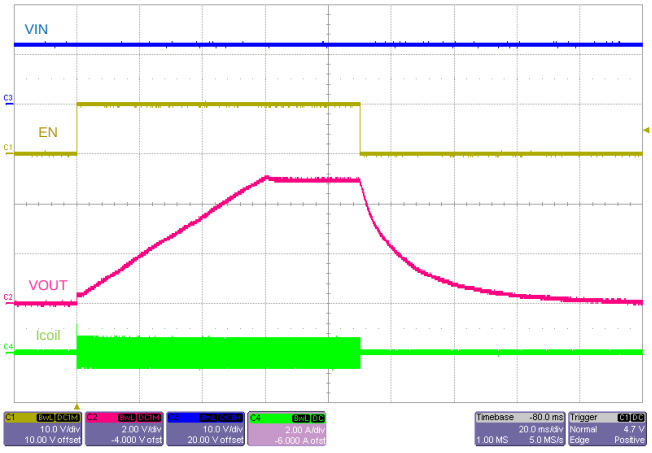

图 14. Start-Up and Shutdown (V_{OUT} = 5 V, Load = 0 A)

3.2.6 Bode Plots

图 15 and 图 16 show the bode plot (loop response) of both output voltages. The phase margin is well above 30°, which indicates stability.

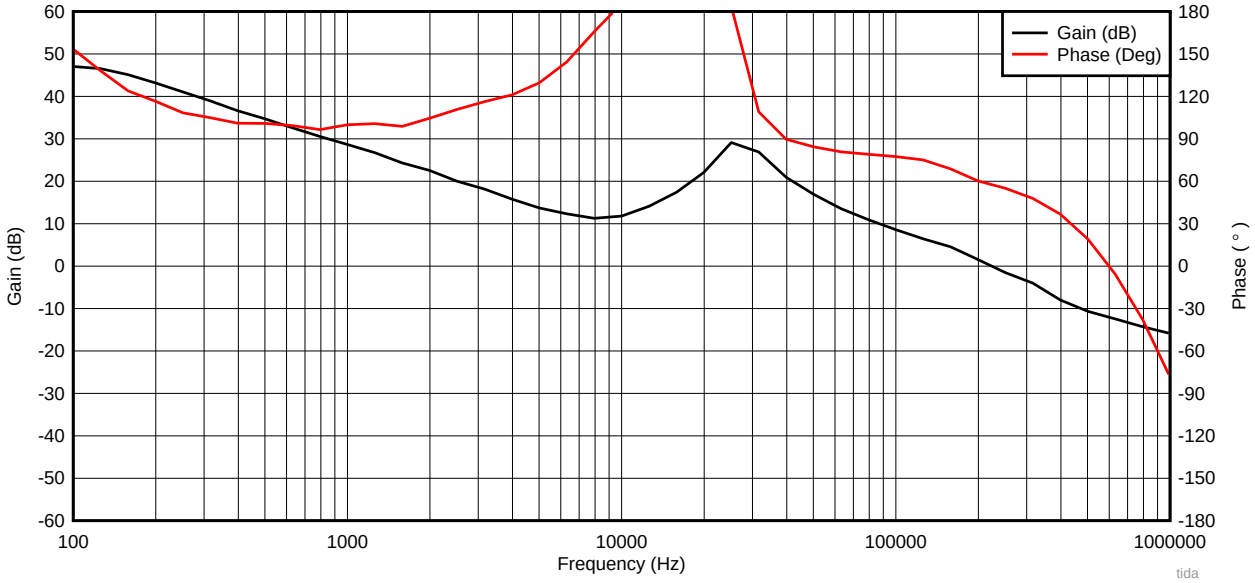

图 15. Bode Plot (V_{OUT} = 5 V, Load = 4 A), Bandwidth = 224 kHz, Phase Margin = 58°

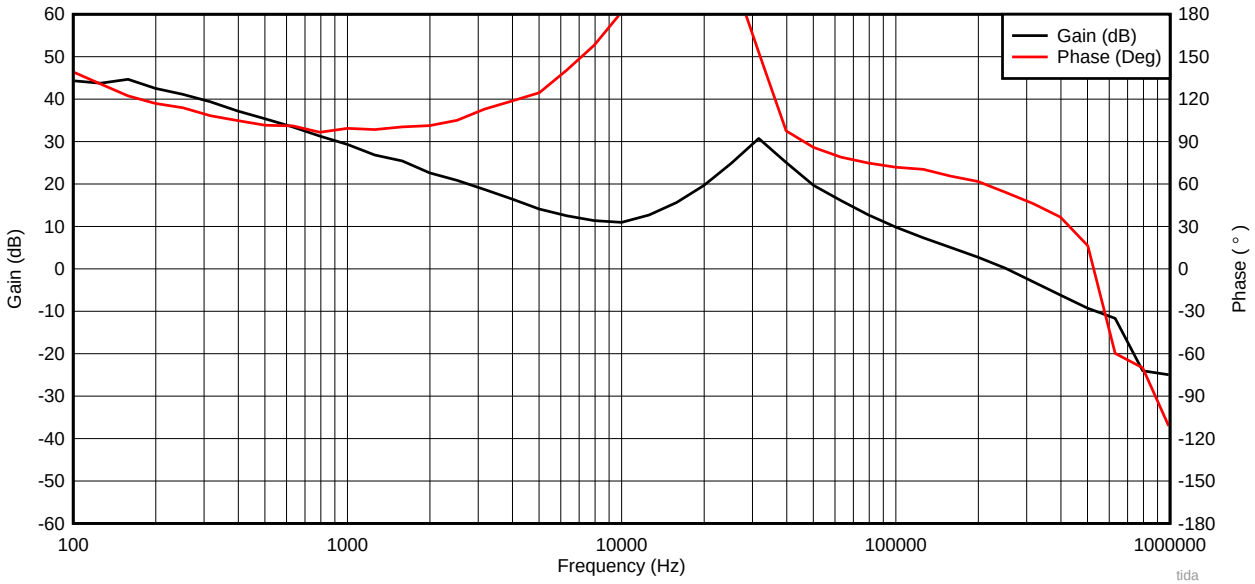

图 16. Bode Plot (V_{OUT} = 9 V, Load = 4 A), Bandwidth = 254 kHz, Phase Margin = 54°

3.2.7 Thermal Performance

图 17 shows the thermal performance at full load.

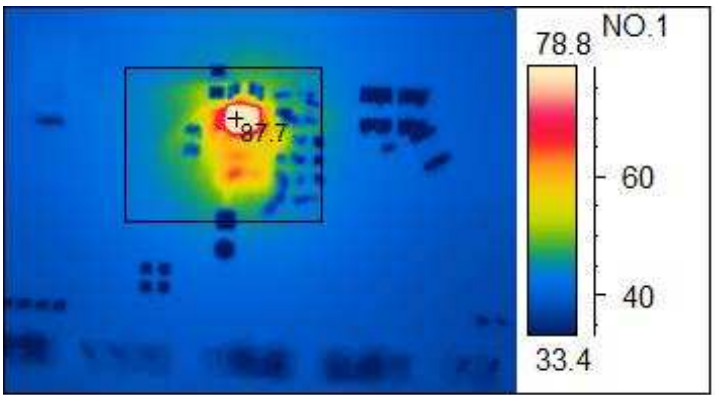

图 **17. Thermal Performance (V_{OUT} = 5 V, Load = 4 A)**

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01567.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01567.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01567.

4.4 Gerber Files

To download the Gerber files, see the design files at TIDA-01567.

4.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01567.

5 Related Documentation

1. Texas Instruments, *TPS62136, TPS621361 1-MHz High Accuracy 3-V to 17-V 4-A Step-Down Converters with DCS-Control™*

5.1 商标

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