TI Designs：TIDA-01498
具有宽输入电压范围的 4W PLC 电源参考设计

说明

此参考设计展示了非隔离式 PLC 电源产生稳定输出电压（该电压介于最小和最大输入电压之间）的一种替代方法。虽然降压/升压拓扑更为常用，但是耦合电感器单端初级电感转换器（通常称为 SEPIC）的效率会高得多，成本也更低。

资源

TIDA-01498	设计文件夹
LM5001NISOEVAL	工具文件夹
LM5001	产品文件夹

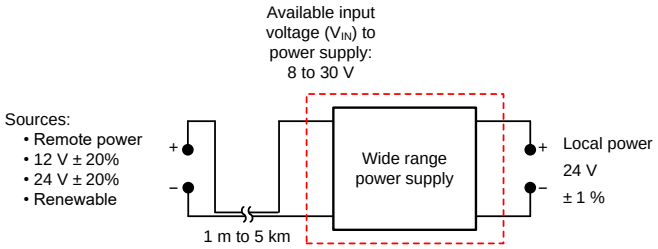
TI E2E™ Community — 咨询我们的 E2E™ 专家

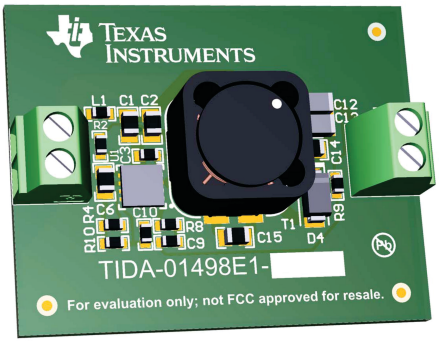
特性

- 功率高达 4W
- 效率高达 91%
- 宽 V_{IN} 范围：8V 至 36V
- 精确电压输出：24V ± 2%
- 外形小巧
- 部件数量少
- 短路保护
- 支持软启动

应用

- 通信模块
- CPU（PLC 控制器）
- 特殊功能模块





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1 System Description

Factory automation equipment operates sometimes in rough environments with input voltages that vary in a wide range. One reason could be that the system is connected to a power supply through a very long power supply line; 2-mile (or 3.5-km) connections are not rare. There are cases where the system specification might want to support a wide input voltage range to enable powering applications off a vehicle battery. This battery could have 12 V or 24 V. Internally, the system needs a stable power supply—in many cases 24 V. Typical topologies to use for this type of challenge are:

- Flyback
- Fly-Buck™
- Buck-boost
- Boost with separate buck
- SEPIC

This reference design evaluates the SEPIC topology in a special form. The two inductors of the SEPIC topology are implemented here as a coupled inductor with a 1:1 winding ratio on the same core.

CPU modules for smaller PLCs and communication modules for remote I/O systems have a similar build. Both modules are designed around a CPU or MPU, can drive a backplane, and have ideally some form of industrial ethernet on board. Therefore, at an equivalent system size, these modules have similar CPU performance and in particular power requirements. A third module category with similar power requirements are the special function modules. They can have a wide variety of functionality and include in many cases a local MPU, CPU, or FPGA/ASIC. A special function module offloads the main CPU by executing critical functions in local firmware. Local execution reduces the amount of communication over the backplane or over an industrial communication link. It also improves the response time in time sensitive control situations. It is the complexity of a special function module which sets the power requirement into the same range as the one from CPU and communication modules. Therefore, these modules are in many cases individually field powered.

All of these module types can benefit from a stable internal main power rail. A constant and defined internal voltage simplifies the design of onboard isolating converters and point-of-load regulators. If the system must run in a harsh environment with a variable field input supply voltage, this reference design can help to create the required stable internal power supply voltage.

1.1 Key System Specifications

表 **1. Key System Specifications**

SYMBOL	PARAMETER	CONDITIONS	SPECIFICATION			UNIT	DETAILS
			MIN	TYP	MAX		
V_{IN}	Input voltage		8	24	36[1]	V	2.3 节
I_Q	Quiescent current	I_{OUT} = 0	4	6	10	mA	
V_{OUT}	Output voltage	0 < I_{OUT} < $I_{OUT(max)}$	23.5	24	24.5	V	3.1 节
I_{OUT}	Output current	8 V < V_{IN} < 36 V	0		180	mA	
		9 V < V_{IN} < 36 V	0		200	mA	
h	Efficiency	P_{OUT} >10%	80	90		%	3.2 节
T_a	Ambient temperature	V_{IN} = 24 V	–40	25	125	°C	节 3.2.4

(1) Transients on V_{IN} must not exceed 75 V – V_{OUT}. In this reference design, the absolute max for V_{IN} is 51 V.

2 System Overview

2.1 Block Diagram

图 1 shows a typical use case for this type of power supply. Mobile equipment like cars, trucks, or diesel generators can have 12 V or 24 V available. The unit can also receive its power through a long supply wire or from renewable energy sources. In all these cases, a variable input voltage needs to be converted into a fixed output voltage. This reference design performs the task effectively and in a small form factor.

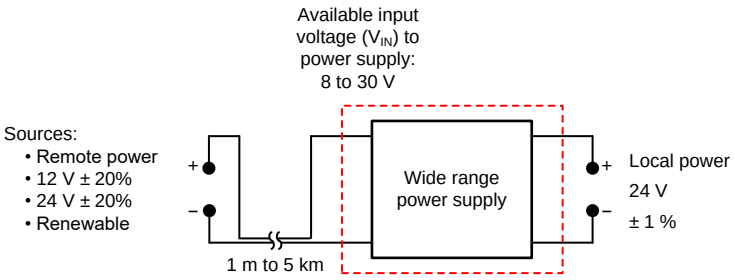

图 **1. Typical Use Case**

2.2 Highlighted Products

2.2.1 LM5001

The LM5001 high-voltage switch-mode regulator features all of the functions necessary to implement efficient high-voltage boost, flyback, SEPIC, and forward converters, using few external components. This easy-to-use regulator integrates a 75-V N-Channel MOSFET with a 1-A peak current limit. Current mode control provides inherently simple loop compensation and line-voltage feed-forward for superior rejection of input transients. The switching frequency is set with a single resistor and is programmable up to 1.5 MHz. The oscillator can also be synchronized to an external clock. Additional protection features include:

- Current limit
- Thermal shutdown
- Undervoltage lockout
- Remote shutdown capability

2.3 System Design Theory

The SEPIC can convert a wide range of input voltage to a fixed output voltage where the input voltage can range from below to above the output voltage.

Classical SEPIC implementations require two inductors that are quite difficult to control. The output inductor can easily get into resonance with the primary-to-secondary coupling capacitor. This resonance has then to be eliminated by the feedback and compensation network.

Off-the-shelf coupled inductors eliminate these problems. Such inductors have a similar cost structure as the standard single inductors. When the SEPIC is constructed with a coupled inductor, the coupling makes the inductor behave like the one of a boost converter. The inductor then has a reduced tendency to resonate and the feedback scheme gets much simpler. The only possible resonances left are circulating currents in the coupling capacitor in combination with the leakage inductance of the inductors, both of which reduce efficiency.

To avoid this effect, keep the parallel resonance of the coupling capacitor and the leakage inductance significantly below the switching frequency. A feasible starting point is to use a coupling capacitor, which resonates with the leakage inductance of the coupled inductor at less than half of the switching frequency. A very detailed analysis of the coupled inductor SEPIC can be found in the article "Designing DC/DC converters based on SEPIC topology" within the *Analog Applications Journal of Fourth Quarter, 2008*.

图 2 shows the principle circuit diagram of a SEPIC.

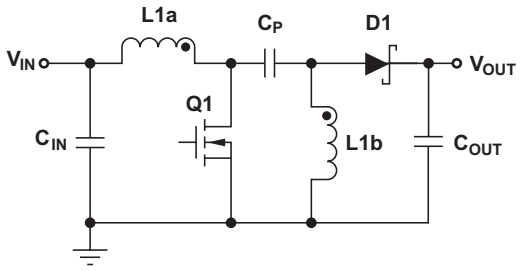

图 **2. Principle Circuit Diagram of Coupled Inductor SEPIC**

The advantage of the SEPIC is its simpler structure compared to a buck-boost converter and its more deterministic behavior under different load and input voltage conditions. The SEPIC has a better cost structure and efficiency because only one transistor is switching compared to four in a buck-boost converter. Therefore, the real estate is smaller when doing a higher power implementation with discrete transistors. A side effect is that there is no primary snubber network for the leakage inductance needed like it would be in a flyback. The energy in the primary leakage inductance can discharge through capacitor C_P into the secondary side and is therefore reused. The lack of a snubber increases efficiency. For the same reason, there is also no snubber needed for the rectifier diode on the secondary side, which further improves efficiency.

The design of this SEPIC controller depends on the optimization target priorities. The SEPIC can be optimized to a combination of the following targets:

- High efficiency
- Low output ripple
- Fast load transient response
- V_{OUT} to V_{IN} ratio
- Small form factor
- Low cost

The tradeoffs are the inductance, the switching current, the switching losses, the mechanical size of the inductor, the output capacitance, and indirectly cost. If maximum efficiency is the main goal, then the frequency must be as low as possible to keep switching losses in the LM5001 low and reduce the core losses in the inductor. Lower frequency results in larger inductance to keep peak currents low. This frequency also results in a larger output capacitor value to keep output ripple in the required range, which in turn has an impact on the load transient response behavior of the circuit. A larger inductance at same load current finally has an impact on the mechanical size and cost. A larger V_{OUT} to V_{IN} ratio affects the inductor and the switcher because it increases the switching current. For example (assuming 100% efficiency), if the circuit has a V_{IN} of 24 V and a V_{OUT} of 24 V, then the average switcher current during on-time is 2× the output current. The inductor sees the same current. If the circuit gets 18 V, then this current becomes 2.33× the output current. Once V_{IN} reaches 12 V, this current is already 3× the output current, and at V_{IN} of 8 V, it is 4×. The maximum possible input current depends on the minimum peak current of the LM5001 regulator. For a low input voltage under 8 V, the maximum output power in this reference design drops below 4 W.

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

TI published an EVM that can be modified in a few steps to implement a coupled inductor SEPIC. Find more details about the board on TI.com by entering the search term "lm5001nisoeval". All the documentation is available and the board can be ordered in the TI store.

This EVM is the starting point for this reference design. 图 3 shows its schematics.

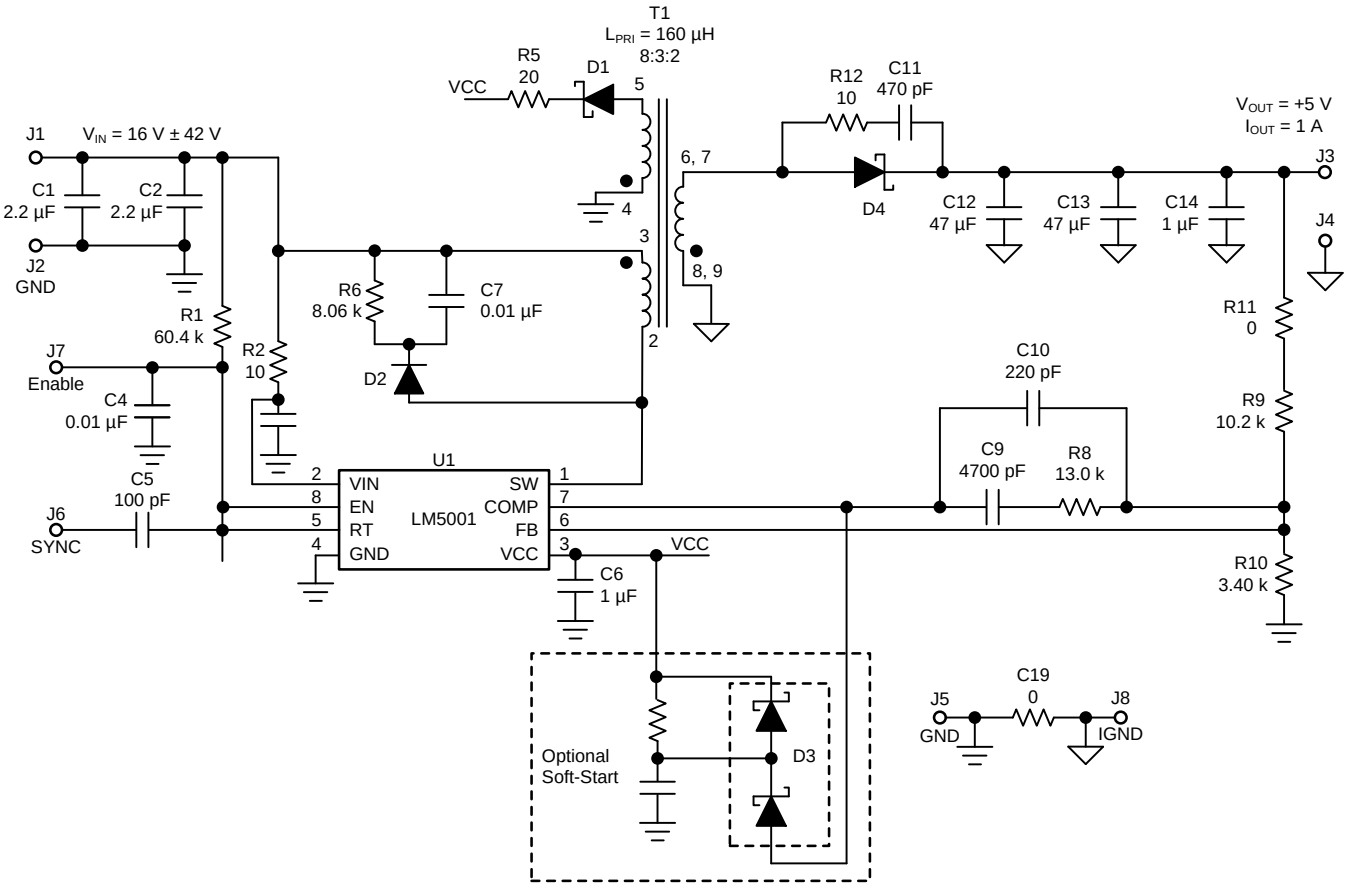

图 3. Circuit Diagram of Non-Isolating Flyback Evaluation Board

3.1.1 Build Instructions

The following step-by-step instructions convert the EVM into a coupled inductor SEPIC with a V_{IN} range from 8 V to 36 V and a fixed output voltage of 24 V.

1. Remove components: R3, D2, R12
2. Change components: R10 = 562 Ω, C12 = C13 = 4.7 µF at 35 V, C14 = 0.1 µF at 35 V, D4 = 60-V Schottky
3. Replace T1 with a 220-µH coupled inductor from Würth (744870221) or Coilcraft (KLMSD1260-224) and add a 1-µF at 60-V low ESR capacitor from the primary-side switching node (pin 1 U1) to the secondary-side switching node (Schottky anode).
4. (Optional) To see the minimum components, if no transients > 75 V are expected on V_{IN}, replace R2 with 0 Ω and remove C3. R1, R5, R6, C7, C11, and D1 can be removed as well.

The modifications look clean and tidy. Do not cut the traces. With four wires and one capacitor soldered on the inductor, the effort for the modifications is limited. The loop compensation built from C9, C10, and R8 is left unchanged for the first tests.

The coupled inductor has to be connected as per 图 4.

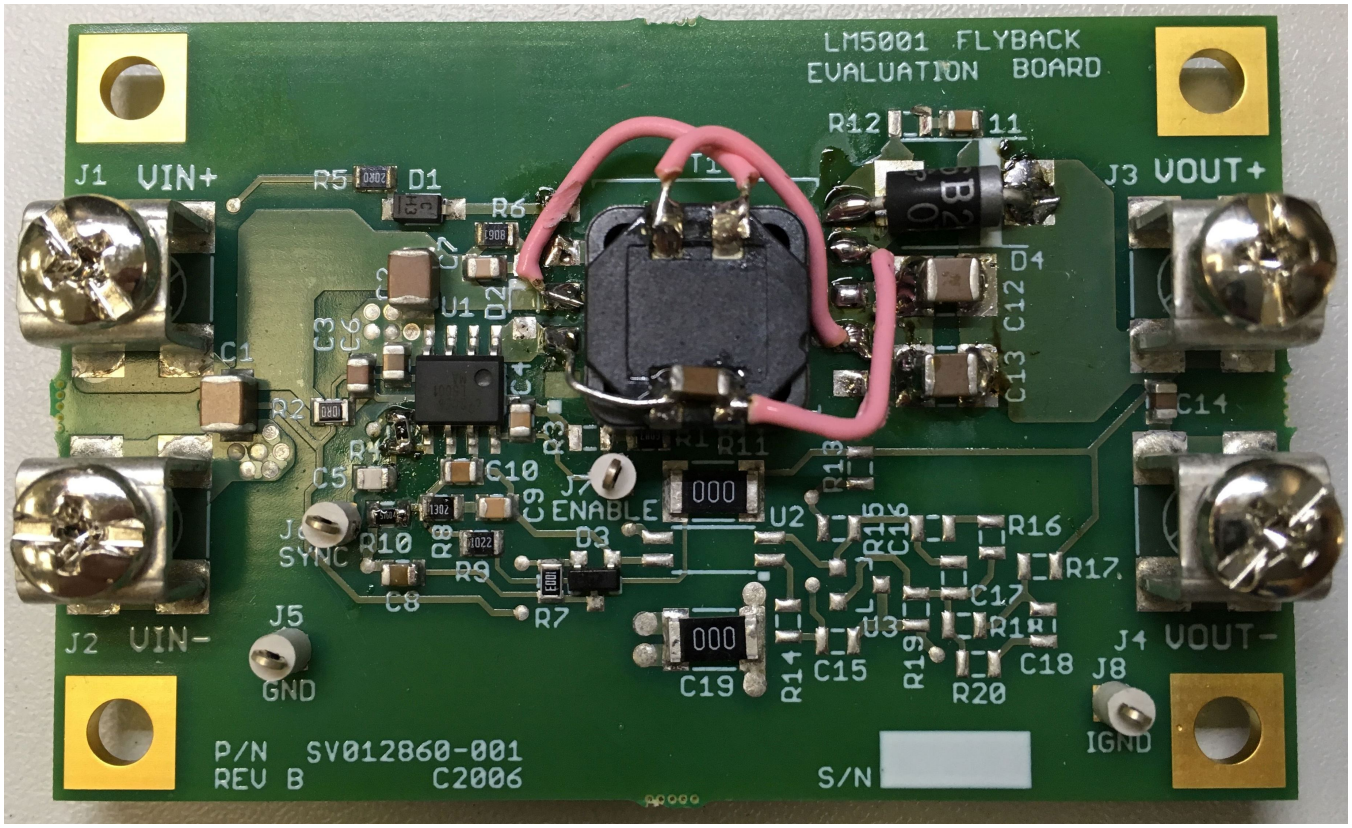

图 4. Photo of EVM After Modification

With these modifications, the board can now convert from 8 V to 36 V on J1, J2 into a stable 24 V on J3, J4. The board is short circuit proof and can be overloaded significantly without damage.

In 节 3.1.2, the power supply has to be optimized with regards to stability and regulation speed against load transients. This step involves the components C9, C10, and R8.

3.1.2 Loop Optimization

A SEPIC converter must optimize the feedback loop to get stability over the range of specified input voltages and loads. This optimization can be done by injecting a distortion into the feedback loop and checking the response on the generated output voltage. The measurement instrument used for this purpose is a Venable Instruments 3120 frequency response analyzer. 图 5 shows the gain and phase before loop optimization.

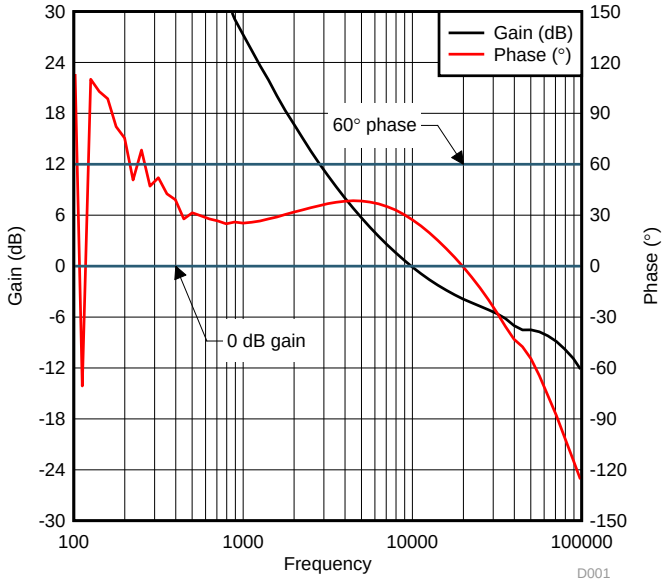

图 **5. Gain Phase Plot Recorded by Frequency Response Analyzer From Venable Instruments**

图 5 shows that the phase margin at a 0-dB gain is only 30 degrees. A good phase margin for stability over load variances, component tolerances, temperature, and aging is 60 degrees. The change of R8 from 13 kΩ to 4.02 kΩ reduces the gain by a factor of 3, which corresponds to a down shift of the gain plot by 8 dB. Increasing C9 gradually from 4.7 nF to 220 nF shifts the filter zero to lower frequencies and shows a continuous improvement on the phase margin. The next three diagrams show the phase and gain at different input voltage conditions. With C9 set at 220 nF, the margin is always greater than 60 degrees at a 0-dB gain. The loop bandwidth is now 2.5 kHz at $V_{IN(min)}$.

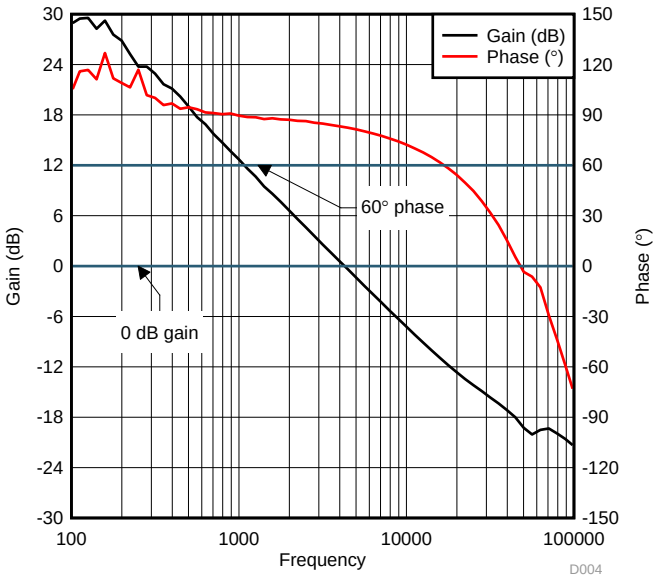

图 **6. Gain Phase Plot at 30 V**

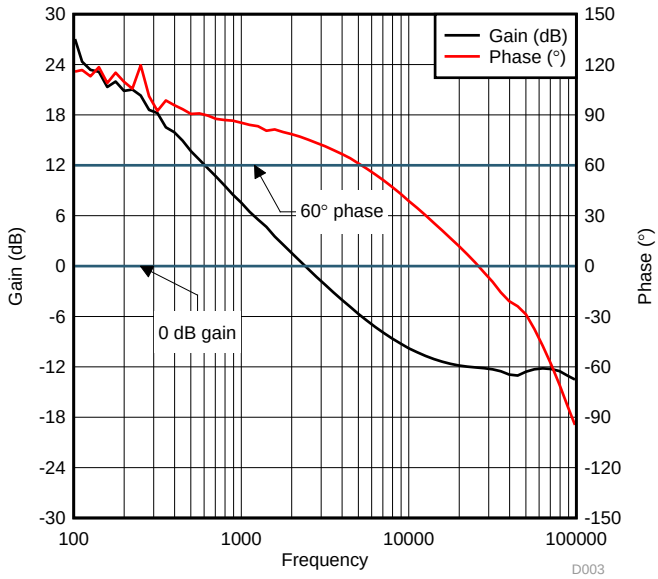

图 **7. Gain Phase Plot at 12 V**

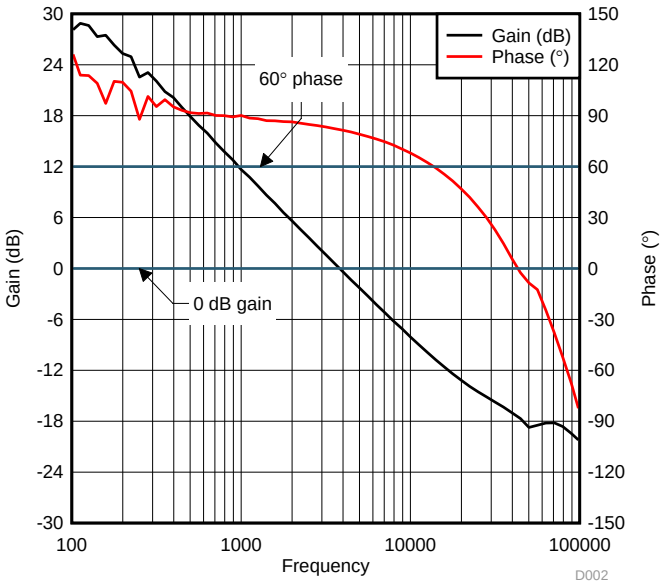

图 **8. Gain Phase Plot at 24 V**

A margin of greater than 60 degrees satisfies the requirement for stable operation. This margin provides enough guardband for aging, temperature variation, and component variations. If the amount of guardband is not needed, then increase the gain up to 6 dB for a faster transient response.

3.1.3 Calculations and Inductor Selection

This section shows the calculations for the critical components. These formulas create a starting point to optimize the design. The main prerequisite for this reference design is using an off-the-shelf coupled inductor with a 1:1 winding ratio. Any circuit change for one of the various optimizations requires a revisit of the loop optimization.

For the best reliability and low electromagnetic influence (EMI), it is essential to select an inductor with a saturation current larger than the current limit of the switching device. When the inductor is saturated, the current can rise very quickly because only leakage inductance is present. The LM5001 has a response time of 200 ns. The resulting peak current can be calculated with the equation below.

$$I = t \times V_L \quad (1)$$

With an input voltage of 36 V and a leakage inductance of 1 µH the current increases up to 7 A within 200 ns. Such a current transient can induce undesired voltages on traces and within the device. Therefore, it must be avoided during normal operation.

The following is a list of possible optimization targets as shown in 2.3 节:

- High efficiency
- Low output ripple
- Fast load transient response
- V_{OUT} to V_{IN} ratio
- Small form factor
- Low cost

The following calculations are for the different optimization targets. This reference design uses the LM5001, which has a maximum current limit of 1200 mA and a minimum current limit of 0.8 A. All optimizations except the input range optimization use a minimum input voltage of 8 V and a maximum input voltage of 36 V. The output voltage is 24 V and the maximum output current is 0.2 A. Input voltage and output voltage determine together the switching duty cycle:

$$D = V_{OUT} V_{IN} + V_{OUT} \quad (2)$$

Subsequent calculations need the minimum and maximum duty cycle based on the input voltage range. The duty cycle at $V_{IN(min)}$ calculates as 0.75 and at $V_{IN(max)}$ it is 0.4.

At an output power of 4 W (24 V × 0.167 A), the input current at minimum input voltage of 8 V is 0.5 A. At a maximum input voltage of 36 V, the current is 0.11 A. With

$$I_{AVG} = I_{OUT} 1 - D \quad (3)$$

the average inductor current I_{AVG} is 0.67 A at $V_{IN(min)}$ and 0.28 A at $V_{IN(max)}$.

3.1.3.1 Optimization for Efficiency

If the main goal is efficiency, then keep the frequency low and the current ripple ratio (r) between 0.3 and 0.5. This ratio minimizes switching losses and core losses. The calculation starts with a frequency of 200 kHz with

$$I_{RIP} = r \times I_{PK} \quad (4)$$

The ripple current can have a value of 320 mA based on an LM5001 minimum peak current of 0.8 A and r = 0.4.

The average inductor current based on the peak current is

$$I_{AVG} = I_{PK} - I_{RIP} 2 = I_{PK} - r \times I_{PK} 2 = I_{PK} \times 1 - r 2 \quad (5)$$

and has 0.64 A. This measurement is below the required inductor current for a maximum power of 4 W at a minimum input voltage of 8 V. Therefore, it is not possible to achieve maximum efficiency and supporting $V_{IN(min)}$ = 8 V at a power level of 4 W. For this optimization target, the specification of $V_{IN(min)}$ needs an increase to 10 V. At $V_{IN(min)}$ = 10 V, the required average inductor current is only 0.57 A. The difference from 0.57 A to 0.64 A is large enough for a stable output voltage at 89% efficiency.

The next step is to calculate the on- and off-times based on the cycle time and duty cycle. The calculation is only needed for $V_{IN(min)}$ because at this input voltage the inductor current can become critical:

$$t C Y C = 1 f S W \quad (6)$$

The on-time of the switch is:

$$t O N = D \times t C Y C \quad (7)$$

The off-time of the switch is:

$$t O F F = 1 - D \times t C Y C \quad (8)$$

With these equations, it is possible to calculate the required inductance:

$$L = t O N \times V I N I R I P = D \times t C Y C \times V I N r \times I P K = V I N \times V O U T V I N + V O U T f s w \times r \times I P K \quad (9)$$

An inductance of 110 µH is required for r = 0.4. The ideal output power is then 4.5 W at V_{IN} = 10 V, or 4 W assuming efficiency of 90%. An r of 0.44 allows this design to use a standard inductor of 100 µH and still maintain the output power at 4 W.

3.1.3.2 Optimization for Transient Response

If the desired design behavior is fast load transient response, then the energy transfer per switching cycle must be maximized. In this case, the switching circuit can quickly add energy if the load increases. If the load decreases, the regulation goes faster if less energy is in the inductor. Therefore, the stored energy in the inductor must be minimized. Both cases can be achieved at the same time by increasing the current ripple ratio. The transient response improves further if the switching frequency is higher as well.

This method has a negative side effect. A larger current ripple ratio decreases the average inductor current because the peak current is capped. Therefore, the minimum input voltage must increase for a given power level. The calculations start with r = 1 and a power level of 4 W. The increased ripple current requires an increased switching frequency by the same factor for a constant output voltage ripple.

$$f N E W r N E W = f O L D r O L D \quad (10)$$

A frequency of 500 kHz is needed to fulfil the equation for r = 1. Alternatively, the output capacitor can increase.

公式 11 shows that with r = 1 the average inductor current can be maximum 0.4 A.

$$I A V G = I P K \times 1 - r 2 \quad (11)$$

To achieve 4.5 W (which is needed for 4-W output power at 90% efficiency), a certain $V_{IN(min)}$ is needed.

$$I O U T = P O U T V O U T ; \quad I A V G = I O U T 1 - D ; \quad D = V O U T V O U T + V I N \quad (12)$$

$$V I N = I A V G \times V O U T 2 I A V G \times V O U T - P O U T \quad (13)$$

For r = 1 and P_{OUT} = 4.5 W, $V_{IN(min)}$ is 21.2 V. The required inductor value is based on 公式 14, which calculates to 28 µH. Relaxing r slightly to 0.9 requires $V_{IN(min)}$ of 18 V, a switching frequency of 450 kHz, and an inductor value of 31.8 µH.

$$L = V I N \times V O U T V I N + V O U T f S W \times r \times I P K \quad (14)$$

If $V_{IN(min)}$ and P_{OUT} are given, then 公式 15 calculates the largest possible current ripple ratio.

$$r = 2 - 2 \times P O U T V O U T \times I P K \times 1 - V O U T V O U T + V I N \quad (15)$$

For example, with a $V_{IN(min)}$ of 15 V, r can be up to 0.78.

The faster transient response requires one final step. These optimizations shift the so-called right half plane zero (RHPZ) to a higher frequency. Because of this, the loop filter bandwidth can also increase, which leads to the better transient response.

3.1.3.3 Optimization for Output Ripple

The amount of output ripple depends on the current flow in the output capacitor, the capacitor value and the on-time (during which is no energy transfer into the output capacitor). This relationship is shown in 公式 16:

$$V_{CAP} = V_{RIP} = I_{OUT} \times t_{ONC} \quad (16)$$

The output voltage ripple reduces at a given output current if t_{ON} decreases or if the output capacitance increases. For less ripple, one option is to increase the frequency to reduce efficiency. The designer can also increase the output capacitor value, which increases size and cost. The following formulas present these two options.

$$t_{ON} = C \times V_{RIP} I_{OUT} \quad (17)$$

If the design uses a load capacitor value of 10 µF and needs to support a ripple of less than 25 mV at an output current of 188 mA (4.5 W), then the on-time needs to be less than 1.3 µs. For $V_{IN(min)}$, this corresponds to a switching frequency of 580 kHz.

$$C = t_{ON} \times I_{OUT} V_{RIP} \quad (18)$$

For a switching frequency of 200 kHz, an output current of 188 mA (4.5 W), and a required ripple of less than 25 mV at $V_{IN(min)}$, a capacitor value of 28 µF is needed. With a value of 3 × 10 µF, the ripple voltage is less than 23 mV.

3.1.3.4 Optimization for Large V_{OUT} to V_{IN}

There are different possibilities for a larger ratio from V_{IN} to V_{OUT}. For a given inductor peak current, it is possible to decrease the current ripple ratio (r). This adjustment elevates the average current in the inductor so the input voltage can decrease maintaining the same power level. The decreased r can stem from increased inductance or increased switching frequency. The drawback of an increased inductance is the reduced transient response.

The only viable alternative with this reference design is to accept a lower power level when V_{IN} approaches $V_{IN(min)}$.

$$r = 2 - 2 \times P O U T V O U T \times I P K \times 1 - V O U T V O U T + V I N \quad (19)$$

With P_{OUT} = 4.5 W, I_{PK} = 0.8 A, V_{OUT} = 24 V, and V_{IN} = 8 V, r is 0.125. Reducing V_{IN} from 8 V to 7.8 V gives an r value of 0.088. This result shows that the ratio $V_{IN(min)}$ versus V_{OUT} is at the limit for this switching device.

Based on r, it is now possible to calculate the inductor or the frequency. The inductor value for an r of 0.088 at 200 kHz is:

$$L = V I N \times V O U T V I N + V O U T f s w \times r \times I P K \quad (20)$$

which results in 420 µH. The frequency for an r of 0.088 with an inductance of 100 µH

$$f s w = V I N \times V O U T V I N + V O U T L \times r \times I P K \quad (21)$$

would be 820 kHz. The same with r = 0.125 gives 294 µH or 580 kHz. If $V_{IN(min)}$ needs to be significantly below 8 V, then a stronger switching solution is necessary. A combination of switching controller and external MOSFET transistor provides the required high current at the cost of slightly more complexity.

3.1.3.5 Optimization for Form Factor

The optimization for a smaller form factor follows the same rules as 节 3.1.3.6.

3.1.3.6 Optimization for Low Cost

Main cost drivers are the size and quality of the output capacitor and the dimensions of the inductor. To reduce cost, make the inductance and the capacitance as small as possible. The switching frequency and r need to increase. As a consequence, the minimum voltage needs to increase or the power level must decrease. In all cases, efficiency lowers because of the higher switching speed. 公式 20 also be used for this optimization:

$$L = V I N \times V O U T V I N + V O U T f s w \times r \times I P K$$

With a switching frequency of 500 kHz and an r of 0.8, the inductor size reduces from 100 µH to 15 µH and $V_{IN(min)}$ increases from 8 V to 16 V. The size of the inductor can then shrink from 12.5 mm × 12.5 mm × 8.5 mm to 8 mm × 8 mm × 2 mm. With the higher frequency, the output capacitor can get smaller from 10 µF to 4 µF.

3.2 Testing and Results

3.2.1 Input Voltage and Output Load Test

In this test, six different input voltages are applied to the board: 8 V, 12 V, 18 V, 24 V, 30 V, and 36 V. At each voltage, an output load current in six steps is applied: 0 mA, 10 mA, 20 mA, 50 mA, 100 mA, and 200 mA. For each of the input voltage and output load combinations, the input current and output voltage is measured. 图 9 shows the measurement results.

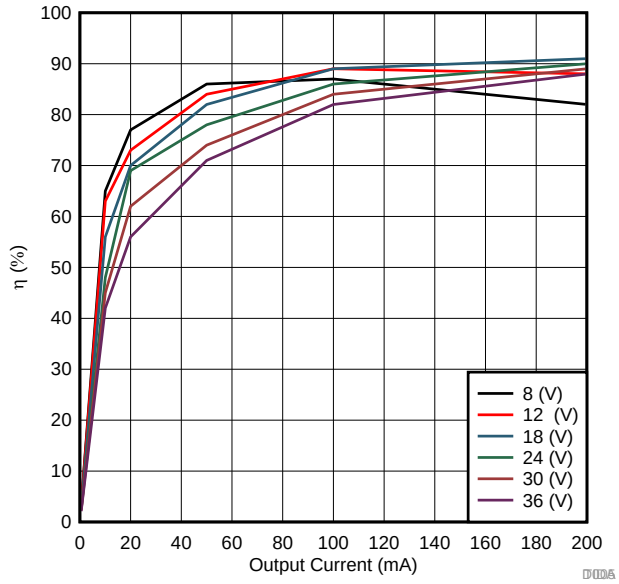

图 **9. Efficiency versus Output Current**

3.2.2 Input Voltage and Maximum Load Test

In this test, the input voltage is varied from 8 V to 36 V in 2-V steps. For each step, the maximum power is measured and the corresponding efficiency.

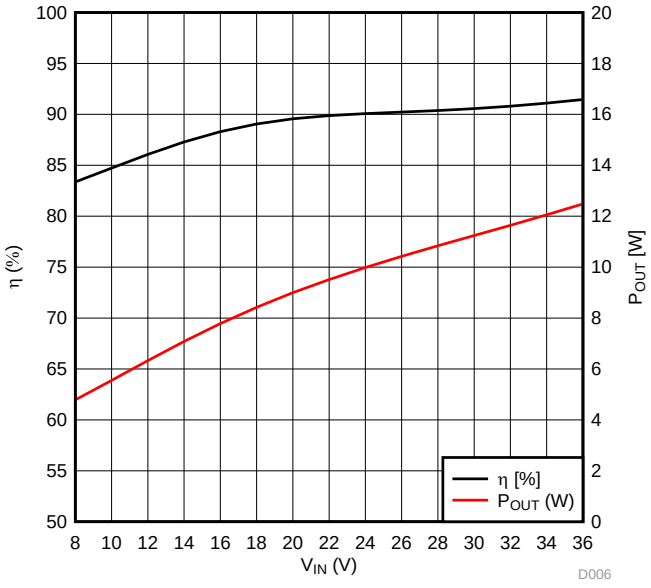

图 **10. Maximum Power and Efficiency versus V_{IN}**

The result of this test shows that the design can also be used for higher power if the input minimum voltage is increased. For a minimum voltage of 17 V, the design delivers 8 W with an efficiency of 88%.

3.2.3 Output Current and Efficiency Test

In this test, the input voltage is set to a fixed 24 V. The output current is varied from 0 to 300 mA in 20-mA steps.

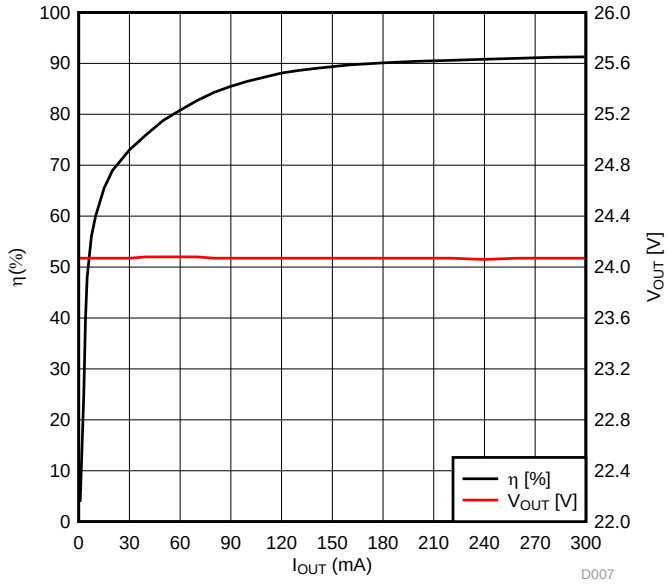

图 **11. Efficiency at 24 V versus Load**

At a V_{IN} of 24 V, the design shows greater than 80% efficiency at an output current of more than 60 mA (36% of maximum load). At this V_{IN}, it is possible to overload up to 10 W without degradation.

3.2.4 Thermal Images

The following images show the heat distribution on the test board. The main contributor of heat is the LM5001 device. At the maximum load and minimum input voltage V_{IN}, the switching transistor in the device has maximum current. This current is visible in the thermal image plots as the warmest spot. The environment temperature is 25°C, which means the device had a temperature rise of 36.3°C in this measurement. The first two images show the thermal behavior of the circuit at the upper and lower extremes of V_{IN}, which are 36 V and 8 V, respectively. The third image shows the measurement at a nominal V_{IN} of 24 V. At the higher voltages, the switching current of the device is lower, so the temperature rise is smaller as well.

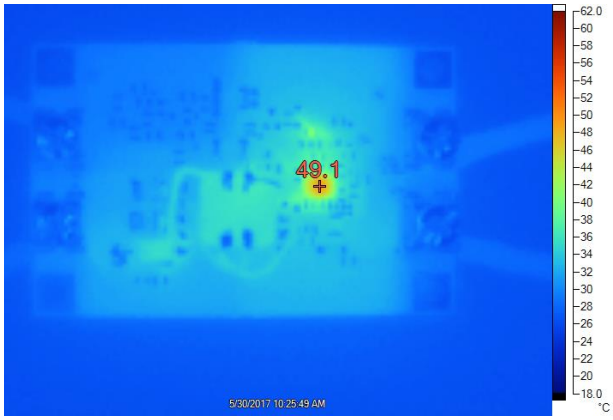

图 **12. Thermal Image at V_{IN} = 36 V**

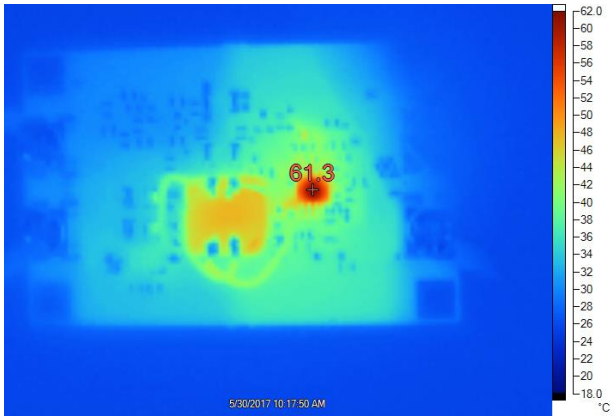

图 **13. Thermal Image at V_{IN} = 8 V**

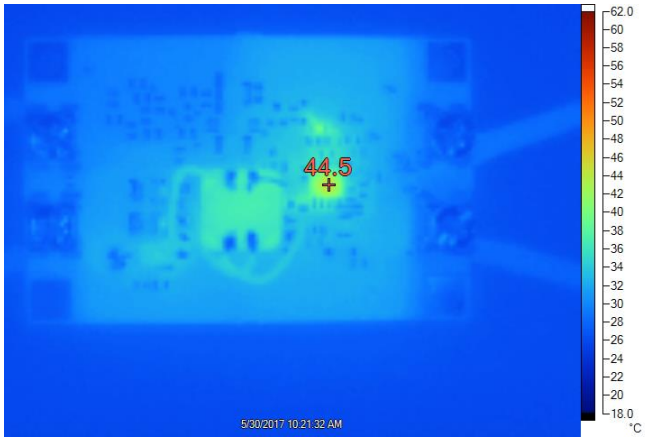

图 **14. Thermal Image at V_{IN} = 24 V**

The thermal images also show the possibility for improvement at light load conditions. The one warm spot above the device is the resistor of the output divider, which has the highest voltage drop. Increasing this resistance can lift the light load (10% load) efficiency.

4 Design Notes

The sum of input voltage and output voltage in this reference design is limited to the maximum switch voltage. This voltage is 75 V in the LM5001 regulator. For an output voltage of 24 V, the input voltage must therefore be lower than 51 V. It is possible to make this design immune against destruction from voltages between 51 V and 75 V. For this immunity, the switch must stop switching while the input voltage is too large. A circuit like the one in 图 15 can disable the switch above a certain input voltage (in this case, 45 V). The circuit checks V_{IN} against a reference voltage (in this case, 1.25 V) and pulls its open drain output low when V_{IN} is too high. This disables the LM5001 regulator.

For proper operation, a pullup resistor is required if the output leakage current of the comparator is larger than the built-in 6-µA current source of the LM5001 regulator. The pullup resistor can be part of the undervoltage lockout circuit. The designer must consider a time for the disable circuit to become effective. This time is approximately the duration of one clock cycle in the LM5001 plus the time the comparator needs to detect the overvoltage condition. For a 250-kHz switching frequency, this takes around 5 µs assuming a 1-µs detection time. With a disable threshold set at 45 V, the circuit can then protect against overvoltage conditions, which have less than a 1-V/µs rising voltage slope. This slope is sufficient for standard PLC power supplies.

The LM5001 has two built-in undervoltage lockout circuits. One has a fixed V_{IN} voltage threshold level of 2.8 V (typical). The other one is programmable with an external voltage divider. These circuits can help to prevent abnormal high input currents on V_{IN} associated with low input voltage conditions. When the voltage ramps during start-up, the current can be higher than at normal operation because the device tries to pull the full power needed to generate the output voltage. The designer has two options to limit this increased current:

1. Soft start: This option generates a defined voltage ramp at the output of the converter. If this ramp is aligned with the input ramp, then excessive currents do not occur. This method works best when the designer knows the exact input and output conditions. For more details, see *LM5001x High-Voltage Switch-Mode Regulator* .
2. Undervoltage lockout: This option starts the LM5001 only once a certain input voltage level is available. This method helps to prevent operation at input voltage levels where too high currents are needed to achieve load regulation. It is simple to implement in the LM5001 regulator. 图 15 shows the circuit.

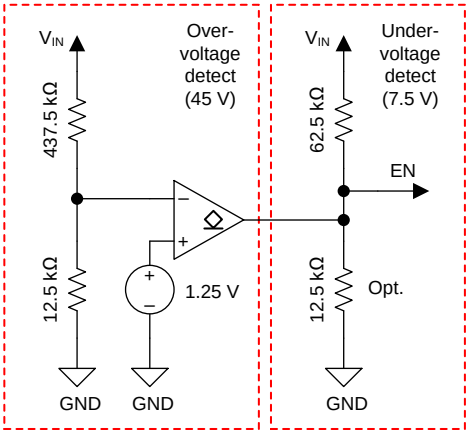

图 **15. Principle Circuit for Disabling LM5001 at V_{IN} > 45 V and V_{IN} < 7.5 V**

5 Design Files

This reference design comes with a set of design files to enable a quick and flawless conversion into other designs. These design files are located in the TIDA-01498 design folder.

The design files consist of schematics, BOM, an Altium Designer project, and the Gerber files of the LM5001 flyback evaluation board.

6 Related Documentation

1. Texas Instruments, *Designing DC/DC converters based on SEPIC topology* , Article from Analog Applications Journal 4Q 2008
2. Texas Instruments, *LM5001 Non-Isolated Flyback Evaluation Board User's Guide*

6.1 商标

7 About the Author

INGOLF FRANK is a systems engineer in the Texas Instruments Factory Automation and Control Team, focusing on PLC I/O modules. Ingolf works across multiple product families and technologies to leverage the best solutions possible for system level application design. Ingolf earned his electrical engineering degree (Dipl. Ing. (FH)) in the field of information technology at the University of Applied Sciences Bielefeld, Germany in 1991.

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